30 V, Micropower, Overvoltage Protection, Rail-to-Rail Input/Output Amplifiers

Data Sheet **ADA4096-2/ADA4096-4**

FEATURES

Input overvoltage protection, 32 V above and below the supply rails
No phase reversal for input voltage up to ±32 V beyond the power supply
Rail-to-rail input and output swing
Low power: 60 µA per amplifier typical
Unity-gain bandwidth
800 kHz typical at V_{SY} = ±15 V
550 kHz typical at V_{SY} = ±5 V
465 kHz typical at V_{SY} = ±1.5 V
Single-supply operation: 3 V to 30 V
Low offset voltage: 300 µV maximum
Large signal voltage gain: 120 dB typical
Unity gain stable
Qualified for automotive applications

APPLICATIONS

Battery monitoring
Sensor conditioners
Portable power supply controls
Portable instrumentation

GENERAL DESCRIPTION

The ADA4096-2 dual and ADA4096-4 quad operational amplifiers feature micropower operation and rail-to-rail input and output ranges. The extremely low power requirements and guaranteed operation from 3 V to 30 V make these amplifiers perfectly suited to monitor battery usage and to control battery charging. Their dynamic performance, including 27 nV/√Hz voltage noise density, recommends them for battery-powered audio applications. Capacitive loads to 200 pF are handled without oscillation.

The ADA4096-2 and ADA4096-4 have overvoltage protection inputs and diodes that allow the voltage input to extend 32 V above and below the supply rails, making this device ideal for robust industrial applications. The ADA4096-2 and ADA4096-4 feature a unique input stage that allows the input voltage to exceed either supply safely without any phase reversal or latch-up; this is called overvoltage protection, or OVP.

The dual ADA4096-2 is available in 8-lead LFCSP (2 mm × 2 mm) and 8-lead MSOP packages. The ADA4096-2 is available in 16-lead LFCSP (3 mm × 3 mm) and 14-lead TSSOP packages. The ADA4096-2W is qualified for automotive applications and is available in an 8-lead MSOP package.

PIN CONNECTION DIAGRAMS

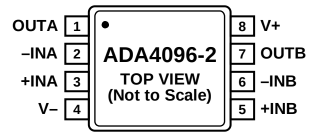


Figure 1. 8-Lead, MSOP (RM-8), ADA4096-2

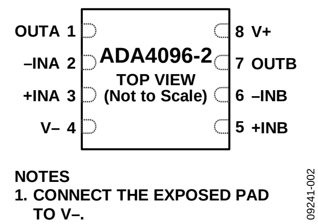


Figure 2. 8-Lead LFCSP (CP-8-10), ADA4096-2

Note: For the ADA4096-4, see the Pin Configurations and Function Descriptions section.

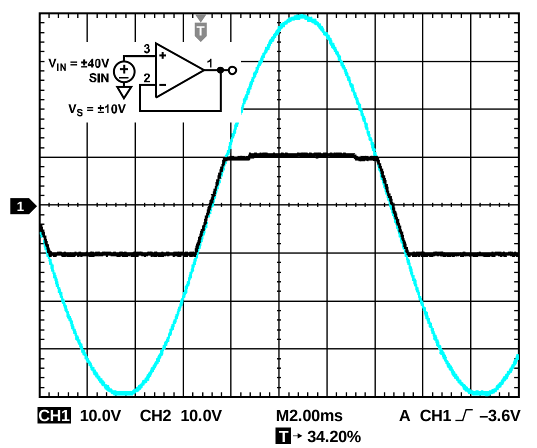


Figure 3. No Phase Reversal

The ADA4096-2 family is specified over the extended industrial temperature range of (−40°C to +125°C) and is part of the growing selection of 30 V, low power op amps from Analog Devices, Inc. (see Table 1).

Table 1. Low Power, 30 V Operational Amplifiers

Op Amp	Rail-to-Rail I/O	PJFET	Low Noise
Dual	ADA4091-2	AD8682	AD8622
Quad	ADA4091-4	AD8684	AD8624

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support **www.analog.com**

TABLE OF CONTENTS

Features ... 1
Applications ... 1
Pin Connection Diagrams ... 1
General Description ... 1
Revision History ... 3
Specifications ... 4
Electrical Specifications, V_{SY} = ±1.5 V ... 4
Electrical Specifications, V_{SY} = ±5 V ... 5
Electrical Specifications, V_{SY} = ±15 V ... 6
Absolute Maximum Ratings ... 7
Thermal Resistance ... 7
ESD Caution ... 7
Pin Configurations and Function Descriptions ... 8
Typical Performance Characteristics ... 10
±1.5 V Characteristics ... 10
±5 V Characteristics ... 13
±15 V Characteristics ... 16
Comparative Voltage and Variable Voltage Graphs ... 19
Theory of Operation ... 20
Input Stage ... 20
Phase Inversion ... 20
Input Overvoltage Protection ... 21
Comparator Operation ... 21
Outline Dimensions ... 22
Ordering Guide ... 24
Automotive Products ... 24

REVISION HISTORY

9/2017—Rev. F to Rev. G

Changed ADA409x to ADA4096-2 .... Throughout
Changed CP-16-27 to CP-16-22............ Throughout
Changes to Figure 12 and Figure 13 10
Changes to Figure 26 13
Changes to Figure 39 16
Updated Outline Dimensions............ 22
Changes to Ordering Guide............ 24

12/2014—Rev. E to Rev. F

Changes to EPAD Note, Figure 2 1
Changes to EPAD Note, Figure 5 and Table 7 7
Changes to EPAD Note, Figure 7 and Table 8 8

3/2014—Rev. D to Rev. E

Changes to Figure 10 and Figure 12 9
Changes to Figure 23 and Figure 25 12
Changes to Figure 36 and Figure 38 15

5/2013—Rev. C to Rev. D

Changes to Pin Connection Diagrams Section............ 1
Changes to Pin Configurations and Function Descriptions Section 7
Added Figure 10, Renumbered Sequentially............ 9
Added Figure 23 12
Added Figure 36 15

8/2012—Rev. B to Rev. C

Changes to Table 8 8

8/2012—Rev. A to Rev. B

Added ADA4096-4 .... Universal
Changes to Features Section 1
Added Figure 3 1
Changes to Pin Connection Diagrams Section............ 1
Changes to Input Bias Current, Common-Mode Rejection Ratio, Large Signal Voltage Gain, and Supply Current per Amplifier Parameters, and −3 dB Closed-Loop Bandwidth Symbol, Table 2............ 3
Changes to Input Bias Current, Common-Mode Rejection Ratio, Large Signal Voltage Gain, and Parameters, and −3 dB Closed-Loop Bandwidth Symbol, Table 3 4
Changes to Input Bias Current, Common-Mode Rejection Ratio, Large Signal Voltage Gain, Output Voltage High, and Output Voltage Low Parameters, and −3 dB Closed-Loop Bandwidth Symbol, Table 4 5
Changes to Table 6 7
Added Pin Configurations and Function Descriptions Section 8
Added Figure 4 and Figure 5, Renumbered Sequentially............ 8
Added Table 7, Renumbered Sequentially............ 8
Added Figure 6, Figure 7, and Table 8............ 9
Updated Outline Dimensions............ 18
Changes to Ordering Guide............ 20

3/2012—Rev. 0 to Rev. A

Changed −3 dB Closed-Loop Bandwidth from 97 kHz to 970 kHz, Table 2 3
Changed −3 dB Closed-Loop Bandwidth from 114 kHz to 1140 kHz, Table 3 4
Changed to −3 dB Closed-Loop Bandwidth from 152 kHz to 1520 kHz, Table 4 5
Updated Outline Dimensions............ 18

7/2011—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS, V_{SY} = ±1.5 V

V_{SY} = ±1.5 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			35	300	µV
		0°C ≤ T_A ≤ +125°C			450	µV
		−40°C ≤ T_A ≤ +125°C			900	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		1		µV/°C
Input Bias Current	I_B			±10	±25	nA
		−40°C ≤ T_A ≤ +125°C			±30	nA
Input Offset Current	I_{OS}			±0.1	±1.5	nA
		−40°C ≤ T_A ≤ +125°C			±3	nA
Input Voltage Range			−1.5		+1.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to ±1.5 V	61	77		dB
		−40°C ≤ T_A ≤ +125°C	58			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = −1.4 V to +1.4 V	91	94		dB
		−40°C ≤ T_A ≤ +125°C	84			dB
		R_L = 2 kΩ, V_O = −1.3 V to +1.3 V	86	92		dB
		−40°C ≤ T_A ≤ +125°C	77			dB
MATCHING CHARACTERISTICS						
Offset Voltage		T_A = 25°C		100	300	µV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to GND	1.48	1.49		V
		−40°C ≤ T_A ≤ +125°C	1.45			V
		R_L = 2 kΩ to GND	1.45	1.46		V
		−40°C to +125°C	1.40			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to GND		−1.49	−1.48	V
		−40°C ≤ T_A ≤ +125°C			−1.45	V
		R_L = 2 kΩ to GND		−1.48	−1.47	V
		−40°C ≤ T_A ≤ +125°C			−1.40	V
Short-Circuit Limit	I_{SC}	Source/sink		±10		mA
Closed-Loop Impedance	Z_{OUT}	f = 100 kHz, A_V = 1		102		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3 V to 36 V	100			dB
		−40°C ≤ T_A ≤ +125°C	90			dB
Supply Current per Amplifier	I_{SY}	V_O = V_{SY}/2		40	50	µA
		−40°C ≤ T_A ≤ +125°C			80	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 30 pF		0.25		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		501		kHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		465		kHz
Phase Margin	Φ_M			51		Degrees
−3 dB Closed-Loop Bandwidth	$f_{-3\,dB}$	A_V = 1, V_{IN} = 5 mV p-p		970		kHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.7		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		27		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz

ELECTRICAL SPECIFICATIONS, V_{SY} = ±5 V

V_{SY} = ±5 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			35	300	µV
		−40°C ≤ T_A ≤ +125°C			500	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		µV/°C
Input Bias Current	I_B			±10	±25	nA
		−40°C ≤ T_A ≤ +125°C			±30	nA
Input Offset Current	I_{OS}			±1.5	±2	nA
		−40°C ≤ T_A ≤ +125°C			±3	nA
Input Voltage Range			−5		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −5 V to +5 V	72	86		dB
		−40°C ≤ T_A ≤ +125°C	68			dB
		V_{CM} = −3 V to +3 V	91	103		dB
		−40°C ≤ T_A ≤ +125°C	85			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = ±4.8 V	102	111		dB
		−40°C ≤ T_A ≤ +125°C	99			dB
		R_L = 2 kΩ, V_O = ±4.7 V	93	103		dB
		−40°C ≤ T_A ≤ +125°C	88			dB
MATCHING CHARACTERISTICS						
Offset Voltage		T_A = 25°C		100	300	µV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to GND	4.96	4.97		V
		−40°C ≤ T_A ≤ +125°C	4.95			V
		R_L = 2 kΩ to GND	4.80	4.90		V
		−40°C ≤ T_A ≤ +125°C	4.70			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to GND		−4.98	−4.97	V
		−40°C ≤ T_A ≤ +125°C			−4.95	V
		R_L = 2 kΩ to GND		−4.90	−4.80	V
		−40°C ≤ T_A ≤ +125°C			−4.75	V
Short-Circuit Limit	I_{SC}	Source/sink		±10		mA
Closed-Loop Impedance	Z_{OUT}	f = 100 kHz, A_V = 1		71		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3 V to 36 V	100			dB
		−40°C ≤ T_A ≤ +125°C	90			dB
Supply Current per Amplifier	I_{SY}	V_O = V_{SY}/2		47	55	µA
		−40°C ≤ T_A ≤ +125°C			75	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 30 pF		0.3		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		595		kHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		550		kHz
Phase Margin	Φ_M			52		Degrees
−3 dB Closed-Loop Bandwidth	$f_{-3 dB}$	A_V = 1, V_{IN} = 5 mV p-p		1140		kHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.7		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		27		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz

ELECTRICAL SPECIFICATIONS, V_{SY} = ±15 V

V_{SY} = ±15 V, V_{CM} = $V_{SY}/2$, V_O = 0.0 V, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			35	300	µV
		−40°C ≤ T_A ≤ +125°C			500	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		µV/°C
Input Bias Current	I_B			±3	±25	nA
		−40°C ≤ T_A ≤ +125°C			±30	nA
Input Offset Current	I_{OS}			±0.1	±1.5	nA
		−40°C ≤ T_A ≤ +125°C			±3	nA
Input Voltage Range			−15		+15	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −15 V to +15 V	81	95		dB
		−40°C ≤ T_A ≤ +125°C	75			dB
		V_{CM} = −13 V to +13 V	95	107		dB
		−40°C ≤ T_A ≤ +125°C	89			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = ±14.7 V	109	120		dB
		−40°C ≤ T_A ≤ +125°C	105			dB
		R_L = 2 kΩ, V_O = ±11 V	99	112		dB
		−40°C ≤ T_A ≤ +125°C	90			dB
Input Capacitance						
Differential Mode	C_{DM}			2.5		pF
Common Mode	C_{CM}			7		pF
MATCHING CHARACTERISTICS						
Offset Voltage		T_A = 25°C		100	300	µV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to GND	14.92	14.94		V
		−40°C ≤ T_A ≤ +125°C	14.90			V
		R_L = 2 kΩ to GND	14.0	14.3		V
		−40°C ≤ T_A ≤ +125°C	11.0			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to GND		−14.96	−14.80	V
		−40°C ≤ T_A ≤ +125°C			−14.75	V
		R_L = 2 kΩ to GND		−14.75	−14.60	V
		−40°C ≤ T_A ≤ +125°C			−14.0	V
Short-Circuit Limit	I_{SC}	Source/sink		±10		mA
Closed-Loop Impedance	Z_{OUT}	f = 100 kHz, A_V = 1		40		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3 V to 36 V	100			dB
		−40°C ≤ T_A ≤ +125°C	90			dB
Supply Current per Amplifier	I_{SY}	V_O = $V_{SY}/2$		60	75	µA
		−40°C ≤ T_A ≤ +125°C			100	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 30 pF		0.4		V/µ
Settling Time	t_S	To 0.1%, 10 V step		23.4		µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		786		kHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		800		kHz
Phase Margin	Φ_M			60		Degrees
−3 dB Closed-Loop Bandwidth	$f_{-3\,dB}$	A_V = 1, V_{IN} = 5 mV p-p		1520		kHz
Channel Separation	CS	f = 1 kHz		100		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.7		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		27		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	
Operating Condition	$-V \le V_{IN} \le +V$
Overvoltage Condition[1]	$(-V) - 32\ V \le V_{IN} \le (+V) + 32\ V$
Differential Input Voltage[2]	$\pm V_{SY}$
Input Current	±5 mA
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

[1] Performance not guaranteed during overvoltage conditions.
[2] Limit the input current to ±5 mA.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

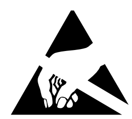
THERMAL RESISTANCE

θ_{JA} is specified for the device soldered on a 4-layer JEDEC standard printed circuit board (PCB) with zero airflow. The exposed pad is soldered to the application board.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (RM-8)	142	45	°C/W
8-Lead LFCSP (CP-8-10)	76	43	°C/W
14-Lead TSSOP (RU-14)	112	35	°C/W
16-Lead LFCSP (CP-16-22)	75	12	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

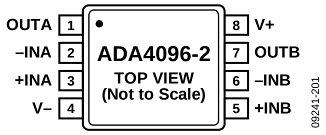


Figure 4. 8-Lead, MSOP (RM-8), ADA4096-2

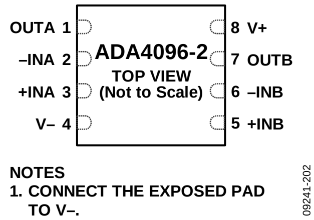


Figure 5. 8-Lead LFCSP (CP-8-10), ADA4096-2

Table 7. Pin Function Descriptions, ADA4096-2

Pin No.[1]			
8-Lead MSOP	**8-Lead LFCSP**	**Mnemonic**	**Description**
1	1	OUTA	Output Channel A.
2	2	−INA	Negative Input Channel A.
3	3	+INA	Positive Input Channel A.
4	4	V−	Negative Supply Voltage.
5	5	+INB	Positive Input Channel B.
6	6	−INB	Negative Input Channel B.
7	7	OUTB	Output Channel B.
8	8	V+	Positive Supply Voltage.
N/A	EP[2]	EPAD	Exposed Pad.[2] For the ADA4096-2 (8-lead LFCSP only), connect the exposed pad to V−.

[1] N/A means not applicable.
[2] The exposed pad is not shown in the pin configuration diagram.

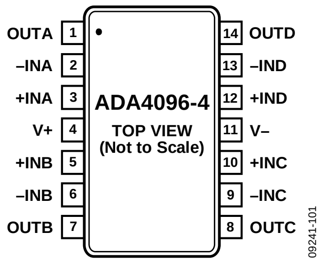


Figure 6. 14-Lead TSSOP (RU-14), ADA4096-4

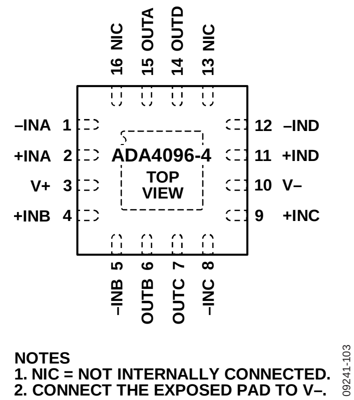


Figure 7. 16-Lead LFCSP (CP-16-22), ADA4096-4

Table 8. Pin Function Descriptions, ADA4096-4

Pin No.[1]			
14-Lead TSSOP	**16-Lead LFCSP**	**Mnemonic**	**Description**
1	15	OUTA	Output Channel A.
2	1	−INA	Negative Input Channel A.
3	2	+INA	Positive Input Channel A.
4	3	V+	Positive Supply Voltage.
5	4	+INB	Positive Input Channel B.
6	5	−INB	Negative Input Channel B.
7	6	OUTB	Output Channel B.
8	7	OUTC	Output Channel C.
9	8	−INC	Negative Input Channel C.
10	9	+INC	Positive Input Channel C.
11	10	V−	Negative Supply Voltage.
12	11	+IND	Positive Input Channel D.
13	12	−IND	Negative Input Channel D.
14	14	OUTD	Output Channel D.
N/A	13	NIC	No Internal Connection.
N/A	16	NIC	No Internal Connection.
N/A	EP[2]	EPAD	Exposed Pad.[2] For the ADA4096-4 (16-lead LFCSP only), connect the exposed pad to V−.

[1] N/A means not applicable.
[2] The exposed pad is not shown in the pin configuration diagram.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted. All typical performance characteristics shown are for the ADA4096-2 only.

±1.5 V CHARACTERISTICS

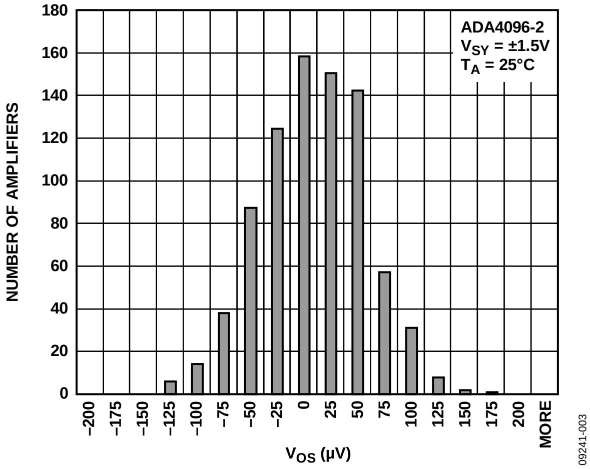


Figure 8. Input Offset Voltage (V_{OS}) Distribution

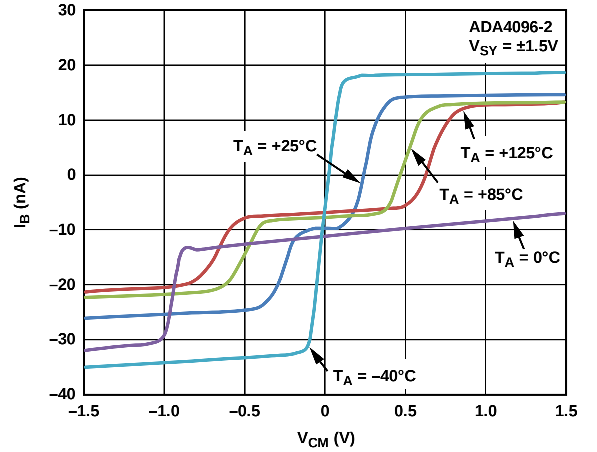


Figure 11. Input Bias Current (I_B) vs. V_{CM} for Various Temperatures

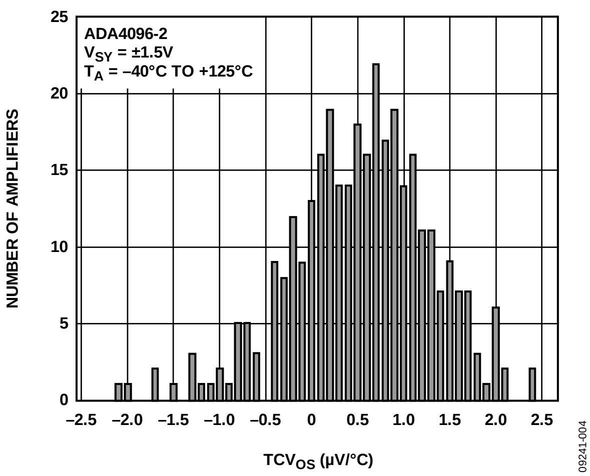


Figure 9. Offset Voltage Drift (TCV_{OS}) Distribution

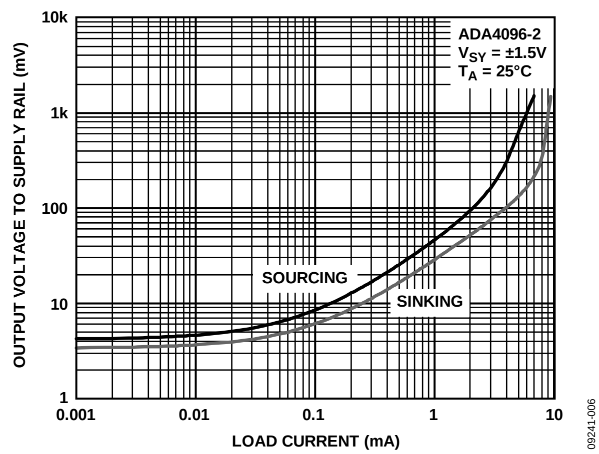


Figure 12. Output Voltage to Supply Rail vs. Load Current

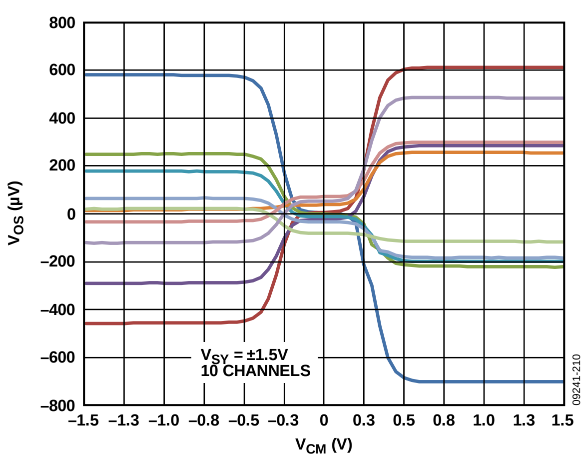


Figure 10. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM})

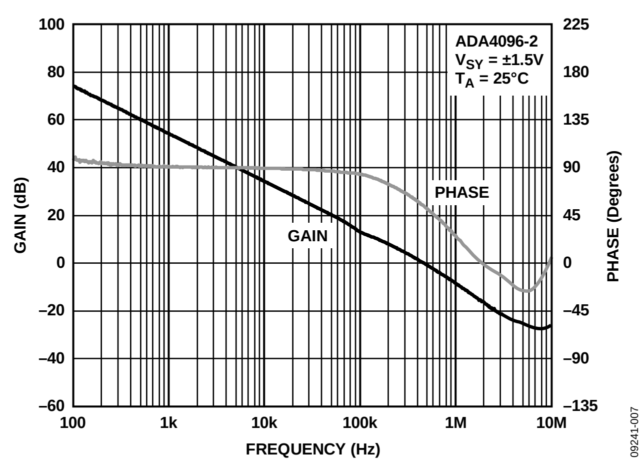


Figure 13. Open-Loop Gain and Phase vs. Frequency

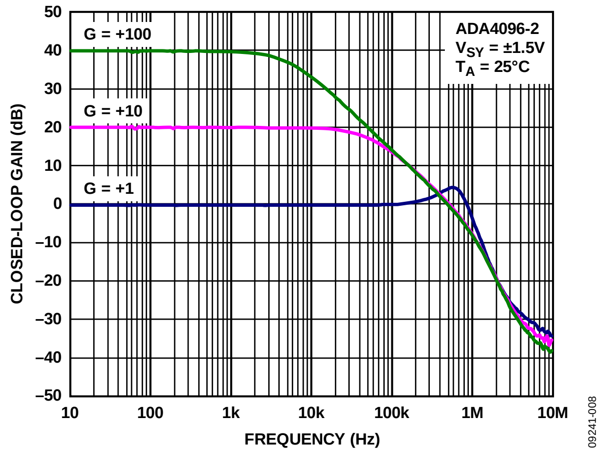


Figure 14. Closed-Loop Gain vs. Frequency

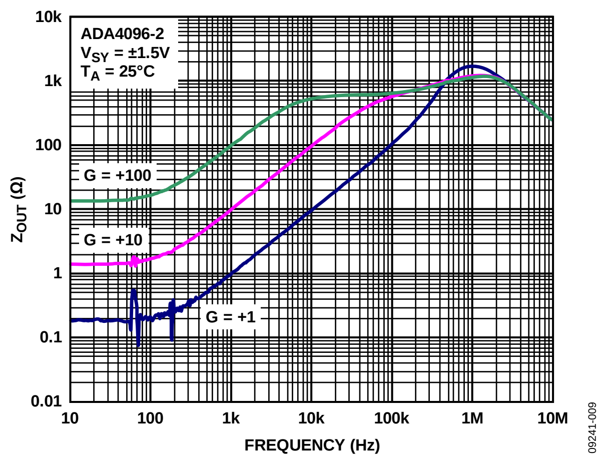


Figure 15. Output Impedance (Z_{OUT}) vs. Frequency

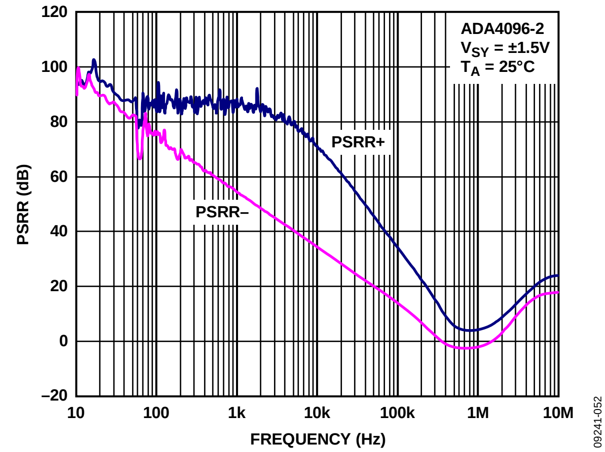


Figure 16. PSRR vs. Frequency

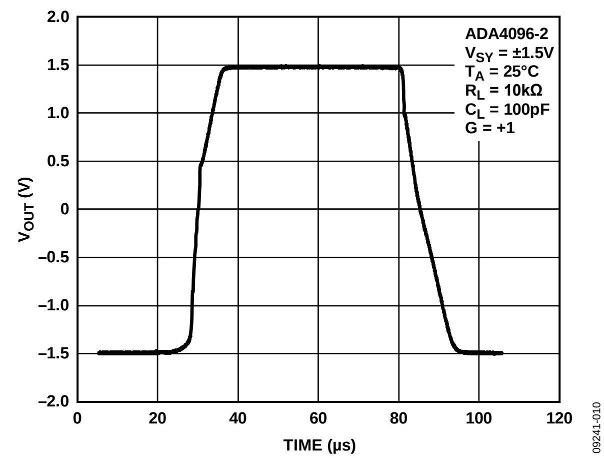


Figure 17. Large Signal Transient Response

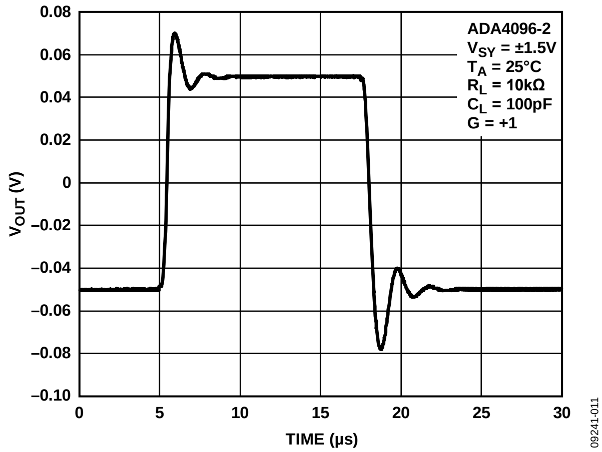


Figure 18. Small Signal Transient Response

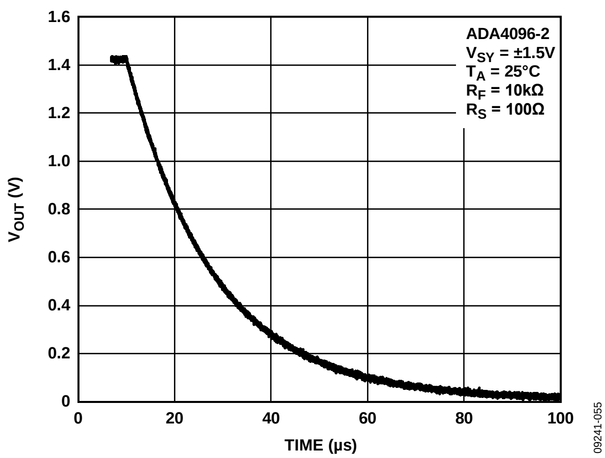


Figure 19. Positive Overload Recovery

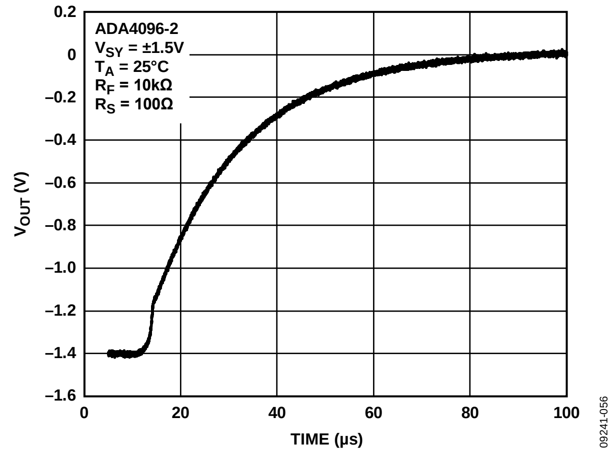


Figure 20. Negative Overload Recovery

±5 V CHARACTERISTICS

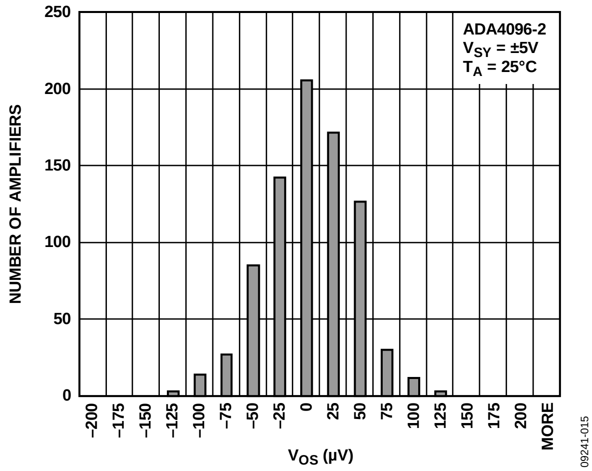


Figure 21. Input Offset Voltage (V_{OS}) Distribution

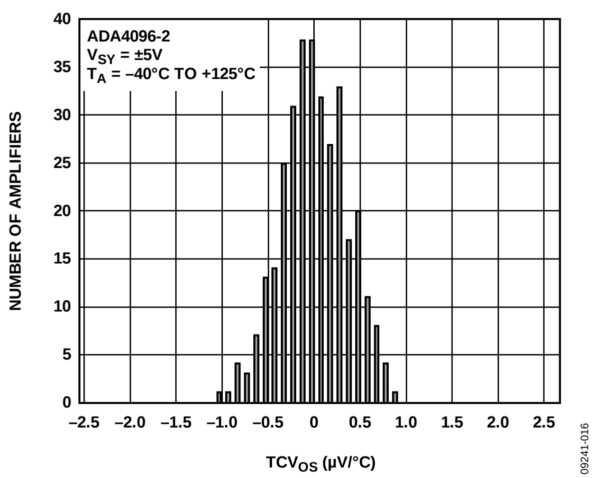


Figure 22. Offset Voltage Drift (TCV_{OS}) Distribution

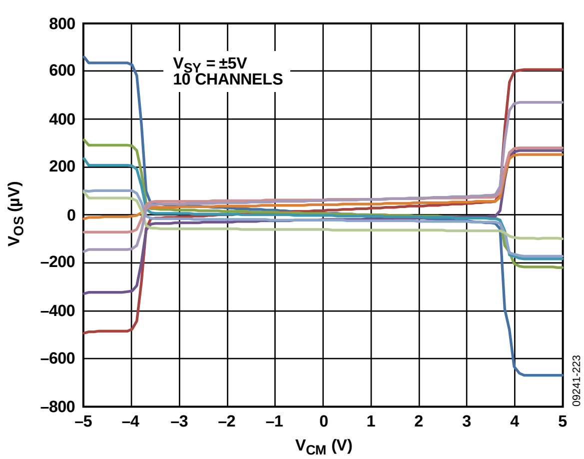


Figure 23. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM})

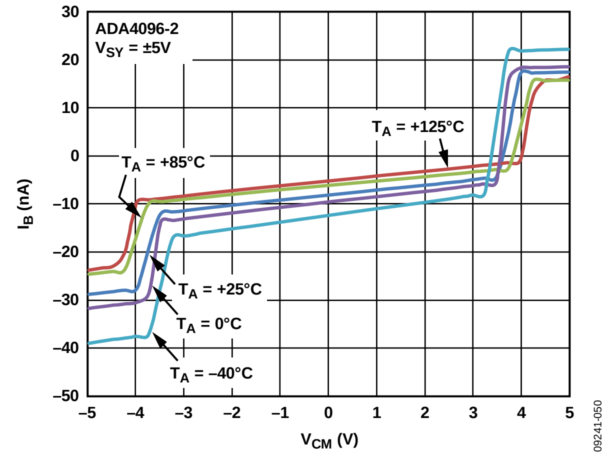


Figure 24. Input Bias Current (I_B) vs. V_{CM} for Various Temperatures

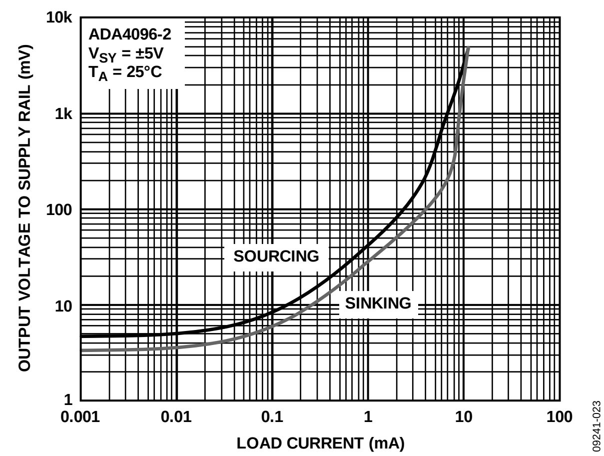


Figure 25. Output Voltage to Supply Rail vs. Load Current

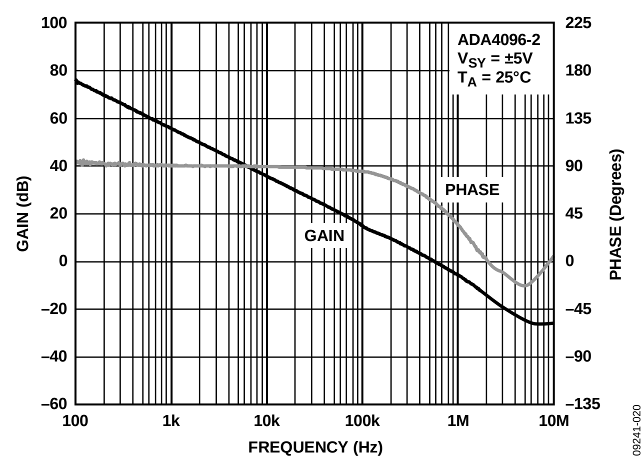


Figure 26. Open-Loop Gain and Phase vs. Frequency

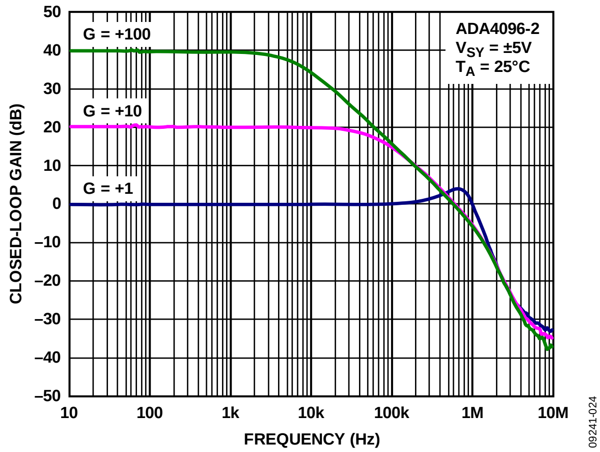


Figure 27. Closed-Loop Gain vs. Frequency

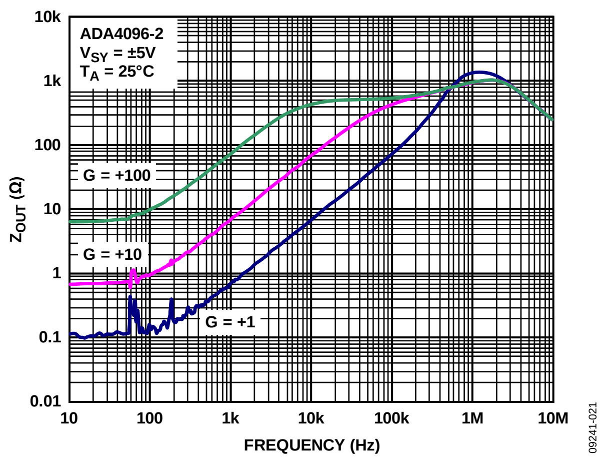


Figure 28. Output Impedance (Z_{OUT}) vs. Frequency.

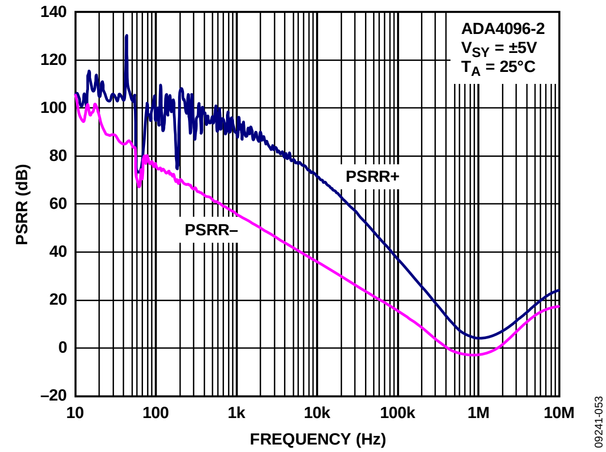


Figure 29. PSRR vs. Frequency

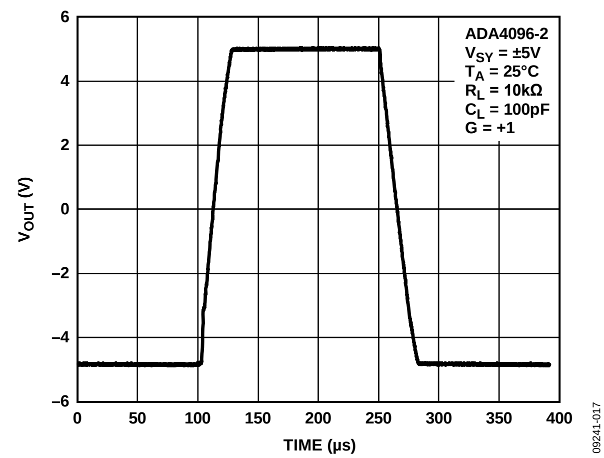


Figure 30. Large Signal Transient Response

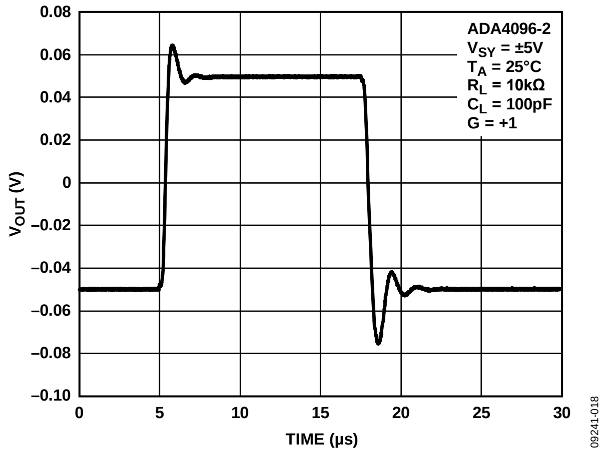


Figure 31. Small Signal Transient Response

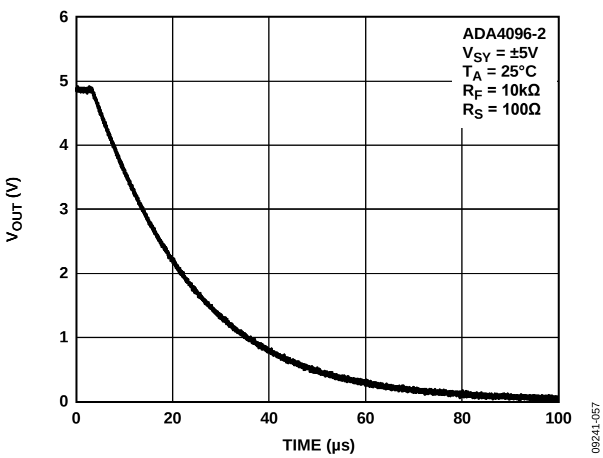


Figure 32. Positive Overload Recovery

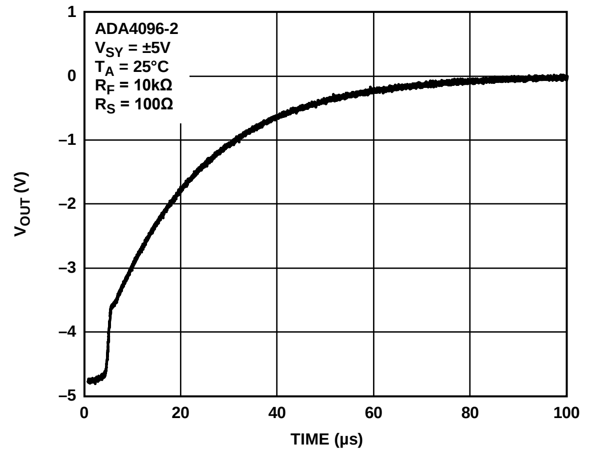


Figure 33. Negative Overload Recovery

±15 V CHARACTERISTICS

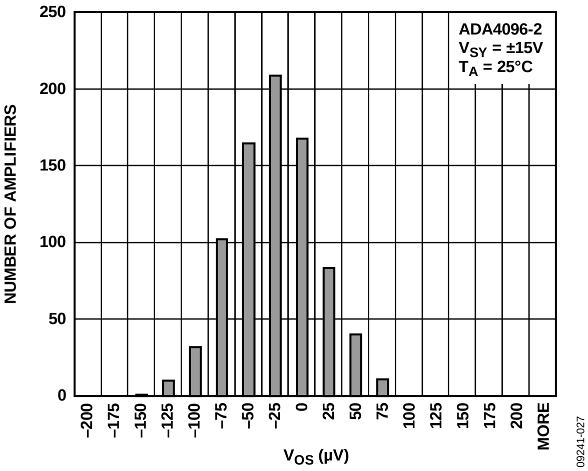


Figure 34. Input Offset Voltage (V_{OS}) Distribution

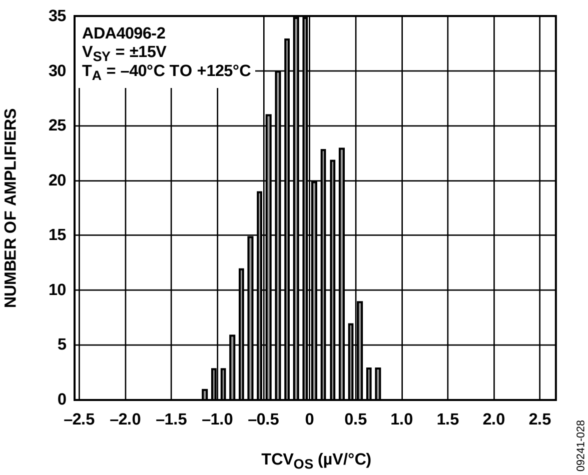


Figure 35. Offset Voltage Drift (TCV_{OS}) Distribution

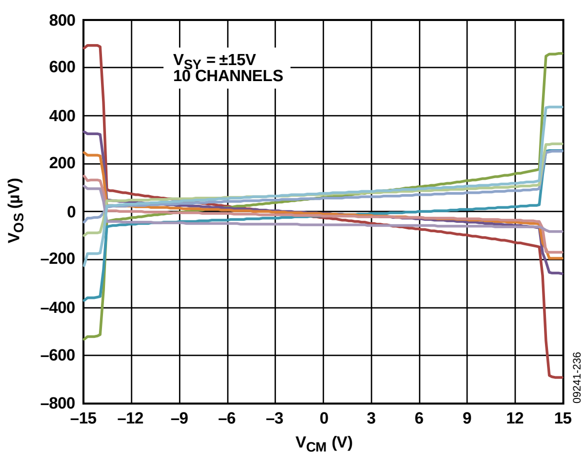


Figure 36. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM})

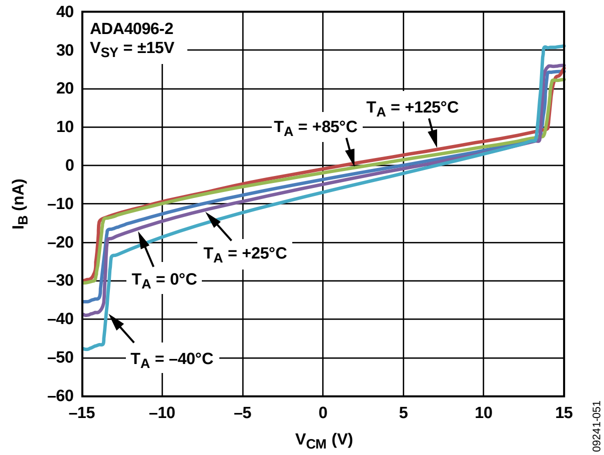


Figure 37. Input Bias Current (I_B) vs. V_{CM} for Various Temperatures

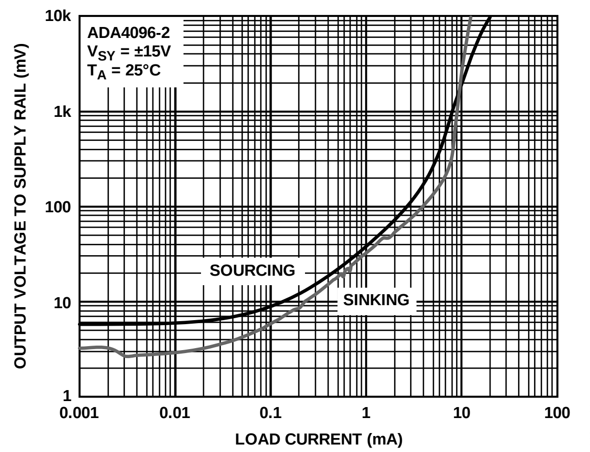


Figure 38. Output Voltage to Supply Rail vs. Load Current

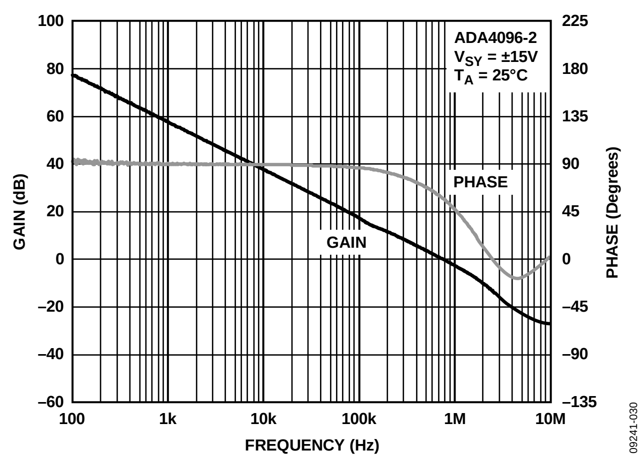


Figure 39. Open-Loop Gain and Phase vs. Frequency

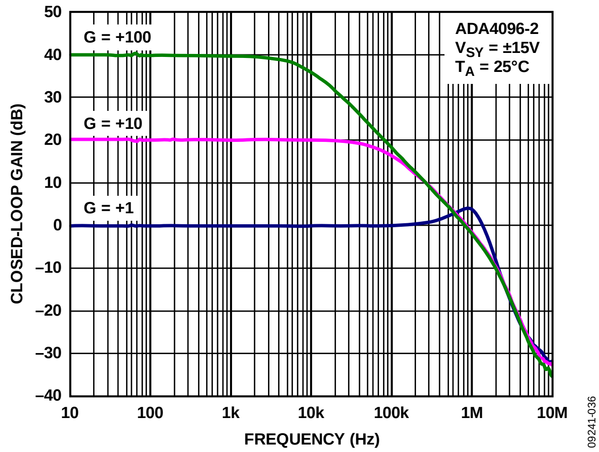


Figure 40. Closed-Loop Gain vs. Frequency

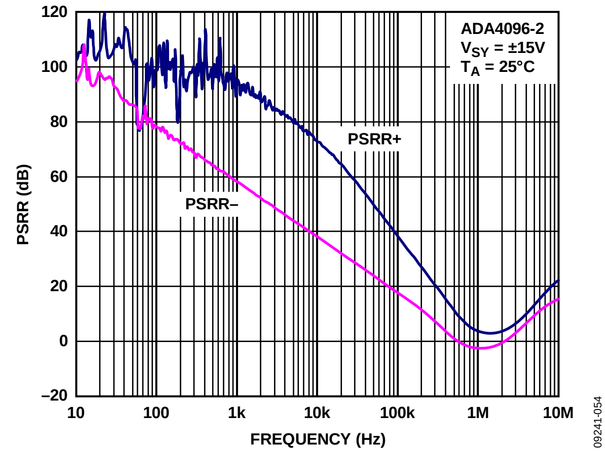


Figure 42. PSRR vs. Frequency

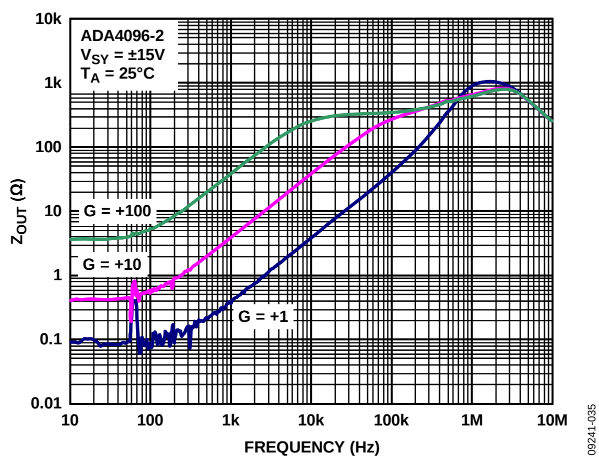


Figure 41. Output Impedance (Z_{OUT}) vs. Frequency

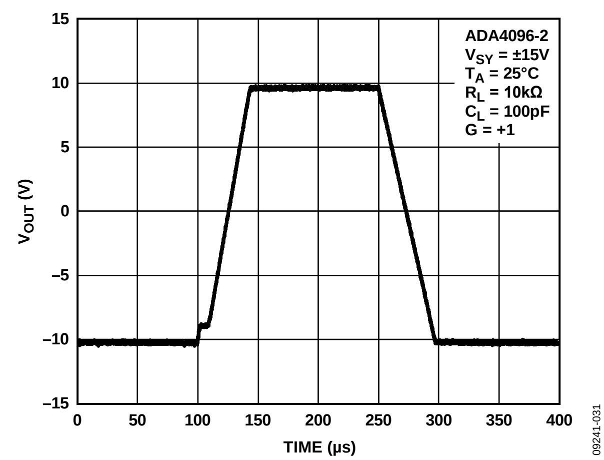


Figure 43. Large Signal Transient Response

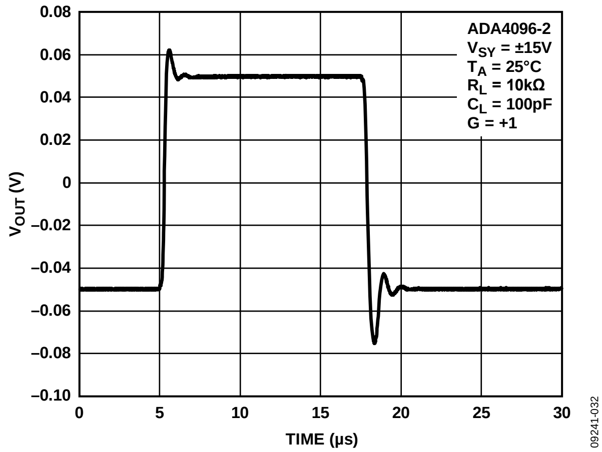


Figure 44. Small Signal Transient Response

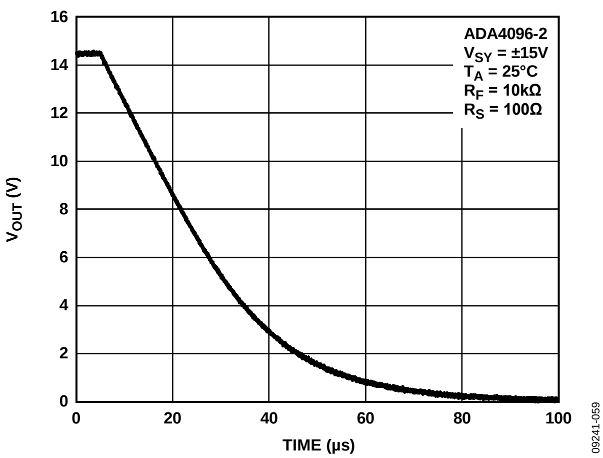


Figure 45. Positive Overload Recovery

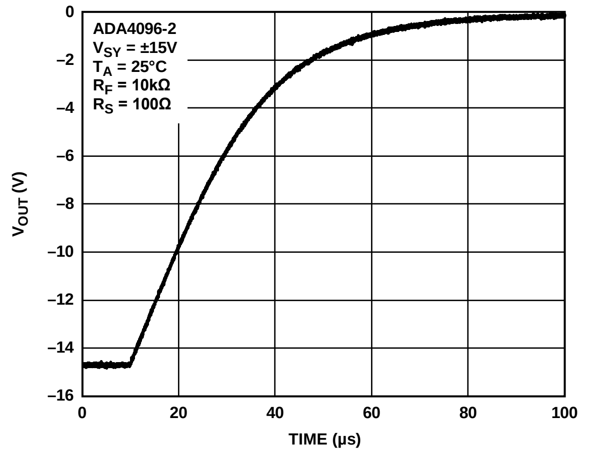


Figure 46. Negative Overload Recovery

COMPARATIVE VOLTAGE AND VARIABLE VOLTAGE GRAPHS

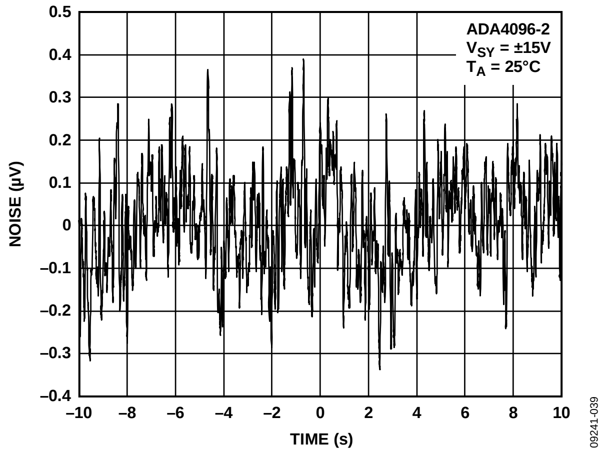


Figure 47. Input Voltage Noise, 0.1 Hz to 10 Hz Bandwidth

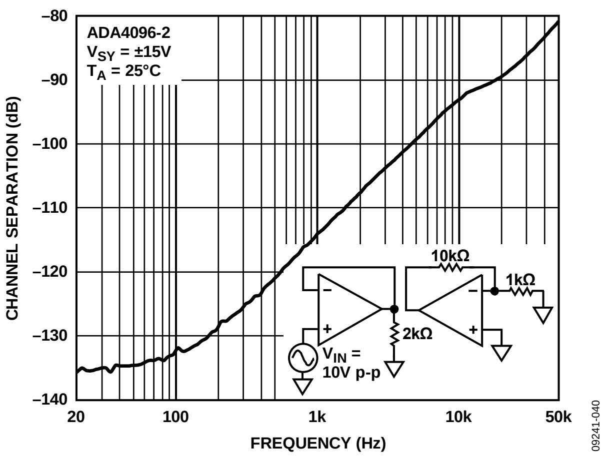


Figure 48. Channel Separation vs. Frequency

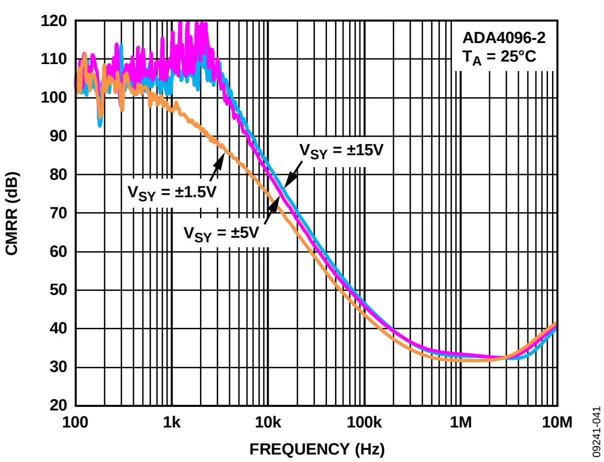


Figure 49. CMRR vs. Frequency

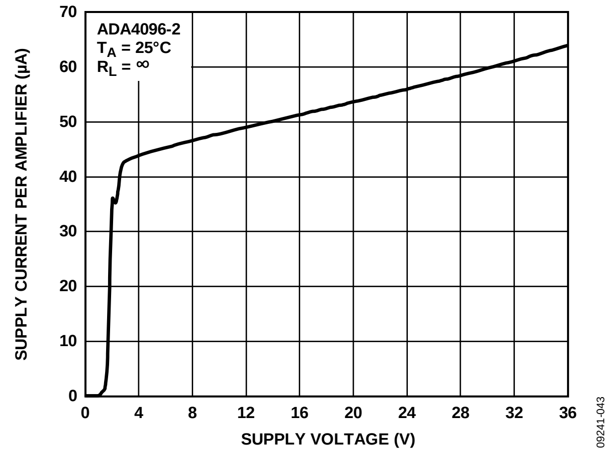


Figure 50. Supply Current per Amplifier vs. Supply Voltage

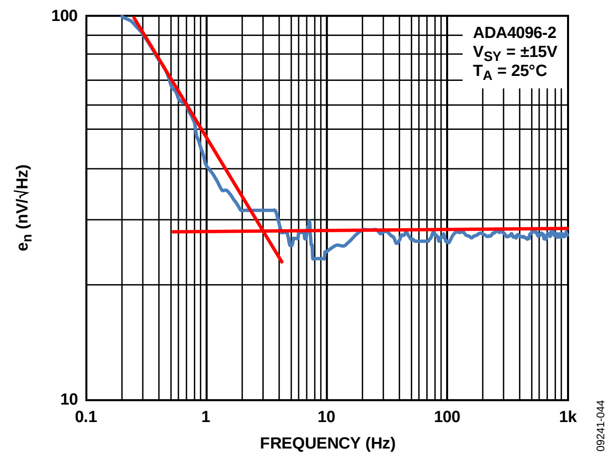


Figure 51. Voltage Noise Density (e_N) vs. Frequency

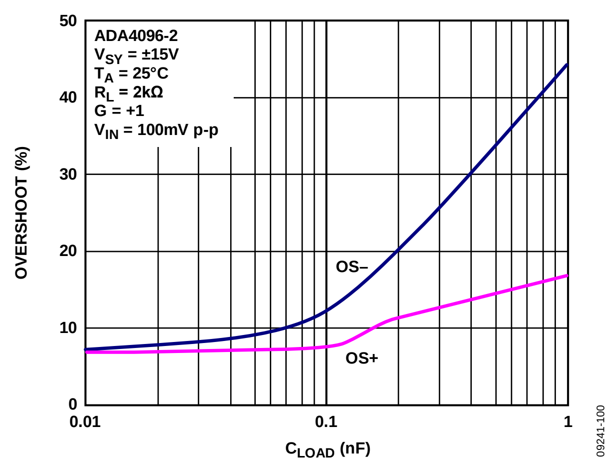


Figure 52. Overshoot vs. Load Capacitance (C_{LOAD})

THEORY OF OPERATION

INPUT STAGE

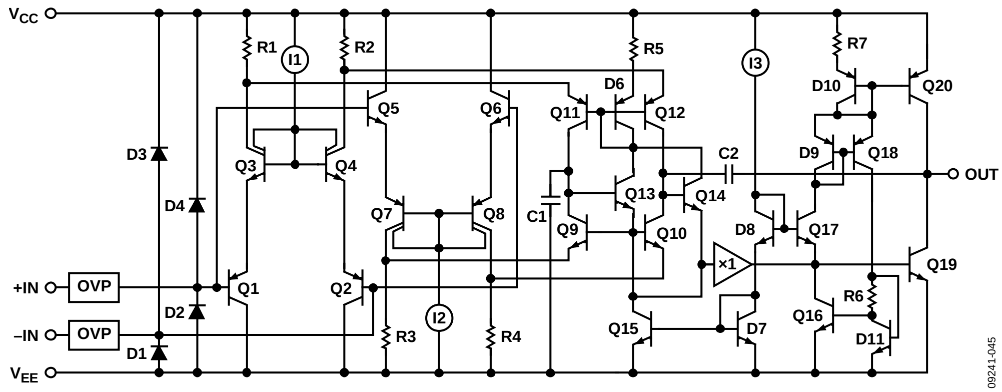


Figure 53. Simplified Schematic, ADA4096-2

Figure 53 shows a simplified schematic of the ADA4096-2. The input stage comprises two differential pairs (Q1 to Q4 and Q5 to Q8) operating in parallel. When the input common-mode voltage approaches VCC − 1.5 V, Q1 to Q4 shut down as I1 reaches its minimum voltage compliance. Conversely, when the input common-mode voltage approaches V_{EE} + 1.5 V, Q5 to Q8 shut down as I2 reaches its minimum voltage compliance. This topology allows for maximum input dynamic range because the amplifier can function with its inputs at 200 mV outside the rail (at room temperature).

As with any rail-to-rail input amplifier, V_{OS} mismatch between the two input pairs determines the CMRR of the amplifier. If the input common-mode voltage range is kept within 1.5 V of each rail, transitions between the input pairs are avoided, thus improving the CMRR by approximately 10 dB (see Table 3 and Table 4).

PHASE INVERSION

Some single-supply amplifiers exhibit phase inversion when the input signal extends beyond the common-mode voltage range of the amplifier. When the input devices become saturated, the inverting and noninverting inputs exchange functions, causing the output to move in the opposing direction.

Although phase inversion persists for only as long as the inputs are saturated, it can be detrimental to applications where the amplifier is part of a closed-loop system. The ADA4096-2 family is free from phase inversion over the entire common-mode voltage range, as well as the overvoltage protected range that is stated in the Absolute Maximum Ratings section, Table 5. Figure 54 shows the ADA4096-2 in a unity-gain configuration with the input signal at ±40 V and the amplifier supplies at ±10 V.

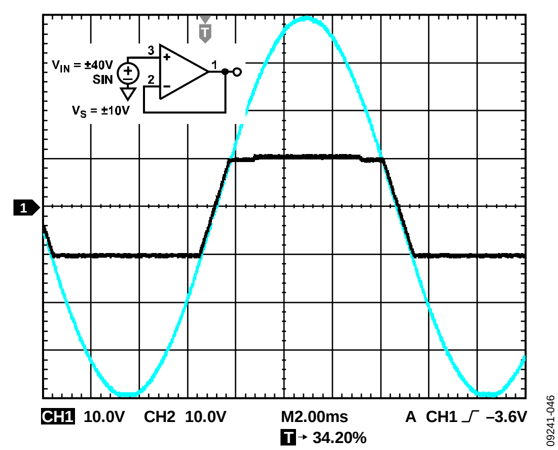


Figure 54. No Phase Reversal

INPUT OVERVOLTAGE PROTECTION

The ADA4096-2 family inputs are protected from input voltage excursions up to 32 V outside each rail. This feature is of particular importance in applications with power supply sequencing issues that could cause the signal source to be active before the power supplies.

Figure 55 shows the input current limiting capability of the ADA4096-2 (green curves) compared to using a 5 kΩ series resistor (red curves).

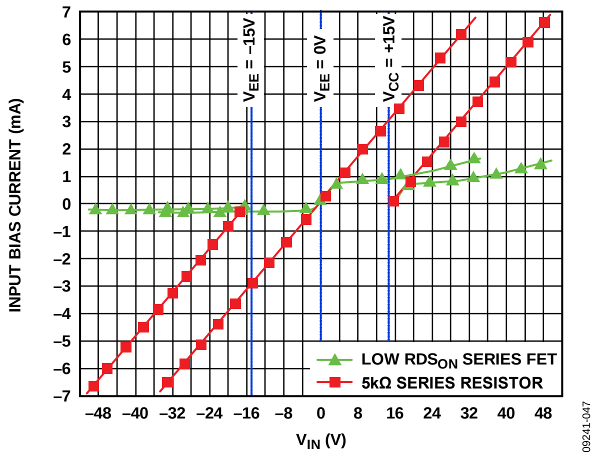


Figure 55. Input Current Limiting Capability

Figure 55 was generated with the ADA4096-2 in a buffer configuration with the supplies connected to GND (or ±15 V) and the positive input swept until it exceeds the supplies by 32 V. In general, input current is limited to 1 mA during positive overvoltage conditions and 200 µA during negative undervoltage conditions. For example, at an overvoltage of 20 V, the ADA4096-2 input current is limited to 1 mA, providing a current-limit equivalent to a series 20 kΩ resistor. Figure 55 also shows that the current limiting circuitry is active whether the amplifier is powered or not.

Note that Figure 55 represents input protection under abnormal conditions only. The correct amplifier operation input voltage range (IVR) is specified in Table 2 to Table 4.

COMPARATOR OPERATION

Although op amps are quite different from comparators, occasionally an unused section of a dual or a quad op amp may be pressed into service as a comparator; however, this is not recommended for any rail-to-rail output op amps. For rail-to-rail output op amps, the output stage is generally a ratioed current mirror with bipolar or metal-oxide semiconductor field-effect (MOSFET) transistors. With the device operating in open loop, the second stage increases the current drive to the ratioed mirror to close the loop, but it cannot, which results in an increase in supply current. With the op amp configured as a comparator, the supply current can be significantly higher (see Figure 56).

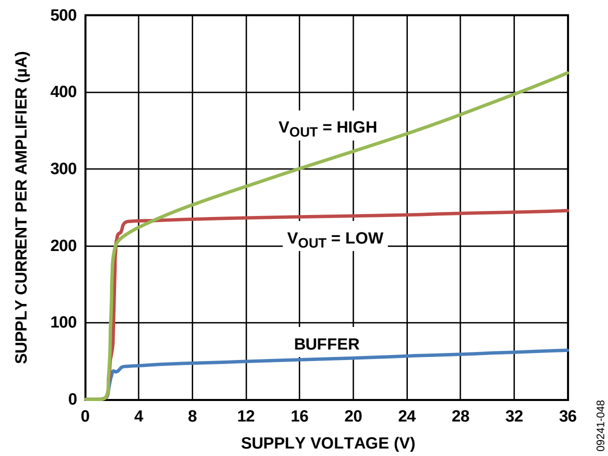


Figure 56. Comparator Supply Current

OUTLINE DIMENSIONS

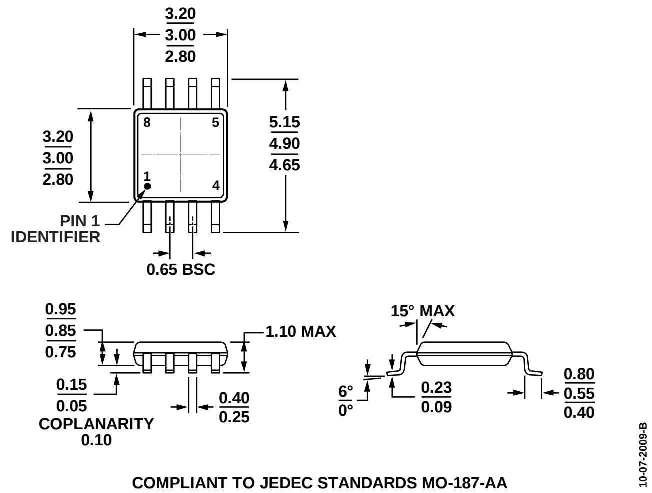


Figure 57. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

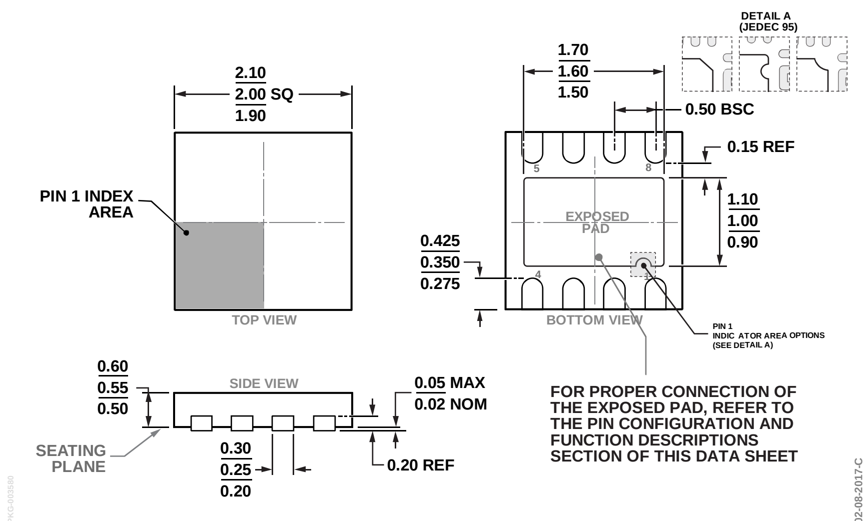
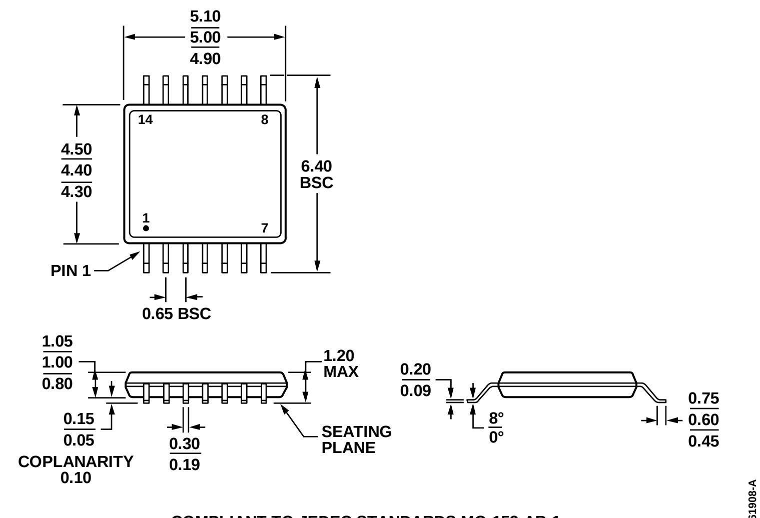
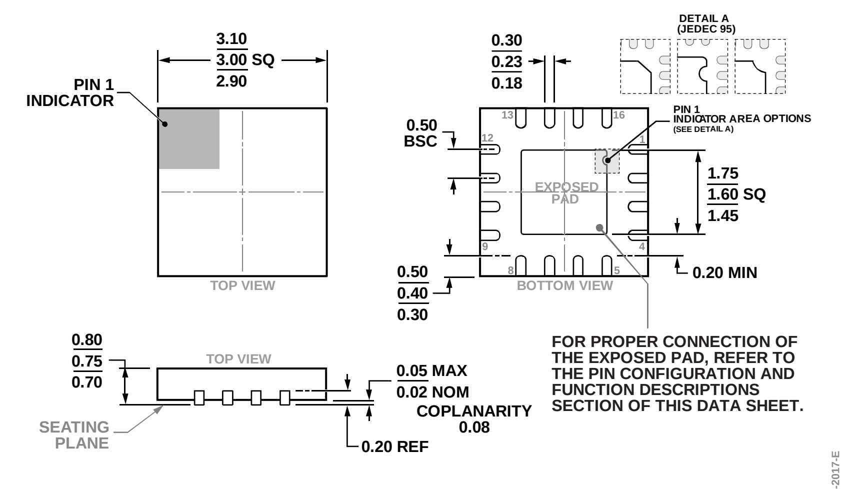


Figure 58. 8-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2 mm Body and 0.55 mm Package Height
(CP-8-10)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 59. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 60. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option	Branding
ADA4096-2ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2T
ADA4096-2ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2T
ADA4096-2ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2T
ADA4096-2ACPZ-R7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_UD]	CP-8-10	A4
ADA4096-2ACPZ-RL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_UD]	CP-8-10	A4
ADA4096-2WARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2T
ADA4096-2WARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2T
ADA4096-4ARUZ	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	
ADA4096-4ARUZ-R7	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	
ADA4096-4ARUZ-RL	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	
ADA4096-4ACPZ-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	A30
ADA4096-4ACPZ-RL	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	A30

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADA4096-2W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.