

50 V, 1 MHz, 165  $\mu$ A per Channel, Robust, Over-The-Top, Precision Op Amps

**FEATURES**

- ▶ Ultrawide common-mode input range:  $-V_S - 0.1$  V to  $-V_S + 70$  V
- ▶ Wide power supply voltage range: +3 V to +50 V (to  $\pm 25$  V for PSRR)
- ▶ Low power supply current: 165  $\mu$ A per channel (typical)
- ▶ Low input offset voltage:  $\pm 35$   $\mu$ V maximum
- ▶ Low input offset voltage drift:  $\pm 0.5$   $\mu$ V/ $^{\circ}$ C maximum (B grade)
- ▶ Low input voltage noise
  - ▶ 1/f noise corner: 6 Hz typical
  - ▶ 400 nV p-p typical at 0.1 Hz to 10 Hz
  - ▶ 17 nV/ $\sqrt{\text{Hz}}$  typical at 100 Hz
- ▶ High speed
  - ▶ GBP: 1.05 MHz typical for  $f_{\text{TEST}} = 2.5$  kHz
  - ▶ Slew rate: 0.85 V/ $\mu$ s typical at  $\Delta V_{\text{OUT}} = 25$  V
- ▶ Low power supply current shutdown: 20  $\mu$ A maximum
- ▶ Low input offset current:  $\pm 700$  pA maximum
- ▶ Large signal voltage gain: 126 dB minimum for  $\Delta V_{\text{OUT}} = 3.5$  V
- ▶ CMRR: 120 dB minimum at  $V_{\text{CM}} = -0.1$  V to +70 V
- ▶ PSRR: 123 dB minimum at  $V_{\text{SY}} = +3$  V to  $\pm 25$  V
- ▶ Input overdrive tolerant with no phase reversal
- ▶  $\pm 3$  kV HBM and  $\pm 1.25$  kV FICDM
- ▶ Wide temperature range:  $-55^{\circ}$ C to  $+150^{\circ}$ C (H grade)

**APPLICATIONS**

- ▶ Industrial sensor conditioning
- ▶ Supply current sensing
- ▶ Battery and power supply monitoring
- ▶ Front-end amplifiers in abusive environments
- ▶ 4 mA to 20 mA transmitters

**TYPICAL APPLICATION CIRCUIT**

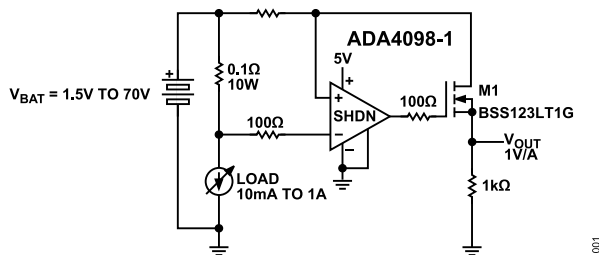


Figure 1. 1 V/A Over-The-Top Current Sense Application (ADA4098-1 6-Lead TSOT,  $V_{\text{BAT}}$  Is the Battery Voltage)

**GENERAL DESCRIPTION**

The ADA4098-1 and ADA4098-2 are single/dual robust, precision, rail-to-rail input and output operational amplifiers (op amps) with inputs that operate from  $-V_S$  to  $+V_S$  and beyond, which is referred to in this data sheet as Over-The-Top™. The devices feature offset voltages of  $< 35$   $\mu$ V, input bias currents ( $I_B$ ) of  $< 700$  pA, and can operate on single or split supplies that range from 3 V to 50 V. The ADA4098-1 and ADA4098-2 draw 165  $\mu$ A of supply current per channel.

The ADA4098-1 and ADA4098-2 Over-The-Top™ input stages have robust input protection features for abusive environments. The inputs can tolerate up to 80 V of differential voltage without damage or degradation to dc accuracy. The operating common-mode input range extends from rail-to-rail and beyond, up to  $70$  V  $> -V_S$ , independent of the  $+V_S$  supply.

The ADA4098-1 and ADA4098-2 are unity-gain stable and can drive loads requiring up to 20 mA per channel. The devices can also drive capacitive loads as large as 200 pF. The amplifiers are available with low power shutdown.

The ADA4098-1 is available in a standard, 6-lead thin small outline transistor (TSOT) package. The ADA4098-2 is available in an 8-lead standard small outline (SOIC\_N) package, 8-lead mini small outline package (MSOP), and 10-lead lead-frame chip-scale package (LFCSP).

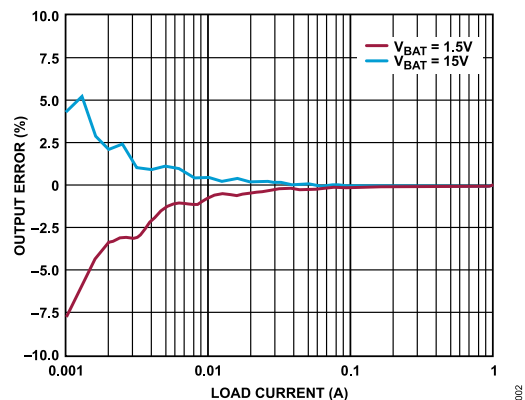


Figure 2. Output Error vs. Load Current

Rev. B

**DOCUMENT FEEDBACK**

**TECHNICAL SUPPORT**

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**TABLE OF CONTENTS**

Features.....	1	Output.....	22
Applications.....	1	Shutdown Pins (SHDN and SHDNx) .....	22
General Description.....	1	Applications Information.....	23
Typical Application Circuit.....	1	Large Resistor Gain Operation.....	23
Specifications.....	3	Recommended Values for Various Gains.....	23
5 V Supply.....	3	Noise.....	24
±15 V Supply.....	5	Distortion.....	24
Absolute Maximum Ratings.....	8	Power Dissipation and Thermal Shutdown.....	25
Maximum Power Dissipation.....	8	Circuit Layout Considerations.....	25
Thermal Resistance.....	8	Power Supply Bypassing.....	25
Electrostatic Discharge (ESD) Ratings.....	8	Grounding.....	26
ESD Caution.....	9	ESD Protection when Powered.....	26
Pin Configuration and Function Descriptions.....	10	Related Products.....	26
Typical Performance Characteristics.....	12	Typical Applications.....	27
Theory of Operation.....	20	Outline Dimensions.....	29
Input Protection.....	21	Ordering Guide.....	33
Over-The-Top Operation Considerations.....	21	Evaluation Boards.....	33

**REVISION HISTORY****5/2023—Rev. A to Rev. B**

Changes to Table 7.....	10
Changes to Table 8.....	11

**3/2022—Rev. 0 to Rev. A**

Added ADA4098-2.....	1
Change to Data Sheet Title.....	1
Changes to Features Section.....	1
Changes to General Description Section.....	1
Changes to 5 V Supply Section and Table 1.....	3
Changes to ±15 V Supply Section and Table 2.....	5
Changes to Table 3.....	8
Changes to Table 4.....	8
Changes to Table 5 and Table 5 Title.....	8
Changes to Figure 4 Title and Table 6 Title.....	10
Added Figure 5, Figure 6, Table 7, and Table 8; Renumbered Sequentially.....	10
Changes to Shutdown Pins (SHDN and SHDNx) Section and Title.....	22
Changes to Power Supply Bypassing Section.....	25
Changes to Table 10.....	26
Added Figure 75, Figure 76, and Figure 77.....	29
Changes to Ordering Guide.....	33
Added Evaluation Boards Section.....	33

**4/2021—Revision 0: Initial Version**

## SPECIFICATIONS

## 5 V SUPPLY

Common-mode voltage ( $V_{CM}$ ) = 2.5 V, SHDN pin (ADA4098-1) and SHDNx pins (ADA4098-2 10-lead LFCSP) are open, load resistance ( $R_L$ ) = 499 k $\Omega$  to midsupply, and ambient temperature ( $T_A$ ) = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	B Grade			H Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
DC PERFORMANCE								
Input Offset Voltage ( $V_{OS}$ ) <sup>1</sup>	0.25 V < $V_{CM}$ < 3.25 V		±15	±35		±15	±35	$\mu$ V
	Minimum temperature ( $T_{MIN}$ ) < $T_A$ < maximum temperature ( $T_{MAX}$ )			±90			±100	$\mu$ V
	0.25 V < $V_{CM}$ < 70 V		±20	±40		±20	±40	$\mu$ V
	0.25 V < $V_{CM}$ < 70 V (LFCSP)		±20	±200		±20	±200	$\mu$ V
	$T_{MIN}$ < $T_A$ < $T_{MAX}$			±135			±135	$\mu$ V
	-0.1 V < $V_{CM}$ < +70 V		±20	±40		±20	±40	$\mu$ V
	-0.1 V < $V_{CM}$ < +70 V (LFCSP)		±20	±200		±20	±200	$\mu$ V
Input Offset Voltage Drift <sup>2</sup>	$T_{MIN}$ < $T_A$ < $T_{MAX}$		±0.1	±0.5		±0.1	±0.8	$\mu$ V/°C
	$T_{MIN}$ < $T_A$ < $T_{MAX}$			±200			±250	$\mu$ V
Input Bias Current ( $I_B$ )	$T_{MIN}$ < $T_A$ < $T_{MAX}$		±0.35	±0.7		±0.35	±0.7	nA
	$T_{MIN}$ < $T_A$ < $T_{MAX}$			±10			±25	nA
	$V_{CM}$ = 70 V, Over-The-Top	3.5	8	12	3.5	8	12	$\mu$ A
	$T_{MIN}$ < $T_A$ < $T_{MAX}$	1.75		14.8	1.5		15	$\mu$ A
	0 V < $V_{CM}$ < 70 V, power supply voltage ( $V_{SY}$ ) = 0 V		0.001	1		0.001	1	$\mu$ A
Input Offset Current ( $I_{OS}$ )	$T_{MIN}$ < $T_A$ < $T_{MAX}$			10			10	$\mu$ A
	$T_{MIN}$ < $T_A$ < $T_{MAX}$		±350	±700		±350	±700	pA
	$T_{MIN}$ < $T_A$ < $T_{MAX}$			±5			±15	nA
	$V_{CM}$ = 70 V, Over-The-Top <sup>3</sup>		±0.05	±0.15		±0.05	±0.15	$\mu$ A
	$T_{MIN}$ < $T_A$ < $T_{MAX}$			±0.2			±0.2	$\mu$ A
Common-Mode Rejection Ratio (CMRR)	$V_{CM}$ = -0.1 V to +70 V	120	140		120	140		dB
	$T_{MIN}$ < $T_A$ < $T_{MAX}$	110			109			dB
	$V_{CM}$ = 0.25 V to 3.25 V	116	134		116	134		dB
	$T_{MIN}$ < $T_A$ < $T_{MAX}$	110			110			dB
Common-Mode Input Range	Guaranteed by CMRR tests	-0.1		+70	-0.1		+70	V
Large Signal Voltage Gain ( $A_{OL}$ )	Delta output voltage ( $\Delta V_{OUT}$ ) = 3.5 V	126	150		126	150		dB
	$T_{MIN}$ < $T_A$ < $T_{MAX}$	120			120			dB
	$\Delta V_{OUT}$ = 3.5 V, $R_L$ = 10 k $\Omega$	112	122		112	122		dB
	$T_{MIN}$ < $T_A$ < $T_{MAX}$	106			106			dB
NOISE PERFORMANCE								
Input Voltage Noise	Frequency (f) = 0.1 Hz to 10 Hz		400			400		nV p-p
	1/f noise corner		6			6		Hz
	f = 100 Hz		17			17		nV/ $\sqrt{\text{Hz}}$
Over-The-Top	f = 100 Hz, $V_{CM}$ > 5 V		20			20		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	f = 100 Hz		0.15			0.15		pA/ $\sqrt{\text{Hz}}$
	Over-The-Top	f = 100 Hz, $V_{CM}$ > 5 V		1.8		1.8		pA/ $\sqrt{\text{Hz}}$

## SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	B Grade			H Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
<b>DYNAMIC PERFORMANCE</b>								
Slew Rate	$\Delta V_{OUT} = 2\text{ V}$	0.15	0.4		0.15	0.4		V/ $\mu\text{s}$
	$T_{MIN} < T_A < T_{MAX}$	0.1			0.1			V/ $\mu\text{s}$
Gain Bandwidth Product (GBP)	Test frequency ( $f_{TEST}$ ) = 2.5 kHz	0.9	1.05		0.9	1.05		MHz
	$T_{MIN} < T_A < T_{MAX}$	0.9			0.9			MHz
Phase Margin			55			55		Degrees
1% Settling Time	$\Delta V_{OUT} = \pm 2\text{ V}$		14			14		$\mu\text{s}$
0.1% Settling Time	$\Delta V_{OUT} = \pm 2\text{ V}$		18			18		$\mu\text{s}$
Total Harmonic Distortion Plus Noise (THD + N)	$f = 10\text{ kHz}$ , $V_{OUT} = 1\text{ V p-p}$ , $R_L = 10\text{ k}\Omega$ , bandwidth = 80 kHz		0.01			0.01		%
Channel Separation	$f = 1\text{ kHz}$ , $R_L = 2\text{ k}\Omega$		115			115		dB
<b>INPUT CHARACTERISTICS</b>								
Input Resistance	Differential mode		1			1		M $\Omega$
	Common mode		>1			>1		G $\Omega$
Over-The-Top	Differential mode, $V_{CM} > 5\text{ V}$		7			7		k $\Omega$
	Common mode, $V_{CM} > 5\text{ V}$		>250			>250		M $\Omega$
Input Capacitance	Differential mode		1			1		pF
	Common mode		3			3		pF
<b>SHDN AND SHDNx PINS</b>								
Input Logic Low	Amplifier active, SHDN and SHDNx pin voltage ( $V_{SHDN}$ ) $< -V_S + 0.5\text{ V}$ , $T_{MIN} < T_A < T_{MAX}$			$-V_S + 0.5$			$-V_S + 0.5$	V
Input Logic High	Amplifier shutdown, $V_{SHDN} > -V_S + 1.5\text{ V}$ , $T_{MIN} < T_A < T_{MAX}$	$-V_S + 1.5$			$-V_S + 1.5$			V
Response Time	Amplifier active to shutdown		2.5			2.5		$\mu\text{s}$
	Amplifier shutdown to active		30			30		$\mu\text{s}$
Pull-Down Current	$V_{SHDN} = -V_S + 0.5\text{ V}$ , $T_{MIN} < T_A < T_{MAX}$		0.6	3		0.6	3	$\mu\text{A}$
	$V_{SHDN} = -V_S + 1.5\text{ V}$ , $T_{MIN} < T_A < T_{MAX}$		0.3	2.5		0.3	2.5	$\mu\text{A}$
<b>OUTPUT CHARACTERISTICS</b>								
Output Voltage Swing Low	Overdrive voltage ( $V_{OD}$ ) <sup>1</sup> = 30 mV, no load		20	45		20	45	mV
	$T_{MIN} < T_A < T_{MAX}$			50			55	mV
	$V_{OD} = 30\text{ mV}$ , sink current ( $I_{SINK}$ ) = 10 mA		260	360		260	360	mV
	$T_{MIN} < T_A < T_{MAX}$			435			450	mV
Output Voltage Swing High	$V_{OD} = 30\text{ mV}$ , no load		2.5	15		2.5	15	mV
	$T_{MIN} < T_A < T_{MAX}$			25			30	mV
	$V_{OD} = 30\text{ mV}$ , source current ( $I_{SOURCE}$ ) = 10 mA		900	1100		900	1100	mV
	$T_{MIN} < T_A < T_{MAX}$			1500			1650	mV
Short-Circuit Current	$I_{SOURCE}$	24	40		24	40		mA
	$T_{MIN} < T_A < T_{MAX}$	15			12			mA
	$I_{SINK}$	35	50		35	50		mA
	$T_{MIN} < T_A < T_{MAX}$	25			20			mA
Output Pin Leakage During Shutdown	$V_{SHDN} = -V_S + 1.5\text{ V}$		$\pm 0.01$	$\pm 100$		$\pm 0.01$	$\pm 100$	nA
	$T_{MIN} < T_A < T_{MAX}$			$\pm 10$			$\pm 10$	$\mu\text{A}$

## SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	B Grade			H Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
<b>POWER SUPPLY</b>								
Maximum Operating Voltage <sup>5</sup>				50			50	V
V <sub>SY</sub> Range	Guaranteed by Power Supply Rejection Ratio (PSRR)	3		50	3		50	V
Supply Current per Channel	Amplifier active		165	175		165	175	μA
	T <sub>MIN</sub> < T <sub>A</sub> < T <sub>MAX</sub>			242			250	μA
	Amplifier shutdown, V <sub>SHDN</sub> = -V <sub>S</sub> + 1.5 V		12	20		12	20	μA
PSRR	T <sub>MIN</sub> < T <sub>A</sub> < T <sub>MAX</sub>			22.5			22.5	μA
	V <sub>SY</sub> = +3 V to ±25 V	123	145		123	145		dB
	T <sub>MIN</sub> < T <sub>A</sub> < T <sub>MAX</sub>	120			120			dB
<b>THERMAL SHUTDOWN<sup>6</sup></b>								
Temperature	Junction temperature (T <sub>J</sub> )		175			175		°C
Hysteresis			20			20		°C
Operating Temperature	T <sub>A</sub>	-40		+125	-55		+150	°C

<sup>1</sup> Thermoelectric voltages present in the high speed production test limit the measurement accuracy of this parameter. The limits shown in Table 1 are determined by test capability and are not necessarily indicative of actual device performance.

<sup>2</sup> Offset voltage drift is guaranteed through lab characterization and is not production tested.

<sup>3</sup> Test accuracy is limited by high speed production test equipment repeatability. Bench measurements indicate that the input offset current in Over-The-Top configuration is typically controlled to under 50 nA at +25°C and 100 nA over the -55°C < T<sub>A</sub> < +150°C temperature range.

<sup>4</sup> V<sub>OD</sub> is +30 mV for V<sub>OUT</sub> high and -30 mV for V<sub>OUT</sub> low.

<sup>5</sup> Maximum operating voltage is limited by the time-dependent dielectric breakdown (TDDB) of the on-chip capacitor oxides. The amplifiers tolerate temporary transient overshoot up to the specified absolute maximum rating, but the dc supply voltage must be limited to the maximum operating voltage.

<sup>6</sup> Thermal shutdown is lab characterized only and is not tested in production.

**±15 V SUPPLY**

V<sub>CM</sub> = 0 V, SHDN pin (ADA4098-1) and SHDNx pins (ADA4098-2 10-lead LFCSP) are open, R<sub>L</sub> = 499 kΩ to ground, and T<sub>A</sub> = 25°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	B Grade			H Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
<b>DC PERFORMANCE</b>								
V <sub>OS</sub> <sup>1</sup>			±15	±40		±15	±40	μV
	T <sub>MIN</sub> < T <sub>A</sub> < T <sub>MAX</sub>			±90			±100	μV
	V <sub>SY</sub> = ±25 V		±15	±40		±15	±40	μV
Input Offset Voltage Drift <sup>2</sup>	T <sub>MIN</sub> < T <sub>A</sub> < T <sub>MAX</sub>			±90			±100	μV
	T <sub>MIN</sub> < T <sub>A</sub> < T <sub>MAX</sub>		±0.1	±0.5		±0.1	±0.8	μV/°C
Input Bias Current (I <sub>B</sub> )			±0.35	±0.7		±0.35	±0.7	nA
	T <sub>MIN</sub> < T <sub>A</sub> < T <sub>MAX</sub>			±10			±25	nA
	V <sub>SY</sub> = ±25 V		±0.35	±0.7		±0.35	±0.7	nA
I <sub>OS</sub>	T <sub>MIN</sub> < T <sub>A</sub> < T <sub>MAX</sub>			±10			±25	nA
			±0.35	±0.7		±0.35	±0.7	nA
	T <sub>MIN</sub> < T <sub>A</sub> < T <sub>MAX</sub>			±5			±15	nA
	V <sub>SY</sub> = ±25 V		±0.35	±0.7		±0.35	±0.7	nA
	T <sub>MIN</sub> < T <sub>A</sub> < T <sub>MAX</sub>			±5			±15	nA

## SPECIFICATIONS

Table 2. (Continued)

Parameter	Test Conditions/Comments	B Grade			H Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
CMRR	$V_{CM} = -14.75\text{ V to }+13.25\text{ V}$	118	135		118	135		dB
	$T_{MIN} < T_A < T_{MAX}$	116			116			dB
	$V_{CM} = -15.1\text{ V to }+13.25\text{ V}$	117	135		117	135		dB
	$T_{MIN} < T_A < T_{MAX}$	102			100			dB
	$V_{CM} = -15.1\text{ V to }+55\text{ V}$	120	140		120	140		dB
	$T_{MIN} < T_A < T_{MAX}$	110			108			dB
Common-Mode Input Range	Guaranteed by CMRR tests	-15.1		+55	-15.1		+55	V
AOL	$\Delta V_{OUT} = 25\text{ V}$	134	150		134	150		dB
	$T_{MIN} < T_A < T_{MAX}$	126			123			dB
	$\Delta V_{OUT} = 25\text{ V}, R_L = 10\text{ k}\Omega$	117	120		117	120		dB
	$T_{MIN} < T_A < T_{MAX}$	108			106			dB
NOISE PERFORMANCE								
Input Voltage Noise	$f = 0.1\text{ Hz to }10\text{ Hz}$		400			400		nV p-p
	1/f noise corner		6			6		Hz
	$f = 100\text{ Hz}$		17			17		nV/ $\sqrt{\text{Hz}}$
Over-The-Top	$f = 100\text{ Hz}, V_{CM} > +V_S$		20			20		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\text{ Hz}$		0.15			0.15		pA/ $\sqrt{\text{Hz}}$
	Over-The-Top	$f = 100\text{ Hz}, V_{CM} > +V_S$		1.8		1.8		pA/ $\sqrt{\text{Hz}}$
DYNAMIC PERFORMANCE								
Slew Rate	$\Delta V_{OUT} = 25\text{ V}$	0.35	0.85		0.35	0.85		V/ $\mu\text{s}$
	$T_{MIN} < T_A < T_{MAX}$	0.2			0.2			V/ $\mu\text{s}$
GBP	$f_{TEST} = 2.5\text{ kHz}$	0.9	1.05		0.9	1.05		MHz
	$T_{MIN} < T_A < T_{MAX}$	0.9			0.9			MHz
Phase Margin			57			57		Degrees
1% Settling Time	$\Delta V_{OUT} = \pm 2\text{ V}$		14			14		$\mu\text{s}$
0.1% Settling Time	$\Delta V_{OUT} = \pm 2\text{ V}$		18			18		$\mu\text{s}$
THD + N	$f = 10\text{ kHz}, V_{OUT} = 1\text{ V p-p}, R_L = 10\text{ k}\Omega, \text{bandwidth} = 80\text{ kHz}$		0.01			0.01		%
Channel Separation	$f = 1\text{ kHz}, R_L = 2\text{ k}\Omega$		115			115		dB
INPUT CHARACTERISTICS								
Input Resistance	Differential mode		1			1		M $\Omega$
	Common mode		>1			>1		G $\Omega$
Input Capacitance	Differential mode		1			1		pF
	Common mode		3			3		pF
SHDN AND SHDNx PINS								
Input Logic Low	Amplifier active, $V_{SHDN} < -V_S + 0.5\text{ V}$			$-V_S + 0.5$			$-V_S + 0.5$	V
Input Logic High	Amplifier shutdown, $V_{SHDN} > -V_S + 1.5\text{ V}$	$-V_S + 1.5$			$-V_S + 1.5$			V
Response Time	Amplifier active to shutdown		2.5			2.5		$\mu\text{s}$
	Amplifier shutdown to active		30			30		$\mu\text{s}$
Pull-Down Current	$V_{SHDN} = -V_S + 0.5\text{ V}, T_{MIN} < T_A < T_{MAX}$	0.6	3		0.6	3		$\mu\text{A}$
	$V_{SHDN} = -V_S + 1.5\text{ V}, T_{MIN} < T_A < T_{MAX}$	0.3	2.5		0.3	2.5		$\mu\text{A}$

## SPECIFICATIONS

Table 2. (Continued)

Parameter	Test Conditions/Comments	B Grade			H Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
OUTPUT CHARACTERISTICS								
Output Voltage Swing Low	$V_{OD}^3 = 30 \text{ mV}$ , no load $T_{MIN} < T_A < T_{MAX}$		20	45		20	45	mV
	$V_{OD} = 30 \text{ mV}$ , $I_{SINK} = 10 \text{ mA}$ $T_{MIN} < T_A < T_{MAX}$		260	360		260	360	mV
Output Voltage Swing High	$V_{OD} = 30 \text{ mV}$ , no load $T_{MIN} < T_A < T_{MAX}$		2.5	15		2.5	15	mV
	$V_{OD} = 30 \text{ mV}$ , $I_{SOURCE} = 10 \text{ mA}$ $T_{MIN} < T_A < T_{MAX}$		900	1100		900	1100	mV
	$T_{MIN} < T_A < T_{MAX}$			1500			1650	mV
Short-Circuit Current	$I_{SOURCE}$ $T_{MIN} < T_A < T_{MAX}$	24	34		24	34		mA
	$I_{SINK}$ $T_{MIN} < T_A < T_{MAX}$	15			12			mA
		35	50		35	50		mA
		20			20			mA
POWER SUPPLY								
Maximum Operating Voltage <sup>4</sup>				50			50	V
$V_{SY}$ Range	Guaranteed by PSRR	3		50	3		50	V
Supply Current per Channel	Amplifier active $T_{MIN} < T_A < T_{MAX}$		185	205		185	205	$\mu\text{A}$
	$V_{SY} = \pm 25 \text{ V}$ $T_{MIN} < T_A < T_{MAX}$		195	215		195	215	$\mu\text{A}$
	Amplifier shutdown, $V_{SHDN} = -V_S + 1.5 \text{ V}$ $T_{MIN} < T_A < T_{MAX}$		17	24		17	24	$\mu\text{A}$
				27			27	$\mu\text{A}$
PSRR	$V_{SY} = 3 \text{ V to } 50 \text{ V}$ $T_{MIN} < T_A < T_{MAX}$	123	145		123	145		dB
		120			120			dB
THERMAL SHUTDOWN <sup>5</sup>								
Temperature	$T_J$		175			175		$^{\circ}\text{C}$
Hysteresis			20			20		$^{\circ}\text{C}$
Operating Temperature	$T_A$	-40		+125	-55		+150	$^{\circ}\text{C}$

<sup>1</sup> Thermoelectric voltages present in the high speed production test limit the measurement accuracy of this parameter. The limits shown in Table 2 are determined by test capability and are not necessarily indicative of actual device performance.

<sup>2</sup> Offset voltage drift is guaranteed through lab characterization and is not production tested.

<sup>3</sup>  $V_{OD}$  is +30 mV for  $V_{OUT}$  high and -30 mV for  $V_{OUT}$  low.

<sup>4</sup> Maximum operating voltage is limited by the TDDB of the on-chip capacitor oxides. The amplifiers tolerate temporary transient overshoot up to the specified absolute maximum rating and the dc supply voltage must be limited to the maximum operating voltage.

<sup>5</sup> Thermal shutdown is lab characterized only and is not tested in production.

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage <sup>1</sup>	
Transient	60 V
Continuous	50 V
Power Dissipation ( $P_D$ )	See Figure 3
Differential Input Voltage	$\pm 80$ V
$\pm$ IN Pin Voltage	
Continuous	-10 V to +80 V
Survival	-20 V to +80 V
$\pm$ IN Pin Current	15 mA
SHDN and SHDNx Pin Voltage <sup>2</sup>	-0.3 V to +60 V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
$T_J$	175°C

<sup>1</sup> Maximum supply voltage is limited by the TDDB of the on-chip capacitor oxides. The amplifiers tolerate temporary transient overshoot up to the specified transient maximum rating. The continuous operating supply voltage must be limited to no more than 50 V.

<sup>2</sup> SHDN is Pin 5 on the ADA4098-1. SHDNx refers to SHDN1 and SHDN2 (Pin 5 and Pin 6, respectively) on the ADA4098-2 (10-lead LFCSP).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Junction temperatures ( $T_J$ ) exceeding 125°C promotes accelerated aging. The ADA4098-1 and ADA4098-2 demonstrate  $\pm 25$  V supply operation beyond 1000 hours at  $T_A = 150^\circ\text{C}$ .

## MAXIMUM POWER DISSIPATION

The maximum safe  $P_D$  on the devices is limited by the associated rise in either case temperature ( $T_C$ ) or  $T_J$  on the die. At approximately  $T_C = 150^\circ\text{C}$ , which is the glass transition temperature, the properties of the plastic changes. Exceeding this temperature limit, even temporarily, may change the stresses that the package exerts on the die, which permanently shifts the parametric performance of the ADA4098-1 and ADA4098-2. Exceeding  $T_J = 175^\circ\text{C}$  for an extended period may result in changes in the silicon devices and may potentially cause failure of the devices.

The  $P_D$  on the package is the sum of the quiescent power dissipation and the power dissipated in the package due to the output load drive. The quiescent power is expressed as  $V_{SY} \times I_{SY}$ , where  $I_{SY}$  is the quiescent current.

The  $P_D$  due to the load drive depends on the application. The  $P_D$  due to load drive is calculated by multiplying the load current by the associated voltage drop across the devices. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing  $\theta_{JA}$ . Additional metal that is directly in contact with the package leads from metal traces through vias, ground, and power planes reduces  $\theta_{JA}$ .

Figure 3 shows the maximum  $P_D$  vs.  $T_A$  for the single and dual 6-lead TSOT packages on a JEDEC standard, 4-layer board, with  $-V_S$  connected to a pad that is thermally connected to a printed circuit board (PCB) plane.  $\theta_{JA}$  values are approximations.

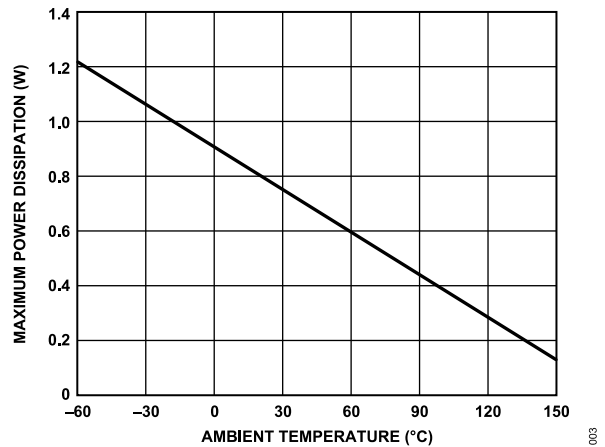


Figure 3. Maximum Power Dissipation vs. Ambient Temperature

## THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$  is the junction to ambient thermal resistance.

Table 4. Thermal Resistance

Package Type	$\theta_{JA}$	Unit
UJ-6	192	$^\circ\text{C}/\text{W}$
R-8	120	$^\circ\text{C}/\text{W}$
RM-8	163	$^\circ\text{C}/\text{W}$
05-08-1699	43	$^\circ\text{C}/\text{W}$

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

## ESD Ratings for ADA4098-1/ADA4098-2

Table 5. ADA4098-1 6-Lead TSOT, ADA4098-2 8-Lead SOIC\_N, ADA4098-2 8-Lead MSOP, ADA4098-2 10-Lead LFCSP

ESD Model	Withstand Threshold (kV)	Class
HBM	$\pm 3$	2
FICDM	$\pm 1.25$	3



**ABSOLUTE MAXIMUM RATINGS****ESD CAUTION**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**PIN CONFIGURATION AND FUNCTION DESCRIPTIONS**

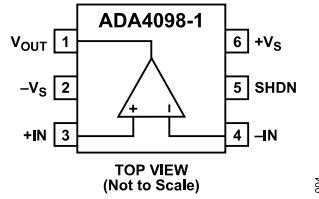


Figure 4. Pin Configuration for ADA4098-1 6-Lead TSOT

Table 6. Pin Function Descriptions for ADA4098-1 6-Lead TSOT

Pin No.	Mnemonic	Description
1	V <sub>OUT</sub>	Amplifier Output.
2	-V <sub>S</sub>	Negative Power Supply. In single-supply applications, the -V <sub>S</sub> pin is normally soldered to a low impedance ground plane. In split-supply applications, bypass the -V <sub>S</sub> pin with a capacitance of at least 0.1 μF to a low impedance ground plane, as close to the -V <sub>S</sub> pin as possible.
3	+IN	Noninverting Input of the Amplifier.
4	-IN	Inverting Input of the Amplifier.
5	SHDN	Op Amp Shutdown. The threshold for shutdown is approximately 1 V above the negative supply. If the SHDN pin is hard tied to the -V <sub>S</sub> pin or floating, the amplifier is active. If the SHDN pin is asserted high (V <sub>SHDN</sub> > -V <sub>S</sub> + 1.5 V), the amplifier is placed in a shutdown state, and the output of the amplifier goes to a high impedance state. If the SHDN pin is left floating, it is recommended to connect a small capacitor of 1 nF between the SHDN pin and the -V <sub>S</sub> pin to prevent signals from the -IN pin from capacitively coupling to the SHDN pin.
6	+V <sub>S</sub>	Positive Power Supply. Bypass the +V <sub>S</sub> pin with a capacitance of at least 0.1 μF to a low impedance ground plane, as close to the +V <sub>S</sub> pin as possible.

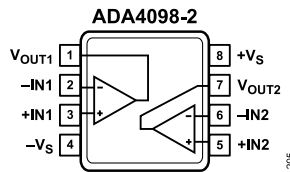


Figure 5. Pin Configuration for ADA4098-2 8-Lead SOIC\_N and 8-Lead MSOP

Table 7. Pin Function Descriptions for ADA4098-2 8-Lead SOIC\_N and 8-Lead MSOP

Pin No.	Mnemonic	Description
1	V <sub>OUT1</sub>	Amplifier Output, Channel 1.
2	-IN1	Inverting Input of the Amplifier, Channel 1.
3	+IN1	Noninverting Input of the Amplifier, Channel 1.
4	-V <sub>S</sub>	Negative Power Supply. In single-supply applications, the -V <sub>S</sub> pin is normally soldered to a low impedance ground plane. In split-supply applications, bypass the -V <sub>S</sub> pin with a capacitance of at least 0.1 μF to a low impedance ground plane, as close to the -V <sub>S</sub> pin as possible.
5	+IN2	Noninverting Input of the Amplifier, Channel 2
6	-IN2	Inverting Input of the Amplifier, Channel 2.
7	V <sub>OUT2</sub>	Amplifier Output, Channel 2.
8	+V <sub>S</sub>	Positive Power Supply. Bypass the +V <sub>S</sub> pin with a capacitance of at least 0.1 μF to a low impedance ground plane, as close to the +V <sub>S</sub> pin as possible.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

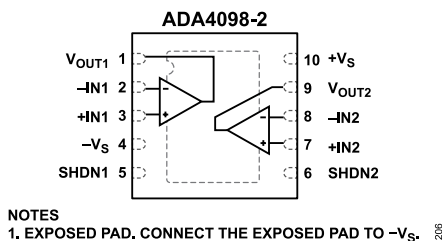


Figure 6. Pin Configuration for ADA4098-2 10-Lead LFCSP

Table 8. Pin Function Descriptions for ADA4098-2 10-Lead LFCSP

Pin No.	Mnemonic	Description
1	$V_{OUT1}$	Amplifier Output, Channel 1.
2	$-IN1$	Inverting Input of the Amplifier, Channel 1.
3	$+IN1$	Noninverting Input of the Amplifier, Channel 1.
4	$-V_S$	Negative Power Supply. In single-supply applications, the $-V_S$ pin is normally soldered to a low impedance ground plane. In split-supply applications, bypass the $-V_S$ pin with a capacitance of at least 0.1 $\mu\text{F}$ to a low impedance ground plane, as close to the $-V_S$ pin as possible.
5	SHDN1	Op Amp Shutdown, Channel 1. The threshold for shutdown is approximately 1 V above the negative supply. If the SHDN1 pin is hard tied to the $-V_S$ pin or floating, the amplifier is active. If the SHDN1 pin is asserted high ( $V_{SHDN} > -V_S + 1.5\text{ V}$ ), the amplifier is placed in a shutdown state, and the output of the amplifier goes to a high impedance state. If the SHDN1 pin is left floating, it is recommended to connect a small capacitor of 1 nF between the SHDN1 pin and the $-V_S$ pin to prevent signals from the $-INx$ pins from capacitively coupling to the SHDN1 pin.
6	SHDN2	Op Amp Shutdown, Channel 2. The threshold for shutdown is approximately 1 V above the negative supply. If the SHDN2 pin is hard tied to the $-V_S$ pin or floating, the amplifier is active. If the SHDN2 pin is asserted high ( $V_{SHDN} > -V_S + 1.5\text{ V}$ ), the amplifier is placed in a shutdown state, and the output of the amplifier goes to a high impedance state. If the SHDN2 pin is left floating, it is recommended to connect a small capacitor of 1 nF between the SHDN2 pin and the $-V_S$ pin to prevent signals from the $-INx$ pins from capacitively coupling to the SHDN2 pin.
7	$+IN2$	Noninverting Input of the Amplifier, Channel 2.
8	$-IN2$	Inverting Input of the Amplifier, Channel 2.
9	$V_{OUT2}$	Amplifier Output, Channel 2.
10	$+V_S$	Positive Power Supply. Bypass the $+V_S$ pin with a capacitance of at least 0.1 $\mu\text{F}$ to a low impedance ground plane, as close to the $+V_S$ pin as possible.
	EPAD	Exposed Pad. Connect the exposed pad to $-V_S$ .

TYPICAL PERFORMANCE CHARACTERISTICS

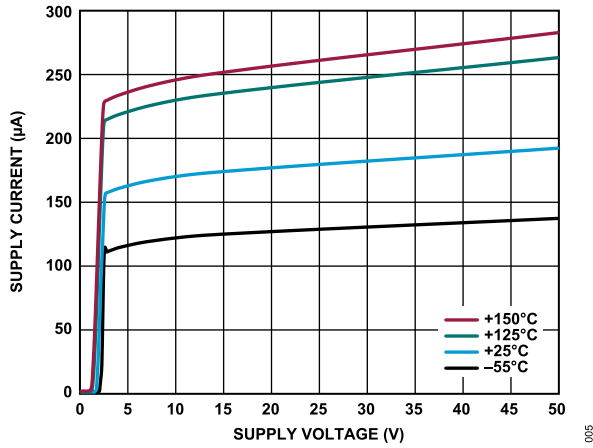


Figure 7. Supply Current vs. Supply Voltage

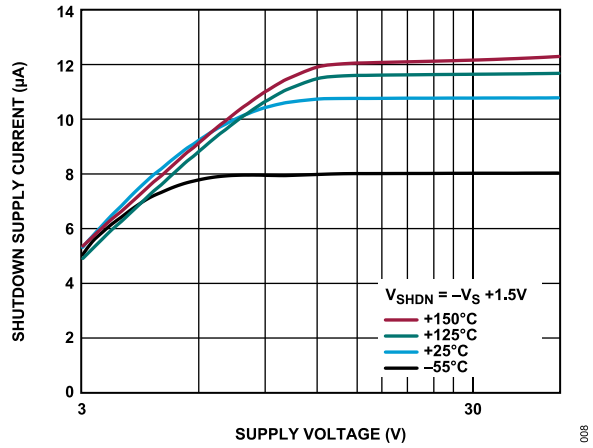


Figure 10. Shutdown Supply Current vs. Supply Voltage

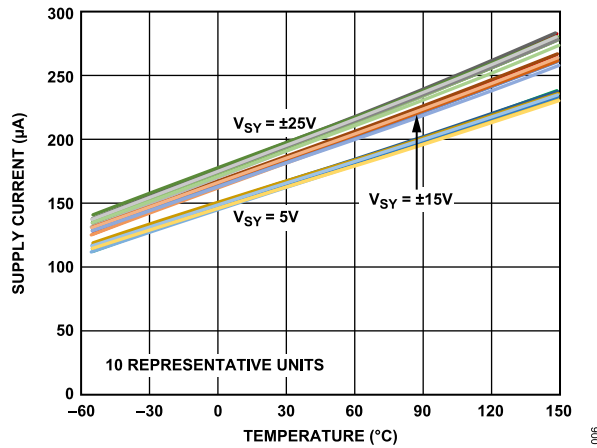


Figure 8. Supply Current vs. Temperature Across Various Supply Voltages

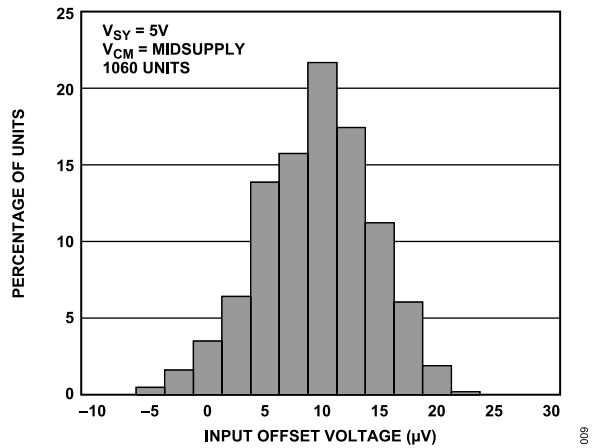


Figure 11. Typical Distribution of Input Offset Voltage,  $V_{SY} = 5V$

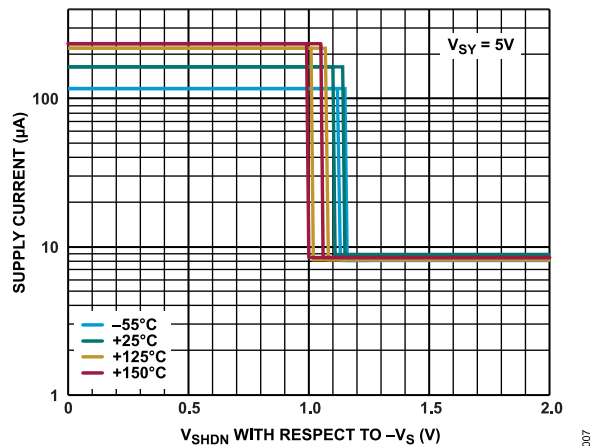


Figure 9. Supply Current vs.  $V_{SHDN}$  with Respect to  $-V_S$

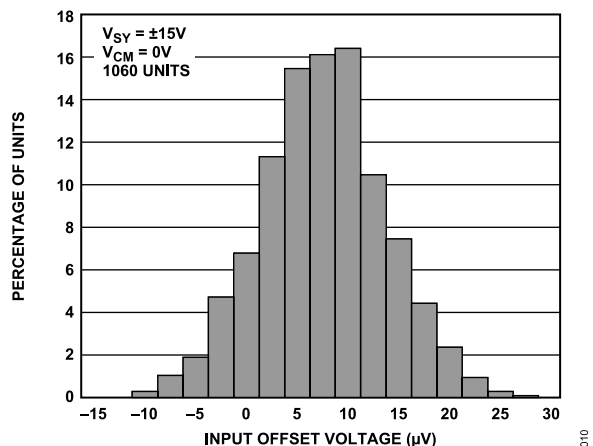


Figure 12. Typical Distribution of Input Offset Voltage with  $V_{SY} = \pm 15V$

TYPICAL PERFORMANCE CHARACTERISTICS

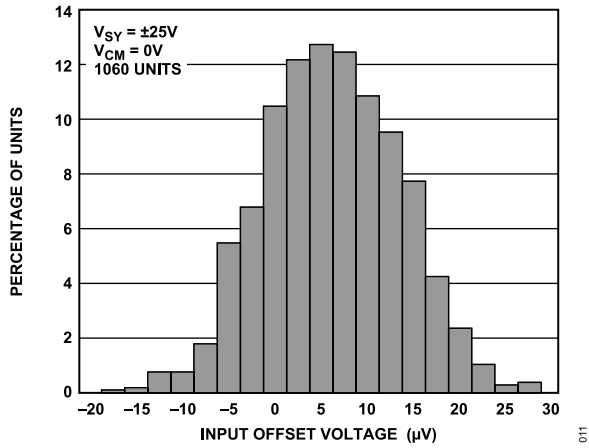


Figure 13. Typical Distribution of Input Offset Voltage with  $V_{SY} = \pm 25\text{ V}$

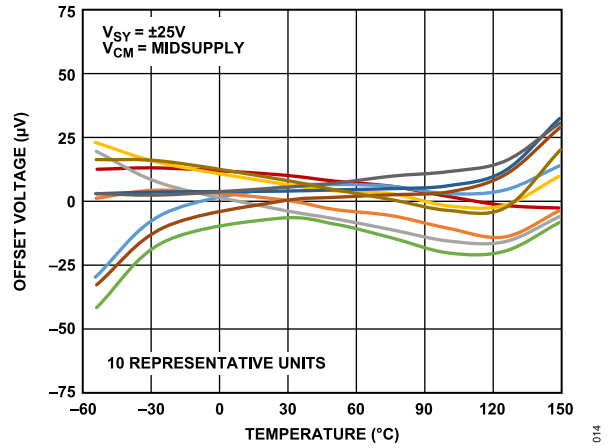


Figure 16. Midsupply Offset Voltage vs. Temperature with  $V_{SY} = \pm 25\text{ V}$

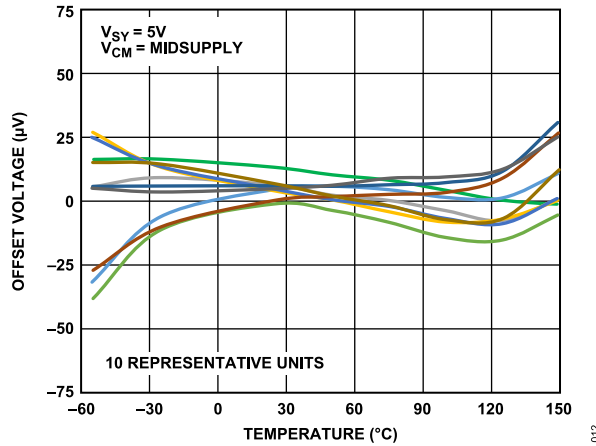


Figure 14. Midsupply Offset Voltage vs. Temperature with  $V_{SY} = 5\text{ V}$

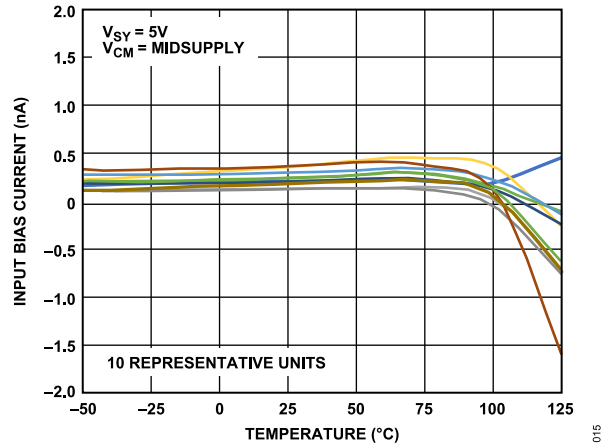


Figure 17. Midsupply Input Bias Current vs. Temperature with  $V_{SY} = 5\text{ V}$

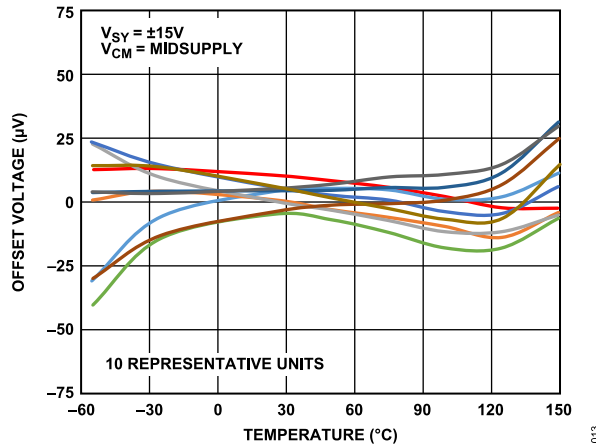


Figure 15. Midsupply Offset Voltage vs. Temperature with  $V_{SY} = \pm 15\text{ V}$

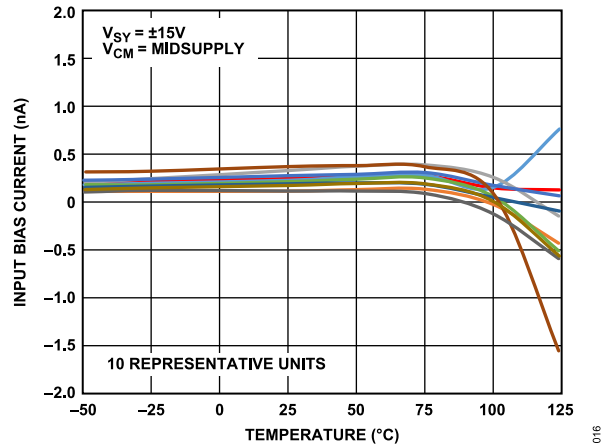


Figure 18. Midsupply Input Bias Current vs. Temperature with  $V_{SY} = \pm 15\text{ V}$

TYPICAL PERFORMANCE CHARACTERISTICS

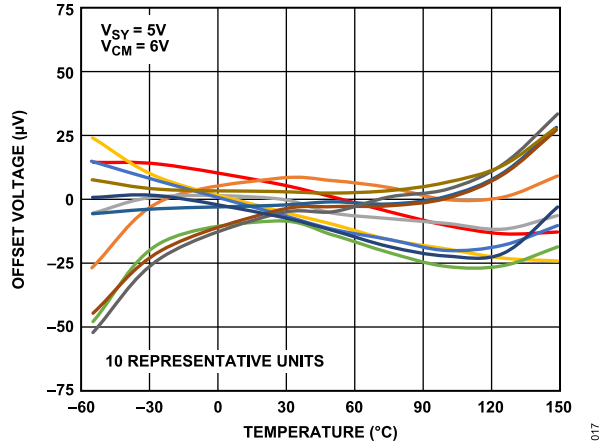


Figure 19. Offset Voltage vs. Temperature with  $V_{CM} = 6\text{ V}$ , Over-The-Top

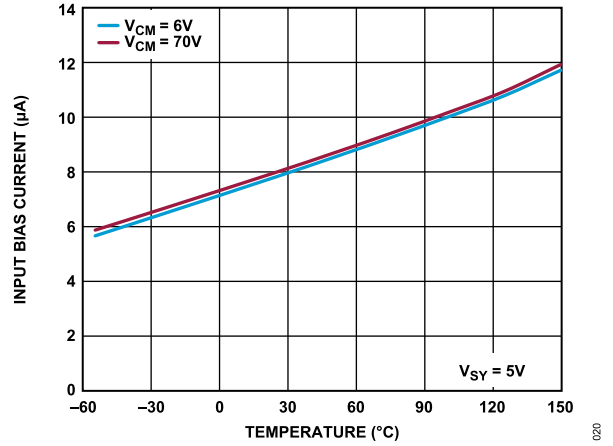


Figure 22. Input Bias Current vs. Temperature with  $V_{SY} = 5\text{ V}$ , Over-The-Top

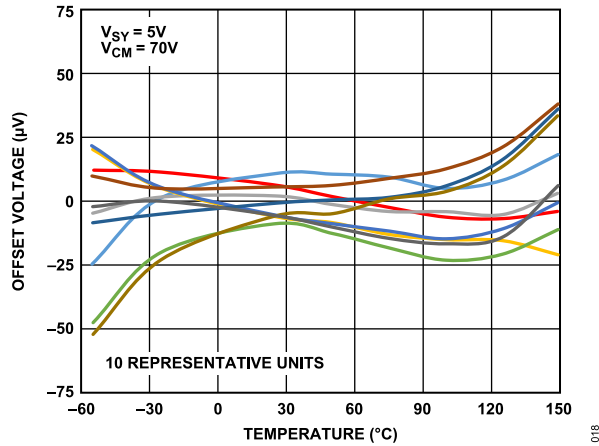


Figure 20. Offset Voltage vs. Temperature with  $V_{CM} = 70\text{ V}$

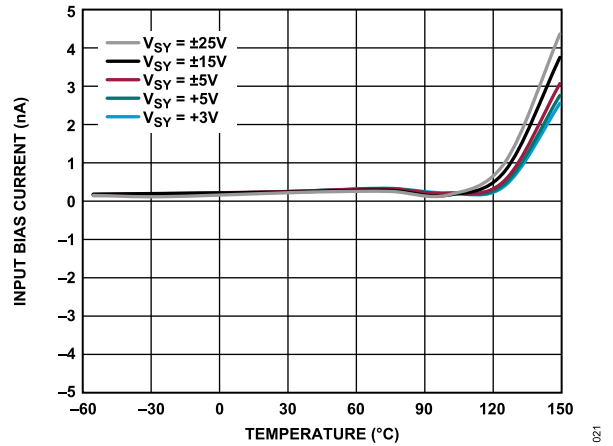


Figure 23. Midsupply Input Bias Current vs. Temperature Across Various Supply Voltages

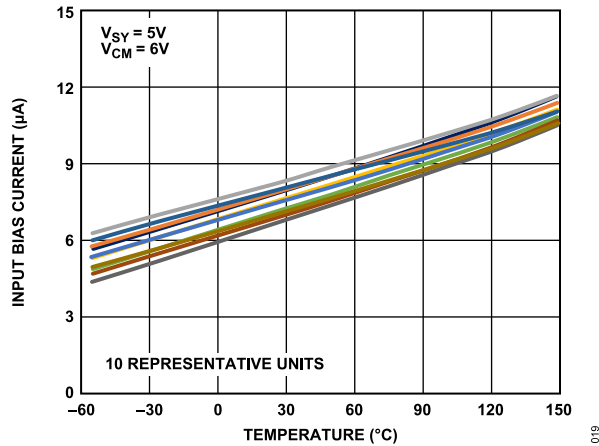


Figure 21. Over-The-Top Input Bias Current vs. Temperature with  $V_{CM} = 6\text{ V}$

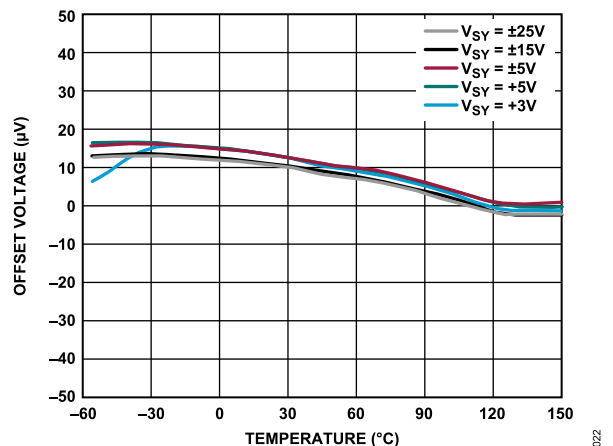


Figure 24. Offset Voltage vs. Temperature Across Various Supply Voltages

TYPICAL PERFORMANCE CHARACTERISTICS

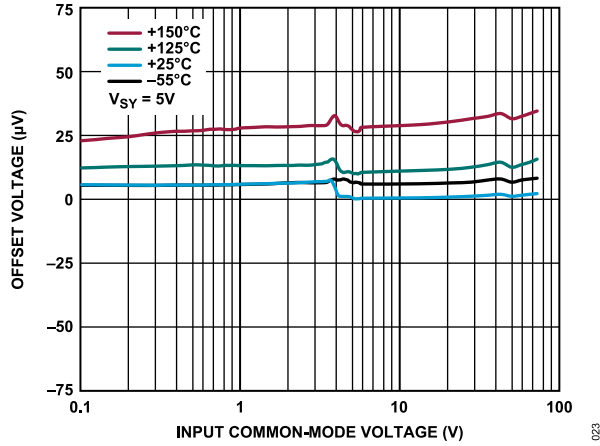


Figure 25. Offset Voltage vs. Input Common-Mode Voltage over the Input Common-Mode Range

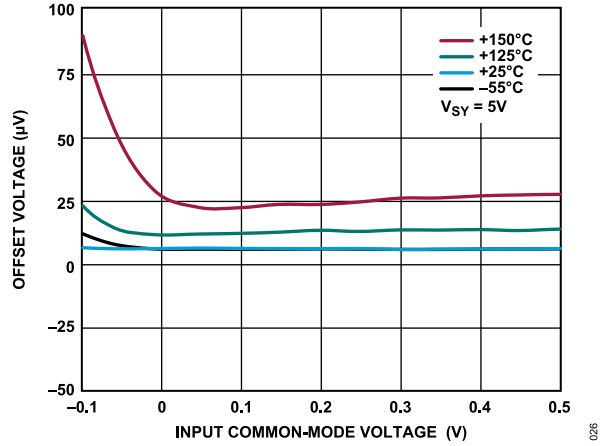


Figure 28. Offset Voltage vs. Input Common-Mode Voltage for Ground Sensing Applications

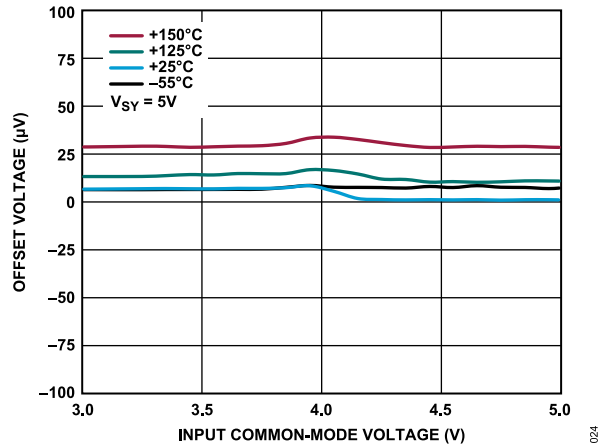


Figure 26. Offset Voltage vs. Input Common-Mode Voltage from Normal Operation to Over-The-Top Operation

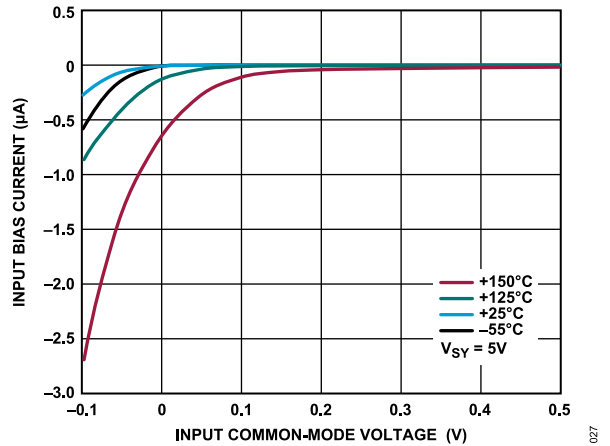


Figure 29. Input Bias Current vs. Input Common-Mode Voltage for Ground Sensing Applications

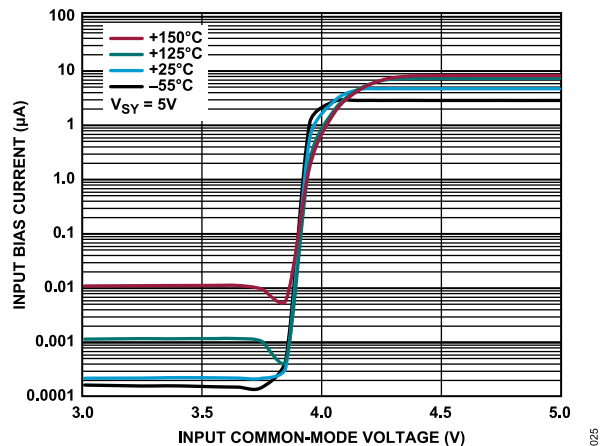


Figure 27. Input Bias Current vs. Input Common-Mode Voltage from Normal Operation to Over-The-Top Operation

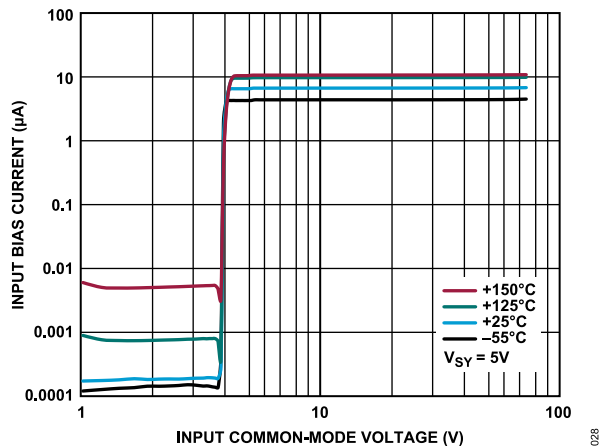


Figure 30. Input Bias Current vs. Input Common-Mode Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

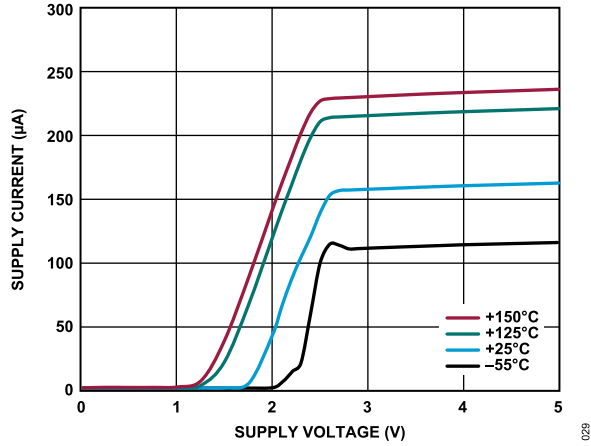


Figure 31. Supply Current vs. Minimum Supply Voltage

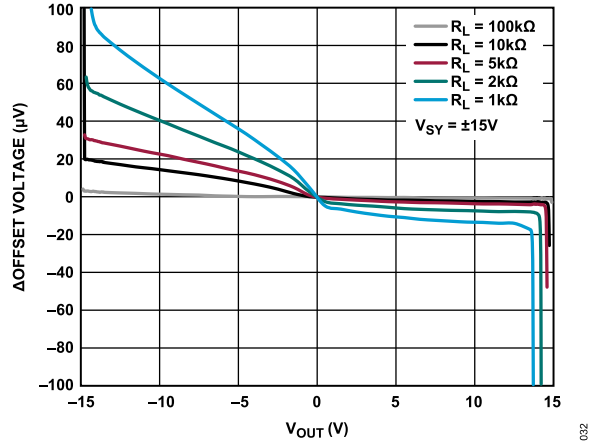


Figure 34. ΔOffset Voltage vs.  $V_{OUT}$

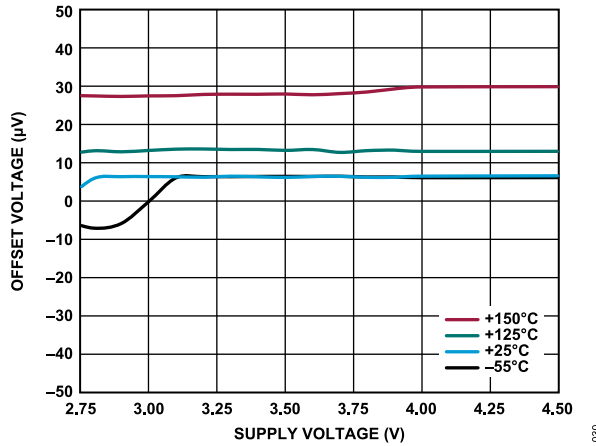


Figure 32. Offset Voltage vs. Minimum Supply Voltage

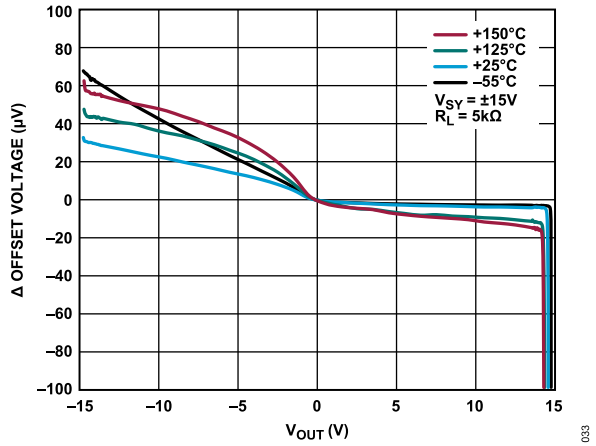


Figure 35. ΔOffset Voltage vs.  $V_{OUT}$  (5 kΩ Load)

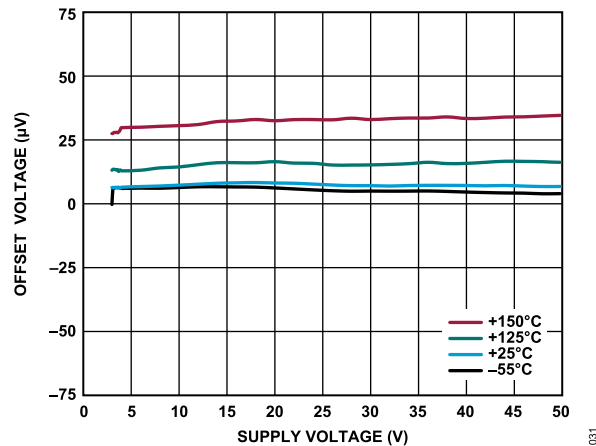


Figure 33. Offset Voltage vs. Supply Voltage

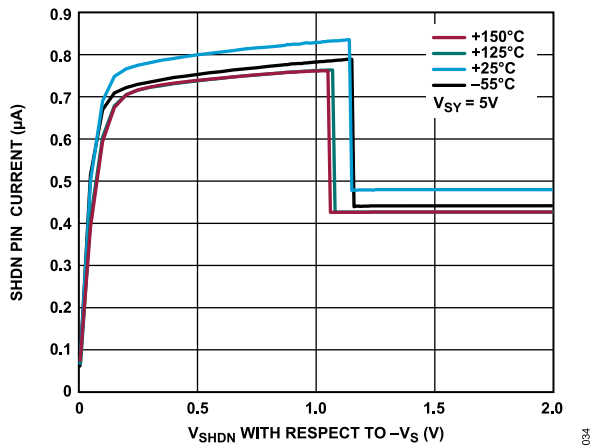


Figure 36. SHDN Pin Current vs.  $V_{SHDN}$  with Respect to  $-V_S$  over Various Temperatures



TYPICAL PERFORMANCE CHARACTERISTICS

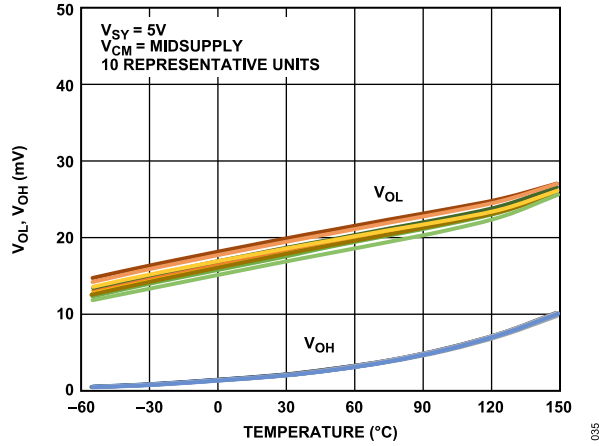


Figure 37. Output Voltage Low ( $V_{OL}$ ) and Output Voltage High ( $V_{OH}$ ) vs. Temperature

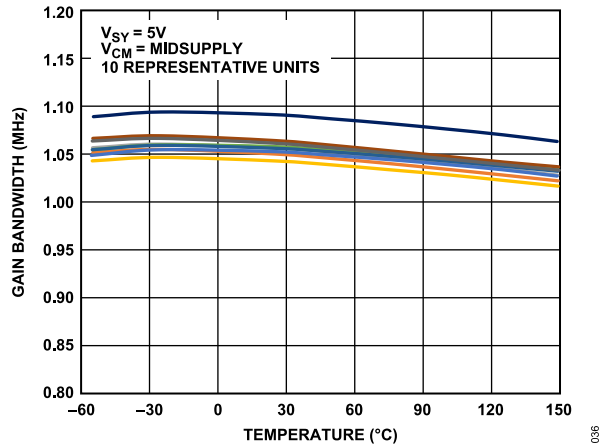


Figure 38. Gain Bandwidth vs. Temperature

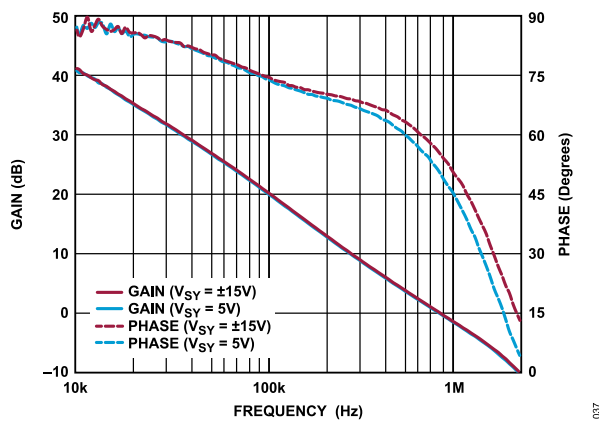


Figure 39. Loop Gain and Phase vs. Frequency

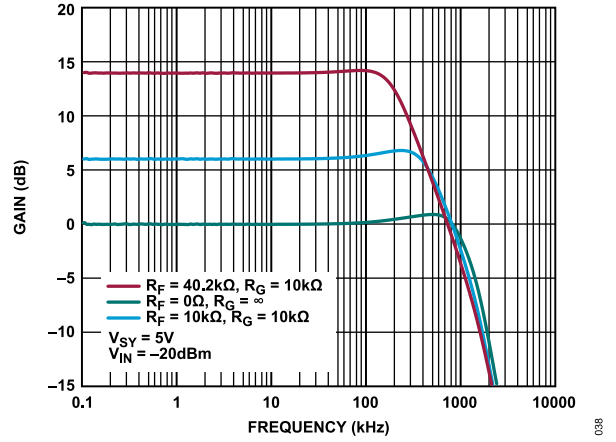


Figure 40. Noninverting Small Signal Frequency Response ( $R_F$  Is the Feedback Resistor,  $R_G$  Is the Gain Setting Resistor, and  $V_{IN}$  Is the Input Voltage)

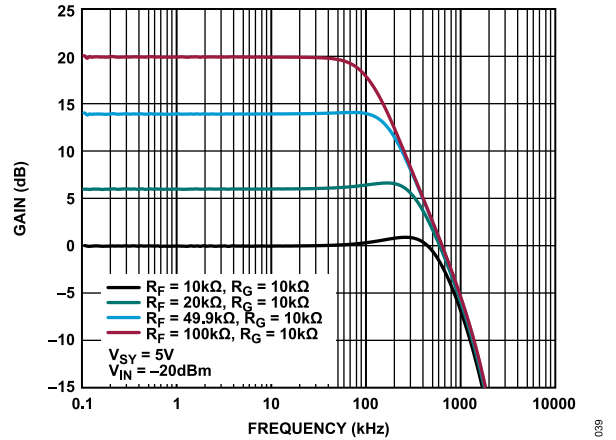


Figure 41. Inverting Small Signal Frequency Response

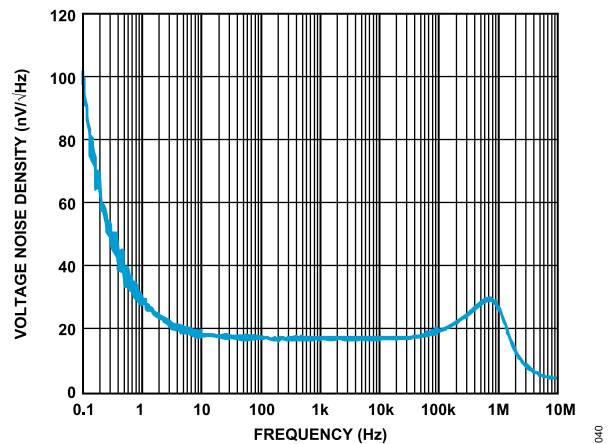


Figure 42. Voltage Noise Density vs. Frequency for a Unity-Gain Configuration

TYPICAL PERFORMANCE CHARACTERISTICS

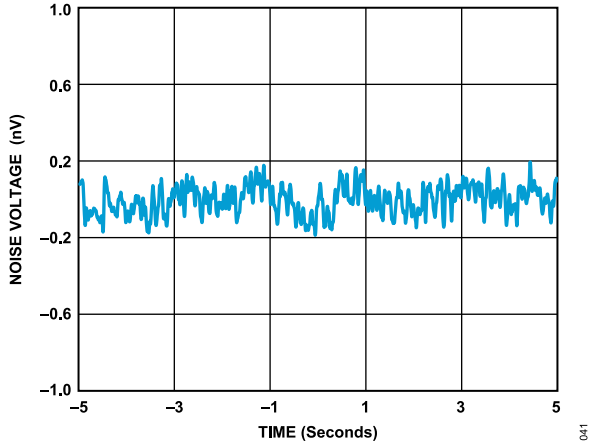


Figure 43. 0.1 Hz to 10 Hz Noise

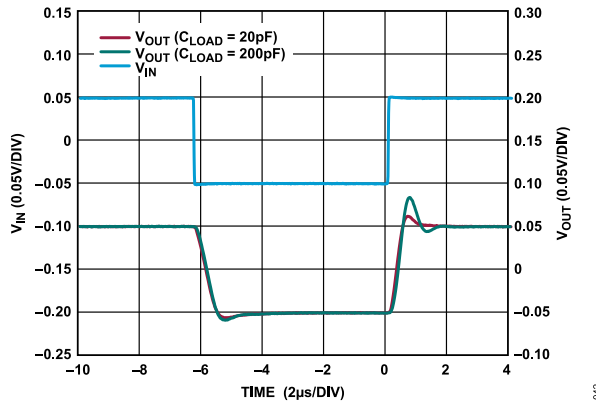


Figure 44. Unity-Gain Small Signal Step Response ( $C_{LOAD}$  Is the Load Capacitor)

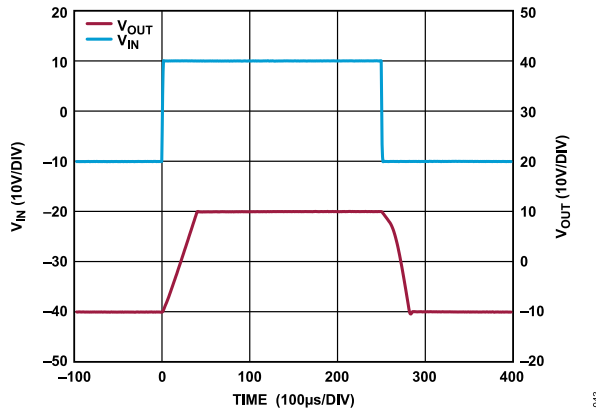


Figure 45. Unity-Gain Large Signal Step Response

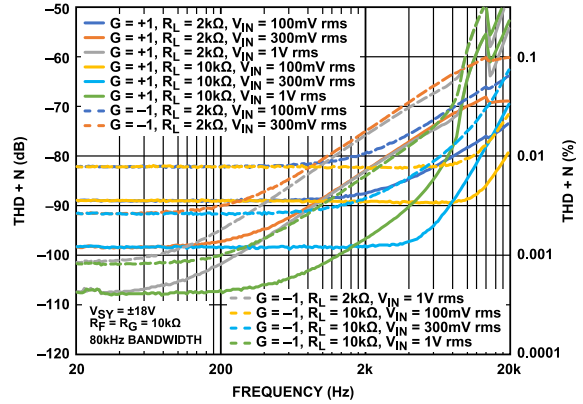


Figure 46. THD + N vs. Frequency over Load

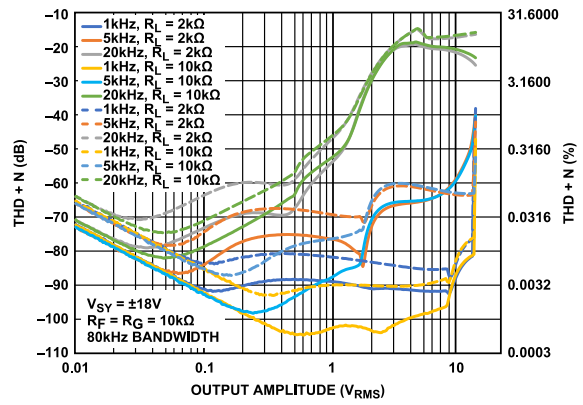


Figure 47. THD + N vs. Output Amplitude

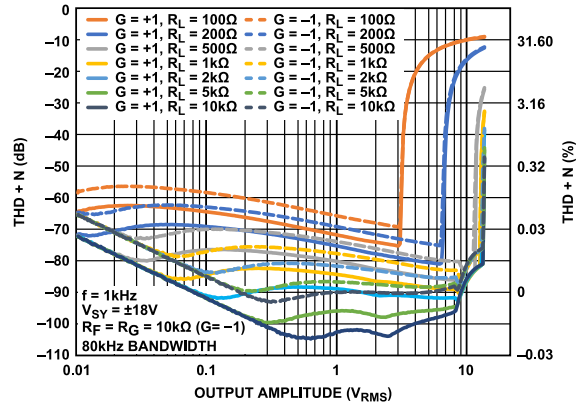


Figure 48. THD + N vs. Output Amplitude and Load

TYPICAL PERFORMANCE CHARACTERISTICS

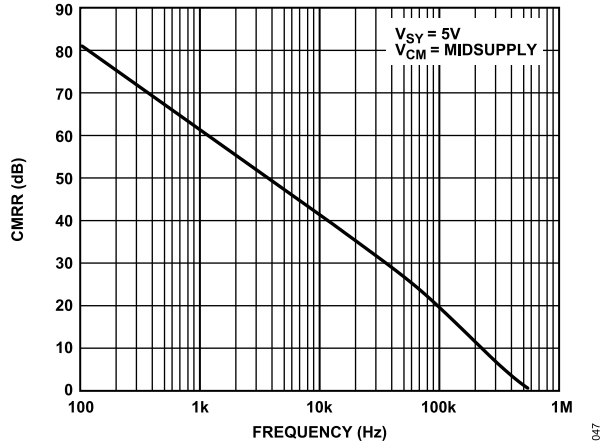


Figure 49. CMRR vs. Frequency

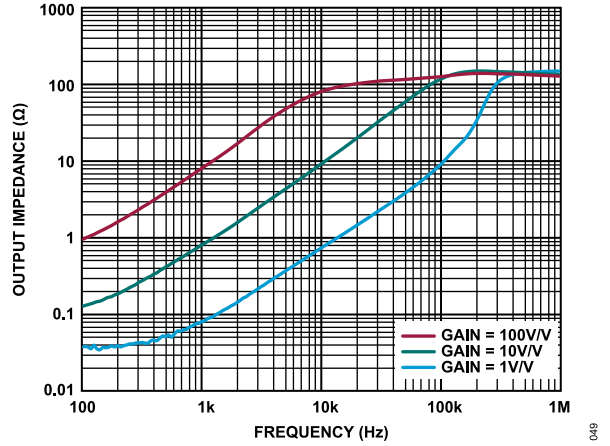


Figure 51. Output Impedance vs. Frequency

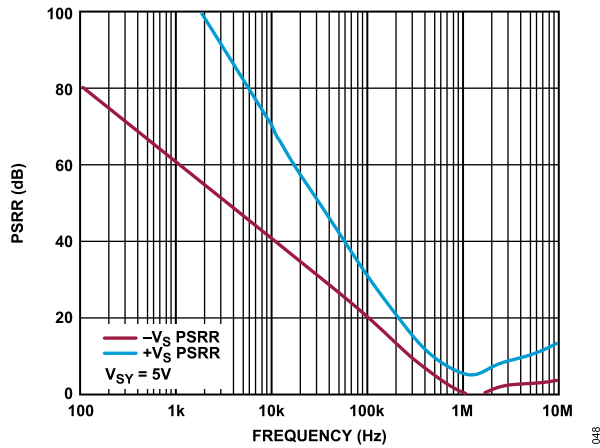


Figure 50. PSRR vs. Frequency

**THEORY OF OPERATION**

The ADA4098-1 and ADA4098-2 are robust, voltage feedback amplifiers that combine unity-gain stability with low offset, low offset drift, and 17 nV/ $\sqrt{\text{Hz}}$  of input voltage noise. Figure 54 shows a simplified schematic of the devices. The ADA4098-1 and ADA4098-2 have two input stages: a common emitter differential input stage consisting of the Q1 and Q2 PNP transistors that operate with the inputs biased between  $-V_S$  and 1.25 V below  $+V_S$ , and a common base input stage that consists of the Q3 to Q6 PNP transistors that operate when the common-mode input is biased  $>+V_S - 1.25$  V. These input stages result in two distinct operating regions, as shown in Figure 52.

For common-mode input voltages that are approximately 1.25 V below the  $+V_S$  supply, where Q1 and Q2 are active (see Figure 52), the common emitter PNP input stage is active and the input bias current is typically  $<700$  pA. When the common-mode input is above  $+V_S - 1.25$  V, the Q9 transistor turns on, which diverts bias current away from the common emitter differential input pair to the mirror that consists of M3 and M4. The current from M4 biases the common base differential input pair (Q3 to Q6). The Over-The-Top input pair operates in a common base configuration and the input bias current increases to  $\sim 8$   $\mu\text{A}$ . The offset voltages of both input stages are tightly trimmed and are specified in Table 1 and Table 2.

As the input common-mode transitions to the Over-The-Top region, the input CMRR degrades slightly when compared to the rest of the input common-mode range, as shown in Figure 53.

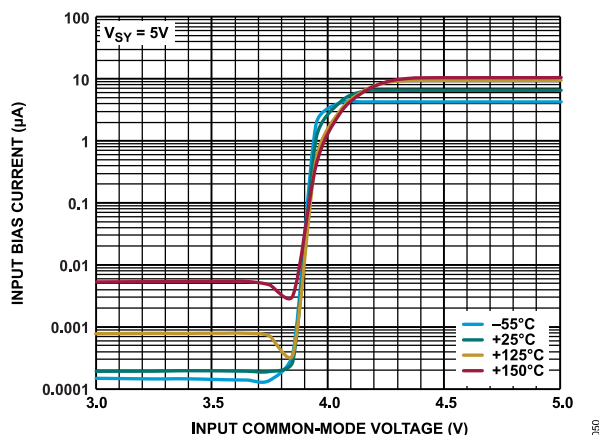


Figure 52. Input Bias Current vs. Input Common-Mode Voltage over Temperature,  $V_{SY} = 5$  V

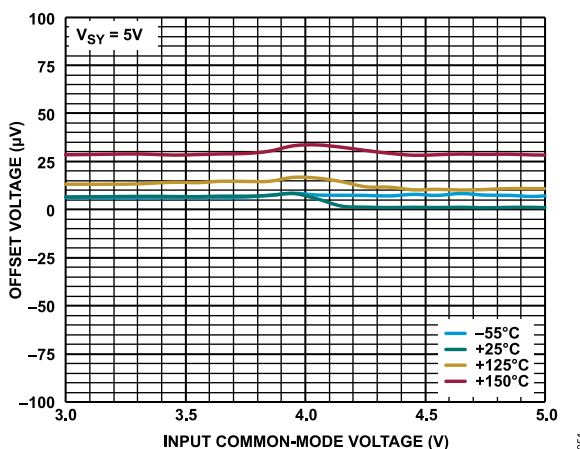


Figure 53. Offset Voltage vs. Input Common-Mode Voltage over Temperature,  $V_{SY} = 5$  V

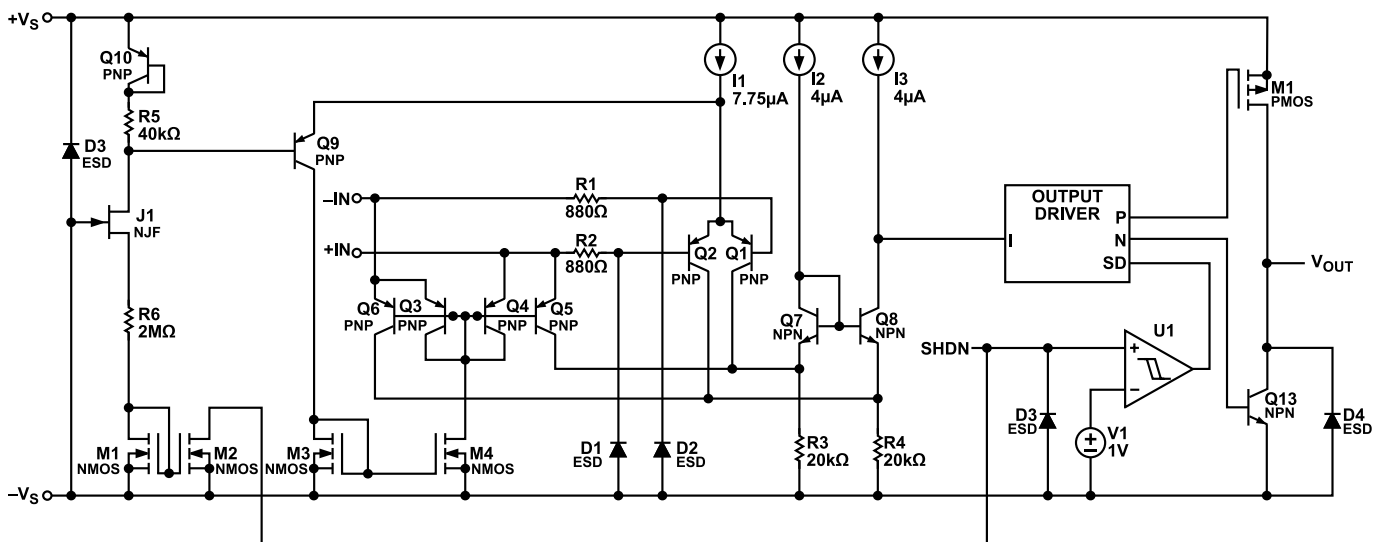


Figure 54. Simplified ADA4098-1 and ADA4098-2 Schematic

**THEORY OF OPERATION**

**INPUT PROTECTION**

The inputs are protected against temporary voltage excursions to 20 V below  $-V_S$  (see Figure 55) by internal 880  $\Omega$  resistors (see Figure 54). These resistors limit the current in the series D1 diode and D2 diode that are tied to the bases of the Q1 and Q2 transistors, respectively. Adding additional external series resistance extends the protection to  $>20$  V below  $-V_S$ , at the cost of stability and added thermal noise. The input stage of the ADA4098-1 and ADA4098-2 incorporates phase reversal protection to prevent the output from phase reversing for inputs below  $-V_S$ . The ADA4098-1 and ADA4098-2 op amps do not have clamping diodes between the inputs and can be differentially overdriven up to 80 V without damage, inducing parametric shifts, or drawing appreciable input current. Figure 56 summarizes the input fault types that can be applied to the ADA4098-1 and ADA4098-2 without compromising input integrity.

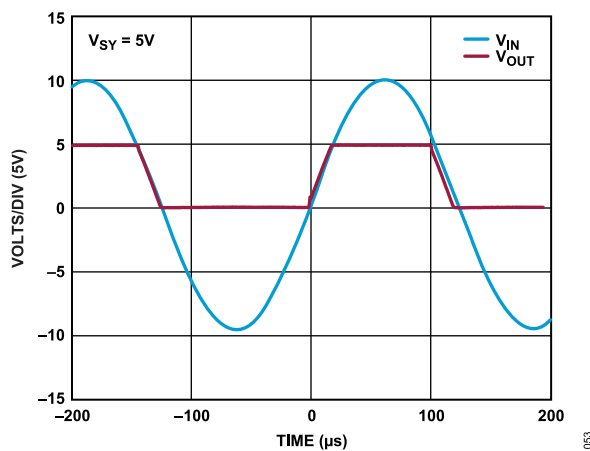


Figure 55. ADA4098-1 and ADA4098-2 as Unity-Gain Buffer with Noninverting Input Driven Beyond the Supply ( $V_{SY} = 5$  V)

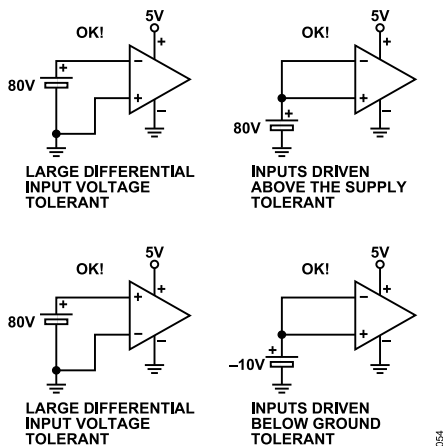


Figure 56. ADA4098-1 and ADA4098-2 Fault Tolerant Conditions

**OVER-THE-TOP OPERATION CONSIDERATIONS**

When the ADA4098-1 and ADA4098-2 input common-modes are biased near or  $>+V_S$  supply, the amplifiers operate in the Over-The-Top configuration. The differential input pair that controls amplifier operation is the common base pair, Q3 to Q6 (see Figure 54).

Input bias currents change from  $\pm 700$  pA in normal operation to approximately 8  $\mu$ A in Over-The-Top operation when the input stage transitions from common emitter to common base. The Over-The-Top input bias currents are well matched, and the associated offset is typically  $<50$  nA. Ensure that the impedance connected to the inverting and noninverting inputs is well matched to avoid any input bias current induced voltage offsets.

Differential input impedance,  $R_{IN}$  (see Figure 57), decreases from  $>1$  M $\Omega$  in normal operation to  $\sim 7$  k $\Omega$  in Over-The-Top operation (see Table 1 and Table 2).

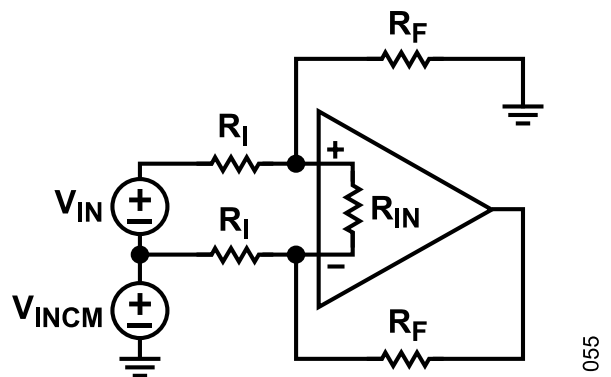


Figure 57. Difference Amplifier Configured for Normal Operation and Over-The-Top Operation ( $R_I$  is a Gain Setting Resistor)

This  $R_{IN}$  resistance appears across the summing nodes in Over-The-Top operation due to the configuration of the common base input stage.

The  $R_{IN}$  value is derived from the specified  $I_B$  that flows to the op amp inputs, as expressed in the following equation:

$$R_{IN} = 2kT/(qI_B)$$

where:

$k$  is Boltzmann's constant.

$T$  is the operating temperature.

$q$  is the charge of an electron.

$I_B$  is the operating input bias current in Over-The-Top operation.

The inputs are biased proportional to absolute temperature. Therefore,  $R_{IN}$  is relatively constant with temperature. This resistance appears across the summing nodes of the amplifier, which is forced to 0 V differentially by the feedback action of the amplifiers and can seem relatively harmless. However, depending on the configuration, this input resistance can boost the noise gain, lower overall amplifier loop gain and closed-loop bandwidth, and raise output

## THEORY OF OPERATION

noise. The singular benefit of this configuration is an increase in closed-loop amplifier stability.

In normal mode ( $-V_S < V_{CM} < +V_S - 1.25\text{ V}$ ),  $R_{IN}$  is typically large compared to the value of the gain setting resistors ( $R_F$  and  $R_I$ ), and  $R_{IN}$  can be ignored.

In this case, the noise gain is defined by the following equation:

$$\text{Noise Gain} = 1 + R_F/R_I$$

When the amplifiers transition to Over-The-Top operation with the input common-mode biased near or above the  $+V_S$  supply, consider the value of  $R_{IN}$ .

The noise gain of the amplifiers increases as shown in the following equation:

$$\text{Noise Gain}_{OTT} = \left( \left( 1 + \frac{R_F}{R_I |R_{IN} + R_I| |R_F|} \right) \times \left( 1 + \frac{R_I |R_F|}{R_{IN}} \right) \right)$$

where  $\text{Noise Gain}_{OTT}$  is the Over-The-Top noise gain.

The dc closed-loop gain remains mostly unaffected ( $R_F/R_I$ ). However, the loop gain of the amplifiers decreases, as expressed in the following equation:

$$\frac{A_{OL}}{1 + \frac{R_F}{R_I}} \text{ to } \frac{A_{OL}}{\text{Noise Gain}_{OTT}}$$

Likewise, the closed-loop bandwidth ( $BW_{CLOSED\_LOOP}$ ) of the amplifiers changes going from normal operation to Over-The-Top operation.

In normal operation,

$$BW_{CLOSED\_LOOP} \approx \frac{GBP}{1 + \frac{R_F}{R_I}}$$

In Over-The-Top operation,

$$BW_{CLOSED\_LOOP} \approx \frac{GBP}{\text{Noise Gain}_{OTT}}$$

Output voltage noise density ( $e_{no}$ ) is impacted when the devices transition from normal operation to Over-The-Top operation. Resistor noise is neglected in both modes of operation in the following equations.

In normal operation, neglecting resistor noise,

$$e_{no} \cong e_n \left( 1 + \frac{R_F}{R_I} \right)$$

where  $e_n$  is input referred voltage noise density.

In Over-The-Top operation, neglecting resistor noise,

$$e_{no} \cong e_n \times \text{Noise Gain}_{OTT}$$

## OUTPUT

The output of the ADA4098-1 and ADA4098-2 can swing rail-to-rail to within 45 mV of either supply with no load. The output can source 24 mA and sink 35 mA. The amplifiers are internally compensated to drive at least 200 pF of  $C_{LOAD}$ . Adding a series resistance of 50  $\Omega$  between the output and larger capacitive loads extends the capacitive drive capability of the amplifiers.

If the ADA4098-1 and ADA4098-2 enter shutdown, the  $V_{OUT}$  pin appears as high impedance with two steering diodes connected to either supply. In this state, the output typically leaks <5 nA.

## SHUTDOWN PINS (SHDN AND SHDNX)

The ADA4098-1 and ADA4098-2 have dedicated shutdown pins (SHDN for the ADA4098-1, and SHDN1 and SHDN2 for the ADA4098-2 10-lead LFCSP) to place the amplifiers in a very low power shutdown state when asserted high. A logic high is defined by a voltage  $\geq 1.5\text{ V}$  applied to the SHDN pin and SHDNx pins with respect to the  $-V_S$  pin. In shutdown, the amplifiers draw <12  $\mu\text{A}$  of supply current (see Figure 9) and the  $V_{OUT}$  pin is placed in a high impedance state.

The SHDN pin and SHDNx pins can be driven beyond the  $+V_S$  supply up to the absolute maximum voltage (60 V with respect to  $-V_S$ ) and draw little current (<1.5  $\mu\text{A}$ ). For normal active amplifier operation, the SHDN pin and SHDNx pins can be floated or driven by an external low voltage source (within 0.5 V of  $-V_S$ ). If the SHDN pin and SHDNx pins are left floating, an internal current source (~600 nA) pulls the SHDN pin and SHDNx pins to  $-V_S$ , which places the amplifiers into a default, active amplifying state. Because of the close proximity of the  $-IN$  pin (ADA4098-1) and  $-INx$  pins (ADA4098-2 10-lead LFCSP) and the SHDN pin and SHDNx pins, respectively, fast edges on the  $-IN$  pin and  $-INx$  pins may ac-couple to the adjacent high impedance SHDN pin and SHDNx pins, inadvertently placing the devices in shutdown. If this scenario is a concern, add a 1 nF capacitor between the SHDN pin and SHDNx pins and the  $-V_S$  pin.

Alternatively, the amplifiers can be effectively placed in a low power state by removing  $+V_S$ . In this low power state, the inputs typically leak <1 nA with either the  $\pm IN$  pins (ADA4098-1) or  $\pm INx$  pins (ADA4098-2 10-lead LFCSP) biased between  $-V_S$  and 70 V above  $-V_S$ . If the  $\pm IN$  pins and  $\pm INx$  pins are taken below  $-V_S$ , they appear as a diode connected to the  $-V_S$  supply in series with a resistance of 880  $\Omega$ . In this condition, limit the current to <20 mA.

Using an external source to drive the output beyond either  $\pm V_S$  supply under shutdown conditions may produce unlimited current and may damage the devices.

APPLICATIONS INFORMATION

LARGE RESISTOR GAIN OPERATION

The ADA4098-1 and ADA4098-2 have approximately 4 pF of input capacitance.

The parallel combination of  $R_F$  and  $R_G$  on the inverting input can combine with this input capacitance ( $C_{IN}$ ) to form a pole that can reduce bandwidth, cause frequency response peaking, or produce oscillations (see Figure 59). To mitigate these consequences, place a feedback capacitor ( $C_F$ ) with a value of  $C_F > C_{IN}(R_G/R_F)$  in parallel with  $R_F$  for summing node impedances  $>20\text{ k}\Omega$  ( $R_F || R_G > 20\text{ k}\Omega$ ). This capacitor placement cancels the input pole and optimizes dynamic performance (see Figure 58).

For applications where the noise gain is unity ( $R_G \rightarrow \infty$ ), and the feedback resistor exceeds 20 k $\Omega$ ,  $C_F \geq C_{IN}$ . Optimize PCB layouts to keep layout related summing node capacitance to an absolute minimum.

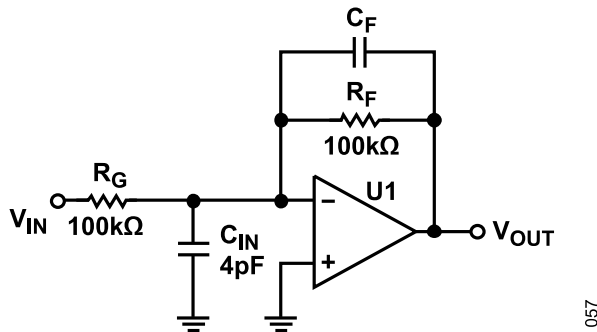


Figure 58. Inverting Gain Schematic

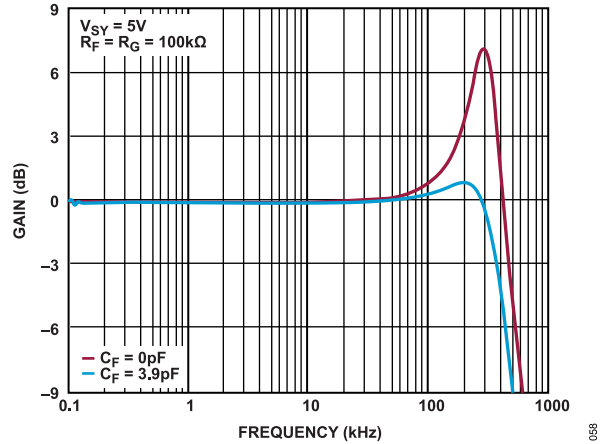


Figure 59. Inverting Gain of 1, Small Signal Frequency Response,  $R_F = R_G = 100\text{ k}\Omega$

RECOMMENDED VALUES FOR VARIOUS GAINS

Table 9 is a reference for determining various recommended gains and associated noise performance. The total impedance seen at the inverting input is kept to  $<20\text{ k}\Omega$  for gains  $>1$  to maintain ideal small signal bandwidth.

Table 9. Gains and Associated Recommended Resistor Values ( $T_A = 25^\circ\text{C}$ )

Gain	$R_G$ (k $\Omega$ )	$R_F$ (k $\Omega$ )	$C_F$ (pF)	Approximate -3 dB Frequency (MHz)	Total System Noise (nV/ $\sqrt{\text{Hz}}$ at 1 kHz, Referred to Input)
+1	Not applicable	0	Not applicable	1.5	16.5
+2	4.99	4.99	0	0.67	16.9
+2	100	100	3.9	0.56	32.4
+5	4.99	20	0	0.26	18.1
+10	4.99	45.3	0	0.13	17.7
-1	100	100	3.9	0.38	64.8
-1	4.99	4.99	0	0.72	16.9
-2	4.99	10	0	0.45	26.2
-5	4.99	24.9	0	0.22	21.6



APPLICATIONS INFORMATION

NOISE

To analyze the noise performance of an amplifier circuit, identify the noise sources, and then determine if each source has a significant contribution to the overall noise performance of the amplifier. To simplify the noise calculations, noise spectral densities (NSDs) are used rather than actual voltages, to leave bandwidth out of the expressions. NSD is generally expressed in nV/√Hz and is equivalent to the noise in a 1 Hz bandwidth.

The noise model shown in Figure 60 has six individual noise sources: the Johnson noise of the three resistors (R1 to R3), the op amp voltage noise, and the current noise ( $I_{N±}$ ) in each input of the amplifiers. Each noise source has its own contribution to the noise at the output. Noise is generally specified as referring to input (RTI), but it is often simpler to calculate the noise referred to the output (RTO), and then divide by the noise gain to obtain the RTI noise.

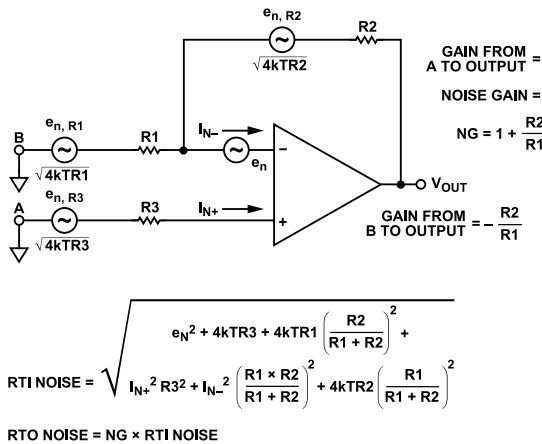


Figure 60. Op Amp Noise Analysis Model

Assuming  $I_{N+} = I_{N-} = I_N$ , the equation for RTI noise can be simplified to the following form:

$$RTI\ Noise = \sqrt{e_n^2 + e_{n,R}^2 + (I_N R_{EQ})^2}$$

$$e_{n,R} = \sqrt{4kTR_{EQ}}$$

$$R_{EQ} = R3 + R1 || R2$$

where:

$e_n$  is the op amp voltage noise.

$e_{n,R}$  is the thermal noise contribution of the surrounding R1 to R3 resistors.

$R_{EQ}$  is the equivalent input resistance.

$T$  is the absolute temperature in Kelvin.

A 50 Ω resistor generates a Johnson noise of 1 nV/√Hz at 25°C.

For optimal performance, the lower bound of resistance in a feedback network is determined by the amount of quiescent power and distortion that can be tolerated. The upper bound is determined by the resistor and current noise density. The ADA4098-1 and ADA4098-2 have an  $e_n$  of 17 nV/√Hz.

If resistor and current noise contributions are less than half this value, the  $e_n$  introduced by the op amps dominates and provides optimal noise performance of the devices.

For the ADA4098-1 and ADA4098-2, this lower bound of resistance in the feedback network is about 4.5 kΩ. For the amplifier configuration shown in Figure 60,  $R_{EQ} < 4.5\ k\Omega$  provides stable noise performance. If noise performance is not important,  $e_n$  is typically fixed for a given  $T_A$ ,  $e_{n,R}$  increases with the square root of the resistor value, and the  $I_N \times R_{EQ}$  resistance increases linearly, but does not impact total noise until it approaches the value of  $e_{n,R}$ . With  $R_{EQ} < \sim 700\ k\Omega$ ,  $e_{n,R}$  is larger than  $I_N \times R_{EQ}$ . A safe value for  $R_{EQ}$  is  $\sim 350\ k\Omega$  to ensure that  $I_N$  is not the majority contributor to total noise seen by the input.

Figure 61 shows the noise contributions for the range of resistance values discussed in this section.

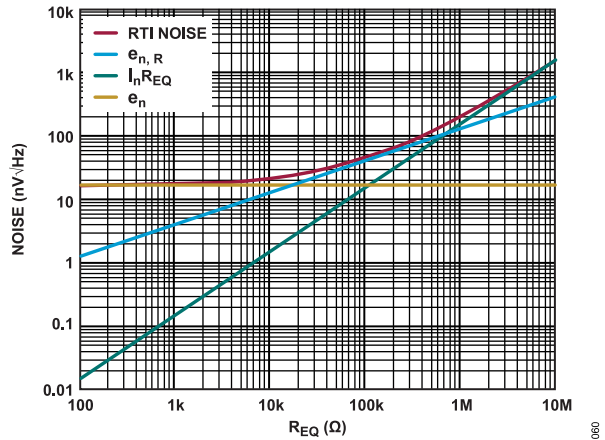


Figure 61. Noise Contributions vs. Equivalent Input Resistance

DISTORTION

There are two main contributors of distortion in op amps: output crossover distortion as the output transitions from sourcing to sinking, and distortion caused by nonlinear common-mode rejection. If the op amps are operating in an inverting configuration, there is no common-mode induced distortion. If the op amps are operating in the noninverting configurations within the normal input common-mode range ( $-V_S$  to  $+V_S - 1.25\ V$ ), distortion is acceptable. When the inputs transition from normal to Over-The-Top operation or vice versa, a significant degradation occurs in linearity due to the change of input circuitry.

As  $R_L$  decreases, distortion increases due to a net decrease in loop gain and greater signal swings internal to the amplifiers that are necessary to drive the load. The lowest distortion can be achieved with the ADA4098-1 and ADA4098-2 operating in Class A operation in an inverting configuration, with the input common-mode biased at midsupply.



APPLICATIONS INFORMATION

POWER DISSIPATION AND THERMAL SHUTDOWN

The ADA4098-1 and ADA4098-2 can drive heavy loads on power supplies up to ±25 V. Therefore, ensure that  $T_J$  on the integrated circuits does not exceed 175°C.

Junction temperatures exceeding 125°C promote accelerated aging. Reliability of the ADA4098-1 and ADA4098-2 may be impaired if the junction temperature exceeds 175°C. If the junction temperature exceeds 175°C, the ADA4098-1 and ADA4098-2 have a final safety measure in the form of a thermal shutdown that shuts off the output stage and reduces the internal device currents. When this thermal shutdown function triggers, the output remains disabled in a high impedance state until the junction temperature drops 20°C. Persistent heavy loads and elevated ambient temperatures can cause the ADA4098-1 and ADA4098-2 to oscillate in and out of thermal shutdown depending on the power dissipated on the die, until the heavy load is removed (see Figure 62).

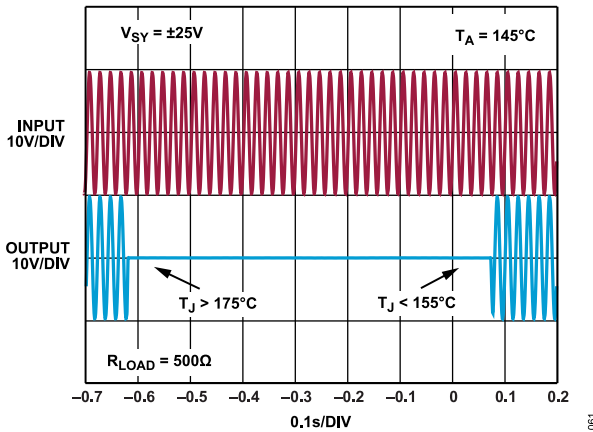


Figure 62. ADA4098-1 and ADA4098-2 Cycling In and Out of Thermal Shutdown

It is not recommended to operate near the maximum junction temperature.

Typically,  $T_J$  can be estimated from  $T_A$  and the device power dissipation ( $P_D \times \theta_{JA}$ ), as shown in the following equation:

$$T_J = T_A + P_D \times \theta_{JA}$$

The power dissipation in the ICs varies as a function of supply voltage, the output voltage, and load resistance. For a given supply voltage, the worst case power dissipation ( $P_{D(MAX)}$ ) in the ICs occurs when the supply current is maximum, and the output voltage is at half of either supply voltage.

$$P_{D(MAX)} = V_S I_{S(MAX)} + \left(\frac{V_{SY}}{2}\right)^2 / R_L$$

For a given supply voltage, use Figure 63 as a guide for estimating the minimum load resistance that the ADA4098-1 and ADA4098-2 can drive for a given rise in junction

temperature ( $\Delta T_J$ ). For example, to limit  $\Delta T_J$  to 50°C, the load driven on the ±15 V supplies (+30 V total supply) must not be lower than 900 Ω. It is assumed that  $\theta_{JA}$  is 192°C/W.

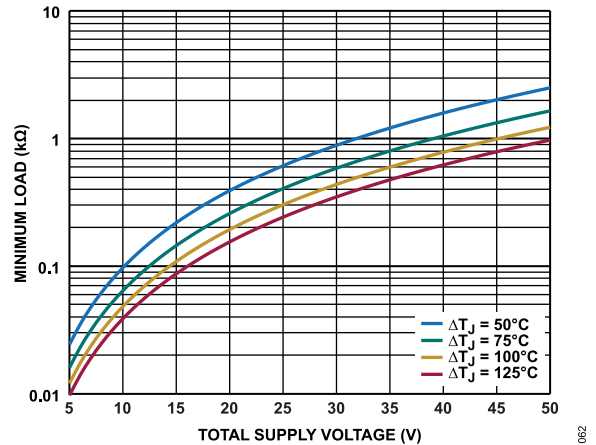


Figure 63. Minimum Load Resistance for Given  $\Delta T_J$  and  $V_{SY}$

CIRCUIT LAYOUT CONSIDERATIONS

Careful and deliberate attention to detail when laying out the ADA4098-1 and ADA4098-2 boards yields optimal performance. Power supply bypassing, parasitic capacitance, and component selection all contribute to the overall performance of the amplifiers.

POWER SUPPLY BYPASSING

On single supplies, solder the  $-V_S$  supply pin directly to a low impedance ground plane. Bypass the  $+V_S$  pin to a low impedance ground plane with a low effective series resistance (ESR) multilayer ceramic capacitor (MLCC) of 0.1 μF, typically, as close to the ± $V_S$  supply pins as possible. When driving heavy loads, add 10 μF of supply capacitance. When using split supplies, these conditions are applicable to the  $-V_S$  supply pin.

The ADA4098-1 and ADA4098-2 have an internal current source of ~0.6 μA on the SHDN pin (ADA4098-1) and SHDNx pins (ADA4098-2 10-lead LFCSP) to pull the pins down to  $-V_S$  and to place the amplifiers in the default amplifying state. If the shutdown state is not required, hard tie the SHDN pin and SHDNx pins to the  $-V_S$  pin. If the SHDN pin and SHDNx pins are left floating or driven by a source with significant source impedance (>100 Ω), bypass the  $-V_S$  supply pin with a small, 1 nF capacitor to prevent stray signals from coupling on the SHDN pin and SHDNx pins, which can inadvertently trigger shutdown.

## APPLICATIONS INFORMATION

## GROUNDING

Use ground and power planes where possible to reduce the resistance and inductance of the supply and ground returns. Place bypass capacitors as close as possible to the  $\pm V_S$  supply pins, with the other ends connected to the ground plane. It is recommended to use a bypass capacitor of at least 0.1  $\mu\text{F}$  when driving light loads (load currents  $< 100 \mu\text{A}$ ), and more capacitance when driving heavier loads. Routing from the output to the load and return to the ground plane must have minimal loop area to keep inductance to a minimum.

## ESD PROTECTION WHEN POWERED

ICs react to ESD strikes differently when unpowered vs. powered, which falls under IEC-61000-4-2 standards (see the [Absolute Maximum Ratings](#) section). A device that performs well under HBM conditions can perform poorly under International Electrotechnical Commission (IEC) conditions. The ADA4098-1 and ADA4098-2 are thoroughly abused with ESD strikes under IEC conditions to create a front-end circuit protection scheme that protects the devices if subjected to ESD strikes. [Figure 64](#) and [Figure 65](#) show two different protection schemes that extend the protection of the ADA4098-1 and ADA4098-2 to  $\pm 8 \text{ kV}$  ESD strikes.

Consider the following when selecting components:

- ▶ A component size of 0805 or larger to reduce chance of arc-over.
- ▶ Pulse withstanding, thick film resistors.
- ▶ COG MLCC with a minimum rating of 100 V.
- ▶ Bidirectional, transient voltage suppression (TVS) diodes.

Table 10. ADA4098-1 and ADA4098-2 Related Products

Model	$V_{OS}$ ( $\mu\text{V}$ )	$I_B$ (nA)	GBP (kHz)	$e_n$ (nV/ $\sqrt{\text{Hz}}$ )	$I_{SY}$ ( $\mu\text{A}$ )	Common-Mode Input Range (V)
ADA4098-1	30	0.7	1000	17	165	$-V_S$ to $-V_S + 70$
ADA4098-2	30	0.7	1000	17	165	$-V_S$ to $-V_S + 70$
ADA4099-1	30	10	8000	7	1500	$-V_S$ to $-V_S + 70$
ADA4099-2	30	10	8000	7	1500	$-V_S$ to $-V_S + 70$
ADA4077-1	35	1	3900	7	500	$-V_S$ to $+V_S$
LT6015	50	5	3200	18	335	$-V_S$ to $-V_S + 76$
LT6014	60	0.4	1600	9.5	165	$-V_S$ to $+V_S$
LT1494	375	1	2.7	185	1.5	$-V_S$ to $-V_S + 36$
LT1490A	500	8	180	50	55	$-V_S$ to $-V_S + 44$

In the circuit shown in [Figure 64](#), R1 is a 220  $\Omega$ , Panasonic, 0805, ERJ-P6 series, and C1 is a 100 pF, Yageo, 0805, 100 V, COG/NPO.

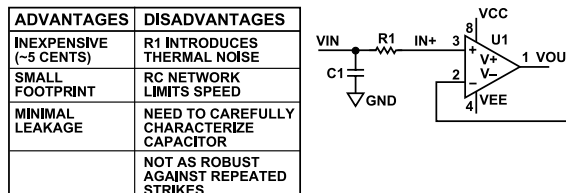


Figure 64. ESD Protection Circuit (RC Network)

In the circuit shown in [Figure 65](#), R1 is a 220  $\Omega$ , Panasonic, 0805, ERJ-P6 series, and D1 is a Bourns CDSOD323-T36SC. An ESD varistor can be considered for D1.

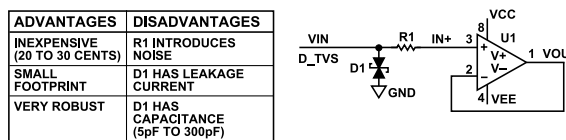


Figure 65. ESD Protection Circuit (R-TVS Network)

For more information on system level ESD considerations, see the technical article, [When Good Electrons Go Bad: How to Protect Your Analog Front End](#), on the Analog Devices, Inc., website.

## RELATED PRODUCTS

Table 10 describes several alternative precision amplifiers that can also be considered for certain applications.

APPLICATIONS INFORMATION

TYPICAL APPLICATIONS

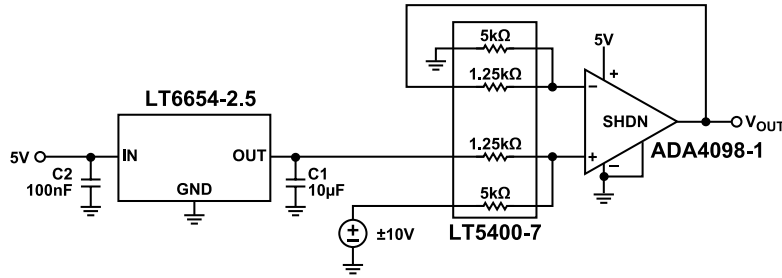


Figure 66. ±10 V to 0 V to +5 V Funnel Amplifier, High CMRR and ±80 V Input Protection via LT5400-7 Resistor Network (ADA4098-1 6-Lead TSOT)

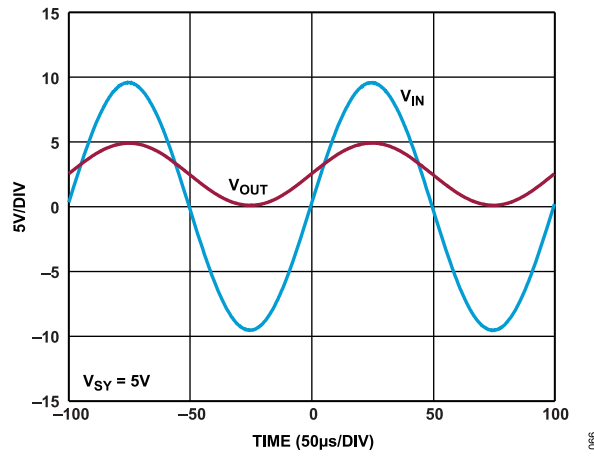


Figure 67. ±10 V to 0 V to +5 V Funnel Amplifier, Input and Output Voltages

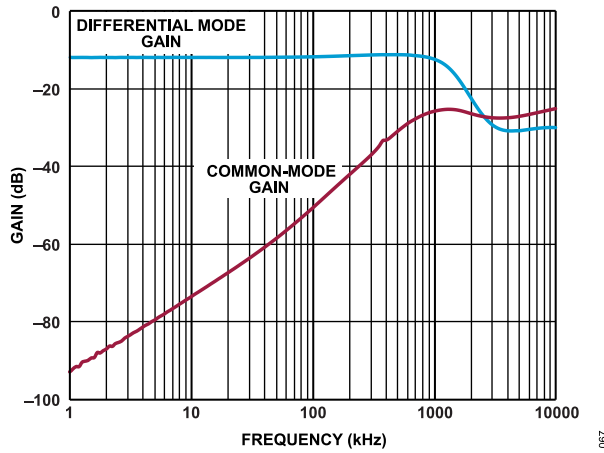


Figure 68. ±10 V to 0 V to +5 V Funnel Amplifier, System Gain

APPLICATIONS INFORMATION

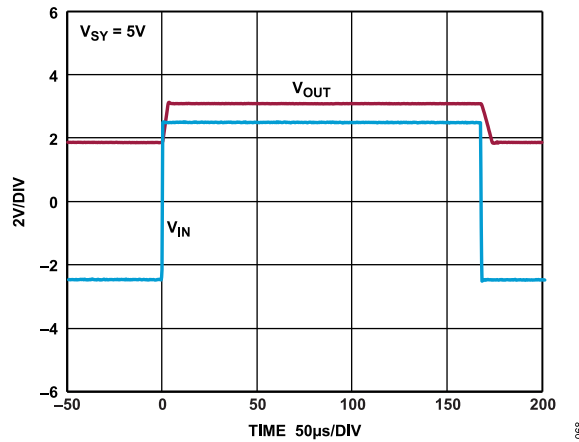


Figure 69. ±10 V to 0 V to +5 V Funnel Amplifier, Large Signal Pulse Response

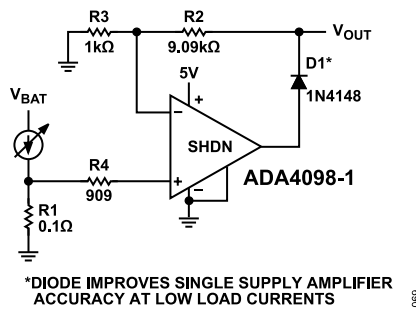


Figure 70. 1 V/A Low-Side Current Sense (ADA4098-1 6-Lead TSOT)

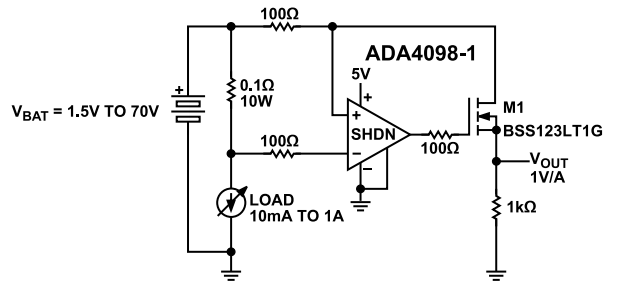


Figure 71. 1 V/A High-Side Current Sense (ADA4098-1 6-Lead TSOT)

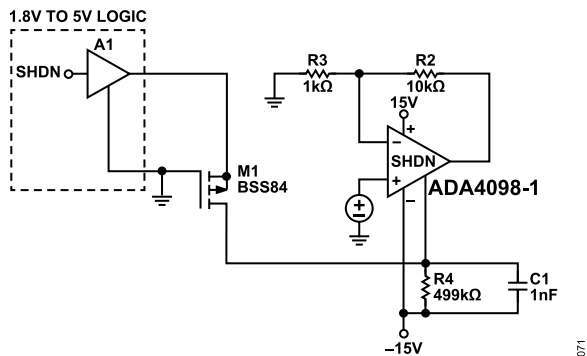
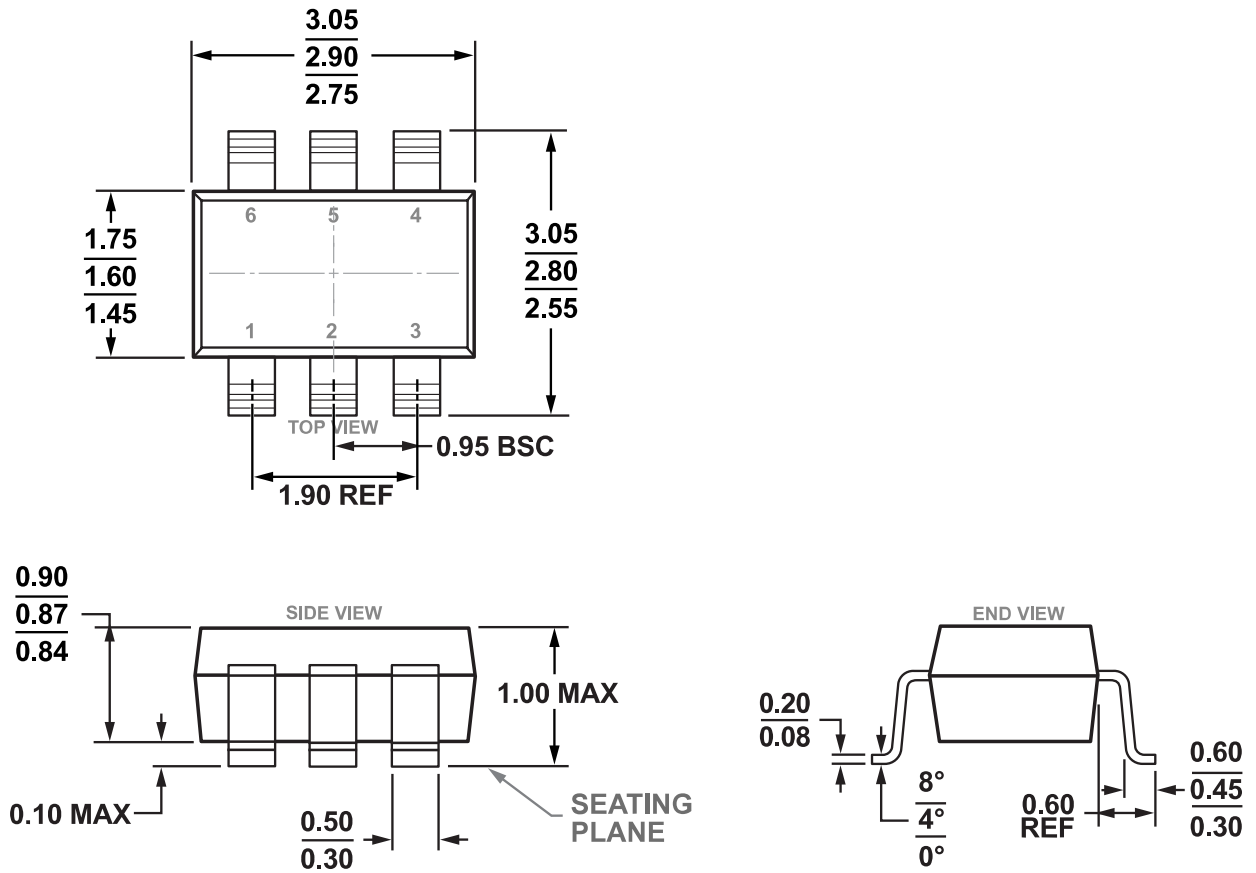


Figure 72. Microprocessor Control of SHDN Pin in Split Supply Applications (ADA4098-1 6-Lead TSOT)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-193-AA

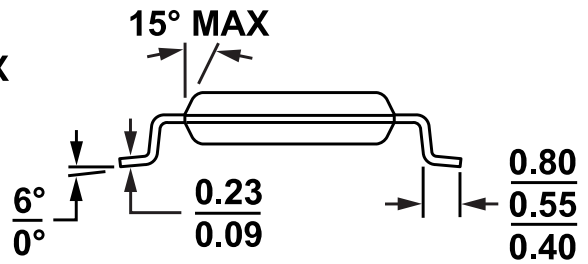
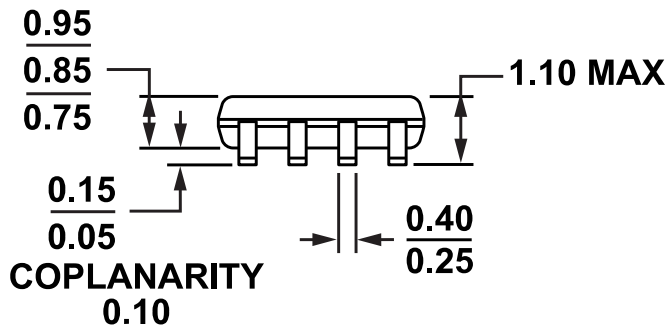
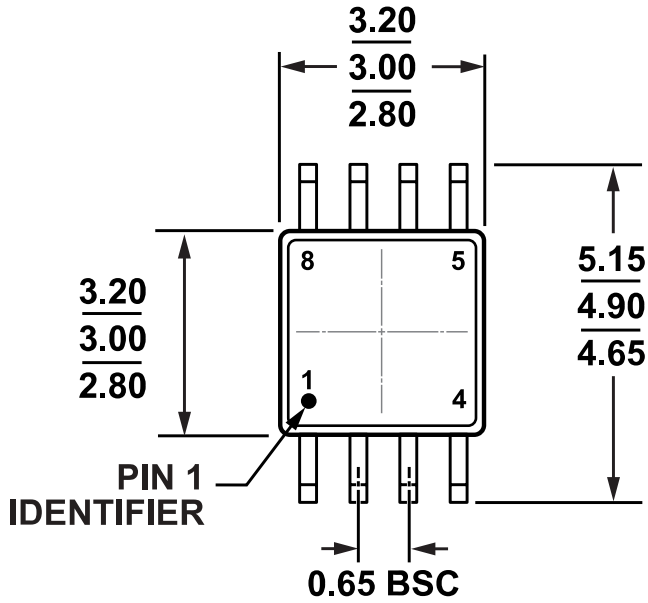
Figure 73. 6-Lead Thin Small Outline Transistor Package [TSOT] (UJ-6)  
Dimensions shown in millimeters

PKG-000881

11-18-2019-B



OUTLINE DIMENSIONS



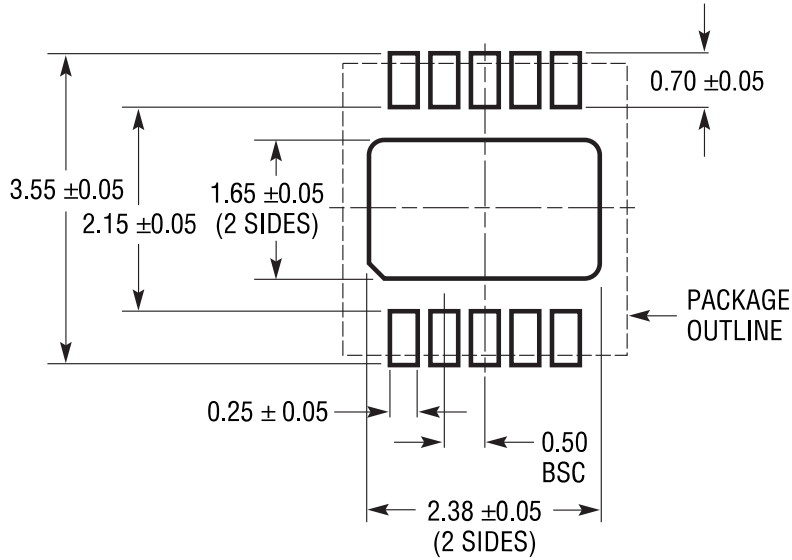
COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 75. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

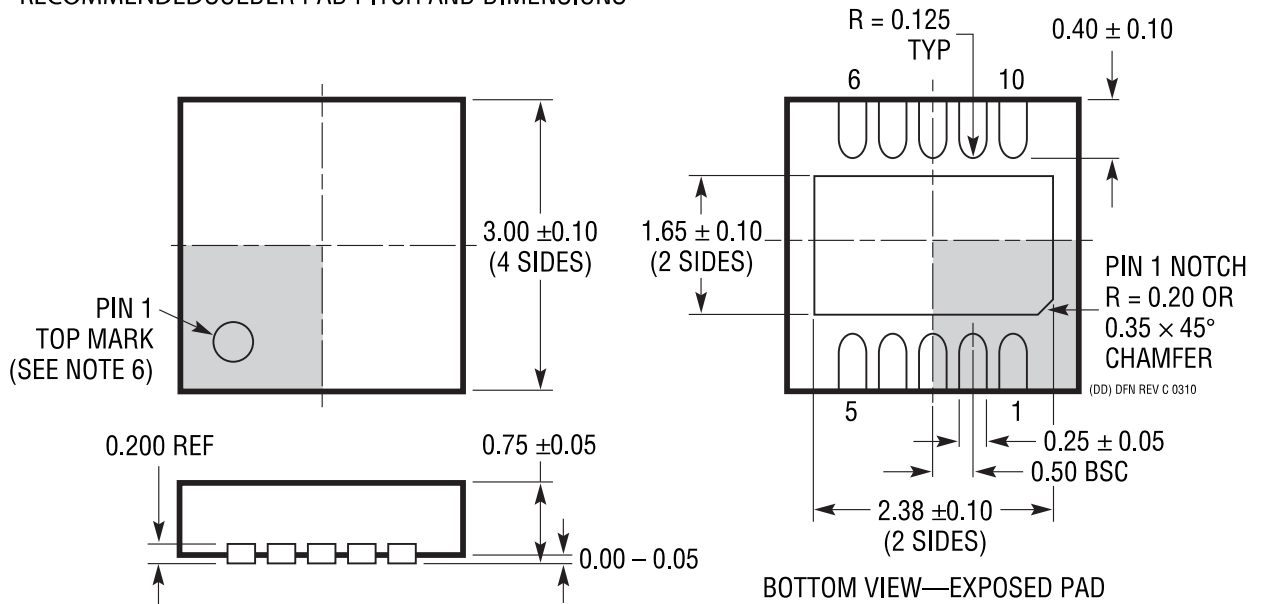
Dimensions shown in millimeters

10-07-2009-B

OUTLINE DIMENSIONS



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Figure 76. 10-Lead Lead Frame Chip Scale Package [LFCSP]  
 3 mm × 3 mm Body and 0.75 mm Package Height  
 (05-08-1699)  
 Dimensions shown in millimeters