Data Sheet

ADA4099-2BCHIPS

50 V, 8 MHz, 1.65 mA per Channel, Robust, Over-The-Top, Precision Op Amp

FEATURES

- Ultrawide common-mode input range: −15.1 V to +55 V
- Wide power supply voltage operating range: 3.15 V to 50 V
- Low supply current: 1.65 mA per channel
- Low input offset voltage: ±12 µV
- Low offset voltage drift: ±0.1 µV/°C
- Low voltage noise
  - 1/f noise corner: 6 Hz
  - 150 nV p-p at 0.1 Hz to 10 Hz
  - 7 nV/√Hz at 100 Hz (e_n)
- High speed
  - GBP: 8 MHz
  - Slew rate: 5.5 V/µs at ΔV_{OUT} = 25 V
- Low power supply shutdown current: 17 µA per channel
- Low input bias current: ±4 nA
- Large signal voltage gain: 154 dB at ΔV_{OUT} = 25 V
- CMRR: 130 dB at V_{CM} = −14.75 to +13.25 V
- PSRR: 136 dB
- Input overdrive tolerant with no phase reversal

APPLICATIONS

- Industrial sensor conditioning
- Supply current sensing
- Battery and power supply monitoring
- Front-end amplifiers in abusive environments

FUNCTIONAL BLOCK DIAGRAM

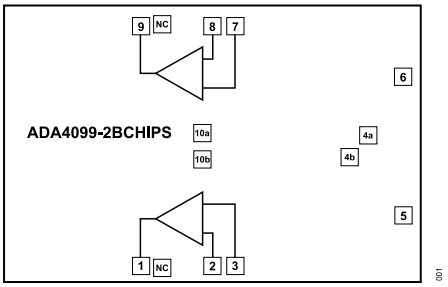

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADA4099-2BCHIPS is a robust, precision, rail-to-rail input and output dual-channel operational amplifier with inputs that operate from $-V_S$ to $+V_S$ and beyond, which is referred to in this data sheet as Over-The-Top™. The device features an offset voltage of ±12 µV, an input bias current (I_B) of ±4 nA, and can operate on supplies that range from 3.15 V to 50 V. The ADA4099-2BCHIPS draws 1.65 mA of supply current per channel.

The ADA4099-2BCHIPS Over-The-Top input stage has robust input protection features for abusive environments. The inputs can tolerate up to 80 V of differential voltage without damage or degradation to dc accuracy. The operating input common-mode range extends from rail-to-rail and beyond, up to 70 V > $-V_S$, independent of the $+V_S$ supply.

The ADA4099-2BCHIPS is unity-gain stable and can drive loads requiring up to 20 mA per channel. The device can also drive capacitive loads as large as 100 pF. The amplifier is available with low power shutdown per channel.

The ADA4099-2BCHIPS is specified at +25°C but is functional over the extended industrial temperature range (−40°C to +125°C). Additional application and technical information can be found in the ADA4099-2 data sheet.

Rev. 0

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REVISION HISTORY

7/2022—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—±15 V SUPPLY

Common-mode voltage (V_{CM}) = 0 V, SHDNx pins are open, load resistance (R_L) = 499 kΩ to ground, and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DC PERFORMANCE					
Input Offset Voltage (V_{OS})[1]			±12		μV
	Power supply voltage (V_{SY}) = ±25 V		±15		μV
Input Voltage Offset Drift[2]	$T_{MIN} < T_A < T_{MAX}$		±0.1		μV/°C
Input Bias Current (I_B)			±4		nA
	V_{SY} = ±25 V		±4		nA
Input Offset Current (I_{OS})			±2		nA
	V_{SY} = ±25 V		±4		nA
Common-Mode Rejection Ratio (CMRR)	V_{CM} = −14.75 V to +13.25 V		130		dB
	V_{CM} = −15.1 V to +13.25 V		126		dB
	V_{CM} = −15.1 V to +55 V		126		dB
Common-Mode Input Range	Guaranteed by CMRR tests	−15.1		+55	V
Large Signal Voltage Gain (A_{OL})	Delta output voltage (ΔV_{OUT}) = 25 V		154		dB
	ΔV_{OUT} = 25 V, R_L =10 kΩ		134		dB
NOISE PERFORMANCE					
Input Voltage Noise	Frequency = 0.1 Hz to 10 Hz		150		nV p-p
	1/f noise corner		6		Hz
	Frequency = 100 Hz		7		nV/√Hz
Over-The-Top	Frequency = 100 Hz, V_{CM} > positive supply voltage (+V_S)		8		nV/√Hz
Input Current Noise	Frequency =100 Hz		0.5		pA/√Hz
Over-The-Top	Frequency = 100 Hz, V_{CM} > +V_S		5		pA/√Hz
DYNAMIC PERFORMANCE					
Slew Rate	ΔV_{OUT} = 25 V		5.5		V/μs
Gain Bandwidth Product (GBP)	Test frequency (f_{TEST}) = 25 kHz		8		MHz
Phase Margin			57		deg
1% Settling Time	ΔV_{OUT} = ±2 V		1.15		μs
0.1% Settling Time	ΔV_{OUT} = ±2 V		1.5		μs
Total Harmonic Distortion plus Noise (THD + N)	Frequency = 10 kHz, output voltage (V_{OUT}) = 5.6 V p-p, R_L = 10 kΩ, bandwidth = 80 kHz		0.001		%
INPUT CHARACTERISTICS					
Input Resistance	Differential mode		100		kΩ
	Common mode		>1		GΩ
Input Capacitance	Differential mode		9		pF
	Common mode		3		pF
SHDN1 AND SHDN2 PINS					
Input Logic Low	Amplifier active, SHDNx voltage (V_{SHDN}) < negative supply voltage (−V_S) + 0.5 V			−V_S + 0.5	V
Input Logic High	Amplifier shutdown, V_{SHDN} > −V_S + 1.5 V	−V_S + 1.5			V
Response Time	Amplifier active to shutdown		2.5		μs
	Amplifier shutdown to active		10		μs
Pull-Down Current	V_{SHDN} = −V_S + 0.5 V		−0.6		μA
	V_{SHDN} = −V_S + 1.5 V		0.3		μA
OUTPUT CHARACTERISTICS					
Output Voltage Swing Low	V_{OD}[3] = 30 mV, no load		45		mV
	V_{OD}[3] = 30 mV, sink current (I_{SINK}) = 10 mA		260		mV

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Output Voltage Swing High	V_{OD}[3] = 30 mV, no load		45		mV
	V_{OD}[3] = 30 mV, source current (I_{SOURCE}) = 10 mA		900		mV
Short-Circuit Current	I_{SOURCE}		34		mA
	I_{SINK}		50		mA
POWER SUPPLY					
Maximum Operating Voltage[4]				50	V
Operating Range	Guaranteed by power supply rejection ratio (PSRR)	3.15		50	V
Supply Current per Channel	Amplifier active		1.65		mA
	V_{SY} = ±25 V		1.75		mA
	Amplifier shutdown, $V_{SHDN} = -V_S + 1.5$ V		17		µA
PSRR	V_{SY} = 3.15 V to 50 V		136		dB
THERMAL SHUTDOWN[5]					
Temperature	T_J		175		°C
Hysteresis			20		°C
Functional Temperature	T_A	−40		+125	°C

[1] Thermoelectric voltages present in the high speed production test limit the measurement accuracy of this parameter. The limits listed in Table 1 represent an upper limit imposed by the test capability and are not necessarily indicative of actual performance of the devices.

[2] Offset voltage drift is guaranteed through lab characterization and is not production tested.

[3] V_{OD} is +30 mV for V_{OUT} high and −30 mV for V_{OUT} low.

[4] Maximum operating voltage is limited by the time-dependent dielectric breakdown (TDDB) of on-chip capacitor oxides. The amplifier tolerates temporary transient overshoot up to the specified absolute maximum rating and the dc supply voltage must be limited to the maximum operating voltage.

[5] Thermal shutdown is lab characterized only and is not tested in production.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage[1]	
Transient	60 V
Continuous	50 V
Differential Input Voltage	±80 V
±INx Pin Voltage	
Continuous	−5 V to +80 V
Survival	−10 V to +80 V
±INx Pin Current	20 mA
SHDNx Pin Voltage	−0.3 V to +60 V
Storage Temperature Range	−65°C to +150°C
Functional Temperature Range	−55°C to +150°C
Junction Temperature (T_J)	175°C

[1] Maximum supply voltage is limited by the TDDB of on-chip capacitor oxides. The amplifier tolerates temporary transient overshoot up to the specified transient maximum rating. The continuous operating supply voltage must be limited to no more than 50 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

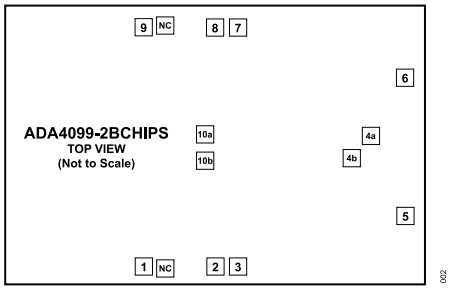

Figure 2. Pad Configuration

Table 3. Pad Function Descriptions[1]

Pad Number	Mnemonic	X Coordinate	Y Coordinate	Description
1	V_{OUT1}	−386	−643	Output, Channel 1
2	−IN1	−001	−643	Inverting Input, Channel 1
3	+IN1	−122	−643	Noninverting Input, Channel 1
4a	$-V_S$	+837	+059	Negative Supply Voltage (Both Must Be Connected)
4b	$-V_S$	+735	−059	Negative Supply Voltage (Both Must Be Connected)
5	SHDN1	+1022	−373	Shutdown Channel 1
6	SHDN2	+1022	+373	Shutdown Channel 2
7	+IN2	−001	+643	Noninverting Input, Channel 2
8	−IN2	+122	+643	Inverting Input, Channel 2
9	V_{OUT2}	−386	+643	Output, Channel 2
10a	$+V_S$	−056	+070	Positive Supply Voltage (Both Must Be Connected)
10b	$+V_S$	−056	−070	Positive Supply Voltage (Both Must Be Connected)

[1] All dimensions are referenced from the center of the die to the center of each bond pad.

OUTLINE DIMENSIONS

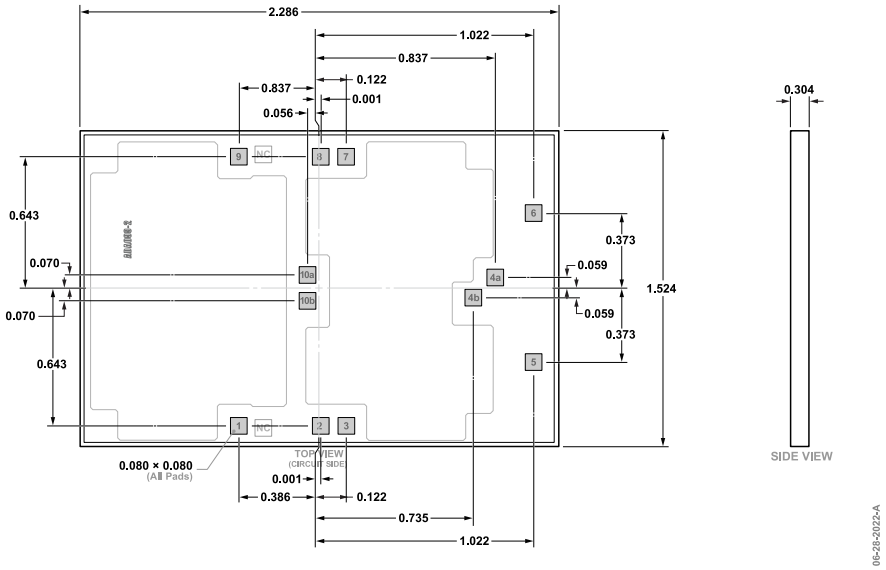

Figure 3. 12-Pad Bare Die [CHIP]
(C-12-5)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Die Specifications

Table 4. Die Specifications

Parameter	Value	Unit
Chip Size	1424 × 2186	µm
Scribe Line Width	100 × 100	µm
Die Size Maximum	1524 × 2286	µm
Thickness	304	µm
Backside	V−	V
Passivation	1.1 (doped silicon and polymer)	µm
Top Coat Thickness	32	µm
Bond Pads (Minimum)	80 × 80	µm
Bond Pad Composition	1.0% aluminum silicon (AlSi), 0.5% copper (Cu)	%

Assembly Recommendations

Table 5. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	ABLESTIK 8200T
Bonding Method	1 mil gold
Bonding Sequence	Unspecified