Zero Drift, High Voltage, Programmable Gain Instrumentation Amplifier with Charge Pump

FEATURES

- Integrated bipolar charge pump
  - Simplified isolation requirements
  - Wide input range on low voltage supplies
- Dedicated output amplifier supplies for ADC protection
- Low power: 83 mW (DVDD = 3 V, VDDCP = 5 V)
- 36 precision gains from 1/16 V/V to 176 V/V
- Robust ±60 V protected 2:1 input multiplexer
- Excellent dc precision
  - Low input offset voltage: ±14 µV maximum
  - Low input offset voltage drift: ±0.08 µV/°C maximum
  - Gain calibration via internal memory
  - Low gain drift: ±1 ppm/°C maximum
  - High CMRR: 111 dB minimum, G = 1 V/V
- Low input bias current: ±1.5 nA maximum at T_A = 25°C
- Integrated input EMI filtering
- 7 GPIOx ports with special functions
- Sequential chip select mode
- Excitation current source
- SPI port with checksum (CRC) support
- Internal/external fault detection
- Compact 28-lead, 5 mm × 5 mm LFCSP
- Specified temperature range: −40°C to +105°C

APPLICATIONS

- Universal process control front ends
- Data acquisition systems
- Test and measurement systems
- System power monitoring

GENERAL DESCRIPTION

The ADA4255 is a precision programmable gain instrumentation amplifier (PGIA) with integrated bipolar charge pumps. With its integrated charge pumps, the ADA4255 internally produces the high voltage bipolar supplies needed to achieve a wide input voltage range (38 V typical with VDDCP = 5 V) without lowering input impedance. The charge pump topology of the ADA4255 allows channels to be isolated with only low voltage components, reducing complexity, size, and implementation time in industrial and process control systems.

The zero drift PGIA topology of the ADA4255 self calibrates dc errors and lower frequency 1/f noise, achieving excellent dc precision over the entire specified temperature range. The combination of 36 precision gains ranging from 1/16 V/V to 176 V/V within the ADA4255 and high voltage, high impedance inputs allow a wide range of inputs to be scaled to the range of the analog-to-digital converter (ADC). By integrating all gain setting and level shifting resistors, the ADA4255 achieves excellent common-mode rejection ratio (CMRR) performance (111 dB minimum at G = 1 V/V) and extremely low gain drift (±1 ppm/°C maximum). This high level of precision maximizes dynamic range and greatly reduces calibration requirements in many applications.

The ±60 V input protection, integrated electromagnetic interferance (EMI) filtering and various safety features make the ADA4255 an ideal choice for robust industrial systems. Seven general-purpose input and output (GPIOx) pins, which can be configured to provide various special functions, are included in the ADA4255. An excitation current source output is available to bias sensors such as resistance temperature detectors (RTDs).

The ADA4255 is specified over the −40°C to +105°C temperature range and is offered in a compact 5 mm × 5 mm, 28-lead LFCSP.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

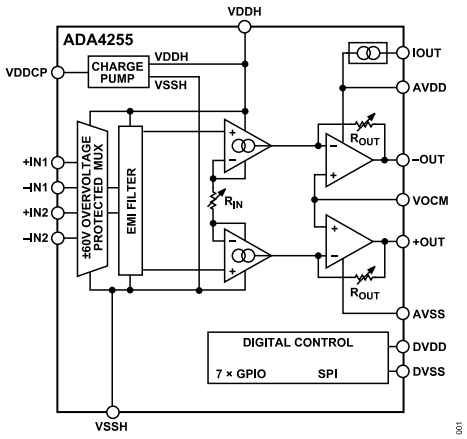

Figure 1. Simplified Functional Block Diagram

COMPANION PRODUCTS

- **ADCs:** AD4007, AD7768, AD7175-2, AD7124-4
- **ADC Drivers:** ADA4945-1, LTC6363
- **Voltage References:** ADR4550, ADR3450, LT6656
- **Isolators:** ADuM6421A Family, ADuM140D Family

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REVISION HISTORY

7/2021—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, VDDCP = 5 V, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, DVSS = 0 V, VOCM = AVDD/2, scaling gain = 1, and no load, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OFFSET VOLTAGE	Total offset, referred to input (RTI) = V_{OSI} + (V_{OSO}/Gain)				
Differential Offset Voltage					
Input Offset Voltage (V_{OSI})			±3	±14	µV
Output Offset Voltage (V_{OSO})			±40	±125	µV
Differential Offset Voltage Drift	T_A = −40°C to +105°C[1], total offset drift, RTI = V_{OSI}/T + ((V_{OSO}/T)/ Gain)				
V_{OSI}/T			±0.03	±0.08	µV/°C
V_{OSO}/T			±0.98	±2.5	µV/°C
Differential Offset Voltage vs. VDDCP Power Supply Rejection Ratio (PSRR), RTI	VDDCP = 2.7 V to 5.5 V				
	Gain (G) = 1/16 V/V	60	73		dB
	G = 1 V/V	84	97		dB
	G = 128 V/V	113	130		dB
Differential Offset Voltage vs. AVDD (PSRR), RTI	AVDD − AVSS = 2.7V to 5.5V				
	G = 1/16 V/V	68	76		dB
	G = 1 V/V	92	100		dB
	G = 128 V/V	115	130		dB
Differential Offset vs. External Clock Frequency, RTI	Clock frequency = 0.8 MHz to 1.2 MHz				
	G = 1/16 V/V		±0.2		µV/kHz
	G = 1 V/V		±0.1		µV/kHz
	G = 128 V/V		±0.002		µV/kHz
CMRR, RTI	+IN = −IN = (VSSH + 3 V) to (VDDH − 3 V)				
	G = 1/16 V/V	87	98		dB
	G = 1 V/V	111	122		dB
	G = 128 V/V	138	150		dB
GAIN	Output voltage (V_{OUT}) = 9.5 V p-p[2]				
Input Gain Range			1/16 to 128		V/V
Output Scaling Gain Settings			1, 1.25, 1.375		V/V
Gain Error					
Before Calibration	All gains		<±0.06	±0.12	%
Using Calibration Coefficient	All gains		<±0.01	±0.025	%
Gain Drift					
All Gains Except the Following:	T_A = −40°C to +105°C[1]		<±0.3	±1	ppm/°C
	T_A = −40°C to +105°C[1], G = 1/16 V/V, all scaling gains		<±0.5	±1.5	ppm/°C
	T_A = −40°C to +105°C[1], G = 32 V/V, all scaling gains		<±0.4	±1.5	ppm/°C
	T_A = −40°C to +105°C[1], G = 64 V/V, all scaling gains		<±0.6	±2	ppm/°C
	T_A = −40°C to +105°C[1], G = 128 V/V, all scaling gains		<±1.5	±4	ppm/°C
Nonlinearity	All gains except 32 V/V, 64 V/V, and 128 V/V[2, 3]		5	15	ppm
	G = 32 V/V		7.5		ppm
	G = 64 V/V		12		ppm
	G = 128 V/V		15		ppm

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE	$Total\ \ Noise,\ \ RTI\ \ = \sqrt{e_{ni}{}^2 + \left(\frac{e_{no}}{Gain}\right)^2}$				
Voltage Noise, 1 kHz, RTI					
Input Noise (e_{ni})			17		nV/√Hz
Output Noise (e_{no})			253		nV/√Hz
0.1 Hz to 10 Hz, RTI					
	G = 1/16 V/V		95		µV p-p
	G = 1 V/V		5.75		µV p-p
	G = 128 V/V		330		nV p-p
0.01 Hz to 10 Hz, RTI					
	G = 1/16 V/V		100		µV p-p
	G = 1 V/V		6.8		µV p-p
	G = 128 V/V		395		nV p-p
Current Noise					
	10 Hz		100		fA/√Hz
	0.1 Hz to 10 Hz		3.1		pA p-p
	0.01 Hz to 10 Hz		4		pA p-p
INPUT CHARACTERISTICS					
Input Bias Current			±0.45	±1.5	nA
	T_A = −40°C to +85°C[1]			±4	nA
	T_A = −40°C to +105°C[1]			±14	nA
Input Offset Current			±0.2	±1.3	nA
	T_A = −40°C to +85°C[1]			±2.5	nA
	T_A = −40°C to +105°C[1]			±3.5	nA
Input Impedance	Common mode		>1‖11		GΩ‖pF
	Differential		>1‖4.7		GΩ‖pF
Input Operating Voltage Range	Guaranteed by CMRR	VSSH + 3		VDDH − 3	V
MUX_OVER_VOLT_ERR	Any input				
Positive Threshold			VDDH − 0.9		V
Negative Threshold			VSSH + 0.9		V
INPUT_ERR/G_RST	Selected input, Common-mode applied				
Positive Threshold			VDDH − 1.5		V
Negative Threshold			VSSH + 1.5		V
Switch Ax and Switch Bx Resistance	See Figure 86 for additional information		560		Ω
Switch D12 Resistance	See Figure 86 for additional information		4.05		kΩ
ANALOG OUTPUTS					
Output Voltage Swing from Each Rail	AVDD = 5 V, load resistor (R_L) = 2.49 kΩ to 2.5 V	AVSS + 0.06		AVDD − 0.08	V
	AVDD = 2.7 V, R_L = 1.8 kΩ to 1.35 V	AVSS + 0.05		AVDD − 0.06	V
Capacitive Load Drive			500		pF
Short-Circuit Current	To 2.5 V, G = 1.375, AVDD = 2.7 V to 5 V	3.5	11	25	mA
OUTPUT_ERR					
Positive Threshold			AVDD − 0.03		V
Negative Threshold			AVSS + 0.03		V
VOCM DYNAMIC PERFORMANCE					
−3 dB Bandwidth			2.3		MHz
Slew Rate			1.9		V/µs
Voltage Noise	Frequency = 1 kHz		160		nV/√Hz
Gain			1		V/V

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VOCM INPUT CHARACTERISTICS					
Input Voltage Range		AVSS		AVDD − 1	V
Input Resistance			10		GΩ
Common-Mode Offset Voltage			20		µV
Common-Mode Offset Voltage Drift			2.5		µV/°C
Input Bias Current			500		pA
DYNAMIC RESPONSE					
Small Signal ±3 dB Bandwidth					
	G = 1/16 V/V		15		kHz
	G = 1/8 V/V		28		kHz
	G = 1/4 V/V		67		kHz
	G = 1/2 V/V		138		kHz
	G = 1 V/V		1800		kHz
	G = 2 V/V		513		kHz
	G = 4 V/V		341		kHz
	G = 8 V/V		319		kHz
	G = 16 V/V		297		kHz
	G = 32 V/V		275		kHz
	G = 64 V/V		257		kHz
	G = 128 V/V		209		kHz
Settling Time 0.01%	V_{OUT} = 8 V p-p				
	G = 1 V/V		10		µs
	G = 8 V/V		8		µs
	G = 128 V/V		5		µs
Settling Time 0.0015% (16-Bit)	V_{OUT} = 8 V p-p				
	G = 1 V/V		18		µs
	G = 8 V/V		15		µs
	G = 128 V/V		15		µs
Slew Rate	V_{OUT} = 8 V p-p[2]				
	G = 1/16 V/V		0.06		V/µs
	G = 1 V/V		0.8		V/µs
	G = 128 V/V		3.1		V/µs
THD	V_{OUT} = 8 V p-p at frequency = 1 kHz				
	G = 1 V/V		−104		dB
	G = 8 V/V		−96		dB
	G = 128 V/V		−80		dB
Overload Recovery Time					
Input	Input voltage (V_{IN}) = 56 V p-p		40		µs
Output	G = 1 V/V, V_{IN} = 10 V p-p		6		µs
EXCITATION CURRENT SOURCE (IOUT)					
Output Current Range		100		1500	µA
Initial Tolerance			±3	±10	%
Drift	T_A = −40°C to +105°C		±200		ppm/°C
WIRE BREAK CURRENTS					
Output Current Range		0.25		16	µA
Impedance Threshold			(VDDH − 4)/I_{WB}[4]		Ω
Initial Tolerance			±12		%
Drift	T_A = −40°C to +105°C		±250		ppm/°C

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUTS					
Low (V_{INL})		0		0.8	V
High (V_{INH})		0.6 × DVDD		DVDD	V
Digital Input Pin Capacitance			5		pF
DIGITAL OUTPUT					
Low (V_{OL})	Sinking 4 mA			0.7	V
High (V_{OH})	Sourcing 2 mA	DVDD − 0.8			V
INTERNAL/EXTERNAL CLOCK					
Internal Clock Frequency		0.8	1	1.2	MHz
Duty Cycle			50		%
Internal Clock Divider Range		1		32	MHz/ MHz
CHARGE PUMP					
VDDH Output	VDDCP = 5 V	21.8	22.3	22.8	V
	T_A = −40°C to +105°C	21.7		22.9	V
	T_A = 25°C, VDDCP = 5 V, 500 µA VDDH load	19.9	21.3	22	V
	T_A = −40°C to +105°C	19.8		22.1	V
VSSH Output	VDDCP = 5 V	−22.8	−21.7	−20.8	V
	T_A = −40°C to +105°C	−22.9		−20.7	V
	T_A = 25°C, VDDCP = 5 V, 500 µA VSSH load	−23	−20.6	−19.8	V
	T_A = −40°C to +105°C	−23.1		−19.7	V
POWER SUPPLY					
VDDCP − DVSS		2.7		5	V
AVDD − AVSS		2.7		5	V
DVDD − DVSS		2.7		5	V
VDDCP Current, I_{VDDCP}			15.6	16.75	mA
DVSS Current, I_{DVSS}			−15.17		mA
DVDD Current, I_{DVDD}	DVDD = 3 V		170	205	µA
AVDD Current, I_{AVDD}			980	1305	µA
Static Power Dissipation	DVDD = 3 V, VDDCP = 5 V		83	91	mW
	DVDD = 3 V, VDDCP = 2.7 V		34	53	mW

[1] Guaranteed by design. These specifications are not production tested but are supported by characterization data at the initial product release.

[2] For gains less than 1/2, a smaller output swing is used.

[3] Only G = 1 V/V is production tested.

[4] I_{WB} means wire break current.

SPECIFICATIONS

TIMING SPECIFICATIONS

VDDCP = 5 V, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3V, DVSS = 0 V, and VOCM = AVDD/2 V.

Table 2. Digital Values and Serial Peripheral Interface (SPI) Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Maximum Clock Rate (SCLK)				5	MHz
Minimum Pulse Width (SCLK)					
High	t_{PWH}	75			ns
Low	t_{PWL}	75			ns
SDI/SDO to SCLK Setup Time	t_{DS}	10			ns
SDI/SDO to SCLK Hold Time	t_{DH}	10			ns
Data Valid, SDO to SCLK	t_{DV}	50			ns
Setup Time, $\overline{CS}$ to SCLK	t_{DCS}	30			ns

Timing Diagrams

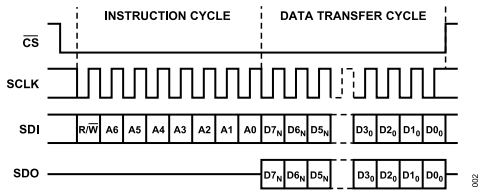

Figure 2. SPI Timing Diagram, MSB First

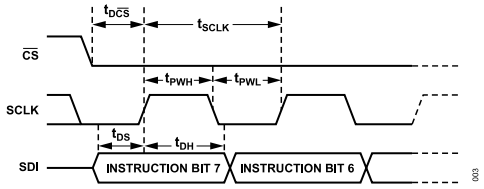

Figure 3. SPI Register Write Timing Diagram

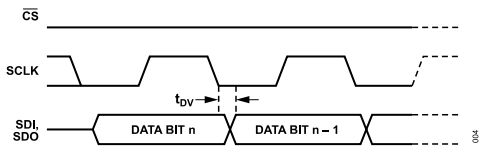

Figure 4. SPI Register Read Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VDDH	VSSH – 0.3 V to VSSH + 60 V
VDDCP	DVSS – 0.3 V to DVSS + 5.5 V
AVDD	AVSS – 0.3 V to AVSS + 5.5 V
DVDD	DVSS – 0.3 V to DVSS + 5.5 V
AVSS or DVSS	
Voltage	VSSH – 0.3 V to VSSH + 30 V
	VDDH – 30 V to VDDH + 0.3 V
Current	±10 mA
VDDH/VSSH Current	±10 mA
Input Voltage (+IN1, −IN1, +IN2, or −IN2)	VSSH − 60 V to VSSH + 60 V
Differential Input Voltage Between Any Two Amplifier Inputs (+IN1, −IN1, +IN2, or −IN2)	60 V
−OUT, +OUT Short-Circuit Current	Indefinite
VOCM	
Voltage	AVSS – 0.3 V to AVDD + 0.3 V
Current	±10 mA
Digital Inputs Voltage and Outputs Voltage (SPI and GPIO)	DVSS – 0.3 V to DVDD + 0.3 V
Digital Inputs Current (SPI and GPIO)	±10 mA
IOUT	
Voltage	AVSS – 0.3 V to AVDD + 0.3 V
Current	±10 mA
Temperature	
Operating Range	−40°C to +125°C
Specified Range	−40°C to +105°C
Maximum Junction	150°C
Storage Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient, thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
CP-28-11	36.9	1.9	°C/W

[1] The thermal resistance values specified in Table 4 are simulated based on JEDEC specifications (unless specified otherwise) and must be used in compliance with JESD51-12.

Refer to the ESD Map section for a schematic of ESD diodes and paths.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

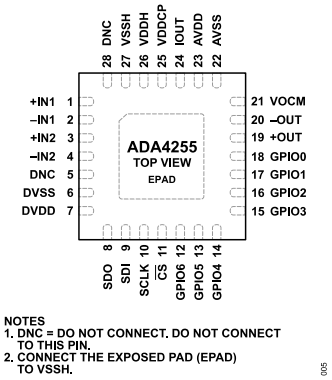

Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Pin Description
1	+IN1	Channel 1 Positive Input.
2	−IN1	Channel 1 Negative Input.
3	+IN2	Channel 2 Positive Input.
4	−IN2	Channel 2 Negative Input.
5, 28	DNC	Do Not Connect. Do not connect to this pin.
6	DVSS	Negative Digital Supply Voltage.
7	DVDD	Positive Digital Supply Voltage.
8	SDO	SPI Serial Data Output.
9	SDI	SPI Serial Data Input.
10	SCLK	SPI Serial Clock Input.
11	$\overline{CS}$	SPI Chip Select Input.
12	GPIO6	GPIO6/SCS6.
13	GPIO5	GPIO5/SCS5.
14	GPIO4	GPIO4/SCS4/Clock Input or Output.
15	GPIO3	GPIO3/SCS3/Fault Interrupt Output.
16	GPIO2	GPIO2/SCS2/Calibration Busy Out.
17	GPIO1	GPIO1/SCS1/External Multiplexer Control 1.
18	GPIO0	GPIO0/SCS0/External Multiplexer Control 0.
19	+OUT	Positive Output.
20	−OUT	Negative Output.
21	VOCM	Output Amplifier Common-Mode Voltage Input. The VOCM pin is high impedance and is not internally biased.
22	AVSS	Output Amplifier Negative Supply Voltage.
23	AVDD	Output Amplifier Positive Supply Voltage.
24	IOUT	Excitation Current Source Output.
25	VDDCP	Charge Pump Supply Voltage.
26	VDDH	Positive High Voltage Charge Pump Output. VDDH handles 500 µA load.
27	VSSH	Negative High Voltage Charge Pump Output. VSSH handles 500 µA load.
EPAD		Exposed Pad. Connect the exposed pad (EPAD) to VSSH.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, VDDCP = 5 V, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, DVSS = 0 V, VOCM = AVDD/2, and no load, unless otherwise noted.

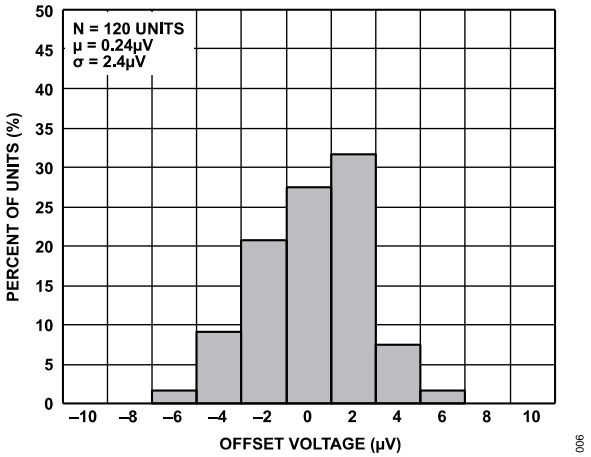

Figure 6. Offset Voltage Distribution, RTI (Gain = 128 V/V)

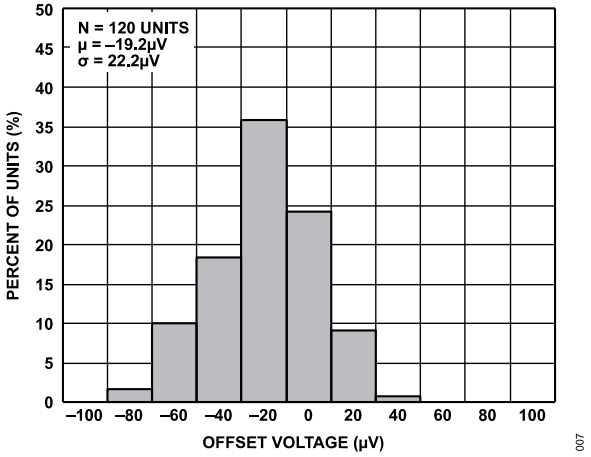

Figure 7. Offset Voltage Distribution, RTI (Gain = 1 V/V)

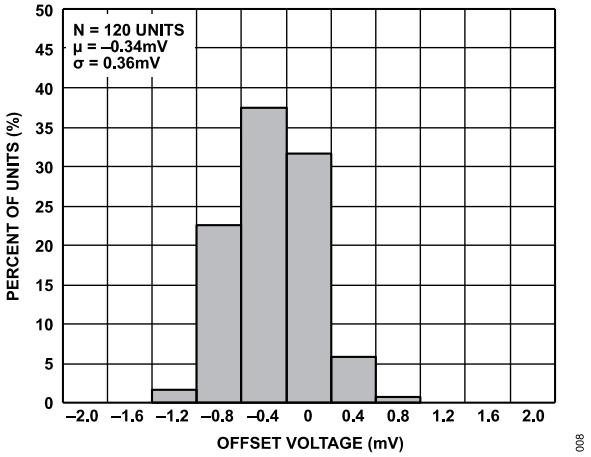

Figure 8. Offset Voltage Distribution, RTI (Gain = 1/16 V/V)

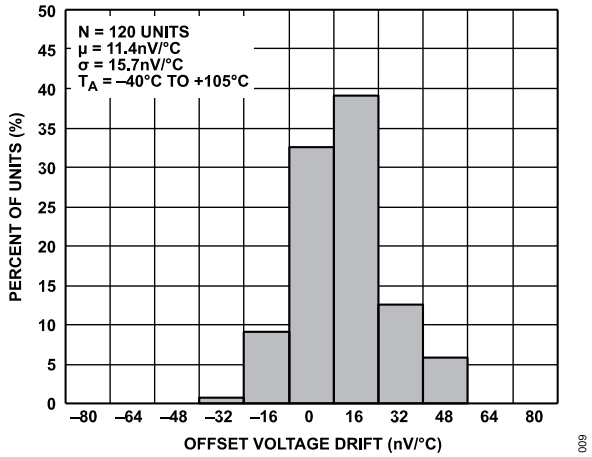

Figure 9. Offset Voltage Drift Distribution, RTI (Gain = 128 V/V)

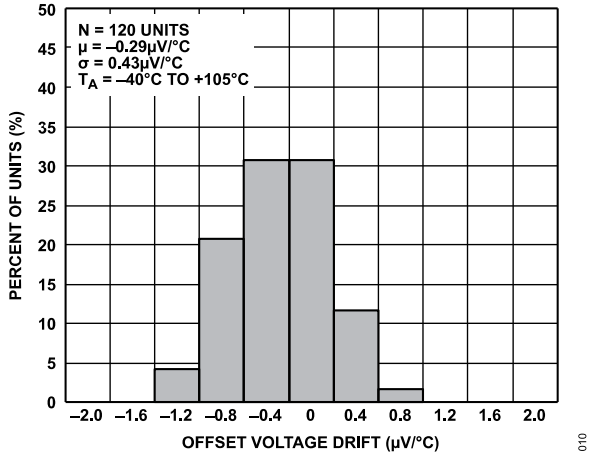

Figure 10. Offset Voltage Drift Distribution, RTI (Gain = 1 V/V)

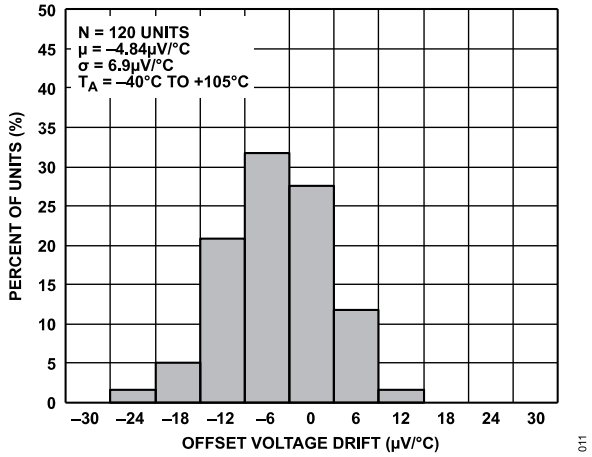

Figure 11. Offset Voltage Drift Distribution, RTI (Gain = 1/16 V/V)

TYPICAL PERFORMANCE CHARACTERISTICS

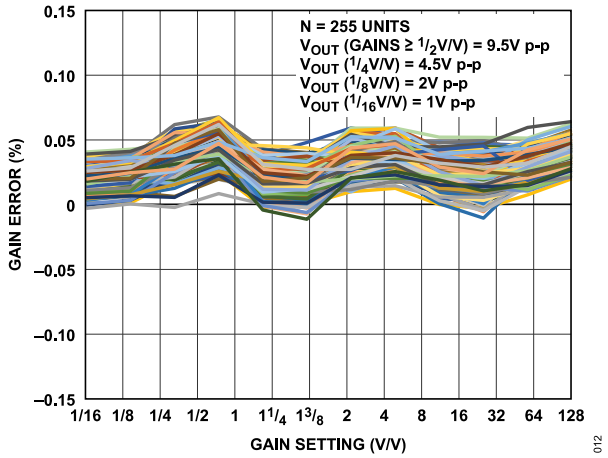

Figure 12. Gain Error vs. Gain Setting

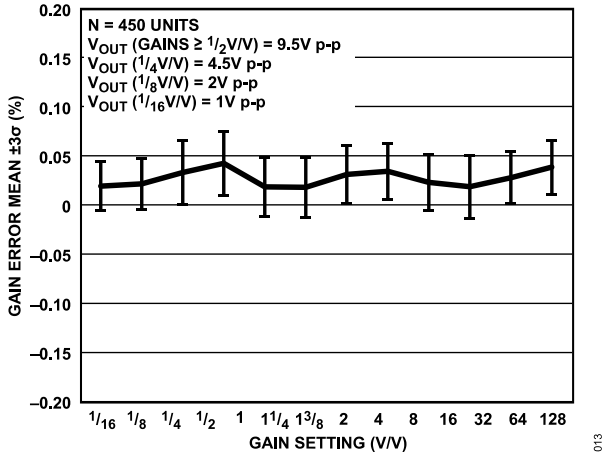

Figure 13. Gain Error Mean ±3 σ vs. Gain Setting

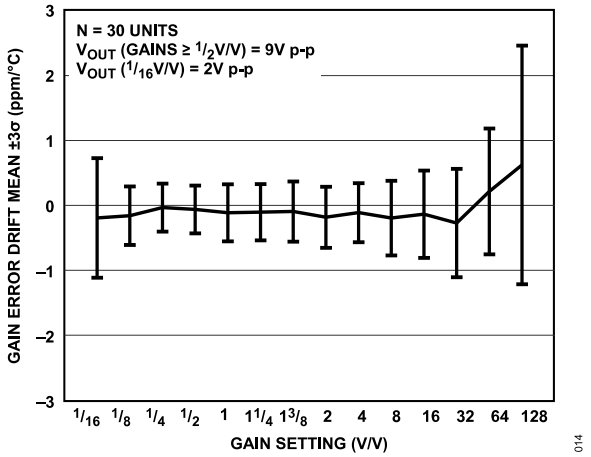

Figure 14. Gain Error Drift Mean ±3 σ vs. Gain Setting

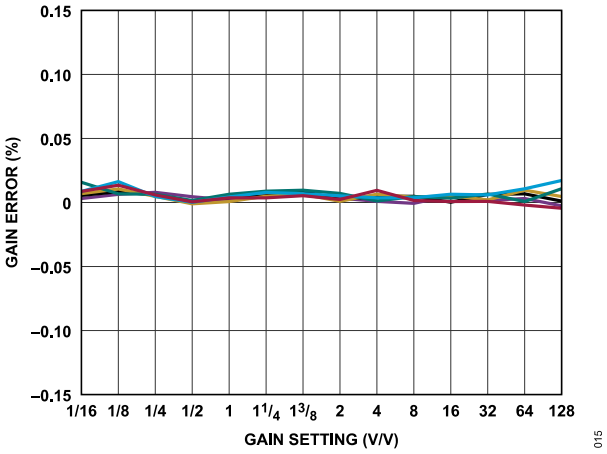

Figure 15. Gain Error vs. Gain Setting Using Calibration Coefficients

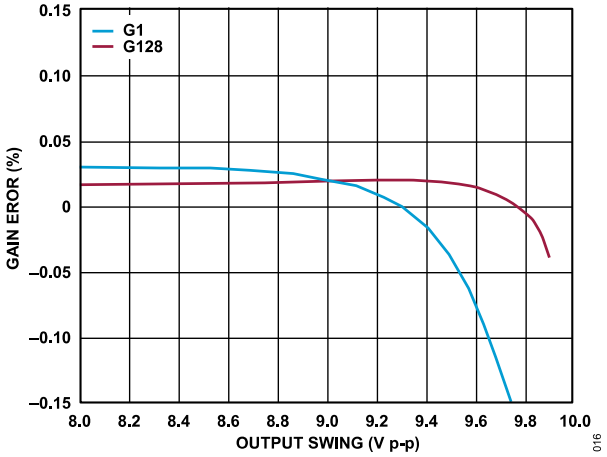

Figure 16. Gain Error vs. Output Swing

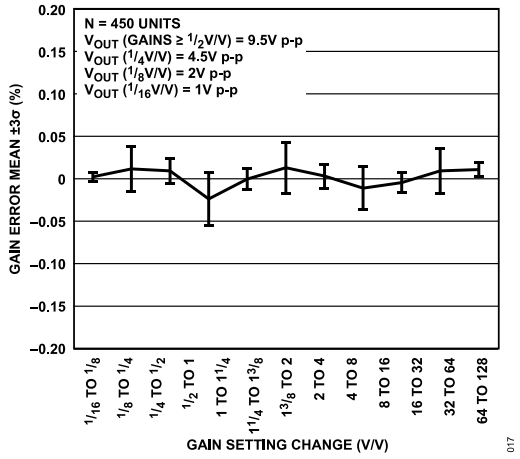

Figure 17. Gain Error Deviation Between Sequential Gain Settings

TYPICAL PERFORMANCE CHARACTERISTICS

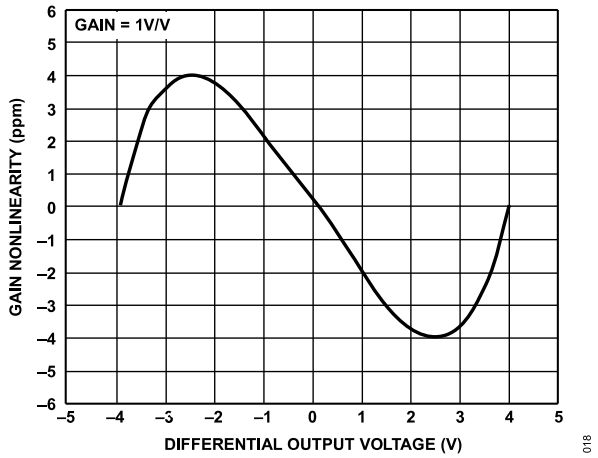

Figure 18. Gain Nonlinearity vs. Differential Output Voltage

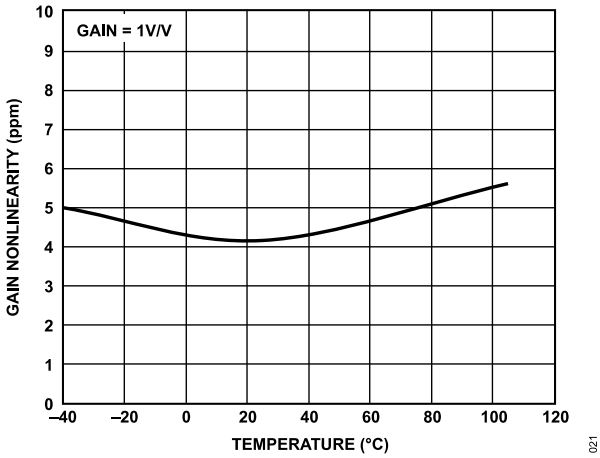

Figure 21. Gain Nonlinearity vs. Temperature

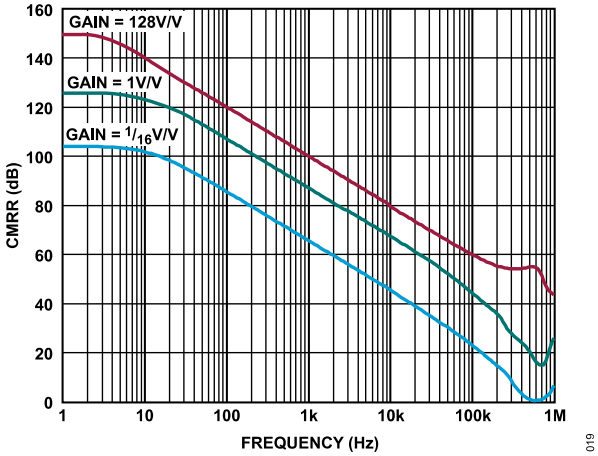

Figure 19. CMRR vs. Frequency

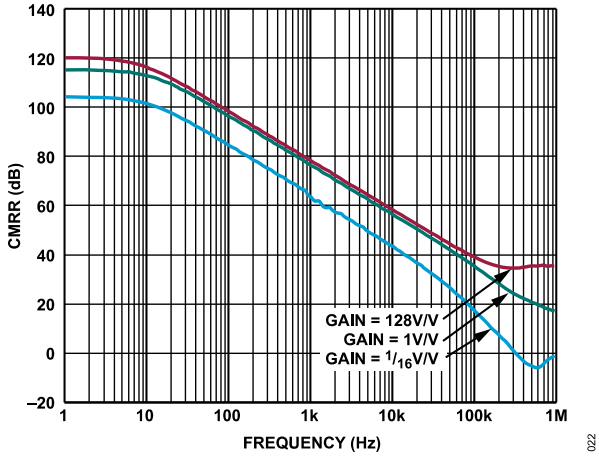

Figure 22. CMRR vs. Frequency with 1 kΩ Imbalance

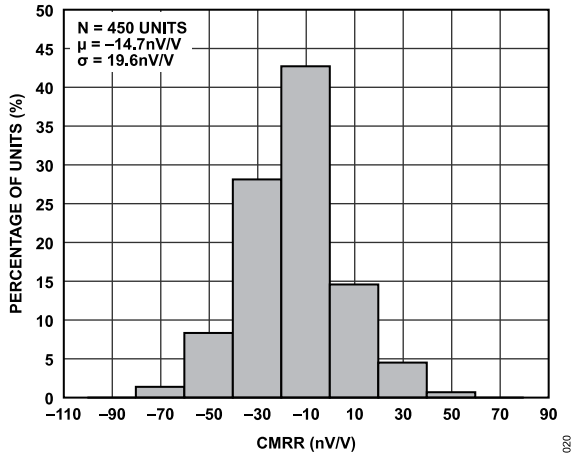

Figure 20. CMRR Distribution (Gain = 128 V/V)

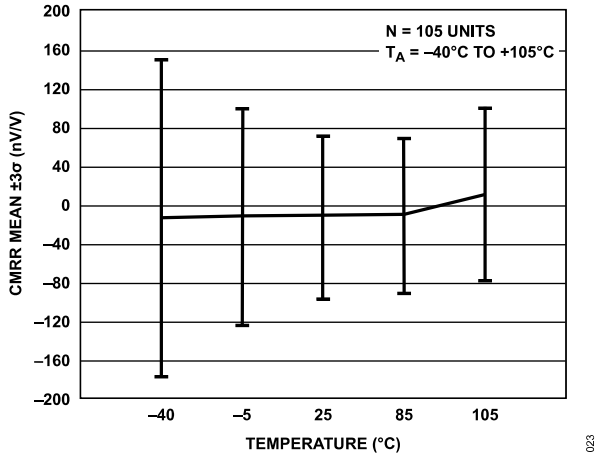

Figure 23. CMRR Mean ±3 σ vs. Temperature (Gain = 128 V/V)

TYPICAL PERFORMANCE CHARACTERISTICS

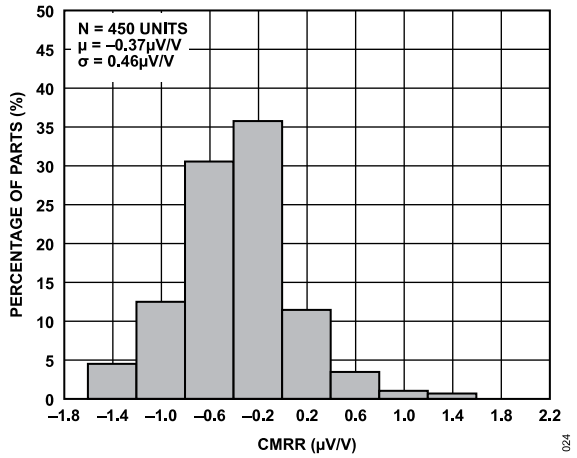

Figure 24. CMRR Distribution (Gain = 1 V/V)

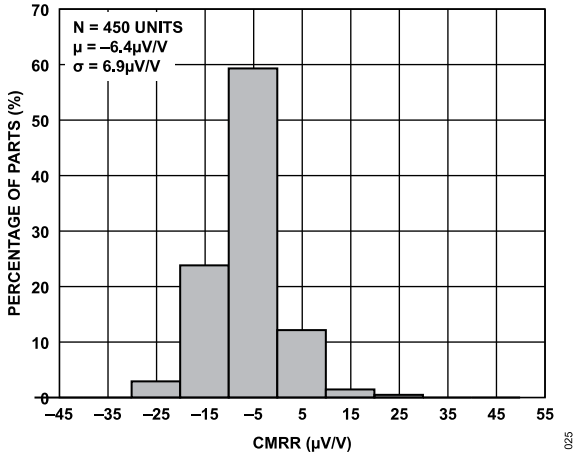

Figure 25. CMRR Distribution (Gain = 1/16 V/V)

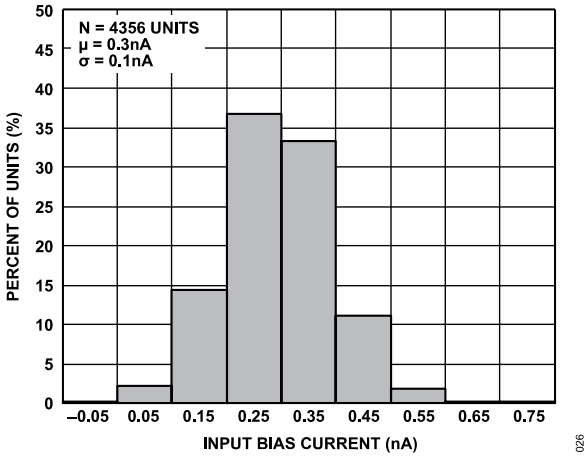

Figure 26. Input Bias Current Distribution

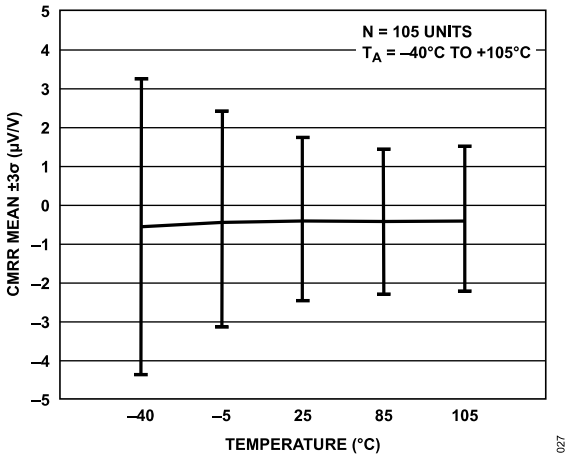

Figure 27. CMRR Mean ±3 σ vs. Temperature (Gain = 1 V/V)

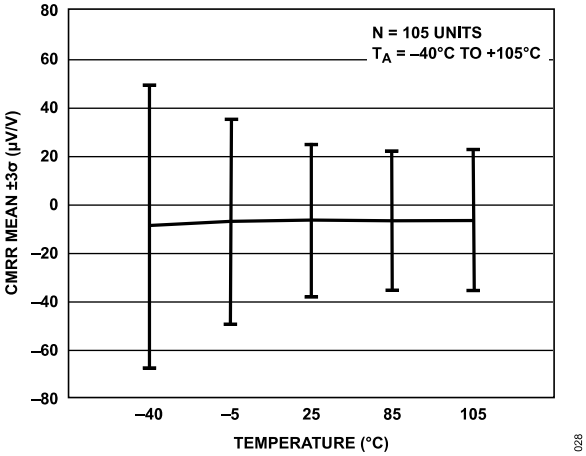

Figure 28. CMRR Mean ±3 σ vs. Temperature (Gain = 1/16 V/V)

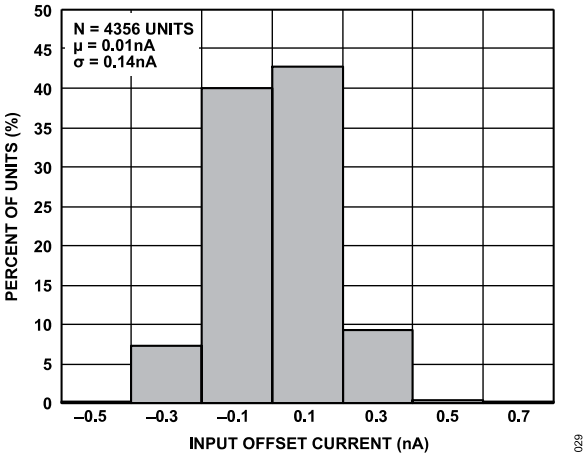

Figure 29. Input Offset Current Distribution

TYPICAL PERFORMANCE CHARACTERISTICS

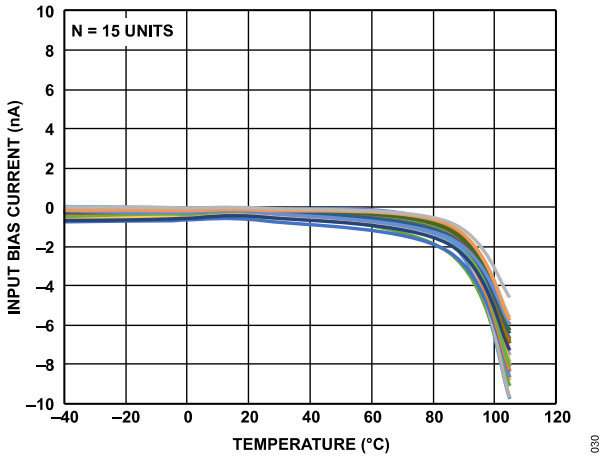

Figure 30. Input Bias Current vs. Temperature

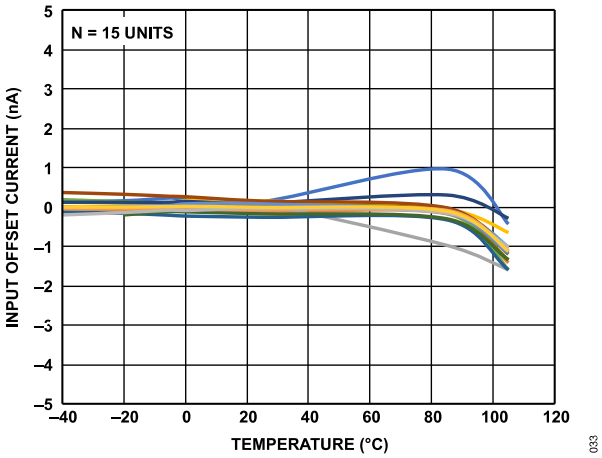

Figure 33. Input Offset Current vs. Temperature

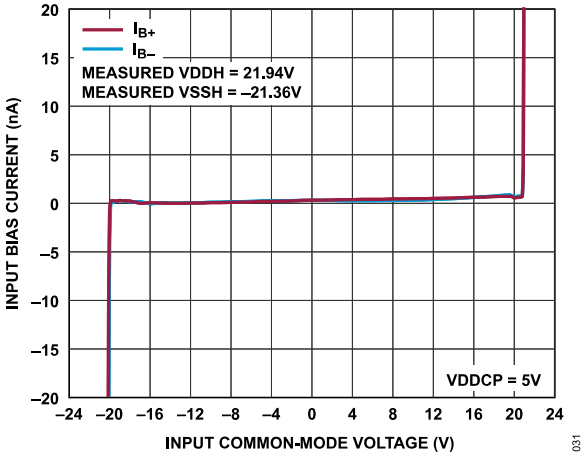

Figure 31. Input Bias Current vs. Input Common-Mode Voltage

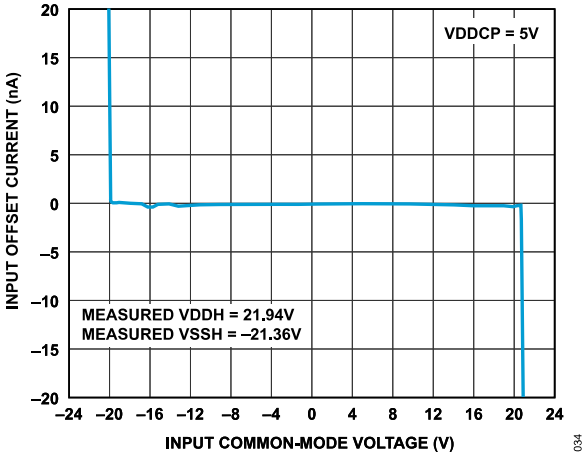

Figure 34. Input Offset Current vs. Input Common-Mode Voltage

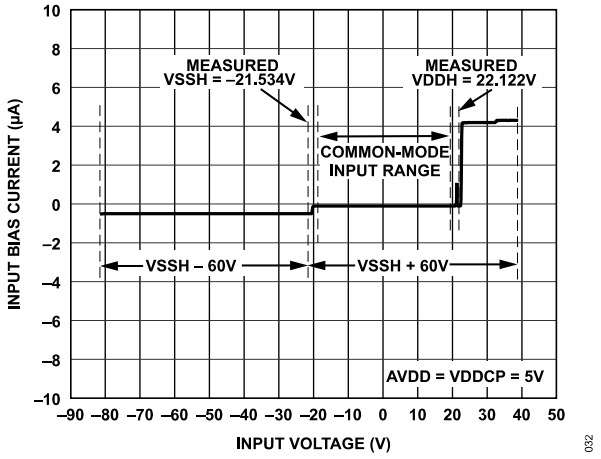

Figure 32. Input Bias Current vs. Input Voltage, VDDCP = AVDD = 5 V

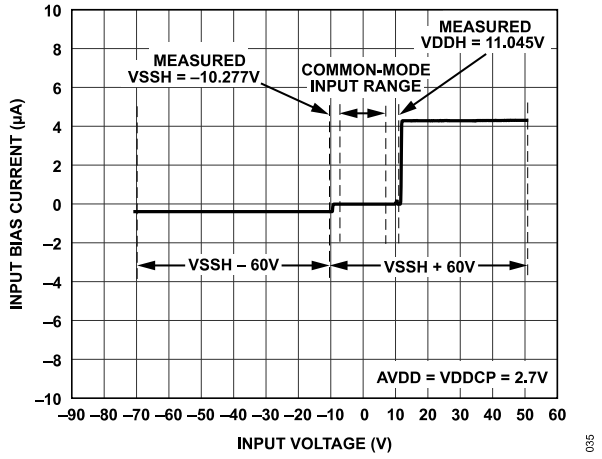

Figure 35. Input Bias Current vs. Input Voltage, VDDCP = AVDD = 2.7 V

TYPICAL PERFORMANCE CHARACTERISTICS

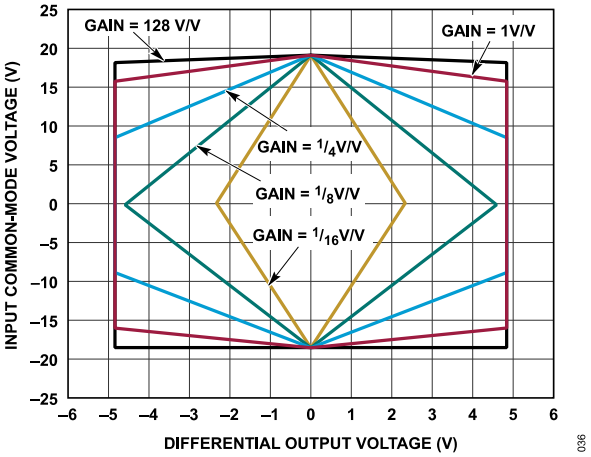

Figure 36. Input Common-Mode Voltage vs. Differential Output Voltage

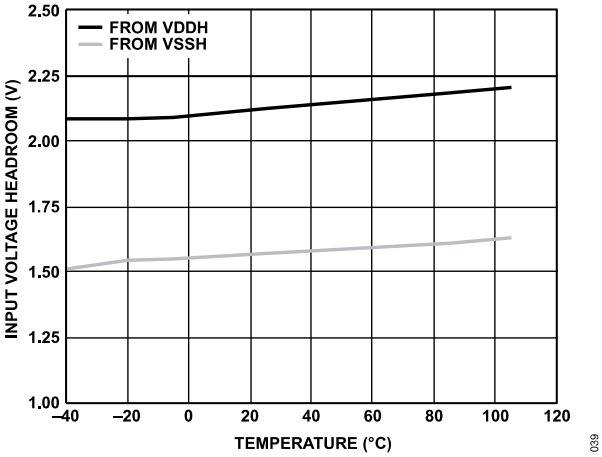

Figure 39. Input Voltage Headroom vs. Temperature

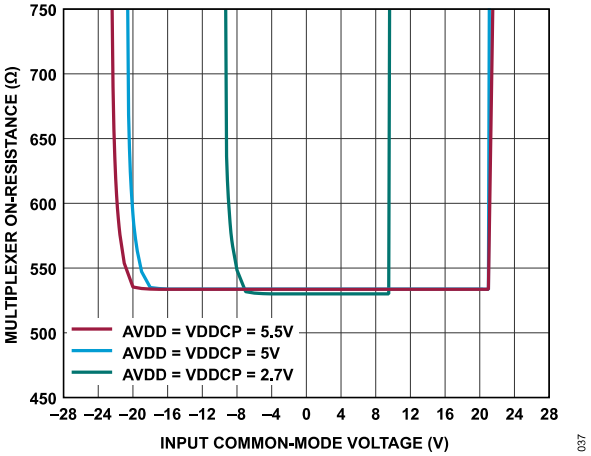

Figure 37. Multiplexer On-Resistance vs. Input Common-Mode Voltage

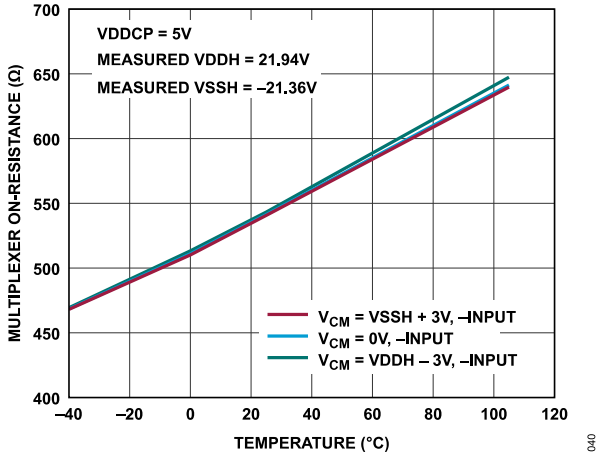

Figure 40. Multiplexer On-Resistance vs. Temperature

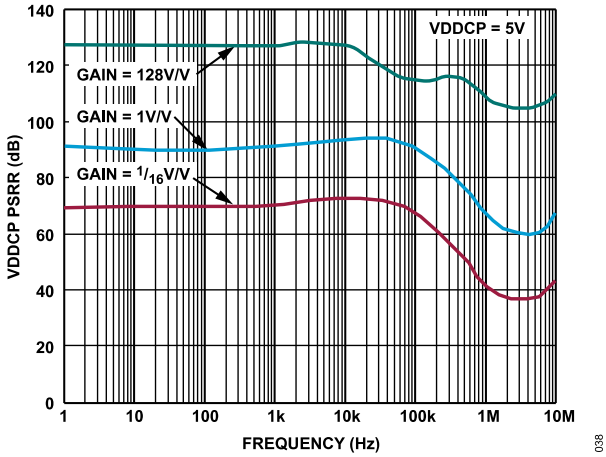

Figure 38. VDDCP PSRR vs. Frequency

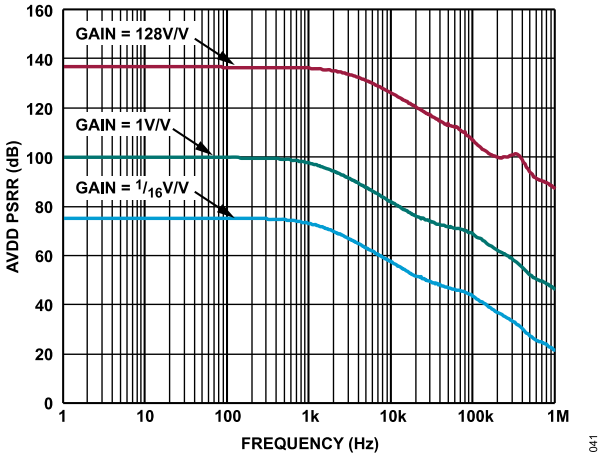

Figure 41. AVDD PSRR vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

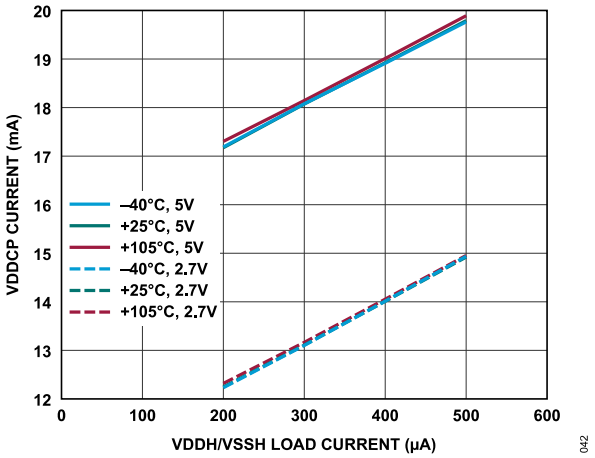

Figure 42. VDDCP Current vs. VDDH/VSSH Load Current

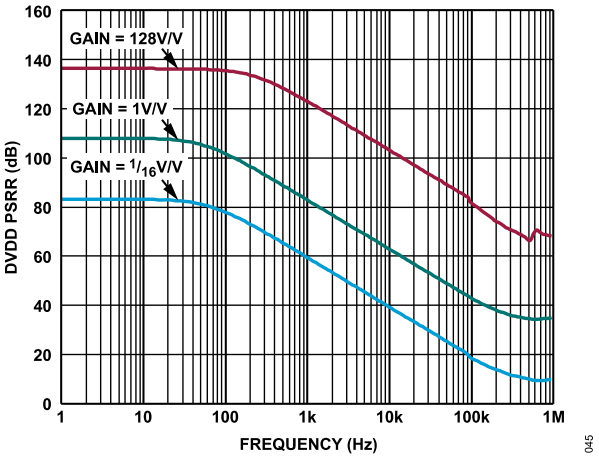

Figure 45. DVDD PSRR vs. Frequency

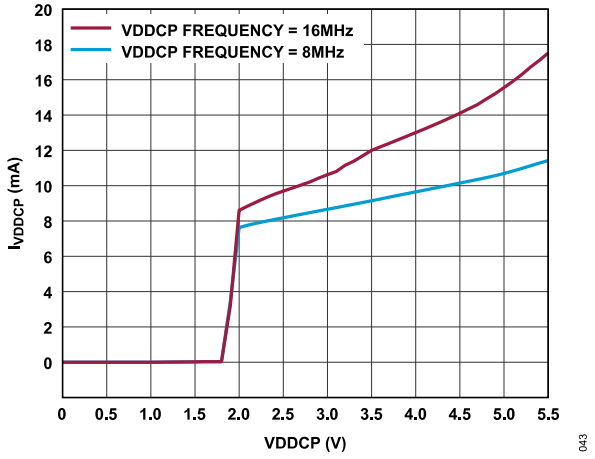

Figure 43. I_{VDDCP} vs. VDDCP

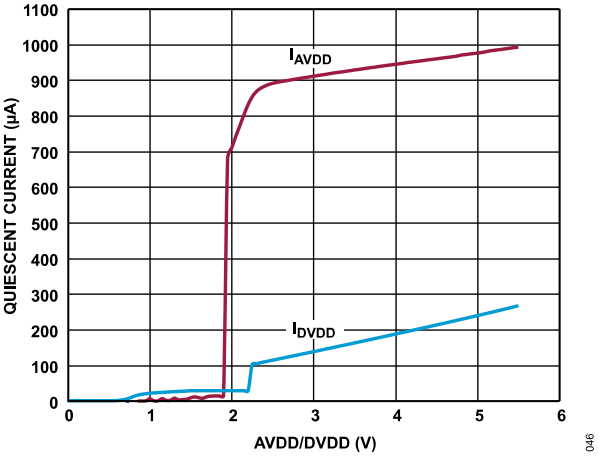

Figure 46. Quiescent Current vs. AVDD and DVDD

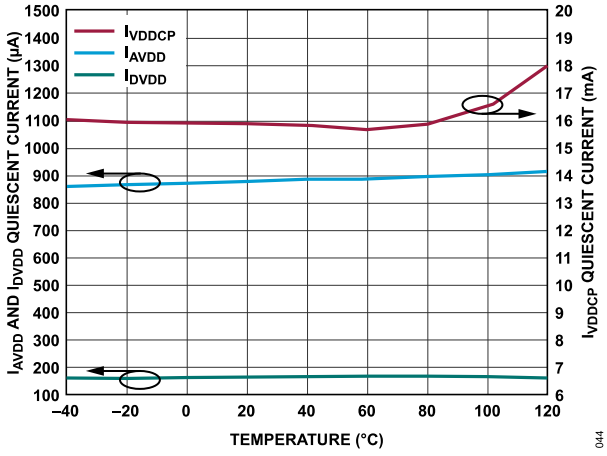

Figure 44. I_{AVDD}, I_{DVDD}, and I_{VDDCP} Quiescent Current vs. Temperature

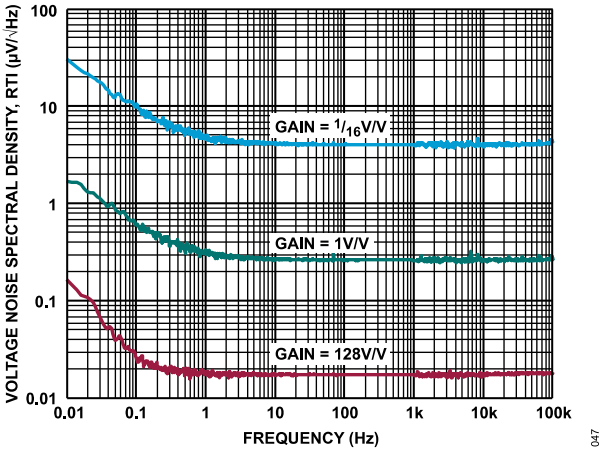

Figure 47. Voltage Noise Spectral Density, RTI vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

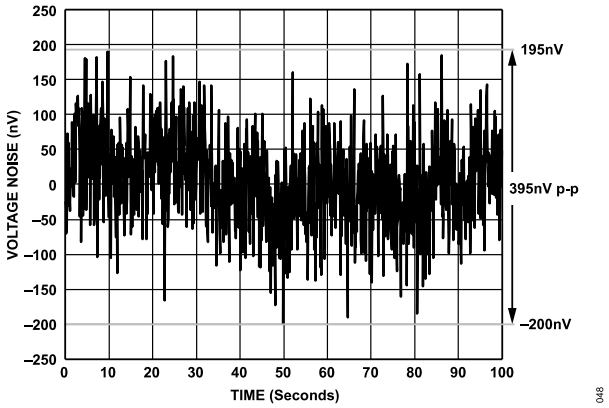

Figure 48. 0.01 Hz to 10 Hz Voltage Noise, RTI (Gain = 128 V/V)

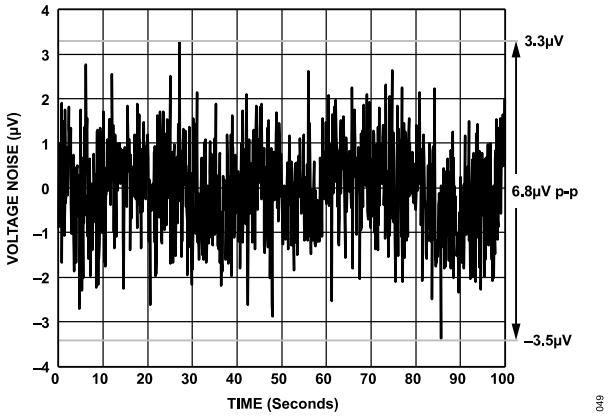

Figure 49. 0.01 Hz to 10 Hz Voltage Noise, RTI (Gain = 1 V/V)

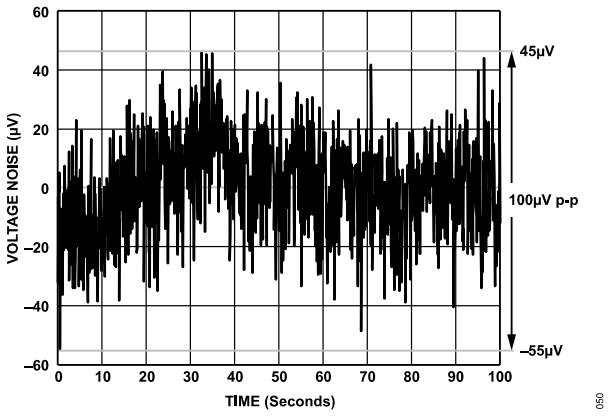

Figure 50. 0.01 Hz to 10 Hz Voltage Noise, RTI (Gain = 1/16 V/V)

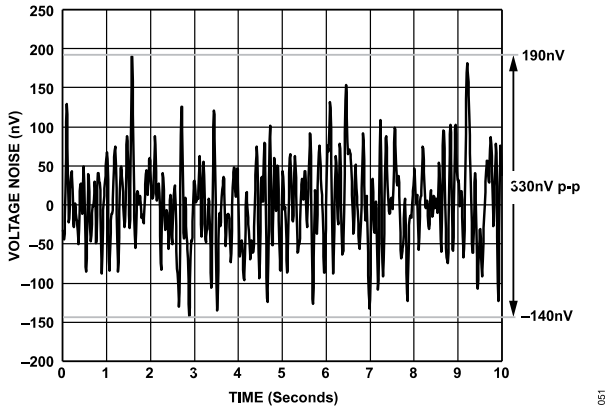

Figure 51. 0.1 Hz to 10 Hz Voltage Noise, RTI (Gain = 128 V/V)

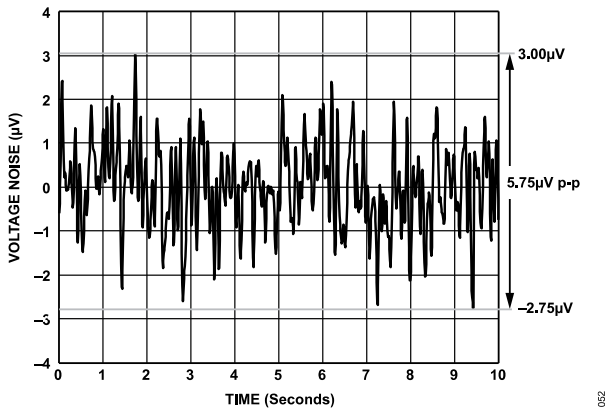

Figure 52. 0.1 Hz to 10 Hz Voltage Noise, RTI (Gain = 1 V/V)

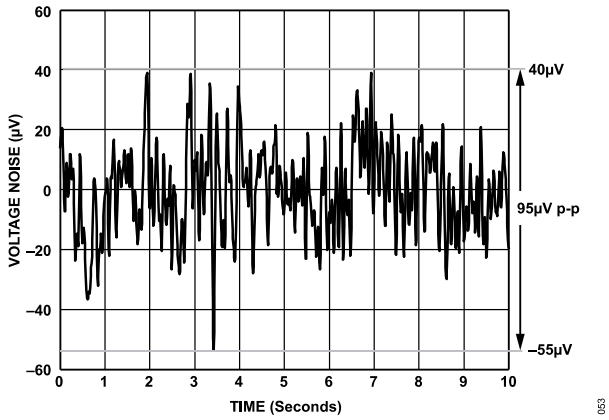

Figure 53. 0.1 Hz to 10 Hz Voltage Noise, RTI (Gain = 1/16 V/V)

TYPICAL PERFORMANCE CHARACTERISTICS

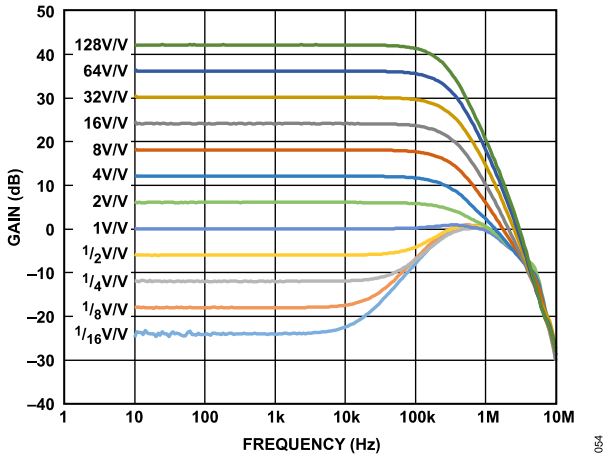

Figure 54. Small Signal Frequency Response

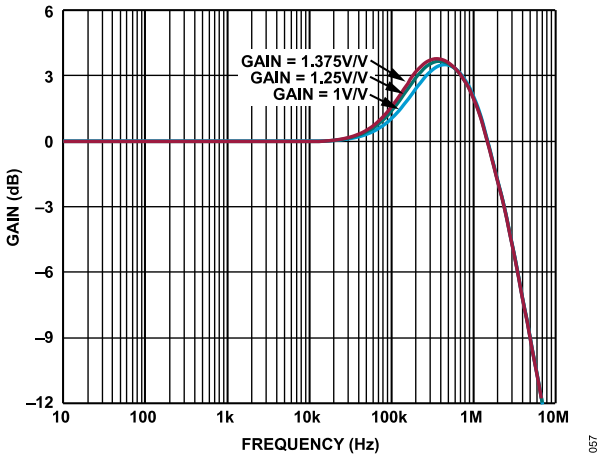

Figure 57. VOCM Small Signal Frequency Response

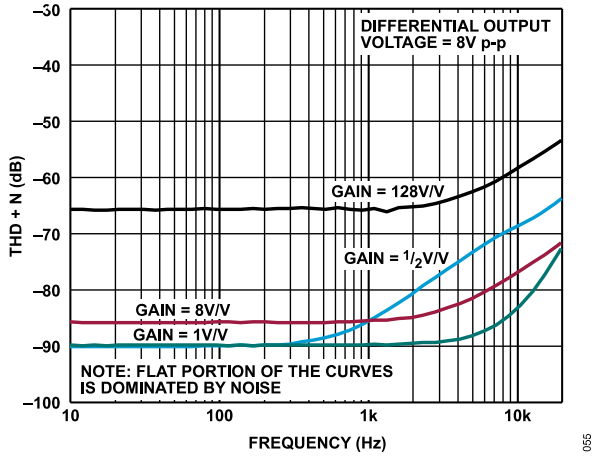

Figure 55. Total Harmonic Distortion Plus Noise (THD + N) vs. Frequency with 100 kHz Filter, Differential Load Resistor ($R_{L, DIFF}$) = 5 kΩ

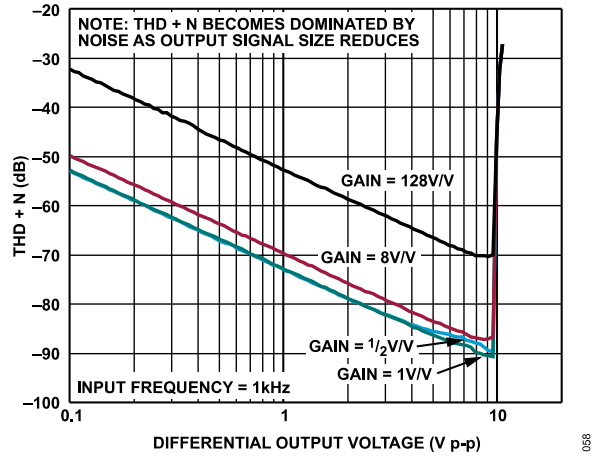

Figure 58. THD + N vs. Differential Output Voltage with 100 kHz Filter, $R_{L, DIFF}$ = 5 kΩ

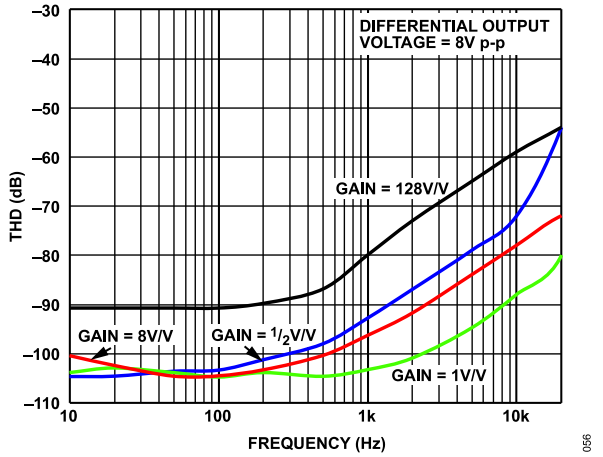

Figure 56. THD vs. Frequency, $R_{L, DIFF}$ = 5 kΩ

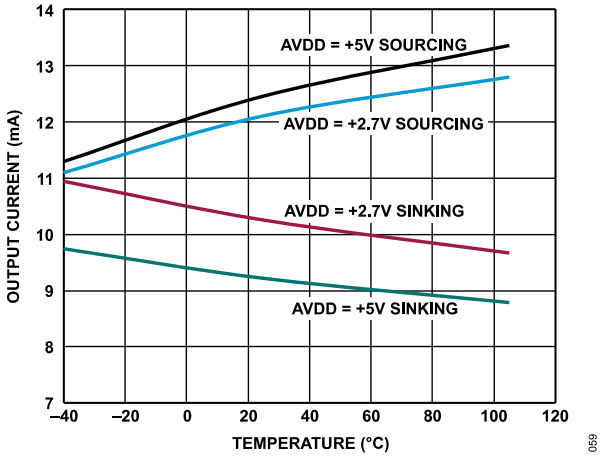

Figure 59. Sinking and Sourcing Short-Circuit Output Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

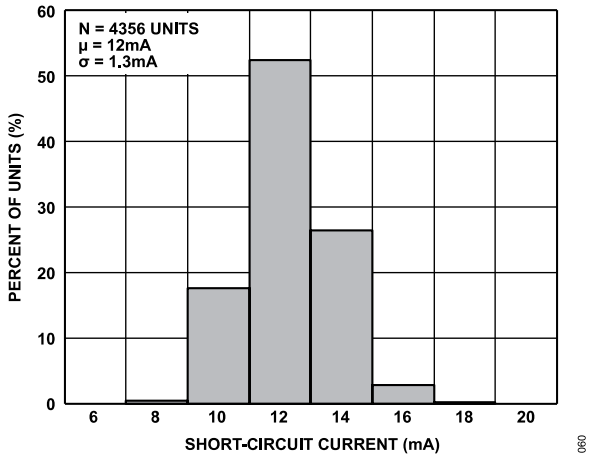

Figure 60. Sourcing Short-Circuit Current Distribution

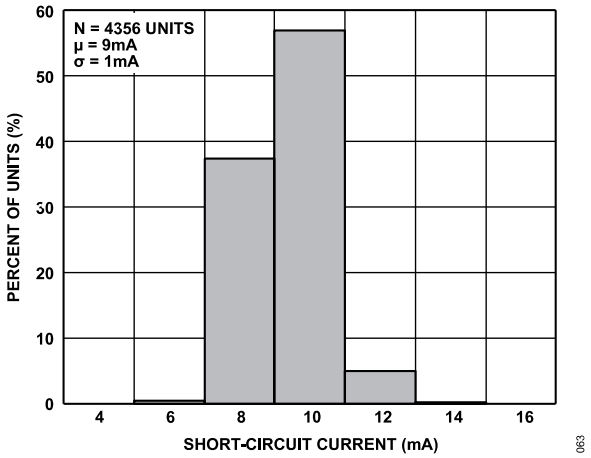

Figure 63. Sinking Short-Circuit Current Distribution

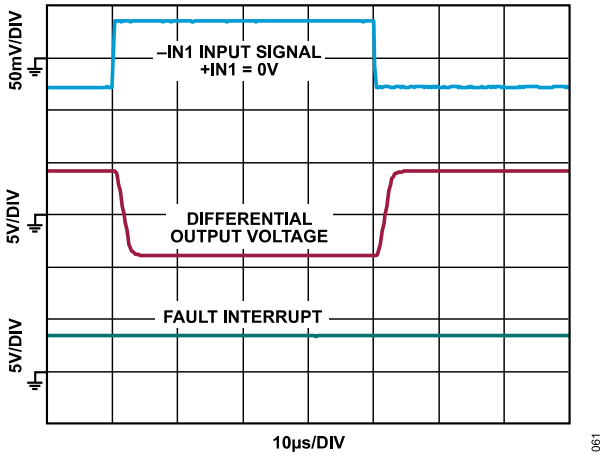

Figure 61. Large Signal Step Response (Gain = 128 V/V)

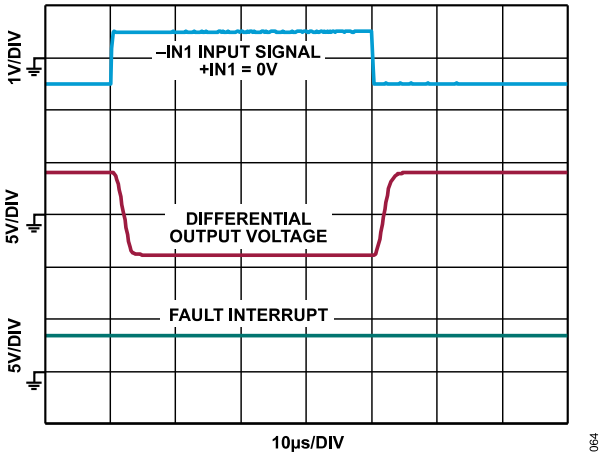

Figure 64. Large Signal Step Response (Gain = 8 V/V)

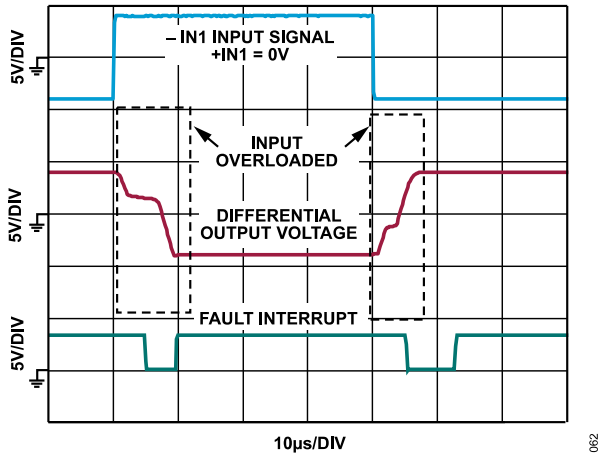

Figure 62. Input Overload Recovery Step Response (Gain = 1 V/V)

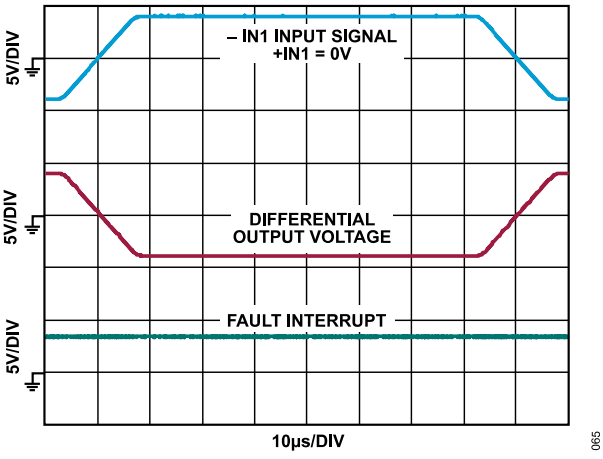

Figure 65. Large Signal Step Response (Gain = 1 V/V)

TYPICAL PERFORMANCE CHARACTERISTICS

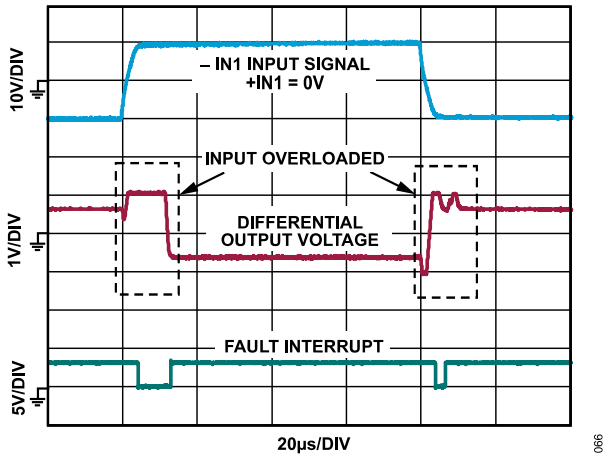

Figure 66. Input Overload Recovery Step Response (Gain = 1/16 V/V)

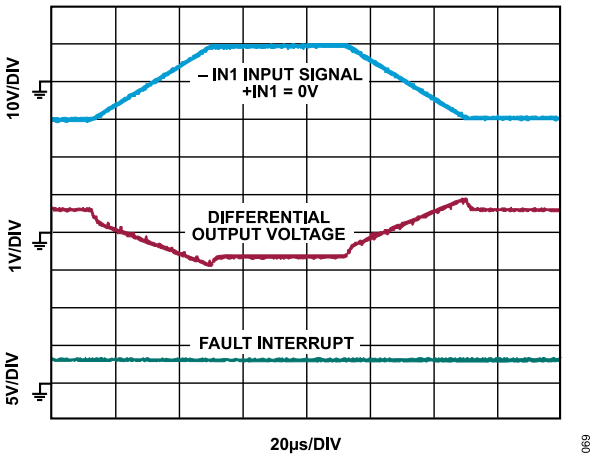

Figure 69. Large Step Response (Gain = 1/16 V/V)

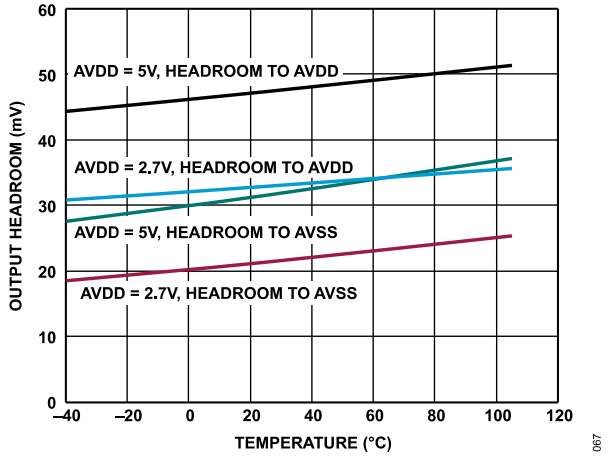

Figure 67. Output Headroom vs. Temperature

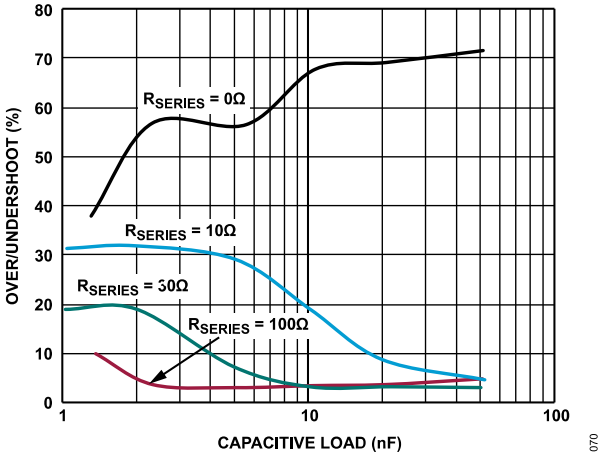

Figure 70. Overshoot and Undershoot vs. Capacitive Load

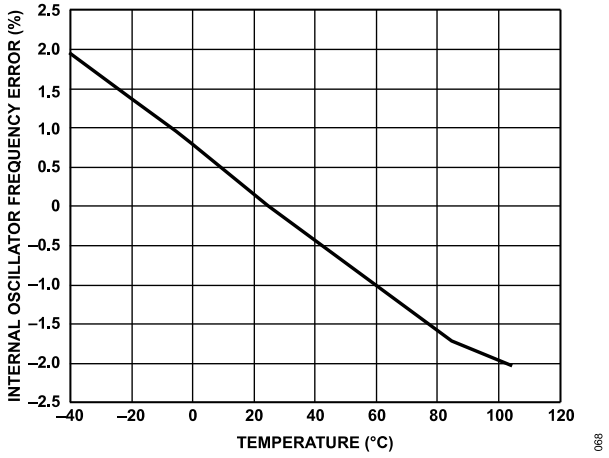

Figure 68. Internal Oscillator Frequency Error vs. Temperature

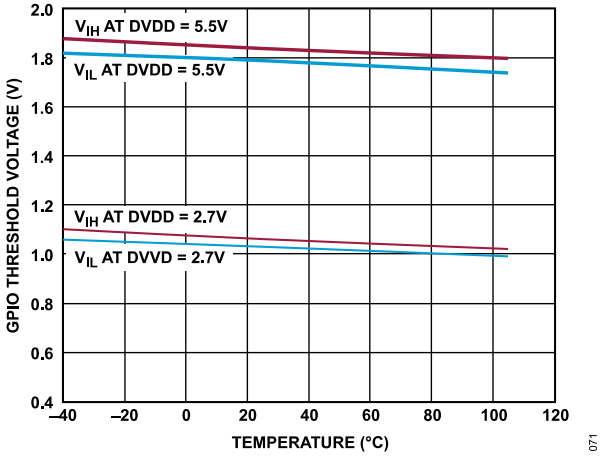

Figure 71. GPIO Threshold Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

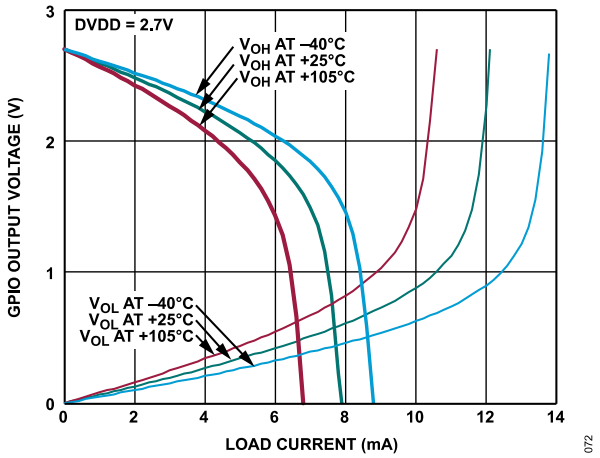

Figure 72. GPIO Output Voltage (V_{OH}/V_{OL}) vs. Load Current for Various Temperatures, DVDD = 2.7 V

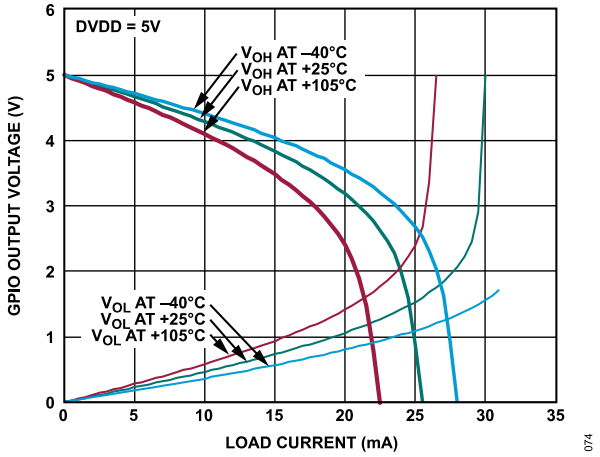

Figure 73. GPIO Output Voltage (V_{OH}/V_{OL}) vs. Load Current for Various Temperatures, DVDD = 5 V

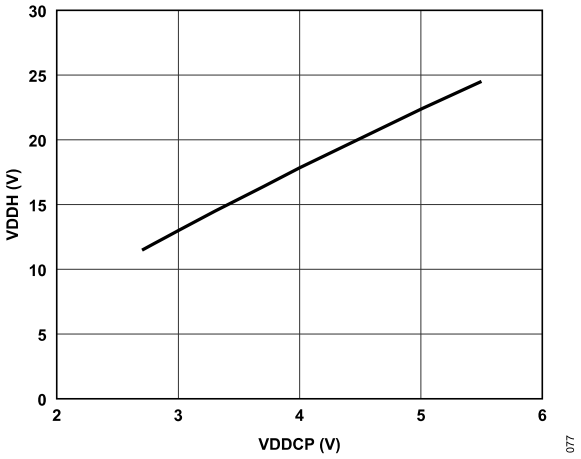

Figure 74. VDDH vs. VDDCP

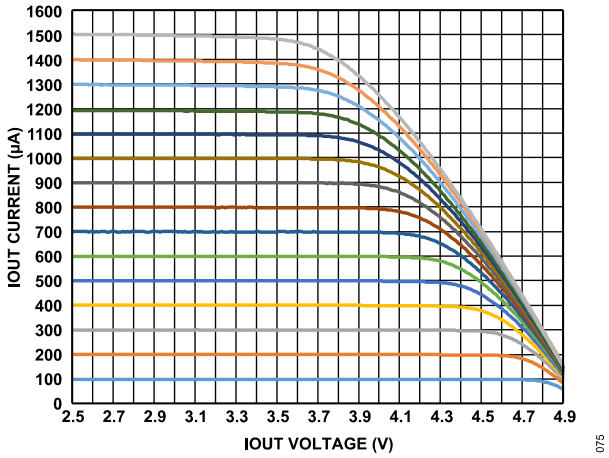

Figure 75. IOUT Current vs. IOUT Voltage

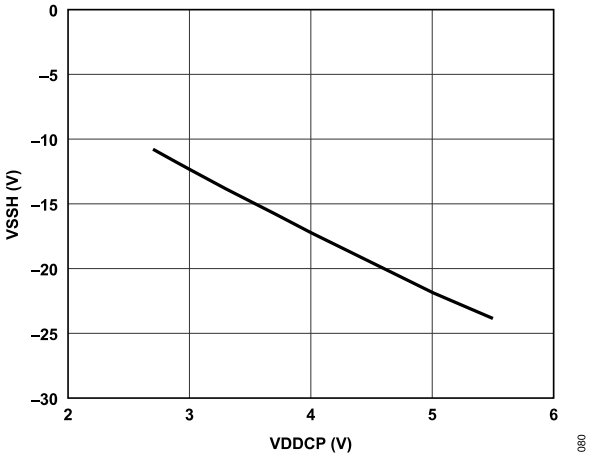

Figure 76. VSSH vs. VDDCP

TYPICAL PERFORMANCE CHARACTERISTICS

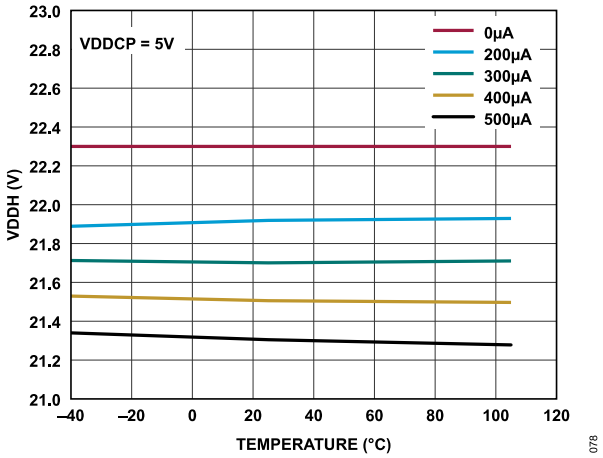

Figure 77. VDDH vs. Temperature for Various VDDH Loads, VDDCP = 5 V

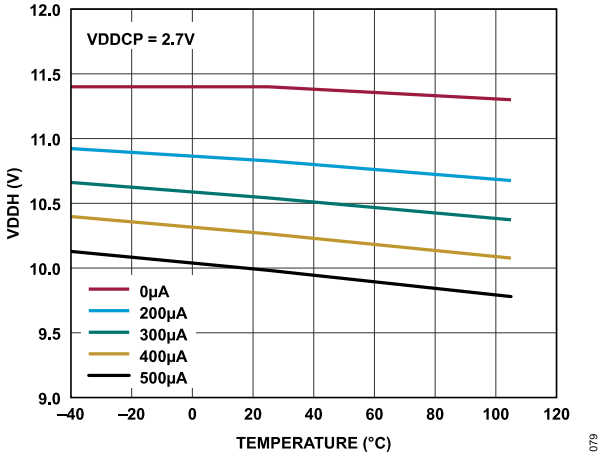

Figure 78. VDDH vs. Temperature for Various VDDH Loads, VDDCP = 2.7 V

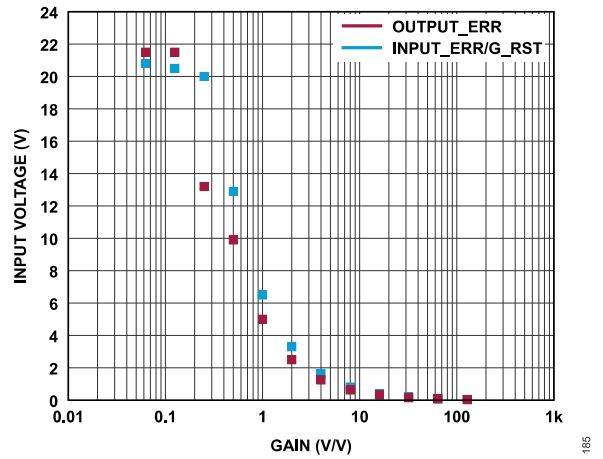

Figure 79. Positive Error Trip Thresholds with Single-Ended Input

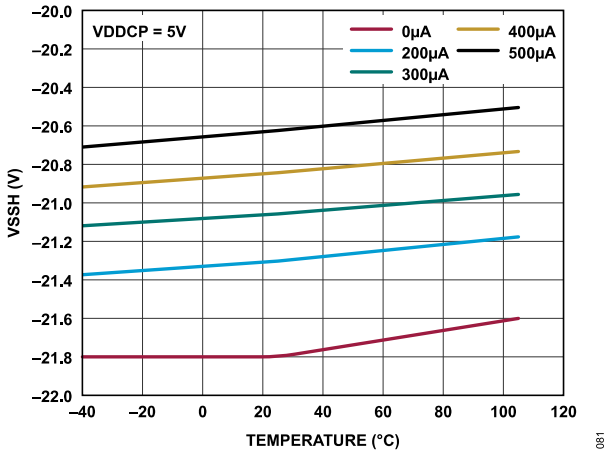

Figure 80. VSSH vs. Temperature for Various VSSH Loads, VDDCP = 5 V

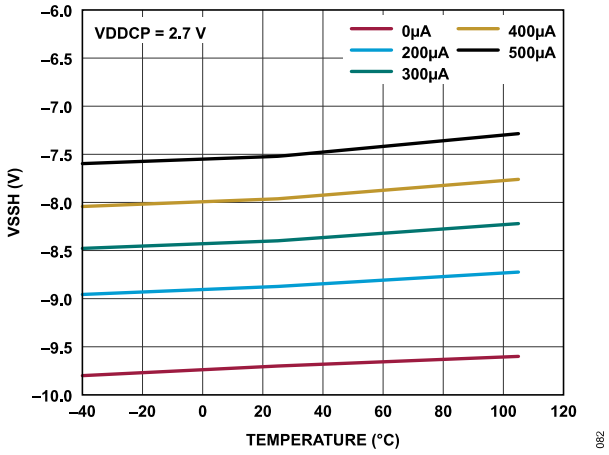

Figure 81. VSSH vs. Temperature for Various VSSH Loads, VDDCP = 2.7 V

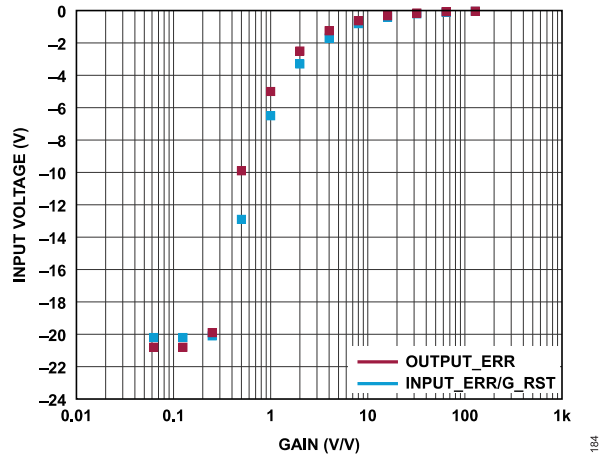

Figure 82. Negative Error Trip Thresholds with Single-Ended Input

TYPICAL PERFORMANCE CHARACTERISTICS

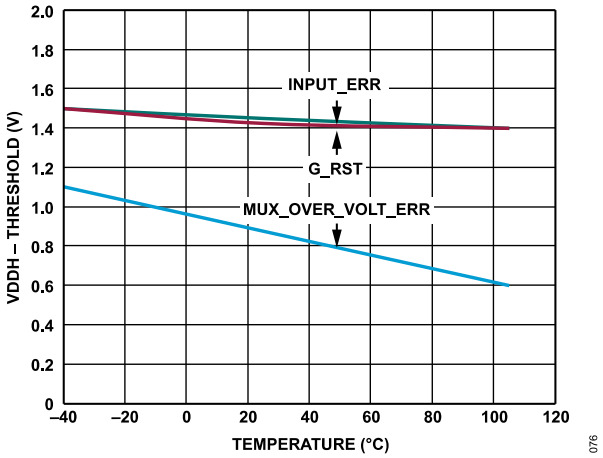

Figure 83. Error Flag Positive Trip Voltage (VDDH – Threshold) vs. Temperature

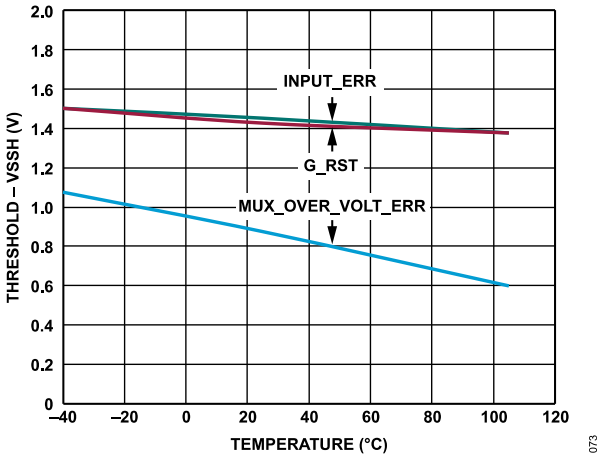

Figure 84. Error Flag Negative Trip Voltage (Threshold – VSSH) vs. Temperature

THEORY OF OPERATION

PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER

The ADA4255 is a direct current mode instrumentation amplifier implemented with zero drift amplifiers. The ADA4255 topology ensures precision operation over temperature. Refer to the simplified architecture shown in Figure 85 to understand the following circuit description.

The input multiplexer connects the inputs to Amplifier A3 and Amplifier A7, which are configured to replicate these input voltages on the R_{IN} input resistor. The A1, A2, A5, and A6 amplifiers are configured to replicate the internal reference voltage, V_{REF}, on R1, R2, R5, and R6, creating four nominally equal dc bias currents in the drains of M1, M2, M5, and M6. Amplifier A4 and Amplifier A8 are configured to replicate the currents in R3 and R7 in the drains of M4 and M8, respectively, forming current mirrors.

When a positive voltage is applied to the ADA4255 inputs, a proportional current is conducted by R_{IN}. The drain currents of M3 and M4 increase by this amount, and the drain currents of M7 and M8 reduce by this amount. This portion of the amplifier operates as a transconductance with differential output, each having a gain of $1/R_{IN}$. Output Amplifier A9 is configured as a transimpedance amplifier with a gain of R_{OUT}. A9 provides a common-mode level shift to the output and produces the differential output voltage ($V_{OUT, DIFF}$) as follows:

$$V_{OUT,\ DIFF} = \frac{(V_{+IN} - V_{-IN}) \times R_{OUT} \times 2}{R_{IN}} \quad (1)$$

where:

V_{+IN} is the positive input voltage.

V_{-IN} is the negative input voltage.

The overall gain of the ADA4255 amplifier is $2 \times R_{OUT}/R_{IN}$. The different gain settings are achieved by internally switching in different values for R_{OUT} and R_{IN}.

The value of R_{IN} can be set to 12 different values via the G3 to G0 bits, resulting in 12 binary weighted input gains. The value of R_{OUT} can also be set to three different values via G4 and G5, resulting in three output scaling gains. Table 6 shows the 36 possible gain configurations, making the ADA4255 versatile when interfacing with a wide selection of sensors and ADCs.

Table 6. Possible Gain Settings

	Output Scaling Gain (V/V)		
Input Gain	**1**	**1.25**	**1.375**
0.0625	0.0625	0.078125	0.085938
0.125	0.125	0.15625	0.171875
0.25	0.25	0.3125	0.34375
0.5	0.5	0.625	0.6875
1	1	1.25	1.375
2	2	2.5	2.75
4	4	5	5.5
8	8	10	11
16	16	20	22
32	32	40	44
64	64	80	88
128	128	160	176

Each amplifier used in the ADA4255 uses a proprietary, zero drift architecture to ensure low offset voltage, offset voltage drift, and 1/f noise.

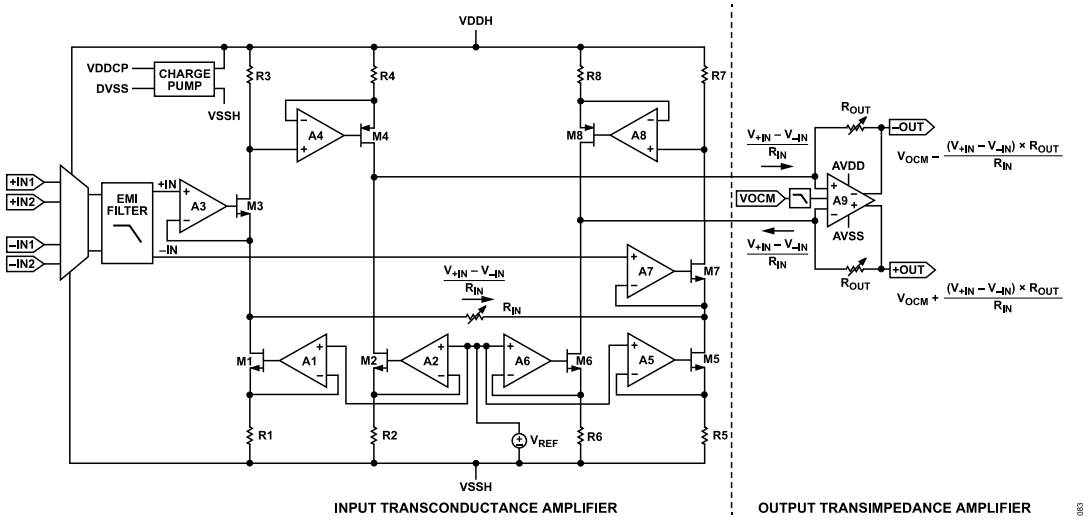

Figure 85. Simplified ADA4255 Programmable Gain Instrumentation Amplifier Topology

THEORY OF OPERATION

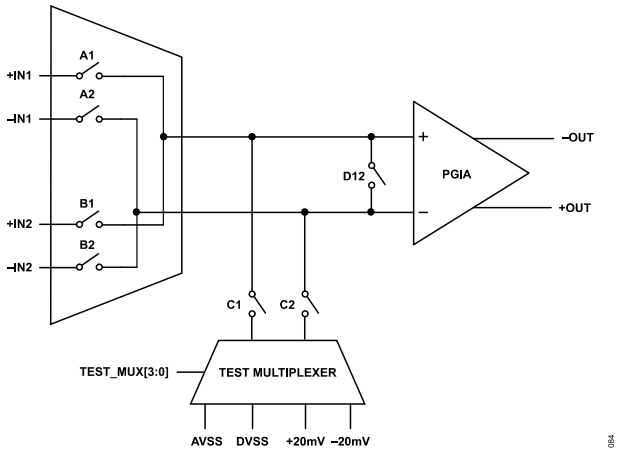

Figure 86. Input Switch Configuration

INPUT MULTIPLEXER

The ADA4255 input multiplexer withstands input voltages up to ±60 V with respect to VSSH and 60 V differentially. As shown in Figure 86, the multiplexer switches between the two sets of inputs and features additional switch functionality on the output of the multiplexer. Input switching is controlled via the INPUT_MUX register. The A1, A2, B1, and B2 switches connect the different inputs to the amplifier. The C1 and C2 switches connect the multiplexer outputs to the test multiplexer. Switch D12 connects both inputs together. The input multiplexer features <140 dB of crosstalk.

If excessive input voltage is detected by the input multiplexer, MUX_OVER_VOLT_ERR in the ANALOG_ERR register trips. When this error flag is set, the multiplexer automatically opens A1, A2, B1, and B2 to protect the input amplifier and input resistor network. This error flag can be disabled by setting MUX_OVER_VOLT_ERR_DIS (Register ANALOG_ERR_DIS). By default, both sets of inputs cannot be selected simultaneously. This protection can be overridden via the MUX_PROT_DIS bit in the ANALOG_ERR_DIS register.

EMI REDUCTION AND THE INTERNAL EMI FILTER

In many industrial and data acquisition applications, the ADA4255 amplifies small signals accurately in the presence of large common-mode voltages or high levels of noise. Typically, the sources of these small signals (in the order of microvolts or millivolts) are sensors that may be a significant distance from the signal conditioning circuit. Although these sensors may be connected to signal conditioning circuitry using shielded or unshielded twisted pair cabling, the cabling may act as an antenna, conveying high frequency interference directly to the inputs of the ADA4255.

The amplitude and frequency of this high frequency interference can have an adverse effect on the input stage of the instrumentation amplifier due to unwanted dc shift in the input offset voltage of the amplifier. This well known effect is called EMI rectification and is produced when out of band interference is coupled (inductively, capacitively, or via radiation) and rectified by the input transistors of the instrumentation amplifier. These transistors act as high frequency signal detectors, in the same way diodes were used as RF envelope detectors in early radio designs. Regardless of the type of interference or the method by which it is coupled to the circuit, an out of band error signal appears in series with the inputs of the instrumentation amplifier.

To minimize this effect, the ADA4255 has 35 MHz on-chip EMI filters to attenuate high frequencies before interacting with the input transistors. These on-chip filters are well matched due to their monolithic construction, which minimizes degradation in ac CMRR. To reduce any further effect of these out of band signals on the input offset voltage of the ADA4255, an additional external low-pass filter can be used at the inputs. Locate the filter very close to the input pins of the circuit. An effective filter configuration is shown in Figure 87 where three capacitors are added to the ADA4255 inputs. The filter limits the input signal according to the following relationship:

$$Filter\quad Frequency_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)} \tag{2}$$

$$Filter\quad Frequency_{CM} = \frac{1}{2\pi RC_C} \tag{3}$$

where:

C_D is the differential capacitor and is ≥10C_C.

C_C is the common-mode capacitor.

C_D affects the difference signal, and C_C affects the common-mode signal. Any mismatch in R × C_C degrades the ADA4255 CMRR. To avoid inadvertently reducing CMRR bandwidth performance, ensure that C_C is at least one magnitude smaller than C_D. The effect of mismatched C_C values is reduced with a larger C_D:C_C ratio.

THEORY OF OPERATION

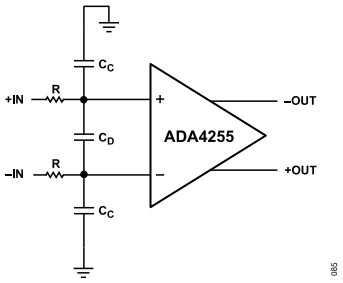

Figure 87. External EMI Filter Improves Noise Rejection

INPUT AMPLIFIER

The ADA4255 input amplifier operates on internally generated high voltage power supplies, VDDH and VSSH. On-chip charge pumps are used by the ADA4255 to generate VDDH and VSSH from the VDDCP supply.

The input amplifiers are internally monitored for clipping due to excessive signal swing. If excessive output swing is detected by any part of the input amplifier (A1 to A8 in Figure 85), the INPUT_ERR flag trips. If INPUT_ERR is tripped for more than 200 µs, the gain settings in the GAIN_MUX register are reset to their default values and the G_RST flag trips. By default, the G_RST event sets all gain bits in the GAIN_MUX register to their default values, which may also result in a MM_CRC_ERR. The gain reset function can be disabled via the G_RST_DIS bit.

OUTPUT AMPLIFIER

The ADA4255 features a fully differential output amplifier running from the dedicated low voltage supplies, AVDD and AVSS. Use AVDD and AVSS in a single-supply configuration. By running the output amplifier on low voltage supplies, circuitry connected to the output of the ADA4255 is inherently protected. The common-mode output voltage is set by the VOCM input voltage. VOCM has a high input impedance and is not biased internally. VOCM also features a 29 MHz EMI filter to minimize EMI interference. Typically, VOCM is biased to midsupply through a voltage divider between AVDD and AVSS to allow the widest swing on the output. The output amplifier can be set to three different scaling gains via G4 or G5: 1 V/V, 1.25 V/V, or 1.375 V/V. On power-up or soft reset, the output amplifier scaling gain defaults to 1 V/V. The output amplifier is monitored for clipping due to excessive signal swing. When the output saturates to either supply, the OUTPUT_ERR flag trips.

The differential output stage of the ADA4255 allows the device to be directly connected to high precision ADCs, such as the AD7768 and the AD4007. When making such a connection, it is recommended to use a low-pass filter to minimize noise and aliasing, as shown in Figure 88. The LTC6363 is configured as a 3-pole, low-pass filter with a cutoff frequency of 40 kHz.

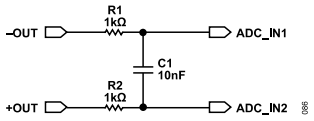

Figure 88. Simple Output Filter Preventing Aliasing and Filters Switching Noise

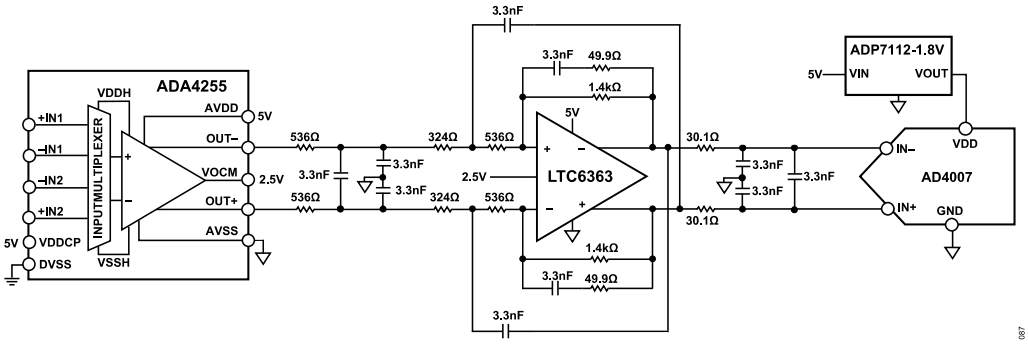

Figure 89. LTC6363 Used as a Low-Pass Filter and Driver

THEORY OF OPERATION

POWER SUPPLIES

The ADA4255 requires that three low voltages supplies be powered: the low voltage charge pump supply (VDDCP), the low voltage analog output amplifier supply (AVDD), and the low voltage digital supply (DVDD).

The low voltage charge pump supply is used internally to generate high voltage, bipolar supplies VDDH and VSSH, which power the input amplifier of the ADA4255. On-chip high voltage supply generation allows the ADA4255 to be isolated using only low voltage components while maintaining high voltage, high impedance input operation. The equations for typical VDDH and VSSH are as follows:

$$VDDH = 4.65 \times VDDCP - 0.9\ V$$
$$VSSH = -4.65 \times VDDCP + 1.6\ V$$

VDDH and VSSH are output to pins so that the required external decoupling capacitance can be applied. This decoupling is not optional and is required to stabilize VDDH and VSSH. Figure 90 shows the minimum recommended 10 µF and 0.1 µF decoupling capacitors connected to VDDH and VSSH. Up to 500 µA of additional load current can be sourced by VDDH or sunk by VSSH with the charge pump clock at its default of 16 MHz. The charge pump frequency can be reduced to 8 MHz, which results in lower current consumption on VDDCP.

VSSH is connected to the substrate of the ADA4255. Therefore, VSSH must be connected to the most negative supply voltage in the circuit, and VSSH must not exceed AVSS. It is recommended to use a Schottky diode to clamp VSSH to AVSS. The Schottky diode must have a forward bias voltage of 0.3 V or lower at 1 mA and withstand −28 V of reverse voltage. The ADA4255 monitors the VDDH and VSSH supplies to detect if the VDDH or VSSH drops below 8 V and sets the POR_HV flag.

The low voltage analog output amplifier supply, AVDD and AVSS, powers the output amplifier of the ADA4255. AVSS must be within VSSH − 0.3 V to VSSH + 30 V and VDDH – 30 V to VDDH + 0.3 V. AVDD − AVSS is typically a 5 V single supply, compatible with most high precision ADCs. Use 0.1 µF and 10 µF decoupling capacitors between AVDD and AVSS as close as possible to the AVDD and AVSS supply pins.

The digital supplies, DVDD and DVSS, power the digital circuitry inside the ADA4255. DVSS must be the same potential as AVSS. Use 0.1 µF and 10 µF decoupling capacitors from DVDD to DVSS as close as possible to the DVDD and DVSS supply pins. Figure 90 shows a typical ADA4255 supply configuration. The recommended decoupling values described in this section are minimum recommendations. Depending on amplifier loading and system noise, higher capacitance values and/or additional lower capacitor values may improve performance.

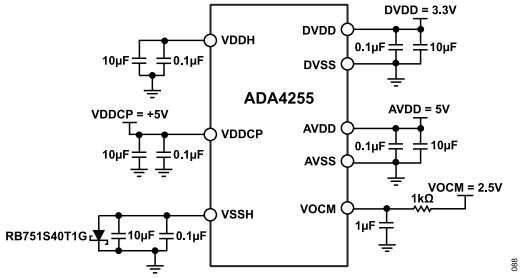

Figure 90. Typical ADA4255 Power Supply Configuration

ESD MAP

Figure 91 shows the various ESD diode paths inside the ADA4255. Figure 91, in conjunction with the Absolute Maximum Ratings section, helps in understanding current paths during power-on and fault conditions.

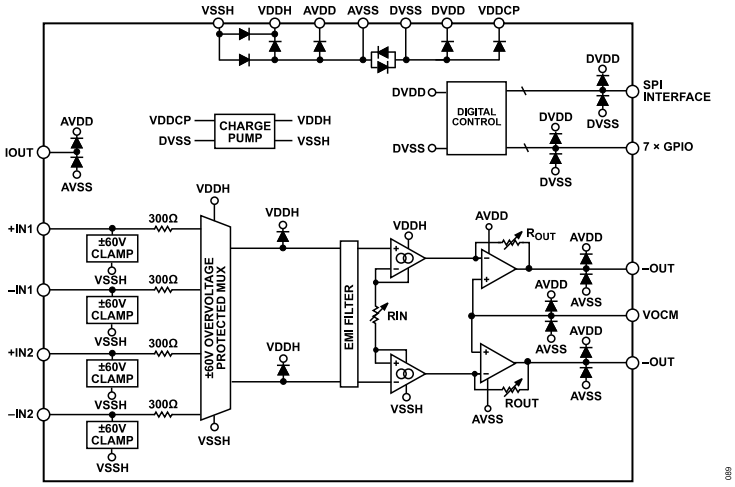

Figure 91. ESD Map

THEORY OF OPERATION

OUTPUT RIPPLE CALIBRATION CONFIGURATION

The amplifiers inside the ADA4255 achieve zero drift by using a technique commonly referred to as chopping. When chopping is used to null the offset of an amplifier, the unchopped offsets are modulated to the frequency at which the chopping is performed. All chopping amplifiers feature this phenomenon, which is commonly referred to as ripple.

The ADA4255 instrumentation amplifier features a proprietary calibration routine that reduces the residual voltage ripple at the output of the ADA4255 by nulling the internal offsets of all amplifiers. This calibration occurs automatically when the ADA4255 is initially powered on, after a POR_HV event, or after a soft reset occurs. Further calibrations can be performed either on a scheduled or triggered basis.

While the ADA4255 is calibrating, the SW_A1, SW_A2, SW_B1, and SW_B2 bits (Register INPUT_MUX) are temporarily opened and the amplifier inputs are internally connected to AVSS through the SW_C1 and SW_C2 bits (Register INPUT_MUX). After a calibration completes, the switches return to their previous states. Two calibration types can be selected via the CAL_SEL bit (Register TEST_MUX): full calibration or quick calibration.

A full calibration sequentially calibrates each individual amplifier and fully computes a new calibration code. This calibration takes approximately 85 ms. Full calibration always occurs after power-up, after a POR_HV event, or after a soft reset.

A quick calibration calculates a new calibration code for all amplifiers at the same time. The calibration code of each amplifier is then adjusted by an incremental amount. This type of calibration takes approximately 8 ms.

By default, calibrations only occur after power-up, after a POR_HV event, or after a reset. Additional scheduled calibrations are configured via CAL_EN (Register TEST_MUX), or are triggered via the TRIG_CAL bit (Register TRIG_CAL).

When scheduled calibrations are configured via the CAL_EN bits (Register TEST_MUX), the selected calibration type occurs at the rate configured via the CAL_EN bits.

Calibrations can also be manually triggered via the TRIG_CAL bit (Register TRIG_CAL).

The internal offsets, which are nulled by the ADA4255 calibration routine, can change when the circuit or the environmental conditions change. Changes in temperature, supply voltage, common-mode input voltage, time, and so on, can all cause an increase in output ripple. Recalibrations, either triggered or scheduled, renull internal offsets and reduce residual output ripple.

During a calibration, noise can limit the ability of the ADA4255 to fully null internal offsets and fully reduce the residual output ripple. Proper decoupling and shielding techniques help ensure accurate calibrations. Avoid large input transients during calibrations. Calibrations typically reduce the output ripple to <200 µV rms, but results as high as 5 mV rms can be observed in the presence of noise or input transients. If excessive residual ripple is detected, subsequent calibrations can be performed to reduce the output ripple.

ADC synchronization and simple filtering, either passive or active, are also effective methods in reducing residual output ripple. These techniques are discussed in detail in the External Clock Synchronization section and the Output Amplifier section.

GENERAL-PURPOSE INPUTS AND OUTPUTS (GPIOS)

The ADA4255 features several multifunction GPIOx pins. These GPIOx pins can be configured to either read a logic input or output a logic signal. A GPIOx pin is configured as an input or an output using the GPIO_DIR register. The bit position in the GPIO_DIR register corresponds to the GPIOx pin number. For example, the bit at Position 0 controls the GPIO0 direction.

The GPIO_DATA register sets the GPIO output when a GPIOx pin is configured as an output. The GPIO_DATA register also reads the data at the GPIOx pin when a GPIO is configured as an input. The bit field position in the GPIO_DATA register corresponds to the GPIOx pin number. For example, the bit at Position 0 corresponds to GPIO0.

The ADA4255 GPIOx pins can be configured to perform additional special functions.

Each GPIO can be configured as an output to extend the chip select signal from the SPI master to other slave devices. This special functionality is referred to as sequential chip select and is particularly useful in limiting the number of communication lines that need to be routed and/or isolated in a system. This special functionality is controlled by the SCS register.

GPIO0 and GPIO1 can also be configured as external multiplexer control signals. This function is enabled in the special function register, SF_CFG. After GPIO0 and GPIO1 are configured as outputs, the EXT_MUX bit field in the GAIN_MUX register controls the state of GPIO0 and GPIO1, allowing the gain and the external mux setting to be modified with one write operation.

GPIO2 can be configured to output a calibration busy signal. This function is enabled via the CAL_BUSY_OUT bit (Register SF_CFG). The calibration busy signal indicates that the ADA4255 is performing a calibration routine. GPIO2 must be configured as an output to use this special function.

GPIO3 can be configured to output a fault interrupt signal. This signal is an OR function of all the analog and digital error indicators found in the ANALOG_ERR and DIGITAL_ERR registers. This function is enabled via the FAULT_INT_OUT bit (Register SF_CFG). GPIO3 must be configured as an output to use this special function.

THEORY OF OPERATION

When configured as an output, GPIO4 can be configured to output the 1 MHz master clock or the 125 kHz chopping clock. This output is configured via the INT_CLK_OUT bit (Register SF_CFG) and the CLK_OUT_SEL bit (Register SYNC_CFG). When configured as an input, GPIO4 can also accept an external clock. This function is configured via the EXT_CLK_IN bit (Register SF_CFG).

EXCITATION CURRENTS

The ADA4255 features a configurable excitation current source, IOUT. This current source can be used to excite external circuitry, such as resistive bridges or RTD sensors.

The current output is controlled via the EX_CURRENT bits (Register EX_CURRENT_CFG).

EXTERNAL CLOCK SYNCHRONIZATION

The ADA4255 uses an internal 1 MHz master clock. The master clock is used to derive the 125 kHz chopping clock used by the internal amplifiers and the 16 MHz clock used by the charge pumps.

Either the 1 MHz or the 125 kHz clock can be brought out on the GPIO4 pin to allow synchronization of external systems. Use the following procedure to enable the external clock synchronization feature:

1. Configure GPIO4 as an output by setting Bit 4 in the GPIO_DIR register to 1.
2. Enable the internal oscillator output special function by setting the INT_CLK_OUT bit to 1 and the EXT_CLK_ IN bit to 0 in the SF_CFG register.
3. To output the 125 kHz clock, set the CLK_OUT_SEL bit in the SYNC_CFG register to 1. To output the 1 MHz clock, set the CLK_OUT_SEL bit to 0.

The ADA4255 can alternatively be configured to accept an external clock on GPIO4. The ADA4255 allows external clocks ranging from 1 MHz up to 32 MHz. In the case of an external clock that is higher than 1 MHz, the input clock must be divided down to 1 MHz using the internal clock divider. The edge on which the ADA4255 synchronizes can also be configured.

Use the following procedure to configure the ADA4255 to accept an external clock on GPIO4:

1. Configure GPIO4 as an input by setting Bit 4 in the GPIO_DIR register to 0.
2. Set the EXT_CLK_IN bit to 1 and ensure that the INT_CLK_OUT bit is set to 0 in the SF_CFG register.
3. Depending on the frequency of the input clock, configure the internal clock divider value such that the resulting clock is 1 MHz. The internal clock divider value is controlled by the SYNC bits in the SYNC_CFG register.
4. For synchronizing on the rising edge, set the SYNC_POL bit in the SYNC_CFG register to 1. For synchronizing on the falling edge, set SYNC_POL to 0.

To maintain the performance of the ADA4255, the external clock must be in the specified range, must always be present, and must have a duty-cycle of 50%. The quality of the clock used may affect the device performance. Prevent any overshoot or undershoot on the clock used, and provide an equal rise and fall to minimize the impact on the offset voltage.

SEQUENTIAL CHIP SELECT (SCS)

SCS is one of the special functions on the ADA4255 that can be configured on the GPIOx pins. This mode simplifies isolation requirements by allowing multiple slave devices to communicate over the SPI using a single host chip select ($\overline{CS}$) line. This communication also supports cyclical redundancy check (CRC) checksums transparently.

A GPIO is configured for SCS by first setting the GPIOx pin as an output using the GPIO_DIR bit (Register GPIO_DIR), and then setting the respective bit in the SCS register. Configuring a GPIOx pin for SCS mode is blocked if the GPIOx pin is already configured for another function from the special functions register, SF_CFG.

When using SCS, the $\overline{CS}$ signal from the SPI host controller is provided to the $\overline{CS}$ pin of the ADA4255. The serial data input (SDI), serial data output (SDO), and serial clock (SCLK) are shared connections with other SPI devices. The ADA4255 SDO pin supports tristate operation. Slave SDO pins can be directly connected to SDO if the slave pins support tristate operation. For slave devices with SDO pins that do not support tristate operation, an OR gate can be used to combine the SDO signals. If external logic is used to combine SDO lines, pull-down or pull-up resistors are recommended to avoid floating logic gate inputs. Figure 92 and Figure 93 show typical implementations. It is recommended to place pull-up resistors on the GPIOx pins configured in SCS mode to prevent any unintended communication with the slave devices when configuring the ADA4255 in SCS mode.

THEORY OF OPERATION

When configured for SCS mode, communication with the ADA4255 and all slave devices follows a predefined pattern. The first $\overline{CS}$ pulse is passed to the first GPIOx that is set up for SCS mode, effectively communicating with the first slave device. Subsequent $\overline{CS}$ pulses progress through any GPIOx pins configured for SCS mode in ascending order. The last $\overline{CS}$ pulse addresses the ADA4255 itself. This pattern repeats until SCS mode is disabled.

Figure 92 and Figure 93 show the ADA4255 operating in SCS mode with GPIO0 and GPIO1 communicating with two slave devices. GPIO0 is connected to the $\overline{CS}$ line of an ADC, and GPIO1 is connected to the $\overline{CS}$ line of a digital-to-analog converter (DAC).

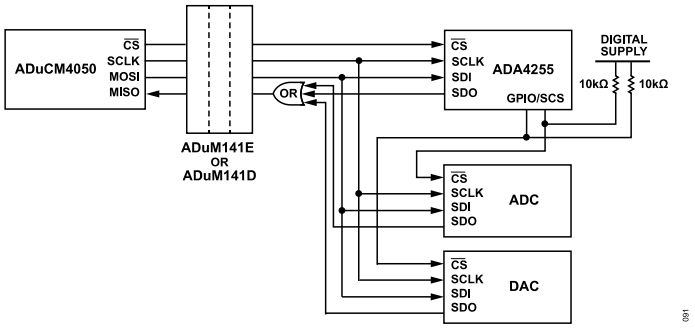

Figure 92. Typical SCS Implementation with Devices Without SDO Tristate Support

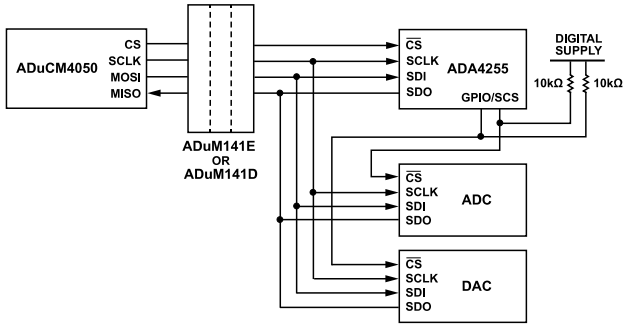

Figure 93. Typical SCS Implementation with All Devices Supporting SDO Tristate

THEORY OF OPERATION

In Figure 94, five distinct $\overline{CS}$ pulses can be seen. The first $\overline{CS}$ pulse writes 0x03 to the GPIO_DIR register to configure GPIO0 and GPIO1 as outputs. The second $\overline{CS}$ pulse writes 0x03 to SCS to configure GPIO0 and GPIO1 for SCS mode. The third $\overline{CS}$ pulse is replicated on GPIO0 and communicates with the first slave device, an ADC in this case. The fourth $\overline{CS}$ pulse is replicated on GPIO1 and communicates with the second slave device, a DAC in this case. The fifth $\overline{CS}$ pulse communicates with the ADA4255 itself. This pattern of communication continues in order of ADC, DAC, and ADA4255 until SCS is changed.

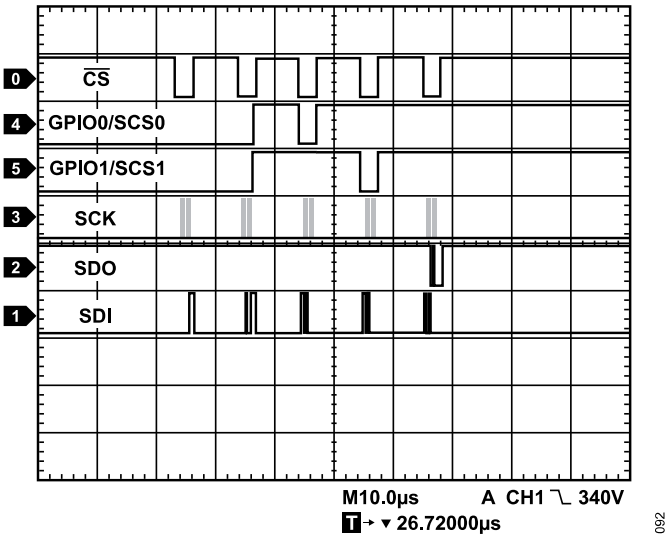

Figure 94. SCS Configuration and Operation with Two Slave Devices

GAIN ERROR CALIBRATION

The ADA4255 includes measured gain errors for all 32 gain combinations, readable from the on-chip, read only memory (ROM). These errors are measured at 25°C and are stored in Register 0x10 through Register 0x27 at the time of production. Using this technology improves gain accuracy by a factor of 5, improving system accuracy and reducing additional calibration requirements.

Each register contains five bits. MSB represents the polarity of the error, with a setting of 1 indicating a negative polarity and a setting of 0 indicating a positive polarity. The remaining four bits contain the magnitude based on a LSB of 100 ppm for GAIN_CAL1 through GAIN_CAL12 and 50 ppm for GAIN_CAL13 through GAIN_CAL24.

GAIN_CAL1 through GAIN_CAL12 directly provide the measured gain errors of all 12 gain values with the scaling gain set to 1 V/V. GAIN_CAL13 through GAIN_CAL24 provide additional gain error incurred when using other scalar gains. This is tabulated in Table 7.

Table 7. Gain Calibration Register Contents[1]

Register	Name	G[3:0]	G4	G5	Contents
0x10	GAIN_CAL1	0b0000	0	0	Gain error for G = 1/16 V/V × 1 V/V
0x11	GAIN_CAL2	0b0001	0	0	Gain error for G = 1/8 V/V × 1 V/V
0x12	GAIN_CAL3	0b0010	0	0	Gain error for G = 1/4 V/V × 1 V/V
0x13	GAIN_CAL4	0b0011	0	0	Gain error for G = 1/2 V/V × 1 V/V
0x14	GAIN_CAL5	0b0100	0	0	Gain error for G = 1 V/V × 1 V/V
0x15	GAIN_CAL6	0b0101	0	0	Gain error for G = 2 V/V × 1 V/V
0x16	GAIN_CAL7	0b0110	0	0	Gain error for G = 4 V/V × 1 V/V
0x17	GAIN_CAL8	0b0111	0	0	Gain error for G = 8 V/V × 1 V/V
0x18	GAIN_CAL9	0b1000	0	0	Gain error for G = 16 V/V × 1 V/V
0x19	GAIN_CAL10	0b1001	0	0	Gain error for G = 32 V/V × 1 V/V
0x1A	GAIN_CAL11	0b1010	0	0	Gain error for G = 64 V/V × 1 V/V
0x1B	GAIN_CAL12	0b1011	0	0	Gain error for G = 128 V/V × 1 V/V
0x1C	GAIN_CAL13	0b000x	1	X	Additional gain error for G = 1/16 V/V × 1.375 V/V or G = 1/8 V/V × 1.375 V/V
0x1D	GAIN_CAL14	0b001x	1	X	Additional gain error for G = 1/4 V/V × 1.375 V/V or G = 1/2 V/V × 1.375 V/V
0x1E	GAIN_CAL15	0b010x	1	X	Additional gain error for G = 1 V/V × 1.375 V/V or G = 2 V/V × 1.375 V/V
0x1F	GAIN_CAL16	0b011x	1	X	Additional gain error for G = 4 V/V × 1.375 V/V or G = 8 V/V × 1.375 V/V
0x20	GAIN_CAL17	0b100x	1	X	Additional gain error for G = 16 V/V × 1.375 V/V or G = 32 V/V × 1.375 V/V
0x21	GAIN_CAL18	0b101x	1	X	Additional gain error for G = 64 V/V × 1.375 V/V or G = 128 V/V × 1.375 V/V
0x22	GAIN_CAL19	0b000x	0	1	Additional gain error for G = 1/16 V/V × 1.25 V/V or G = 1/8 V/V × 1.25 V/V
0x23	GAIN_CAL20	0b001x	0	1	Additional gain error for G = 1/4 V/V × 1.25 V/V or G = 1/2 V/V × 1.25 V/V
0x24	GAIN_CAL21	0b010x	0	1	Additional gain error for G = 1 V/V × 1.25 V/V or G = 2 V/V × 1.25 V/V

THEORY OF OPERATION

Table 7. Gain Calibration Register Contents[1]

Register	Name	G[3:0]	G4	G5	Contents
0x25	GAIN_CAL22	0b011x	0	1	Additional gain error for G = 4 V/V × 1.25 V/V or G = 8 V/V × 1.25 V/V
0x26	GAIN_CAL23	0b100x	0	1	Additional gain error for G = 16 V/V × 1.25 V/V or G = 32 V/V × 1.25 V/V
0x27	GAIN_CAL24	0b101x	0	1	Additional gain error for G = 64 V/V × 1.25 V/V or G = 128 V/V × 1.25 V/V

[1] X means don't care.

For all gains using 1 V/V scalar, calculate the gain error using the following equation:

Gain Error = ((−1) × *GAIN_CALx, Bit 4* + (100) × *GAIN_CALx, Bits[3:0]*) (ppm)

For all gain values using 1.375 V/V or 1.25 V/V scalars, an additional gain error (GE') must be added, using this equation:

GE' = *Gain Error* + ((−1) × *GAIN_CALx, Bit 4* + (50) × *GAIN_CALx, Bits[3:0]*) (ppm)

For example, assume that the ADA4255 is set to a gain of 32 V/V and a scaling gain of 1.375 V/V. To calculate the stored gain error, read the gain error stored in the GAIN_CAL10 register and calculate the error in ppm. In this example, assume this readback is 10101, corresponding to a gain error of −500 ppm.

Then, read the additional gain error stored in GAIN_CAL17 and calculate the error in ppm. In this example, assume this readback is 00010, corresponding to an additional gain error of 100 ppm. The two errors are added to give a total gain error of −400 ppm.

THEORY OF OPERATION

WIRE BREAK DETECTION

The ADA4255 contains two programmable current sources that can be configured to 0.25 µA, 2 µA, 4 µA, or 16 µA via the WB_CURRENT bits (Register WB_DETECT). Both currents are conducted from VDDH. These currents, in conjunction with the on-chip comparators, enable continuity testing on the ADA4255 inputs.

The currents are switched to the amplifier inputs using F1 and F2, as shown in Figure 95. The voltage to which these currents bias the amplifier inputs is monitored internally by the ADA4255. When this voltage is within 4 V of VDDH, the WB_ERR (Register ANALOG_ERR_DIS) flag trips.

When F1 or F2 are closed, the amplifier gain settings in the GAIN_MUX register are temporarily overridden to the default values to avoid saturating the amplifier output in the event of an open-circuit input. Reads of the GAIN_MUX register during this time do not reflect this. When F1 and F2 are open, the GAIN_MUX register values automatically return to their previous values. This override can be disabled via the WB_G_RST_DIS bit (Register WB_DETECT).

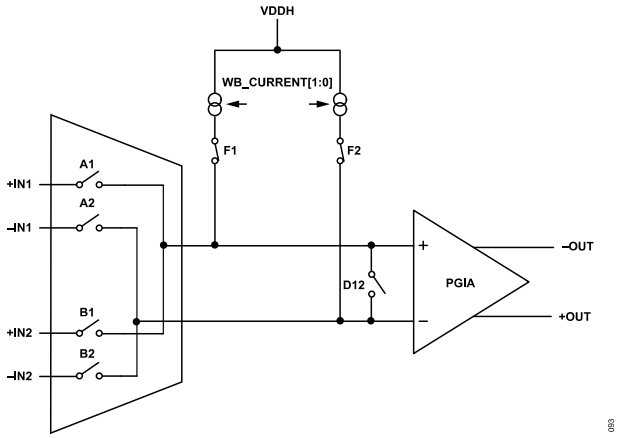

Figure 95. Wire Break Current Connectivity

THEORY OF OPERATION

TEST MULTIPLEXER

The ADA4255 contains an internal test multiplexer, as shown in Figure 96, that connects the inputs of the ADA4255 to useful voltages. To use the test multiplexer, the C1 and C2 switches must be closed. These switches are controlled using the INPUT_MUX register. It is recommended that the input multiplexer be disconnected from any external inputs by opening the A1, A2, B1, and B2 switches.

The TEST_MUX bits in the TEST_MUX register control the test multiplexer. The test multiplexer can be configured in three different states as follows:

- In the default state, the test multiplexer connects the ADA4255 inputs to AVSS. This configuration can be used during a full system calibration to null out errors, such as offset voltage.
- The test multiplexer can connect the noninverting input to DVSS and the inverting input to AVSS, or vice versa. This configuration can be used to detect any voltage difference between AVSS and DVSS, which indicates poor connection.
- The test multiplexer can also provide a +20 mV or −20 mV differential signal to the inputs of the ADA4255. This configuration can be used to verify the gain setting of the ADA4255 and the PGIA functionality without applying an external signal.

EXTERNAL MUX CONTROL

The ADA4255 is able to configure GPIO0 and GPIO1 to control an external multiplexer. Writes to the EXT_MUX bits in the GAIN_MUX register set the state of GPIO0 and GPIO1, which in turn controls an external multiplexer. This setup allows amplifier gain and external multiplexer settings to be configured with a single SPI write, avoiding overload conditions. The external mux special function can be configured via the EXT_MUX_EN bits (Register SF_CFG) and setting GPIO0 and GPIO1 to outputs, as shown in Figure 97.

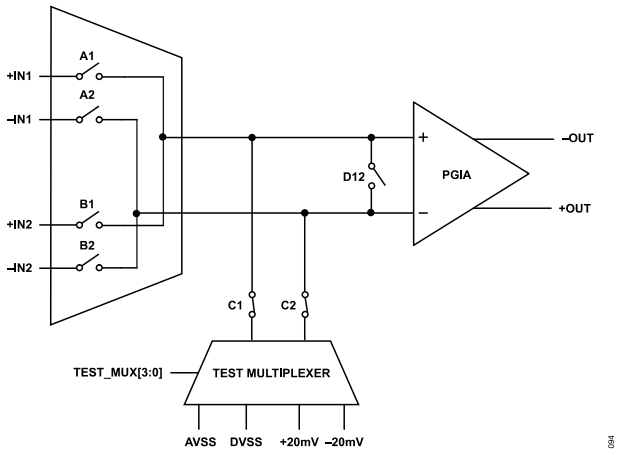

Figure 96. Text Multiplexer Connectivity

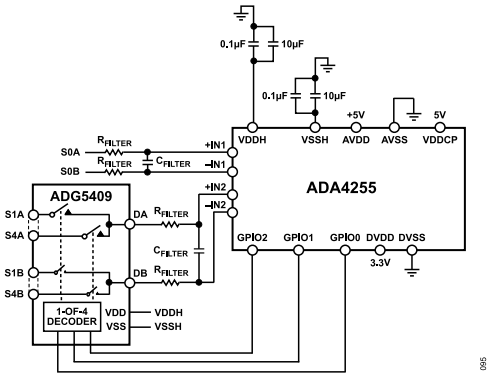

Figure 97. External Multiplexer Control Example

DIGITAL INTERFACE

SPI

The ADA4255 features a 4-wire SPI. This interface operates in SPI Mode 0 and can be operated with $\overline{CS}$ tied low. In SPI Mode 0, SCLK idles low, the falling edge of SCLK is the driving edge, and the rising edge of SCLK is the sampling edge. This setup means that data is clocked out on the falling (driving) edge and clocked in on the rising (sampling) edge.

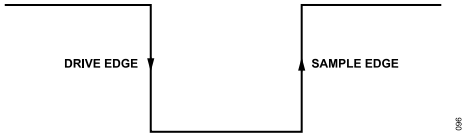

Figure 98. SPI Mode 0 SCLK Edges

ACCESSING THE ADA4255 REGISTER MAP

The ADA4255 SPI uses 16-bit instructions, plus an optional 8-bit CRC checksum. Each instruction contains a read or write bit, a 7-bit address, 8 bits of data, and an 8-bit CRC checksum if the SPI_CRC_ERR bit (Register DIGITAL_ERR) is configured.

Table 8. ADA4255 Instruction Format

R/W	ADDR, Bits[6:0]	Data, Bits[7:0]	CRC, Bits[7:0]

R/W determines whether a read or write operation is performed (1 means read and 0 means write). ADDR, Bits[6:0], is the register address being read from or written to. R/W and the ADDR, Bits[6:0] together are referred to as an 8-bit command. For write operations, DATA, Bits[7:0], is the data being written, and CRC, Bits[7:0], is a user provided checksum for that data.

The ADA4255 internal address counter is automatically incremented after each read and/or write operation, allowing a continuous read and/or write mode. After an initial read operation, if $\overline{CS}$ stays low, the next 8 SCLK pulses read back the contents of the next register address. After an initial write operation, if $\overline{CS}$ stays low, the next 8 SCLK pulses load the data on the SDI to the next register address.

CHECKSUM PROTECTION

The ADA4255 features a checksum mode that can be used to improve interface robustness. Using the checksum ensures that only valid data is written to a register and allows data read from a register to be validated. If an error occurs during a register write, the SPI_CRC_ERR bit (Register DIGITAL_ERR) trips and no data is written. To ensure that a register write is successful, the register contents can be read, and the checksum can be verified.

For CRC checksum calculations, the following polynomial is always used:

$$x^8 + x^2 + x + 1$$

The SPI_CRC_ERR_DIS bit (Register DIGITAL_ERR) enables and disables this checksum. The 8-bit checksum is appended to the end of each read and write transaction. The checksum calculation for the write transaction is calculated using the 8-bit command word and the 8-bit data. For a read transaction, the checksum is calculated using the command word and the 8-bit data output. Figure 99 and Figure 100 show SPI write and read transactions, respectively.

In continuous write mode, the first write command CRC is calculated as described previously in this section. Subsequent CRCs are clocked in after every register data. The CRC in continuous write mode is calculated based on the register value it is associated with. In continuous read mode, the first read command CRC is calculated as described previously. Subsequent CRCs are clocked out after every register data. The CRC in continuous read mode is calculated based only on the register value it is associated with. Figure 101 and Figure 102 show SPI continuous write and read transactions, respectively.

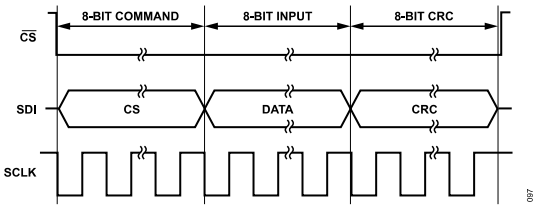

Figure 99. Writing to a Register with CRC

DIGITAL INTERFACE

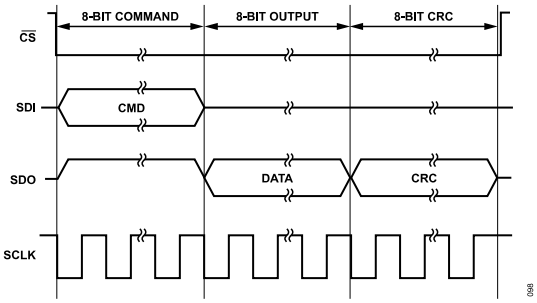

Figure 100. Reading from a Register with CRC

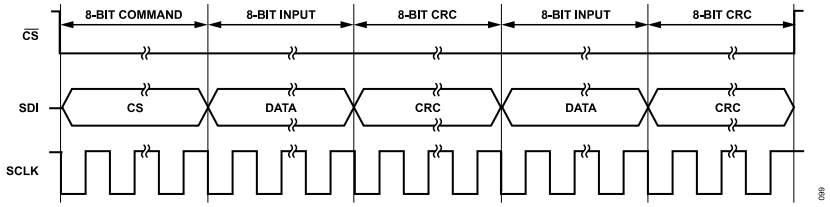

Figure 101. Continuous Write Mode with CRC

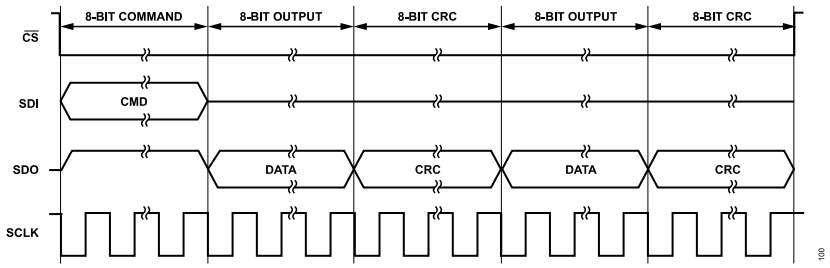

Figure 102. Continuous Read Mode with CRC

DIGITAL INTERFACE

CRC CALCULATION

The checksum, which is 8 bits wide, is generated using the following polynomial (with a seed of 0x00):

$x^8 + x^2 + x + 1$ (0b100000111)

To generate the checksum, the data is left shifted by 8 bits to create a number ending in eight Logic 0s. The polynomial is aligned so that its MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process is repeated until the original data is reduced to a value less than the polynomial. This is the 8-bit checksum.

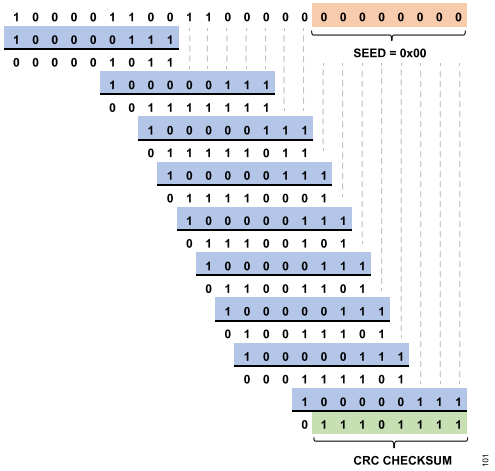

Figure 103. Calculating a CRC Checksum

MEMORY MAP CHECKSUM PROTECTION

For added robustness, a CRC calculation is performed on the on-chip registers as well. Register 0x03, Register 0x04, and Register 0x05 are not included in this check because the contents of these registers change, independent of SPI writes. The CRC is performed at a rate of 15.26 Hz. Each time the register map is changed using an SPI write, the CRC is recalculated.

The memory map CRC function is enabled by default. This function can be disabled via the MM_CRC_ERR_DIS bit (Register DIGITAL_ERR_DIS). If an error occurs, the MM_CRC_ERR bit (Register DIGITAL_ERR) trips.

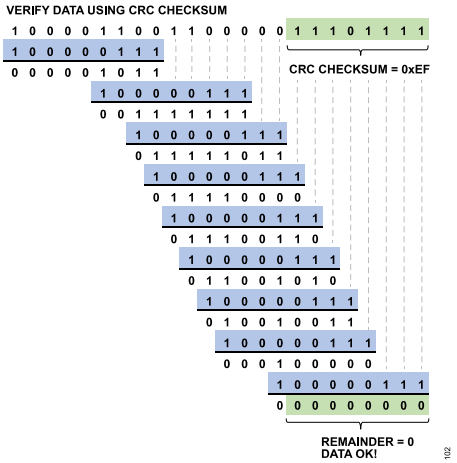

Figure 104. Verifying Data with a CRC Checksum

READ-ONLY MEMORY (ROM) CHECKSUM PROTECTION

On power-up, all fuse registers are set to the default values. These default values are held in ROM. For added robustness, a CRC calculation is performed on the ROM contents as well. This CRC check is performed on power-up. The ROM CRC function is enabled by default. This function can be disabled via the ROM_CRC_ERR_DIS bit (Register DIGITAL_ERR_DIS). If an error occurs, the ROM_CRC_ERR bit (Register DIGITAL_ERR) trips.

SPI READ AND WRITE ERROR DETECTION

The ADA4255 can detect if an invalid register is being addressed. A read or write to an invalid address trips the SPI_RW_ERR bit (Register DIGITAL_ERR). The SPI_RW_ERR bit is enabled by default, and this bit can be disabled via the SPI_RW_ERR_DIS bit (Register DIGITAL_ERR_DIS).

SPI COMMAND LENGTH ERROR DETECTION

When communicating with the ADA4255, the number of clock edges on SCLK is monitored to ensure that, when $\overline{CS}$ returns high, the total number of clock edges received is divisible by 8. If the number of SCLK edges is insufficient or in excess, the SPI_SCLK_CNT_ERR bit (Register DIGITAL_ERR) trips. The SPI_SCLK_CNT_ERR is enabled by default, and this bit can be disabled via the SPI_SCLK_CNT_ERR_DIS bit (Register DIGITAL_ERR_DIS).

APPLICATIONS INFORMATION

INPUT AND OUTPUT OFFSET VOLTAGE AND NOISE

The offset voltage of the ADA4255 has two main components: the input offset voltage due to the input amplifiers and the output offset due to the output amplifier. The total offset voltage RTI is found by dividing the output offset by the programmed gain and adding this value to the input offset voltage. At high gains, the input offset voltage dominates, whereas at low gains, the output offset voltage dominates. The total offset voltage is

Total Input Offset Voltage (RTI) = V_{OSI} + (V_{OSO}/*GAIN*)

Total Output Offset Voltage (Referred to Output (RTO)) = V_{OSI} × *Gain* + V_{OSO}

The preceding equations can also be used to calculate the offset drift in a similar manner.

The noise of the ADA4255 behaves similarly to the voltage offset. There are two components: the input voltage noise due to the input amplifiers and the output voltage noise due to the output amplifiers. The total noise RTI is found by dividing the output voltage noise by the programmed gain and root-sum-squaring with the input voltage noise. At high gains the input voltage noise dominates, whereas at low gains the output voltage noise dominates. The total voltage noise is

$$Total\ \ Input\ \ Voltage\ \ Noise\ \ \left(RTI\right) = \sqrt{{e_{ni}}^2 + \left(\frac{e_{no}}{Gain}\right)^2} \quad (4)$$

$$Total\ \ Output\ \ Voltage\ \ Noise\ \ \left(RTO\right) = \sqrt{\left(e_{ni} \times Gain\right)^2 + \left(e_{no}\right)^2} \quad (5)$$

ADC CLOCK SYNCHRONIZATION

The ADA4255 incorporates several clock synchronization features that allow the internal clock to be synchronized with other circuitry, such as an ADC. Synchronizing the system filters residual ripple due to the internal chopping of the ADA4255. When using these synchronization features, GPIO4 is configured to accept an external clock signal or output one of the internal clock signals.

When an external clock is provided to the ADA4255, an on-chip clock divider is configured via the SYNC bits (Register SYNC_CFG) to achieve a nominal 1 MHz clock. The 1 MHz clock is further divided by 8 to 125 kHz and controls the device chopping. The chopping clock edges can be configured to coincide with either the rising or falling edges of the provided clock via SYNC_POL bit (Register SYNC_CFG). This configuration is recommended for ADC synchronization. The ADA4255, when configured to accept an external clock, requires that this clock always be active and have a duty cycle of 50% to maintain charge pump operation.

Alternatively, the internal clock can be output to GPIO4 so that other circuits can use it. Either 1 MHz or 125 kHz can be selected via the CLK_OUT_SEL bit (Register SYNC_CFG).

When the ADA4255 is driving the AD4007 1 MSPS successive approximation register (SAR) ADC as shown in Figure 105, the recommended configuration is to provide the 50% duty cycle convert signal to the ADA4255 as a clock input. In this case, SYNC is set to 0b000 because the CNV period is 1 µs. Set the SYNC_POL bit to 1 to synchronize the chopping clock to the rising edge of the CNV signal. When configured in this way, the output of the ADA4255 has the maximum time to settle after a chopping edge, and chopping edges do not occur during the ADC conversion phase. It is recommended to enable the high-Z mode of the AD4007 to maximize system performance.

When the ADA4255 is driving the AD7768 Σ-Δ ADC as shown in Figure 106, the recommended configuration is to provide the internal 32 MHz clock of the AD7768 to the ADA4255 as a clock input. In this case, SYNC is set to 0b101 to divide 32 MHz down to 1 MHz for the ADA4255. The SYNC setting has no impact on performance with Σ-Δ converters due to the way the converters operate internally. When driving the AD7768 directly with the ADA4255, enable the internal buffers of the AD7768. Alternatively, a dedicated ADC driver and amplifier can be configured between the ADA4255 and the AD7768.

In both configurations, it is recommended that two reads from the M_CLK_CNT register are performed to ensure that the master clock counter is incrementing, indicating that the ADA4255 is receiving an external clock.

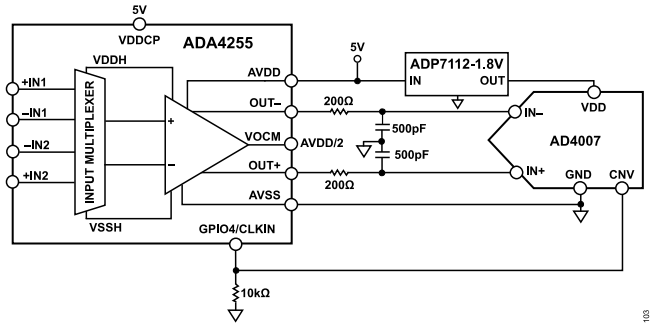

Figure 105. Clock Synchronization with the AD4007

APPLICATIONS INFORMATION

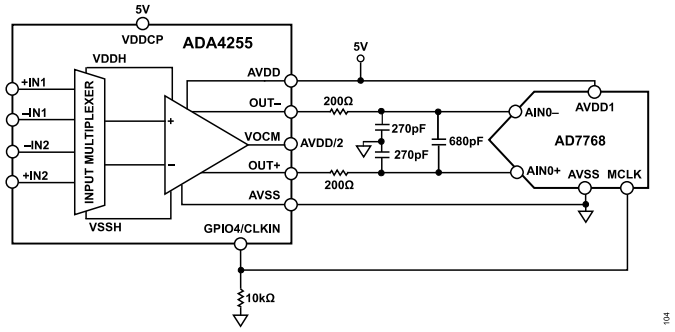

Figure 106. Clock Synchronization with the AD7768

APPLICATIONS INFORMATION

PROGRAMMABLE LOGIC CONTROLLER (PLC) VOLTAGE AND CURRENT INPUT

The circuit in Figure 107 shows the ADA4255 used to convert a typical PLC input signal ranges (±10 V, ±5 V, or 20 mA) to an output voltage from 0 V to +5 V, compatible with high precision ADCs, such as the AD7768. To perform a voltage measurement, the ADA4255 input multiplexer is configured to Channel 1, +IN1 and –IN1, by writing 0x60 to the INPUT_MUX register. The MOSFET switch must be turned off by setting GPIO0 to logic level low. GPIO0 must be configured as an output by setting the corresponding bit field to 1 in the GPIO_DIR register. The state of GPIO0 is controlled by the corresponding bit field in the GPIO_DATA register. The ADA4255 gain can be configured through the GAIN_MUX register, depending on the input voltage level.

To perform a current measurement, the circuit shown in Figure 107 provides two different shunt resistors, 250 Ω and 100 Ω. To select a 250 Ω resistor, the metal-oxide semiconductor field effect transistor (MOSFET) switch must be switched on by setting GPIO0 to logic level high using the GPIO_DATA register. The measurement is performed using Channel 1 of the ADA4255. To select 100 Ω, the MOSFET must be turned off by setting GPIO0 to logic level low. Channel 2 must be selected in this mode by writing 0x18 to the INPUT_MUX register.

The ADA4255 internal chopping circuitry can be synchronized to the companion ADC, which keeps the residual chopping noise at the correct frequency and prevents it from folding back to a frequency band of interest. To use the synchronization functionality, configure GPIO4 to be an input by setting the corresponding bit field in the GPIO_DIR register. Set the ADA4255 to accept an external clock by setting the EXT_CLK_IN bit in the SF_CFG register. Adjust the clock divider such that the resulting clock is equal to 1 MHz. The divider can be adjusted in the SYNC_CFG register. The SYNC_CFG register also controls the synchronizing edge polarity. It is recommended that two reads from the M_CLK_CNT register are performed to ensure that the master clock counter is incrementing, indicating that the ADA4255 is receiving an external clock.

The ADA4255 on-chip diagnostics allow the user to check the circuit connections. In PLC applications, the circuit connections are verified using the wire break detection capabilities of the ADA4255. The WB_DETECT register flag is set if one of the input connections is missing. Finally, the CRC check, SCLK counter, and SPI read and/or write check make the interface more robust as any read and/or write operations that are not valid are detected. The CRC check highlights if any bits are corrupted when transmitted between the processor and the ADA4255.

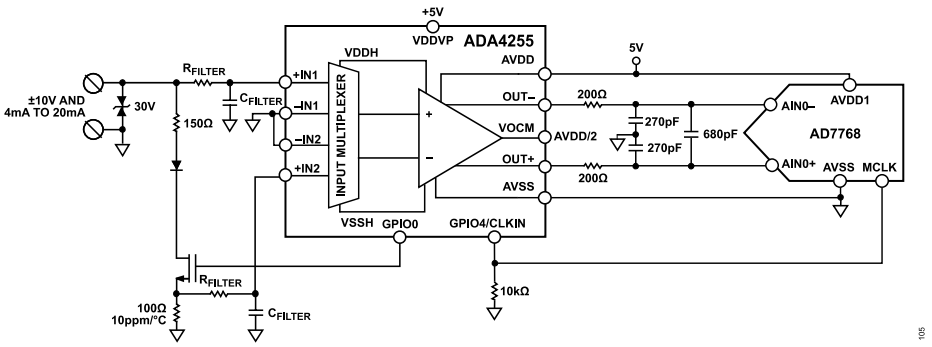

Figure 107. Voltage and Current Input Application

APPLICATIONS INFORMATION

3-WIRE RTD WITH CURRENT EXCITATION

3-wire RTDs are commonly used for precision temperature measurement. Figure 108 shows how the ADA4255 can be used to accurately measure temperature using a 3-wire RTD sensor. In this implementation, the current source of the ADA4255, IOUT, is used to drive the RTD. RL1, RL2, and RL3 represent the parasitic lead resistances of the RTD. Through a sequence of three voltage measurements and by assuming all RLx resistors are equal, a temperature measurement can be made that is insensitive to the parasitic resistances of RL1, RL2 and RL3. Refer to Figure 108 to aid in the following measurement description.

The excitation current flows through RL1, RTD, RL3, and R_{REF}. R_{REF} serves as a current sense resistor used to measure the true value of IOUT. Because of this, the tolerance and drift of R_{REF} are important in achieving system accuracy specifications. The combined voltage on RTD and RL1 can be measured between +IN1 and −IN1. Note that the portion of this measured voltage that is on RL1 is an error term, and it matches the voltage on RL3 because RL1 matches RL3, and the same current flows in both. Next, measure the voltage between −IN2 and +IN2 with the known value of R_{REF} to calculate the true value of IOUT. A final measurement of the voltage between −IN1 and +IN2 results in the combined voltage on RL3 and R_{REF}. From these three voltage measurements, the voltage across RTD and the current conducted in RTD are determined, and the RTD value is calculated and used to determine temperature.

The gain of the ADA4255 must be optimized for each of these three measurements to maximize resolution. To achieve some of the switch combinations, the MUX_PROT_DIS bit (Register ANALOG_ERR_DIS) must also be set.

The ADA4255 internal chopping circuitry can be synchronized to the companion ADC to help keep the residual chopping noise at its frequency and to prevent the noise from folding back into a frequency band of interest. To use the synchronization functionality, configure GPIO4 to be an input by setting its corresponding bit in the GPIO_DIR register. Set the ADA4255 to accept an external clock by setting the EXT_CLK_IN bit in the SF_CFG register. Adjust the clock divider such that the resulting clock is equal to 1 MHz. The divider can be adjusted in SYNC_CFG register. The SYNC_CFG register also controls the syncing edge polarity. It is recommended that two reads from the M_CLK_CNT register are performed to ensure that the master clock counter is incrementing, indicating that the ADA4255 is getting an external clock.

The ADA4255 on-chip diagnostics allow the user to check the circuit connections. In RTD applications, the circuit connections are verified using the wire break detection capabilities of the ADA4255. The WB_DETECT register flag is set if one of the RTD wires is missing. Finally, the CRC check, SCLK counter, and SPI read and/or write check make the interface more robust because any read and/or write operations that are not valid are detected. The CRC check highlights if any bits are corrupted when transmitted between the processor and the ADA4255.

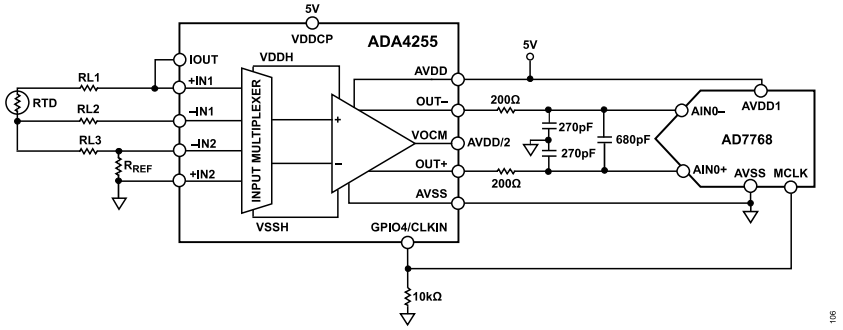

Figure 108. 3-Wire RTD Application

APPLICATIONS INFORMATION

HIGH RAIL CURRENT SENSING

Figure 109 shows a high-side current sense amplifier implemented with ADA4255. The integrated charge pump PGIA topology of the ADA4255 allows this circuit to sense bidirectional current over a 38 V range on a single 5 V supply voltage. The low offset voltage, low offset voltage drift, low input current, and excellent linearity allow this configuration to achieve very high dynamic range.

While the ADA4255 features an integrated EMI filter, an additional low-pass filter can be used externally as shown. The ADA4255 has low input bias current and input bias offset current that minimizes the error introduced by the input bias current flowing through the filter resistor. The matching of the filter resistors and capacitors is required to minimize the errors and preserve AC CMRR.

The ADA4255 on-chip diagnostics allow the user to check the circuit connections. In current sensing applications, the circuit connections are verified using the wire break detection capabilities of the ADA4255. The WB_DETECT register flag is set if one of the connections to the shunt resistors is missing. Finally, the CRC check, SCLK counter, and SPI read and/or write check make the interface more robust because any read and/or write operations that are not valid are detected. The CRC check highlights if any bits are corrupted when transmitted between the processor and the ADA4255.

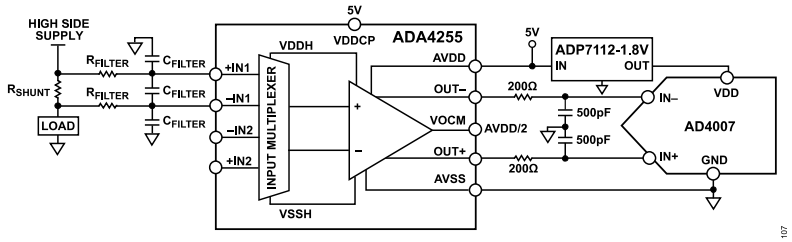

Figure 109. High Voltage, Bidirectional, Current Sense Application

REGISTER SUMMARY

Table 9. Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	GAIN_MUX	G4	G[3:0]				Reserved	EXT_MUX[1:0]	
0x01	Reset	Reserved							RST
0x02	SYNC_CFG	CLK CP_SEL	CLK_ OUT_SEL	Reserved	SYNC_POL	Reserved	SYNC[2:0]		
0x03	DIGITAL_ERR	Reserved	CAL_BUSY	SPI_ CRC_ERR	SPI_RW_ERR	SPI_SCLK_ CNT_ERR	Reserved	MM_CRC_ ERR	ROM_CRC_ERR
0x04	ANALOG_ERR	G_RST	POR_HV	Reserved	WB_ERR	FAULT_INT	OUTPUT_ERR	INPUT_ERR	MUX_OVER_VOLT_ ERR
0x05	GPIO_DATA	Reserved	GPIO_DATA[6:0]						
0x06	INPUT_MUX	Reserved	SW_A1	SW_A2	SW_B1	SW_B2	SW_C1	SW_C2	SW_D12
0x07	WB_DETECT	WB_G_ RST_DIS	Reserved			SW_F1	SW_F2	WB_CURRENT[1:0]	
0x08	GPIO_DIR	Reserved	GPIO_DIR[6:0]						
0x09	SCS	Reserved	SCS[6:0]						
0x0A	ANALOG_ ERR_DIS	G_RST_DIS	POR_HV_ DIS	Reserved	WB_ERR_ DIS	MUX_PROT_ DIS	OUTPUT_ERR_ DIS	INPUT_ERR_ DIS	MUX_OVER_VOLT_ ERR_DIS
0x0B	DIGITAL_ERR_ DIS	Reserved	CAL_ BUSY_DIS	SPI_CRC _ERR_DIS	SPI_RW_ ERR_DIS	SPI_SCLK_ CNT_ERR_DIS	M_CLK_ CNT_ERR_DIS	MM_CRC_ ERR_DIS	ROM_CRC_ ERR_DIS
0x0C	SF_CFG	Reserved		INT_CLK_ OUT	EXT_CLK_IN	FAULT_INT_ OUT	CAL_BUSY_ OUT	EXT_MUX_EN[1:0]	
0x0D	ERR_CFG	ERR_ LATCH_DIS	Reserved			ERR_DELAY[3:0]			
0x0E	TEST_MUX	G5	CAL_SEL	CAL_EN[1:0]		TEST_MUX[3:0]			
0x0F	EX_CURRENT_ CFG	EX_CURRENT_SEL[1:0]		Reserved		EX_CURRENT[3:0]			
0x10	GAIN_CALx[1]	Reserved			GAIN_CAL1[4:0]				
0x11		Reserved			GAIN_CAL2[4:0]				
0x12		Reserved			GAIN_CAL3[4:0]				
0x13		Reserved			GAIN_CAL4[4:0]				
0x14		Reserved			GAIN_CAL5[4:0]				
0x15		Reserved			GAIN_CAL6[4:0]				
0x16		Reserved			GAIN_CAL7[4:0]				
0x17		Reserved			GAIN_CAL8[4:0]				
0x18		Reserved			GAIN_CAL9[4:0]				
0x19		Reserved			GAIN_CAL10[4:0]				
0x1A		Reserved			GAIN_CAL11[4:0]				
0x1B		Reserved			GAIN_CAL12[4:0]				
0x1C		Reserved			GAIN_CAL13[4:0]				
0x1D		Reserved			GAIN_CAL14[4:0]				
0x1E		Reserved			GAIN_CAL15[4:0]				
0x1F		Reserved			GAIN_CAL16[4:0]				
0x20		Reserved			GAIN_CAL17[4:0]				
0x21		Reserved			GAIN_CAL18[4:0]				
0x22		Reserved			GAIN_CAL19[4:0]				
0x23		Reserved			GAIN_CAL20[4:0]				
0x24		Reserved			GAIN_CAL21[4:0]				
0x25		Reserved			GAIN_CAL22[4:0]				
0x26		Reserved			GAIN_CAL23[4:0]				

REGISTER SUMMARY

Table 9. Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x27		Reserved			GAIN_CAL24[4:0]				
0x2A	TRIG_CAL	Reserved							TRIG_CAL
0x2E	M_CLK_CNT	M_CLK_CNT[7:0]							
0x2F	DIE_REV_ID	DIE_REV_ID[7:0]							
0x64	PART_ID	PART_ID[39:32]							
0x65		PART_ID[31:24]							
0x66		PART_ID[23:16]							
0x67		PART_ID[15:8]							
0x68		PART_ID[7:0]							

[1] x is 1 to 24.

REGISTER DETAILS

GAIN MULTIPLEXER REGISTER (GAIN_MUX) DETAILS

Table 10. GAIN_MUX Register Details (Register 0x00)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	G4	G[3:0]				Reserved	EXT_MUX[1:0]	
Access	R/W	R/W				Reserved	R/W	
Reset	0	0	0	0	0	Reserved	0	0

Bit 7, G4—Output Amplifier Scaling Gain (1.375 V/V)

Setting the G4 bit to 1 configures the output amplifier in a scaling gain of 1.375 V/V. This configuration scales the input amplifier gain, G[3:0] (Bits[6:3]), by 1.375 V/V. The G4 bit takes precedence over the G5 bit, located in the TEST_MUX register. Setting the G4 bit to 0 configures the output amplifier in either a gain of 1 V/V or 1.25 V/V, depending on the value written to the G5 bit. These gain settings are summarized in Table 11.

Table 11. Output Amplifier Scaling Gain Settings

G5 Bit	G4 Bit	Output Amplifier Scaling Gain (V/V)
0	0	1
X[1]	1	1.375
1	0	1.25

[1] X means don't care.

Bits[6:3], G[3:0]—Input Amplifier Gain Setting

The G[3:0] bits set the gain of the input amplifier, as shown in Table 12. The overall gain is scaled by the output amplifier scaling gain, which is configured using the G4 bit and the G5 bit. The default input amplifier gain is 1/16 V/V.

Table 12. Register Values for Input Amplifier Gains

	Bits in the G[3:0] Bit Field			
Input Amplifier Gain (V/V)	G3	G2	G1	G0
1/16	0	0	0	0
1/8	0	0	0	1
1/4	0	0	1	0
1/2	0	0	1	1
1	0	1	0	0
2	0	1	0	1
4	0	1	1	0
8	0	1	1	1
16	1	0	0	0
32	1	0	0	1
64	1	0	1	0
128	1	0	1	1
Reserved	1	1	0	0
Reserved	1	1	0	1
Reserved	1	1	1	0
Reserved	1	1	1	1

Bits[1:0], EXT_MUX[1:0]—External Multiplexer Control

When external multiplexer control is enabled using the EXT_MUX_EN bits in Register 0x0C, and GPIO1 and/or GPIO0 are configured as outputs using the GPIO_DIR bits in Register 0x08, EXT_MUX[1:0] sets the output of GPIO1 and/or GPIO0. This setup simplifies communication in externally multiplexed applications because both the gain and the external multiplexer can be configured with a single SPI write to the GAIN_MUX register. Multiplexers larger than 4 to 1 are supported by using additional GPIOx pins and additional SPI writes.

REGISTER DETAILS

SOFTWARE RESET REGISTER (RESET) DETAILS

Table 13. Reset Register Details (Register 0x01)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved							RST
Access	Reserved							W
Reset	Reserved							0

Bit 0, RST—Soft Reset

A soft reset can be initiated by setting the RST bit to 1. A soft reset clears all internal registers and sets them to their default values. The RST bit is self clearing. The RST bit performs the same operation as a power-on reset (POR) and a start-up calibration occurs.

REGISTER DETAILS

CLOCK SYNCHRONIZATION CONFIGURATION REGISTER (SYNC_CFG) DETAILS

Table 14. SYNC_CFG Register Details (Register 0x02)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	CLK_CP_SEL	CLK_OUT_SEL	Reserved	SYNC_POL	Reserved	SYNC[2:0]		
Access	R/W	R/W	Reserved	RW	Reserved	R/W		
Reset	0	0	Reserved	0	Reserved	1	0	0

Bit 7, CLK_CP_SEL—Charge Pump Clock Select

The charge pump of the ADA4255 runs at 16 MHz by default. Alternatively, setting CLK_CP_SEL to 1 changes the charge pump frequency to 8 MHz.

Bit 6, CLK_OUT_SEL—Clock Output Select

The ADA4255 1 MHz master clock is divided down to 125 kHz internally and is used by the zero drift amplifiers. When the INT_CLK_OUT bit in Register 0x0C is set to 1, setting CLK_OUT_SEL to 1 outputs the divided down 125 kHz clock on GPIO4. Clearing CLK_OUT_SEL to 0 outputs the 1 MHz master clock on GPIO4.

Bit 4, SYNC_POL—Clock Synchronization Polarity

When an external clock source is provided to the ADA4255, this bit is used to configure whether the rising or falling edge is used for synchronization. The synchronization edge is the edge at which the ADA4255 performs the chopping. Writing a 1 to this bit synchronizes the ADA4255 to the positive edge of the provided clock. Writing a 0 synchronizes the ADA4255 to the negative edge of the provided clock.

Bits[2:0], SYNC[2:0]—Internal Clock Divider Value

When an external clock is provided to the ADA4255, the SYNC[2:0] bits set the internal clock divider value. If an external clock is supplied to the ADA4255, the clock value must be 1 MHz or must be divided down by the ADA4255 to 1 MHz using the clock divider. Table 15 lists the available divider values.

Table 15. Clock Divider Values

	Bits in the SYNC[2:0] Bit Field		
Divider Value	**SYNC2**	**SYNC1**	**SYNC0**
÷1	0	0	0
÷2	0	0	1
÷4	0	1	0
÷8	0	1	1
÷16	1	0	0
÷32	1	0	1
Reserved	1	1	0
Reserved	1	1	1

REGISTER DETAILS

DIGITAL ERROR REGISTER (DIGITAL_ERR) DETAILS

Table 16. DIGITAL_ERR Register Details (Register 0x03)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved	CAL_BUSY	SPI_CRC_ERR	SPI_RW_ERR	SPI_SCLK_CNT_ERR	Reserved	MM_CRC_ERR	ROM_CRC_ERR
Access	Reserved	R	R/W	R/W	R/W	Reserved	R/W	R/W
Reset	Reserved	0	0	0	0	Reserved	0	0

Bit 6, CAL_BUSY—Calibration Busy (Read Only)

CAL_BUSY indicates that the PGIA is undergoing a calibration and self trim operation. Until this flag is clear, the ADA4255 output is not accurate. Writing a 1 or 0 to CAL_BUSY has no effect. CAL_BUSY can be output on GPIO2 when GPIO2 is configured as an output using the corresponding GPIO_DIR bit and when the CAL_BUSY_OUT bit is set to 1.

Bit 5, SPI_CRC_ERR—SPI CRC Error

The SPI_CRC_ERR error flag indicates that an error occurred during SPI communication with the ADA4255. This error occurs when the user provided CRC does not match the ADA4255 CRC calculation. Clear this error flag by writing a 1 to the SPI_CRC_ERR bit.

Bit 4, SPI_RW_ERR—SPI Read/Write Error

The SPI_RW_ERR error flag indicates that a SPI read and/or write operation is attempted on an invalid address. This error flag can be cleared by writing a 1 to this bit.

Bit 3, SPI_SCLK_CNT_ERR—SPI SCLK Count Error

The SPI_SCLK_CNT_ERR error flag indicates that, during SPI communication while $\overline{CS}$ is low, the number of SCLK edges is either insufficient or excessive. This error flag can be cleared by writing a 1 to this bit.

Bit 1, MM_CRC_ERR—Memory Map CRC Error

The MM_CRC_ERR error flag indicates that the current internal memory map does not match the result from the previous SPI write. If this error occurs, it is recommended to reprogram the ADA4255 registers. This error flag can be cleared by writing a 1 to this bit.

Bit 0, ROM_CRC_ERR—ROM CRC Error

The ROM_CRC_ERR error flag indicates that the internal ROM did not pass the CRC check. If this error occurs, it is strongly recommended to reset or power cycle the device. If the error does not reset with a power cycle or a soft reset, it is possible that the device is permanently damaged.

REGISTER DETAILS

ANALOG ERROR REGISTER (ANALOG_ERR) DETAILS

Table 17. ANALOG_ERR Register Details (Register 0x04)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	G_RST	POR_HV	Reserved	WB_ERR	FAULT_INT	OUTPUT_ERR	INPUT_ERR	MUX_OVER_VOLT_ERR
Access	R/W	R/W	Reserved	R/W	R/W	R/W	R/W	R/W
Reset	0	0	Reserved	0	0	0	0	0

Bit 7, G_RST—Gain Reset Flag

The G_RST flag indicates that the gain settings in the GAIN_ MUX register have been reset to their defaults due to an overvoltage event in one or more of the input amplifiers that lasted more than 200 µs. Bit G5 in the TEST_MUX register is not reset by this event. This safety measure protects the input resistor network from overvoltage. This flag can be cleared by writing a 1 to this bit. Clearing this flag does not restore gain settings to the previous values.

Bit 6, POR_HV—Power-On Reset HV Supply

The POR_HV flag indicates that an event occurred on VDDH, VSSH, or VDDCP, causing the power-on reset circuit to trip. When the supply voltage returns to a valid state, the ADA4255 runs a calibration. Clear this error flag by writing a 1 to this bit position.

Bit 4, WB_ERR—Wire Break Detect Error

When performing a wire break test using the WB_DETECT register, the WB_ERR flag indicates a fault on the inputs of the amplifier. Clear this error by writing a 1 to this bit position.

Bit 3, FAULT_INT—Fault Interrupt

An OR function is performed on all unmasked error flags in the ANALOG_ERR register and the DIGITAL_ERR register to generate the FAULT_INT fault interrupt. Configuring GPIO3 as an output using the corresponding GPIO_DIR bit and setting the FAULT_INT_OUT bit (Register SF_CFG) to 1 outputs this signal to GPIO3. Clear this error by writing a 1 to this bit position. In this mode, GPIO3 is active low.

Bit 2, OUTPUT_ERR—Output Amplifier Error

The OUTPUT_ERR flag indicates that the output amplifier is overloaded. The cause of this overload condition is either the output voltage saturating or excessive current being conducted from the output of the amplifier. Clear this error by writing a 1 to this bit position.

Bit 1, INPUT_ERR—Input Amplifier Error

The INPUT_ERR flag indicates that one of the input amplifiers is overloaded. The cause of this overload condition is either saturation of one of the amplifier outputs, or a violation of the input voltage range. When this error flag is tripped for longer than 200 µs, gain settings in the GAIN_MUX register reset to the default values and the G_RST flag is set to 1. Bit G5 is not reset. Clear this error by writing a 1 to this bit position.

Bit 0, MUX_OVER_VOLT_ERR—Input Multiplexer Overvoltage Error

The MUX_OVER_VOLT_ERR flag indicates that excessive voltage is detected by the input multiplexer. The multiplexer turns all channels off to protect the input amplifier. Reads of the INPUT_MUX register during this time do not reflect this. The threshold for this detection is typically VSSH + 0.9 V and VDDH − 0.9 V. When the input voltage returns to the valid range after 20 µs, the multiplexer returns to the previous settings. If latched mode is in use, the error flag remains until reset. If nonlatched mode is used, the error flag clears when the multiplexer returns to the previous settings.

REGISTER DETAILS

GPIO DATA REGISTER (GPIO_DATA) DETAILS

Table 18. GPIO_DATA Register Details (Register 0x05)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved	GPIO_DATA[6:0]						
Access	Reserved	R/W						
Reset	Reserved	0	0	0	0	0	0	0

Bits[6:0], GPIO_DATA[6:0]—GPIO Data Values

When a GPIOx pin is configured as an output, writing a 1 to the corresponding GPIO_DATA bit causes that GPIOx pin to output a logic high. Conversely, writing a 0 to the corresponding GPIO_DATA bit causes that GPIOx pin to output a logic low.

When a GPIOx pin is configured as an input, each GPIO_DATA bit indicates whether the voltage on the corresponding GPIOx pin is a logic high or logic low. Reading a 1 indicates a logic high, and reading a 0 indicates a logic low. Writing to the GPIO_DATA bits that are configured as inputs has no effect.

REGISTER DETAILS

INTERNAL MUX CONTROL REGISTER (INPUT_MUX) DETAILS

Table 19. INPUT_MUX Register Details (Register 0x06)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved	SW_A1	SW_A2	SW_B1	SW_B2	SW_C1	SW_C2	SW_D12
Access	Reserved	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	Reserved	1	1	0	0	0	0	0

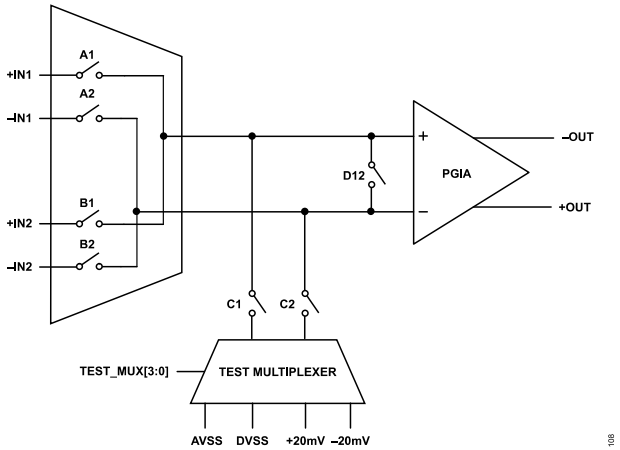

Figure 110. Input Mux Switch Configuration

Bit 6, SW_A1, and Bit 5, SW_A2—Channel 1 Input Switches

The SW_A1 bit and the SW_A2 bit control the Channel 1 input switches, A1 and A2, respectively (see Figure 110). Setting these bits to 1 closes the respective switch. SW_A1 and SW_A2 cannot be connected at the same time as SW_B1 and SW_B2, unless the MUX_PROT_DIS bit (Register ANALOG_ERR_DIS) is set to 1.

Bit 4, SW_B1, and Bit 3, SW_B2—Channel 2 Input Switches

The SW_B1 bit and the SW_B2 bit control the Channel 2 input switches, B1 and B2, respectively (see Figure 110). Setting these bits to 1 closes the respective switch. SW_B1 and SW_B2 cannot be connected at the same time as SW_A1 and SW_A2, unless the MUX_PROT_DIS bit (Register ANALOG_ERR_DIS) is set to 1.

Bit 2, SW_C1, and Bit 1, SW_C2—PGIA Input Test Multiplexer Switches

The SW_C1 bit and the SW_C2 bit can be set to 1 to connect either PGIA input to the output of the input test multiplexer (which is AVSS by default) via the C1 and C2 switches (see Figure 110).

Bit 0, SW_D12—PGIA Input Short Switch

The SW_D12 bit can be set to 1 to connect both PGIA inputs together via the D12 switch.

REGISTER DETAILS

WIRE BREAK DETECT REGISTER (WB_DETECT) DETAILS

Table 20. WB_DETECT Register Details (Register 0x07)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	WB_G_RST_DIS	Reserved			SW_F1	SW_F2	WB_CURRENT[1:0]	
Access	R/W	Reserved			R/W	R/W	R/W	
Reset	0	Reserved			0	0	1	0

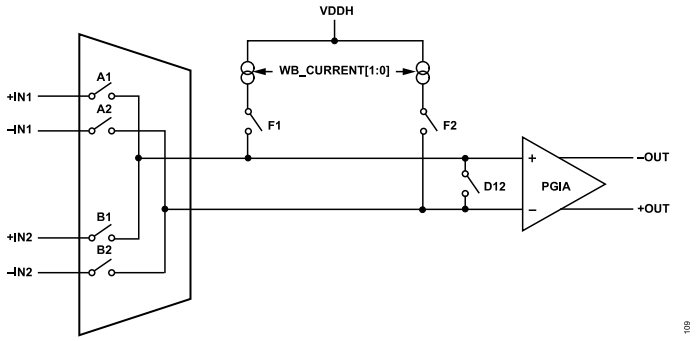

Figure 111. Wire Break Current Connectivity

Bit 7, WB_G_RST_DIS—Wire Break Gain Reset Disable

The WB_G_RST_DIS bit can be set to 1 to prevent the gain settings in the GAIN_MUX register from being overridden to 1/16 V/V when the SW_F1 bit or the SW_F2 bit are set to 1.

Bit 3, SW_F1, and Bit 2, SW_F2—Fault Switch Selection

The SW_F1 bit and the SW_F2 bit are used to connect the wire break current sources to the inputs, as shown in Figure 111. Setting SW_F1 or SW_F2 to 1 closes each corresponding switch. Both switches can be closed simultaneously. When SW_F1 or SW_F2 are set to 1 and WB_G_RST_DIS is cleared to 0, the gain settings in the GAIN_MUX register are temporarily overridden to the default values. Reading the GAIN_MUX register while SW_F1 or SW_F2 are set to 1 does not show this temporary override. When SW_F1 or SW_F2 are cleared to 0, the gain is also restored to the previous value.

Bits[1:0], WB_CURRENT—Detection Current Selection

Table 21 shows four different current values that can be used for wire break detection. Both current sources are set to the programmed value. The comparator used to detect a wire break event has a threshold at approximately 4 V from VDDH.

Table 21. Wire Break Detect Current Values

WB_CURRENT[1:0] Bits		Current Source Value	Threshold VDDCP = 5 V
Bit 1	Bit 0		
0	0	250 nA	73.2 MΩ
0	1	2 µA	9.15 MΩ
1	0	4 µA (default)	4.58 MΩ
1	1	16 µA	1.14 MΩ

REGISTER DETAILS

GPIO DIRECTION REGISTER (GPIO_DIR) DETAILS

Table 22. GPIO_DIR Register Details (Register 0x08)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved	GPIO_DIR[6:0]						
Access	Reserved	R/W						
Reset	Reserved	0	0	0	0	0	0	0

Bits[6:0], GPIO_DIR—GPIO Direction Configuration

The GPIO_DIR bit field is used to configure each GPIOx pin as either an input or an output. Setting a bit in this bit field to 1 configures the corresponding GPIOx pin as an output. Clearing a bit in this bit field to 0 configures the corresponding GPIOx as an input.

SEQUENTIAL CHIP SELECT REGISTER (SCS) DETAILS

Table 23. SCS Register Details (Register 0x09)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved	SCS[6:0]						
Access	Reserved	R/W						
Reset	Reserved	0	0	0	0	0	0	0

Bits[6:0], SCS—Sequential Chip Select Configuration

Bits[6:0] configure the GPIOx pins as sequential chip select (SCS) pins. Setting any bit in SCS6 to SCS0 to 1 and configuring the respective GPIOx pin as an output via the GPIO_DIR register makes that GPIOx function as a chip select pin for a slave device. When SCS is used, the first $\overline{CS}$ pulse addresses the first GPIOx configured for SCS. Subsequent $\overline{CS}$ pulses address the remainder of the GPIOx pins configured for SCS, and the last $\overline{CS}$ pulse addresses the ADA4255. This sequence repeats in a round robin format until the ADA4255 is configured otherwise. This process is shown in Figure 112.

Slave SCS lines may require pull-up resistors to avoid inadvertently communicating with slave devices during SCS configuration.

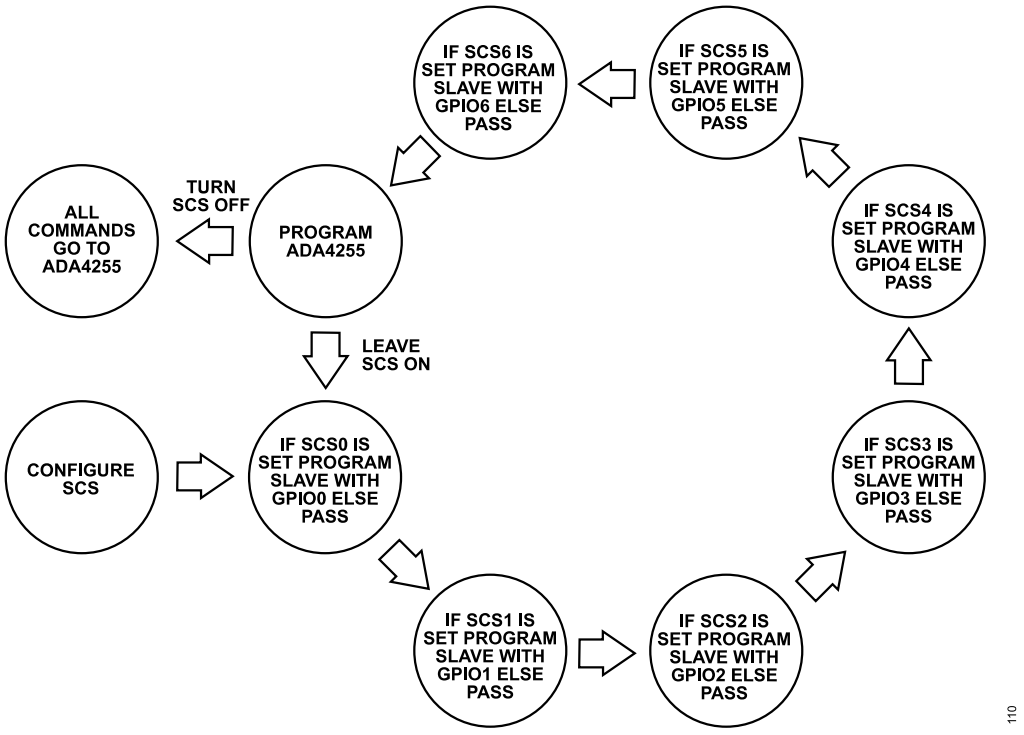

Figure 112. Sequential Chip Select Flowchart

REGISTER DETAILS

ANALOG ERROR MASK REGISTER (ANALOG_ERR_DIS) DETAILS

The ANALOG_ERR_DIS register can be used to mask individual error flags in the ANALOG_ERR register. Setting bits in ANALOG_ERR_DIS to 1 disables the corresponding error flag.

Table 24. ANALOG_ERR_DIS Register Details (Register 0x0A)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	G_RST_DIS	POR_HV_DIS	Reserved	WB_ERR_DIS	MUX_PROT_DIS	OUTPUT_ERR_DIS	INPUT_ERR_DIS	MUX_OVER_VOLT_ERR_DIS
Access	R/W	R/W	Reserved	R/W	R/W	R/W	R/W	R/W
Reset	0	0	Reserved	0	0	0	0	0

Bit 7, G_RST_DIS—Disable Gain Reset Error Flag

The G_RST_DIS bit disables the G_RST error flag

Bit 6, POR_HV_DIS—Disable High Voltage Power Reset Flag

The POR_HV_DIS bit disables the POR_HV error flag.

Bit 4, WB_ERR_DIS—Disable Wire Break Detection Flag

The WB_ERR_DIS bit disables the WB_ERR error flag.

Bit 3, MUX_PROT_DIS—Disable Input Multiplexer Protection

By default, the input multiplexer does not allow both sets of inputs to be connected at the same time (this is a safety feature). This protection can be disabled by setting MUX_PROT_DIS to 1.

Bit 2, OUTPUT_ERR_DIS—Disable Output Amplifier Error Flag

The OUTPUT_ERR_DIS bit disables the OUTPUT_ERR error flag.

Bit 1, INPUT_ERR_DIS—Disable Input Amplifier Error Flag

The INPUT_ERR_DIS bit disables the INPUT_ERR error flag.

Bit 0, MUX_OVER_VOLT_ERR_DIS—Disable Multiplexer Overvoltage Flag

The MUX_OVER_VOLT_ERR_DIS bit disables the MUX_OVER_VOLT_ERR error flag.

REGISTER DETAILS

DIGITAL ERROR MASK REGISTER (DIGITAL_ERR_DIS) DETAILS

The DIGITAL_ERR_DIS register can be used to mask individual error flags in the DIGITAL_ERR register. Setting bits in the DIGITAL_ERR_DIS register to 1 disables the error flag.

Table 25. DIGITAL_ERR_DIS Register Details (Register 0x0B)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved	CAL_BUSY_DIS	SPI_CRC_ERR_DIS	SPI_RW_ERR_DIS	SPI_SCLK_CNT_ERR_DIS	M_CLK_CNT_ERR_DIS	MM_CRC_ERR_DIS	ROM_CRC_ERR_DIS
Access	Reserved	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	Reserved	0	1	0	0	0	0	0

Bit 6, CAL_BUSY_DIS—Disable Calibration Busy Error Flag

The CAL_BUSY_DIS bit disables the CAL_BUSY error flag.

Bit 5, SPI_CRC_ERR_DIS—Disable SPI CRC Error Flag

When SPI_CRC_ERR_DIS is cleared to 0, the ADA4255 expects an additional checksum byte with write commands and transmits an extra checksum byte with read commands. By default, SPI_CRC_ERR_DIS is set to 1, and this functionality is disabled. After enabling CRC, a manual check can be performed to ensure that the CRC configuration command was properly communicated. If the CRC is used, it is recommended to configure the CRC before other registers so that all subsequent communication receives the CRC.

Bit 4, SPI_RW_ERR_DIS—Disable SPI Read/Write Error Flag

The SPI_RW_ERR_DIS bit disables the SPI_RW_ERR error flag.

Bit 3, SPI_SCLK_CNT_ERR_DIS—Disable SPI SCLK Count Error Flag

The SPI_SCLK_CNT_ERR_DIS bit disables the SPI_SCLK_CNT_ERR error flag.

Bit 2, M_CLK_CNT_ERR_DIS—Disable Master Clock Count Output

When the M_CLK_CNT_ERR_DIS bit is set to 0, the master clock is updated in the M_CLK_CNT register. Setting this bit to 1 stops M_CLK_CNT from incrementing.

Bit 1, MM_CRC_ERR_DIS—Disable Memory Map CRC Error Flag

The MM_CRC_ERR_DIS bit disables the MM_CRC_ERR error flag.

Bit 0, ROM_CRC_ERR_DIS—Disable ROM CRC Error Flag

The ROM_CRC_ERR_DIS bit disables the ROM_CRC_ERR error flag.

REGISTER DETAILS

SPECIAL FUNCTION CONFIGURATION REGISTER (SF_CFG) DETAILS

Table 26. SF_CFG Register Details (Register 0x0C)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved		INT_CLK_OUT	EXT_CLK_IN	FAULT_INT_OUT	CAL_BUSY_OUT	EXT_MUX[1:0]	
Access	Reserved		R/W	R/W	R/W	R/W	R/W	
Reset	Reserved		0	0	0	0	0	0

Bit 5, INT_CLK_OUT—Internal Oscillator Output

When GPIO4 is configured as an output via GPIO_DIR and INT_CLK_OUT is set to 1, one of the internal clocks is output to GPIO4. The CLK_OUT_SEL bit in the SYNC_CFG register determines which internal clock is on GPIO4.

Bit 4, EXT_CLK_IN—External Oscillator Input

When GPIO4 is configured as an input via GPIO_DIR and EXT_CLK_IN is set to 1, an external clock can be provided via GPIO4. If this clock frequency is not 1 MHz, the on-chip clock divider must be used to divide the clock via the SYNC[2:0] bits. The default setting for the internal clock divider is 16. The clock must always be present and have a 50% duty cycle to ensure charge pump operation.

Bit 3, FAULT_INT_OUT—Fault Interrupt Output

When GPIO3 is configured as an output via GPIO_DIR and FAULT_INT_OUT is set to 1, the value in the FAULT_INT bit (Register ANALOG_ERR) appears on GPIO3.

Bit 2, CAL_BUSY_OUT—Calibration Busy Output

When GPIO2 is configured as an output via GPIO_DIR and CAL_BUSY_OUT is set to 1, the value in the CAL_BUSY bit (Register DIGITAL_ERR) appears on GPIO2.

Bits[1:0], EXT_MUX_EN[1:0]—Enable External Multiplexer Control

Each bit in the EXT_MUX_EN[1:0] bit range enables GPIO1 and/or GPIO0 to be controlled via the EXT_MUX bits in the GAIN_MUX register.

REGISTER DETAILS

ERROR CONFIGURATION REGISTER (ERR_CFG) DETAILS

Table 27. ERR_CFG Register Details (Register 0x0D)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	ERR_LATCH_DIS	Reserved			ERR_DELAY[3:0]			
Access	R/W	Reserved			R/W	R/W	R/W	R/W
Reset	0	Reserved			0	1	0	0

Bit 7, ERR_LATCH_DIS—Disable Error Latching

By default, ERR_LATCH_DIS is cleared to 0 and error flags are latched and require resetting. Setting ERR_LATCH_DIS to 1 makes the errors appear transparently (nonlatching) on the respective outputs. When ERR_LATCH_DIS is set to 1, errors can be suppressed for the time interval configured by the ERR_DELAY bits.

Bits[3:0], ERR_DELAY[3:0] —Error Suppression Time

When ERR_LATCH_DIS is set to 1, ERR_DELAY determines the number of clock cycles an error must remain present before the error flag is tripped, which eliminates false trips due to noise and transients.

Table 28. Error Flag Suppression Time

ERR_DELAY[3:0]	Clock Cycles (µs)
0x0	0
0x1	1
0x2	2
0x3	3
0x4	4
0x5	5
0x6	6
0x7	7
0x8	8
0x9	12
0xA	16
0xB	24
0xC	32
0xD	48
0xE	64
0xF	127

REGISTER DETAILS

TEST MULTIPLEXER REGISTER (TEST_MUX) DETAILS

Table 29. TEST_MUX Register Details (Register 0x0E)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	G5	CAL_SEL	CAL_EN[1:0]		TEST_MUX[3:0]			
Access	R/W	RW	R/W		R/W			
Reset	0	0	0	0	0	0	0	0

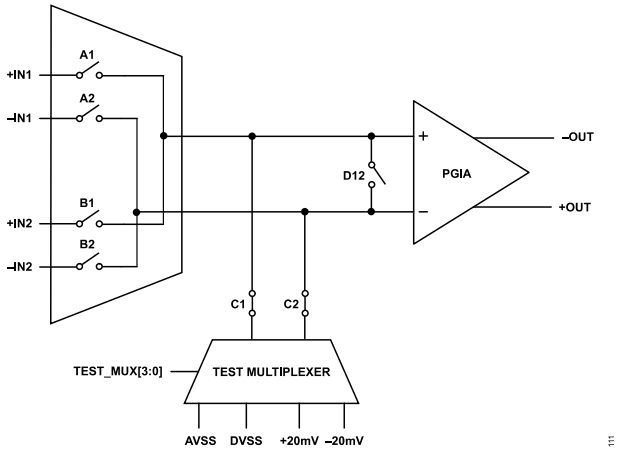

Figure 113. Test Multiplexer Connectivity

Bit 7, G5—Output Amplifier Scaling Gain = 1.25 V/V

Clearing Bit G4 to 0 and setting Bit G5 to 1 configures the output amplifier to a scaling gain value of 1.25 V/V. This setting scales the input amplifier gain configured in the GAIN_MUX register by 1.25 V/V.

Table 30. Output Amplifier Scaling Gain Settings

G5	G4	Output Amplifier Scaling Gain (V/V)
0	0	1
X[1]	1	1.375
1	0	1.25

[1] X means don't care.

Bit 6, CAL_SEL—Calibration Type Configuration

Clearing the CAL_SEL bit to 0 configures the ADA4255 to perform quick calibrations. Setting CAL_SEL to 1 configures the ADA4255 to perform full calibrations.

Bits[5:4], CAL_EN[1:0]—Scheduled Calibration Enable and Interval

CAL_EN enables scheduled calibrations and configures the interval on which these calibrations execute. While calibrations are executing, the inputs of the PGIA are not connected to the input pins. The CAL_BUSY signal indicates when a calibration is executing. CAL_BUSY can be output to GPIO2 by configuring GPIO2 as an output via the GPIO_DIR bits (Register GPIO_DIR) and setting the CAL_BUSY_OUT bit (Register SF_CFG) to 1. Minimize and avoid noise and input transients during calibrations.

Table 31. Scheduled Calibration Configurations

CAL_EN, Bit 1	CAL_EN, Bit 0	Scheduled Calibration Configuration
0	0	Disabled
0	1	Enabled, 33 sec interval
1	0	Enabled, 132 sec interval
1	1	Enabled, 495 sec interval

REGISTER DETAILS

Bits[3:0], TEST_MUX[3:0]—Input Test Multiplexer Configuration

The TEST_MUX[3:0] bits are used to configure the input test multiplexers, which can switch four different signals to either of the inputs for diagnostic and calibration purposes. These potentials are AVSS, DVSS, +20 mV, and −20 mV. SW_C1 and SW_C2 must also be set to 1 for the outputs of these multiplexers to be connected to the amplifier inputs.

Table 32. Test Multiplexer Configurations

TEST_MUX[3:0]	Noninverting Input	Inverting Input
0000	AVSS	AVSS
0001	DVSS	AVSS
0100	AVSS	DVSS
0101	DVSS	DVSS
1010	+20 mV	
1111	−20 mV	

REGISTER DETAILS

EXCITATION CURRENT CONFIGURATION REGISTER (EX_CURRENT_CFG) DETAILS

Table 33. EX_CURRENT_CFG Register Details (Register 0x0F)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	EX_CURRENT_SEL[1:0]		Reserved		EX_CURRENT[3:0]			
Access	R/W		Reserved		R/W			
Reset	0	0	Reserved		0	0	0	0

Bits[7:6], EX_CURRENT_SEL[1:0]—Excitation Current Connection Configuration

EX_CURRENT_SEL[1:0] configures internal current source IOUT. Table 34 shows all available configurations. When IOUT is used, the source of this current is AVDD.

Table 34. Excitation Current Source Connections

EX_CURRENT_SEL[1:0]	Current Source
0b00	None
0b01	IOUT
0b10	None
0b11	IOUT

Bits[3:0], EX_CURRENT[3:0]—Excitation Current Value

The EX_CURRENT[3:0] bits configure the current source value connected via the EX_CURRENT_SEL bits. Table 35 shows all the possible current values.

Table 35. Excitation Current Values

EX_CURRENT[3:0]	Excitation Current Value
0x0	0 µA
0x1	100 µA
0x2	200 µA
0x3	300 µA
0x4	400 µA
0x5	500 µA
0x6	600 µA
0x7	700 µA
0x8	800 µA
0x9	900 µA
0xA	1 mA
0xB	1.1 mA
0xC	1.2 mA
0xD	1.3 mA
0xE	1.4 mA
0xF	1.5 mA

REGISTER DETAILS

GAIN CALIBRATION REGISTERS (GAIN_CALX) DETAILS

The gain calibration registers contain the measured gain error of each individual ADA4255. Refer to the Gain Error Calibration section for details on how to use these values. GAIN_CAL1 through GAIN_CAL12 store gain error results for each input gain setting with a scaling gain of 1 V/V. When a scaling gain of 1 V/V is used, these gain error values are used directly. GAIN_CAL13 through GAIN_CAL24 store any additional gain error incurred when 1.375 V/V or 1.25 V/V scaling gains are used. When scaling gains other than 1 V/V are used, the gain error read from the appropriate GAIN_CAL1 through GAIN_CAL12 register must be summed with the corresponding additional gain error read from the appropriate GAIN_CAL13 through GAIN_CAL24. For example, if the input gain is 2 V/V and the 1.25 V/V scalar is used, the total gain error is GAIN_CAL6 + GAIN_CAL21.

Table 36. GAIN_CAL Registers Details (Register 0x10 to Register 0x27)

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10	GAIN_CALx		Reserved			GAIN_CAL1[4:0]			
0x11			Reserved			GAIN_CAL2[4:0]			
0x12			Reserved			GAIN_CAL3[4:0]			
0x13			Reserved			GAIN_CAL4[4:0]			
0x14			Reserved			GAIN_CAL5[4:0]			
0x15			Reserved			GAIN_CAL6[4:0]			
0x16			Reserved			GAIN_CAL7[4:0]			
0x17			Reserved			GAIN_CAL8[4:0]			
0x18			Reserved			GAIN_CAL9[4:0]			
0x19			Reserved			GAIN_CAL10[4:0]			
0x1A			Reserved			GAIN_CAL11[4:0]			
0x1B			Reserved			GAIN_CAL12[4:0]			
0x1C			Reserved			GAIN_CAL13[4:0]			
0x1D			Reserved			GAIN_CAL14[4:0]			
0x1E			Reserved			GAIN_CAL15[4:0]			
0x1F			Reserved			GAIN_CAL16[4:0]			
0x20			Reserved			GAIN_CAL17[4:0]			
0x21			Reserved			GAIN_CAL18[4:0]			
0x22			Reserved			GAIN_CAL19[4:0]			
0x23			Reserved			GAIN_CAL20[4:0]			
0x24			Reserved			GAIN_CAL21[4:0]			
0x25			Reserved			GAIN_CAL22[4:0]			
0x26			Reserved			GAIN_CAL23[4:0]			
0x27			Reserved			GAIN_CAL24[4:0]			
Access			Reserved			R			

REGISTER DETAILS

TRIGGER CALIBRATION REGISTER (TRIG_CAL) DETAILS

Table 37. TRIG_CAL Registers Details (Register 0x2A)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved							TRIG_CAL
Access	Reserved							W
Reset	Reserved							0

Bit 0, TRIG_CAL—Trigger Calibration Input

Setting TRIG_CAL to 1 initiates a calibration sequence when scheduled calibrations are disabled via CAL_EN. The type of calibration that is triggered can be configured via the CAL_SEL bits (Register TEST_MUX). The TRIG_CAL bit is self clearing.

MASTER CLOCK COUNT REGISTER (M_CLK_CNT) DETAILS

Table 38. M_CLK_CNT Registers Details (Register 0x2E)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	M_CLK_CNT[7:0]							
Access	R							

Bits[7:0], M_CLK_CNT[7:0]—Master Clock Count

M_CLK_CNT contains a master clock counter that increments when M_CLK_CNT_ERR is cleared to 0. The counter is updated every 512 µs. Setting M_CLK_CNT_ERR to 1 stops this register from updating.

DIE REVISION IDENTIFICATION REGISTER (DIE_REV_ID) DETAILS

Table 39. DIE_REV_ID Registers Details (Register 0x2F)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	DIE_REV_ID[7:0]							
Access	R							
Reset	0	0	1	1	0	0	0	0

Bits[7:0], DIE_REV_ID[7:0]—Die Revision Identification Number

DIE_REV_ID contains a fixed value of 0x30 that can be used to verify the SPI communication with the ADA4255.

DEVICE IDENTIFICATION REGISTERS (PART_ID) DETAILS

Table 40. PART_ID Registers Details (Register 0x64 through Register 0x68)[1]

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x64	PART_ID[39:32]							
0x65	PART_ID[31:24]							
0x66	PART_ID[23:16]							
0x67	PART_ID[15:8]							
0x68	PART_ID[7:0]							
Access	R							

PART_ID[39:0]—Part ID Number

The PART_ID register contains a unique device identification number that is programmed at the factory.