

FEATURES

- Lower power at high voltage: 290 μ A per amplifier typical
- Low input bias current: 1 pA maximum
- Wide bandwidth: 1.2 MHz typical
- Slew rate: 1 V/ μ s typical
- Offset voltage drift: 3 μ V/ $^{\circ}$ C typical
- Single-supply operation: 5 V to 16 V
- Dual-supply operation: \pm 2.5 V to \pm 8 V
- Unity gain stable

APPLICATIONS

- Portable systems
- High density power budget systems
- Medical equipment
- Physiological measurement
- Precision references
- Multipole filters
- Sensors
- Transimpedance amplifiers
- Buffer/level shifting

GENERAL DESCRIPTION

The ADA4665-2 is a rail-to-rail input/output dual amplifier optimized for lower power budget designs. The ADA4665-2 offers a low supply current of 400 μ A maximum per amplifier at 25 $^{\circ}$ C and 600 μ A maximum per amplifier over the extended industrial temperature range. This feature makes the ADA4665-2 well suited for low power applications. In addition, the ADA4665-2 has a very low bias current of 1 pA maximum, low offset voltage drift of 3 μ V/ $^{\circ}$ C, and bandwidth of 1.2 MHz. The combination of these features, together with a wide supply voltage range from 5 V to 16 V, allows the device to be used in a wide variety of other applications, including process control, instrumentation equipment, buffering, and sensor front ends. Furthermore, its rail-to-rail input and output swing adds to its versatility. The ADA4665-2 is specified from -40 $^{\circ}$ C to +125 $^{\circ}$ C and is available in standard SOIC and MSOP packages.

PIN CONFIGURATIONS

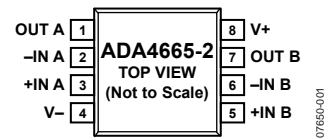


Figure 1. 8-Lead SOIC



Figure 2. 8-Lead MSOP

Table 1. Low Cost Rail-to-Rail Input/Output Op Amps

| Supply | 5 V | 16 V |
|--------|--------|-----------|
| Single | AD8541 | ADA4665-2 |
| Dual | AD8542 | |
| Quad | AD8544 | |

Table 2. Other Rail-to-Rail Input/Output Op Amps

| Supply | 5 V | 16 V | 36 V |
|--------|--------|--------|-----------|
| Single | AD8603 | AD8663 | ADA4091-2 |
| Dual | AD8607 | AD8667 | |
| Quad | AD8609 | AD8669 | |

Rev. 0

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REVISION HISTORY

1/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—16 V OPERATION

$V_{SY} = 16\text{ V}$, $V_{CM} = V_{SY}/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit | |
|--------------------------------------|--------------------------|------------------------------------------------------------------------------|-------|----------|-----|------------------------------|----|
| INPUT CHARACTERISTICS | | | | | | | |
| Offset Voltage | V_{OS} | $V_{CM} = 16\text{ V}$ | | 1 | 4 | mV | |
| | | $V_{CM} = 0\text{ V to }16\text{ V}$ | | 1 | 6 | mV | |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | | 9 | mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 3 | | $\mu\text{V}/^\circ\text{C}$ | |
| Input Bias Current | I_B | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 0.1 | 1 | pA | |
| Input Offset Current | I_{OS} | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | | 200 | pA |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 0.1 | 1 | pA | |
| Input Voltage Range | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 0 | | 16 | V | |
| Common-Mode Rejection Ratio | CMRR | $V_{CM} = 0\text{ V to }16\text{ V}$ | 55 | 75 | | dB | |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 50 | | | dB | |
| Large Signal Voltage Gain | A_{VO} | $R_L = 10\text{ k}\Omega$, $V_O = 0.5\text{ V to }15\text{ V}$ | 85 | 100 | | dB | |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 75 | | | dB | |
| Input Resistance | R_{IN} | | | 4 | | G Ω | |
| Input Capacitance, Differential Mode | C_{INDM} | | | 2 | | pF | |
| Input Capacitance, Common Mode | C_{INCM} | | | 7 | | pF | |
| OUTPUT CHARACTERISTICS | | | | | | | |
| Output Voltage High | V_{OH} | $R_L = 100\text{ k}\Omega$ to V_{CM} | 15.95 | 15.99 | | V | |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 15.9 | | | V | |
| | | $R_L = 10\text{ k}\Omega$ to V_{CM} | 15.9 | 15.95 | | V | |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 15.8 | | | V | |
| Output Voltage Low | V_{OL} | $R_L = 100\text{ k}\Omega$ to V_{CM} | | 4 | 7.5 | mV | |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | 15 | mV | |
| | | $R_L = 10\text{ k}\Omega$ to V_{CM} | | 40 | 75 | mV | |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | 150 | mV | |
| Short-Circuit Current | I_{SC} | | | ± 30 | | mA | |
| Closed-Loop Output Impedance | Z_{OUT} | $f = 100\text{ kHz}$, $A_V = 1$ | | 100 | | Ω | |
| POWER SUPPLY | | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_{SY} = 5\text{ V to }16\text{ V}$ | 70 | 95 | | dB | |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 65 | | | dB | |
| Supply Current per Amplifier | I_{SY} | $I_O = 0\text{ mA}$ | | 290 | 400 | μA | |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | 600 | μA | |
| DYNAMIC PERFORMANCE | | | | | | | |
| Slew Rate | SR | $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$ | | 1 | | V/ μs | |
| Settling Time to 0.1% | t_s | $V_{IN} = 1\text{ V step}$, $R_L = 2\text{ k}\Omega$, $C_L = 50\text{ pF}$ | | 6.5 | | μs | |
| Gain Bandwidth Product | GBP | $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$ | | 1.2 | | MHz | |
| Phase Margin | Φ_M | $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$ | | 50 | | Degrees | |
| NOISE PERFORMANCE | | | | | | | |
| Voltage Noise | e_n p-p | $f = 0.1\text{ Hz to }10\text{ Hz}$ | | 3 | | $\mu\text{V p-p}$ | |
| Voltage Noise Density | e_n | $f = 1\text{ kHz}$ | | 32 | | $\text{nV}/\sqrt{\text{Hz}}$ | |
| | | $f = 10\text{ kHz}$ | | 27 | | $\text{nV}/\sqrt{\text{Hz}}$ | |
| Current Noise Density | i_n | $f = 1\text{ kHz}$ | | 50 | | $\text{fA}/\sqrt{\text{Hz}}$ | |

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ELECTRICAL CHARACTERISTICS—5 V OPERATION

$V_{SY} = 5\text{ V}$, $V_{CM} = V_{SY}/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|--------------------------------------|--------------------------|------------------------------------------------------------------------------|------|---------|-----|------------------------------|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | V_{OS} | $V_{CM} = 5\text{ V}$ | | 1 | 4 | mV |
| | | $V_{CM} = 0\text{ V to }5\text{ V}$ | | 1 | 6 | mV |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | | 9 |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 3 | | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current | I_B | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 0.1 | 1 | pA |
| | | | | | | 100 |
| Input Offset Current | I_{OS} | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 0.1 | 1 | pA |
| | | | | | | 10 |
| Input Voltage Range | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 0 | | 5 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM} = 0\text{ V to }5\text{ V}$ | 55 | 75 | | dB |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 50 | | | dB |
| Large Signal Voltage Gain | A_{VO} | $R_L = 10\text{ k}\Omega$, $V_O = 0.5\text{ V to }4.5\text{ V}$ | 85 | 100 | | dB |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 75 | | | dB |
| Input Resistance | R_{IN} | | | 1 | | G Ω |
| Input Capacitance, Differential Mode | C_{INDM} | | | 2 | | pF |
| Input Capacitance, Common Mode | C_{INCM} | | | 7 | | pF |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | V_{OH} | $R_L = 100\text{ k}\Omega$ to V_{CM} | 4.95 | 4.99 | | V |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 4.9 | | | V |
| | | $R_L = 10\text{ k}\Omega$ to V_{CM} | 4.9 | 4.96 | | V |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 4.8 | | | V |
| Output Voltage Low | V_{OL} | $R_L = 100\text{ k}\Omega$ to V_{CM} | | 3 | 5 | mV |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | 10 | mV |
| | | $R_L = 10\text{ k}\Omega$ to V_{CM} | | 30 | 50 | mV |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | 100 | mV |
| Short-Circuit Current | I_{SC} | | | ± 8 | | mA |
| Closed-Loop Output Impedance | Z_{OUT} | $f = 100\text{ kHz}$, $A_V = 1$ | | 100 | | Ω |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_{SY} = 5\text{ V to }16\text{ V}$ | 70 | 95 | | dB |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 65 | | | dB |
| Supply Current per Amplifier | I_{SY} | $I_O = 0\text{ mA}$ | | 270 | 350 | μA |
| | | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | 600 | μA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$ | | 1 | | V/ μs |
| Settling Time to 0.1% | t_s | $V_{IN} = 1\text{ V step}$, $R_L = 2\text{ k}\Omega$, $C_L = 50\text{ pF}$ | | 6.5 | | μs |
| Gain Bandwidth Product | GBP | $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$ | | 1.2 | | MHz |
| Phase Margin | Φ_M | $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$ | | 50 | | Degrees |
| NOISE PERFORMANCE | | | | | | |
| Voltage Noise | e_n p-p | $f = 0.1\text{ Hz to }10\text{ Hz}$ | | 3 | | $\mu\text{V p-p}$ |
| Voltage Noise Density | e_n | $f = 1\text{ kHz}$ | | 32 | | nV/ $\sqrt{\text{Hz}}$ |
| | | $f = 10\text{ kHz}$ | | 27 | | nV/ $\sqrt{\text{Hz}}$ |
| Current Noise Density | i_n | $f = 1\text{ kHz}$ | | 50 | | fA/ $\sqrt{\text{Hz}}$ |

ABSOLUTE MAXIMUM RATINGS

Table 5.

| Parameter | Rating |
|--------------------------------------|---------------------------------|
| Supply Voltage | 16.5 V |
| Input Voltage ¹ | GND – 0.3 V to $V_{SY} + 0.3$ V |
| Input Current | ±10 mA |
| Differential Input Voltage | ± V_{SY} |
| Output Short-Circuit Duration to GND | Indefinite |
| Storage Temperature Range | –65°C to +150°C |
| Operating Temperature Range | –40°C to +125°C |
| Junction Temperature Range | –65°C to +150°C |
| Lead Temperature (Soldering, 60 sec) | 300°C |

¹ The input pins have clamp diodes to the power supply pins.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. This value was measured using a 4-layer JEDEC standard printed circuit board.

Table 6. Thermal Resistance

| Package Type | θ_{JA} | θ_{JC} | Unit |
|---------------------|---------------|---------------|------|
| 8-Lead SOIC_N (R-8) | 158 | 43 | °C/W |
| 8-Lead MSOP (RM-8) | 186 | 52 | °C/W |

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

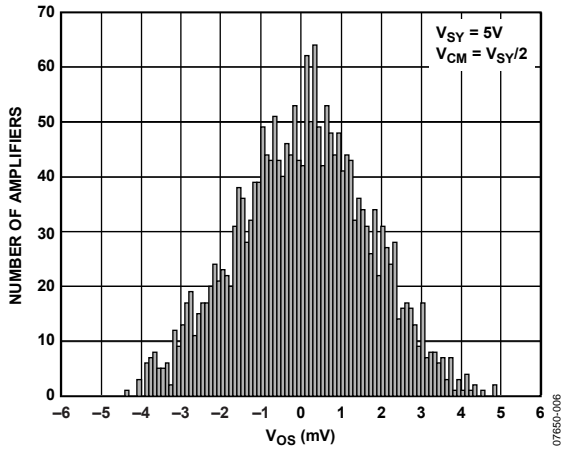


Figure 3. Input Offset Voltage Distribution

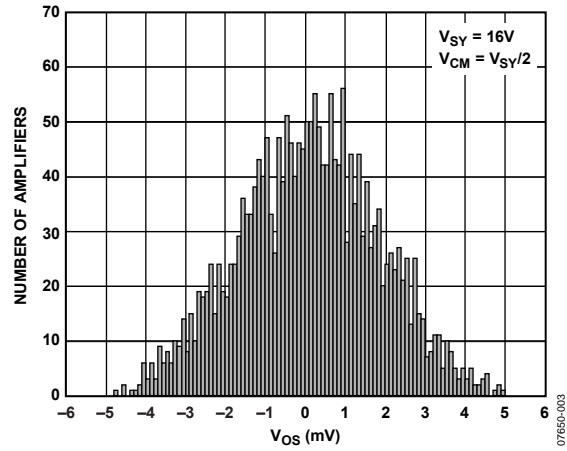


Figure 6. Input Offset Voltage Distribution

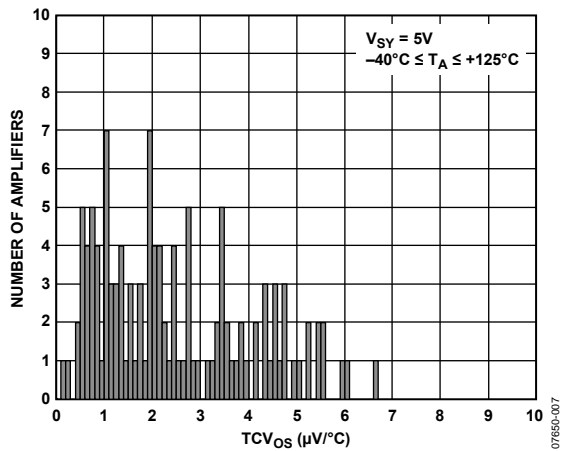


Figure 4. Input Offset Voltage Drift Distribution

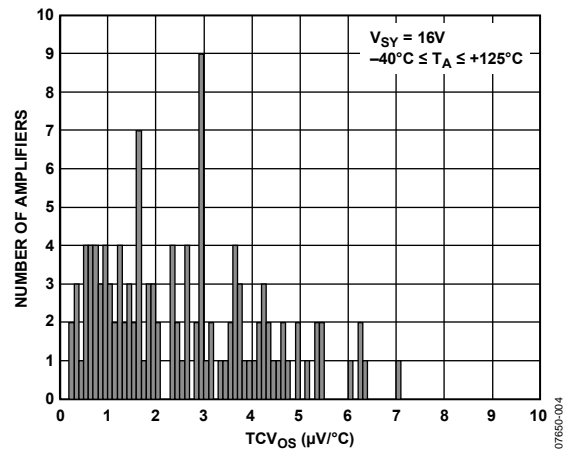


Figure 7. Input Offset Voltage Drift Distribution

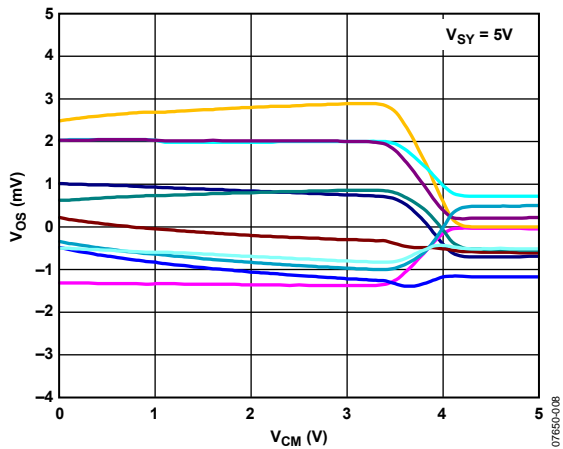


Figure 5. Input Offset Voltage vs. Common-Mode Voltage

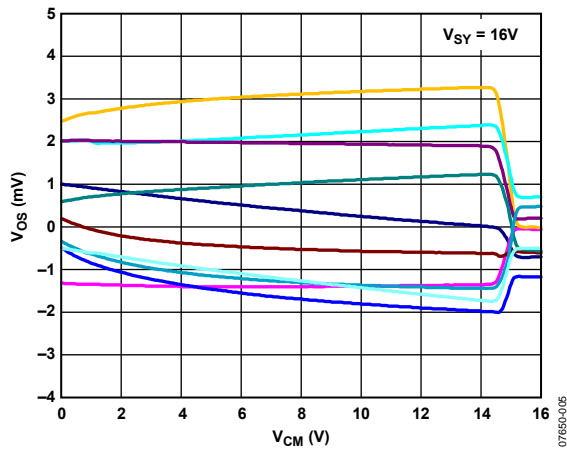


Figure 8. Input Offset Voltage vs. Common-Mode Voltage

T_A = 25°C, unless otherwise noted.

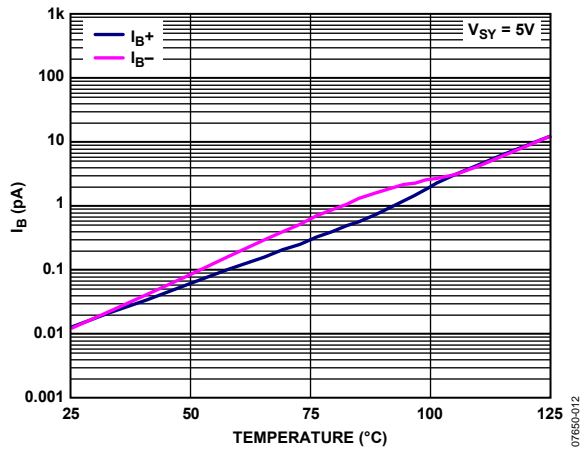


Figure 9. Input Bias Current vs. Temperature

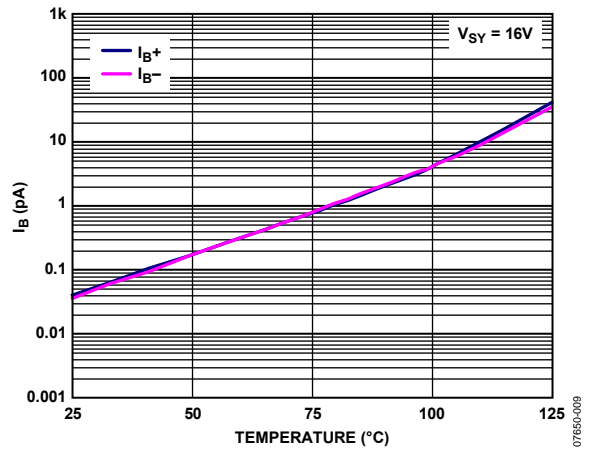


Figure 12. Input Bias Current vs. Temperature

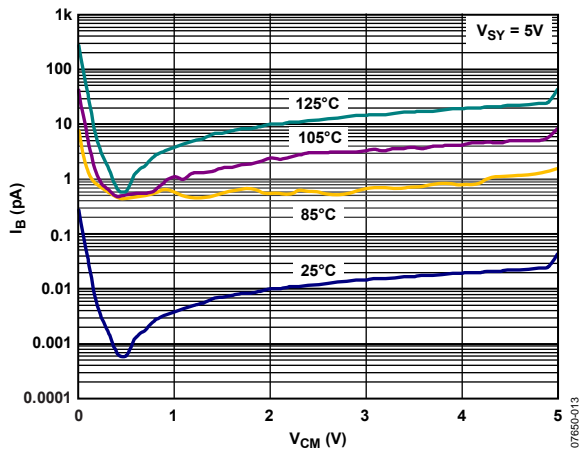


Figure 10. Input Bias Current vs. Input Common-Mode Voltage

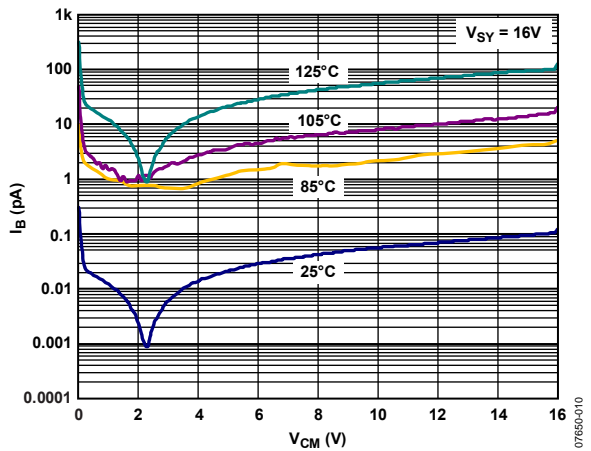


Figure 13. Input Bias Current vs. Input Common-Mode Voltage

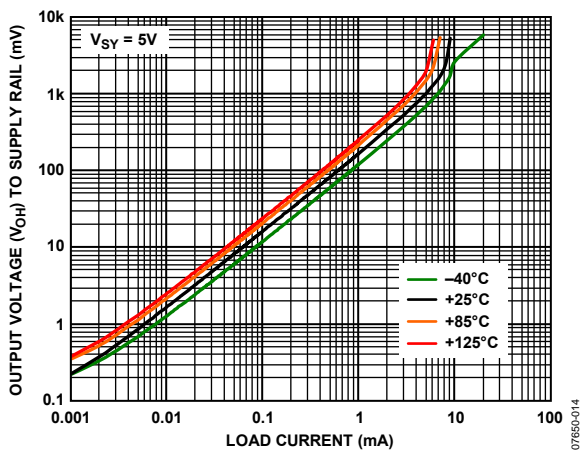


Figure 11. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

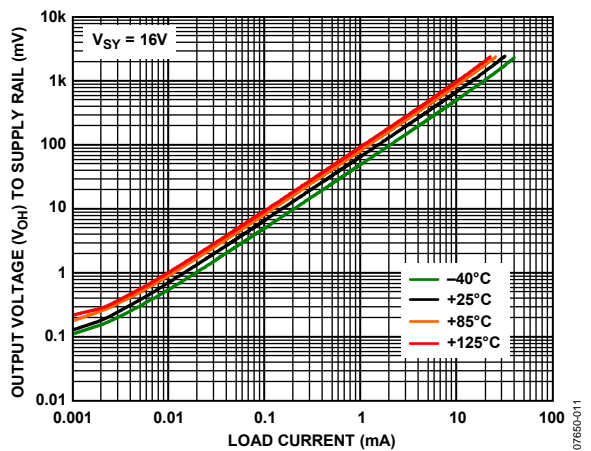


Figure 14. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

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$T_A = 25^\circ\text{C}$, unless otherwise noted.

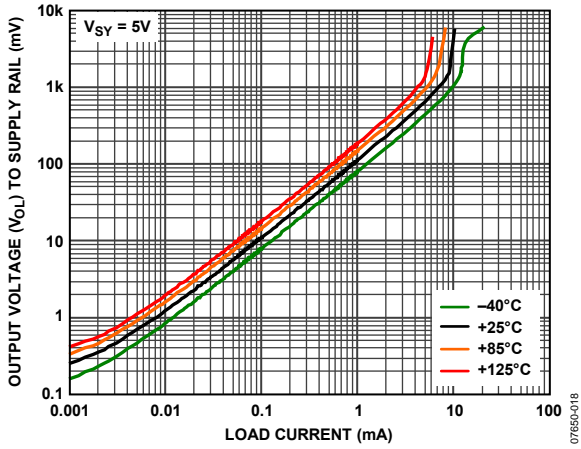


Figure 15. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

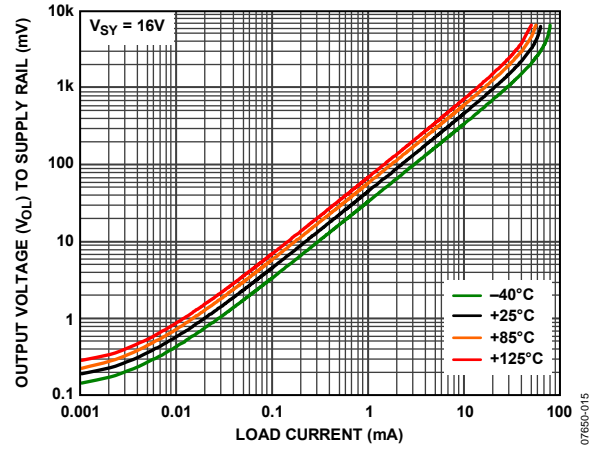


Figure 18. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

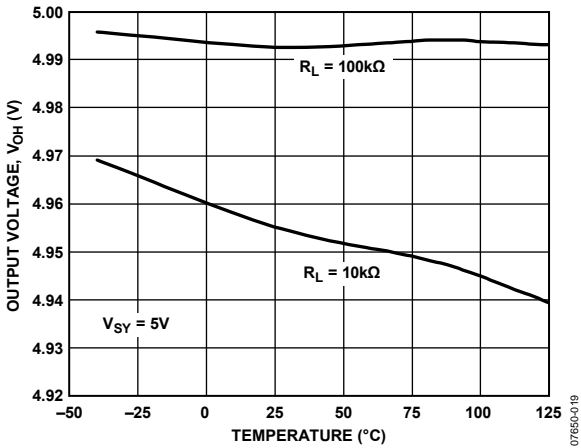


Figure 16. Output Voltage (V_{OH}) vs. Temperature

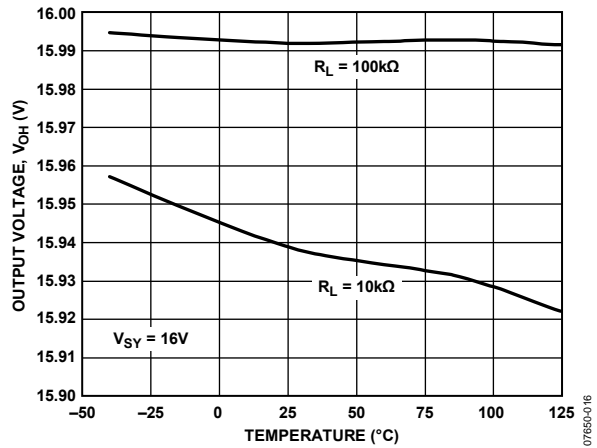


Figure 19. Output Voltage (V_{OH}) vs. Temperature

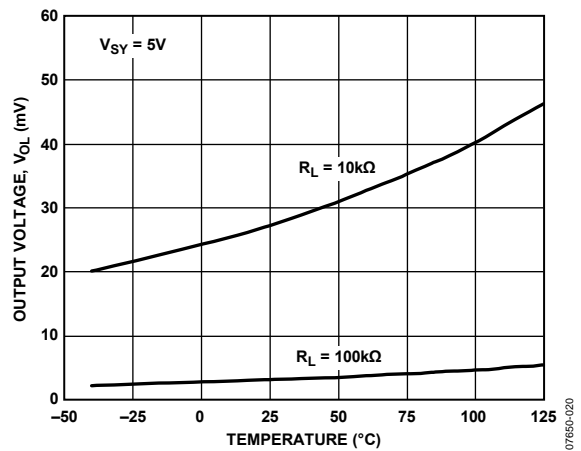


Figure 17. Output Voltage (V_{OL}) vs. Temperature

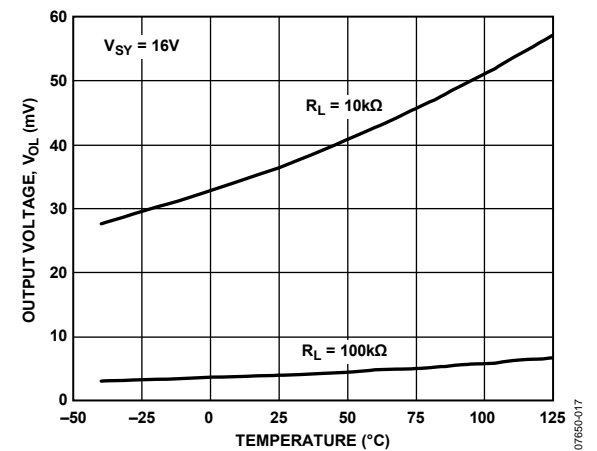


Figure 20. Output Voltage (V_{OL}) vs. Temperature

T_A = 25°C, unless otherwise noted.

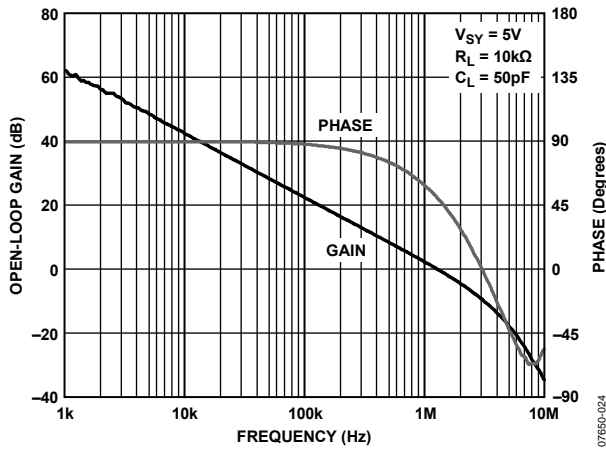


Figure 21. Open-Loop Gain and Phase vs. Frequency

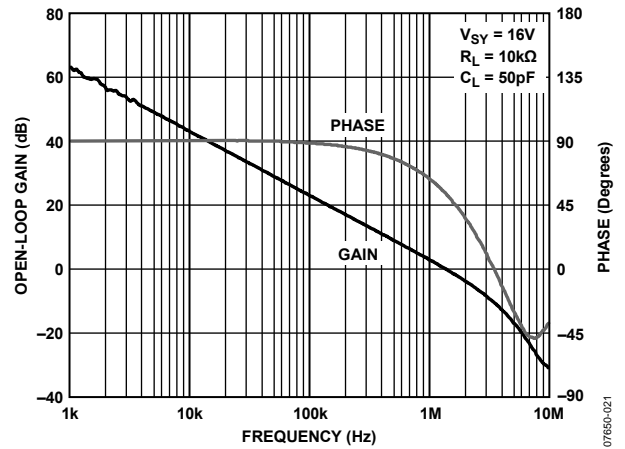


Figure 24. Open-Loop Gain and Phase vs. Frequency

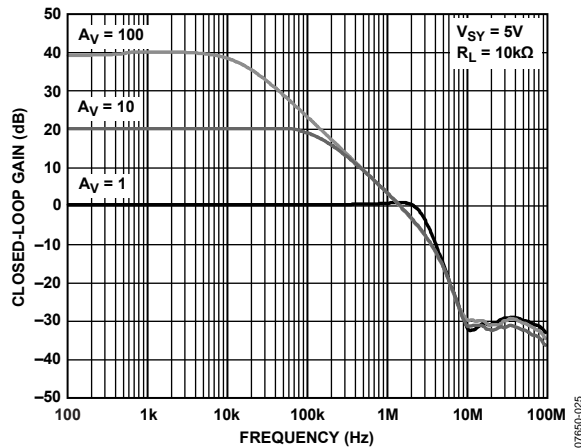


Figure 22. Closed-Loop Gain vs. Frequency

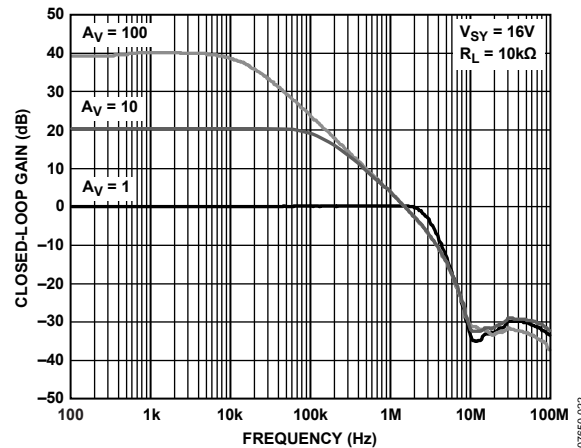


Figure 25. Closed-Loop Gain vs. Frequency

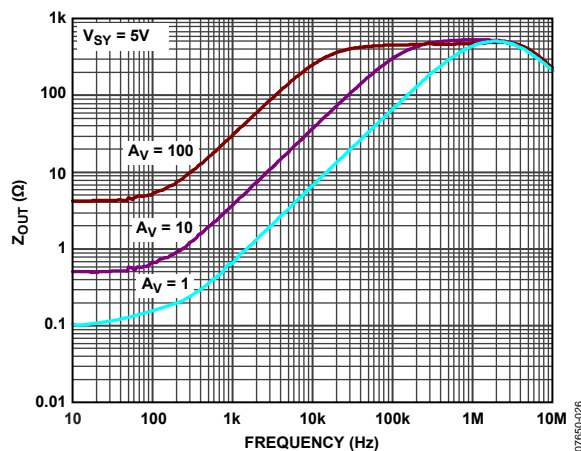


Figure 23. Output Impedance vs. Frequency

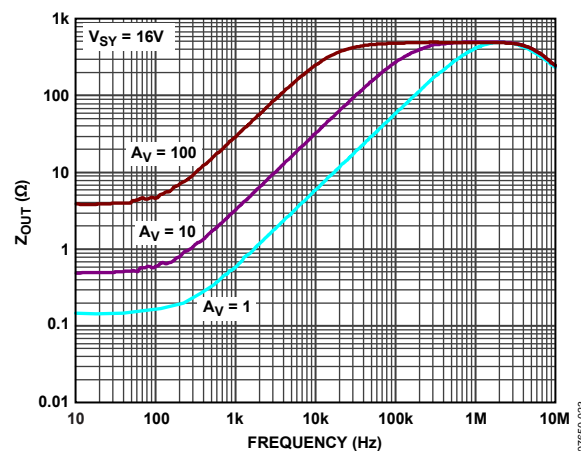


Figure 26. Output Impedance vs. Frequency

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T_A = 25°C, unless otherwise noted.

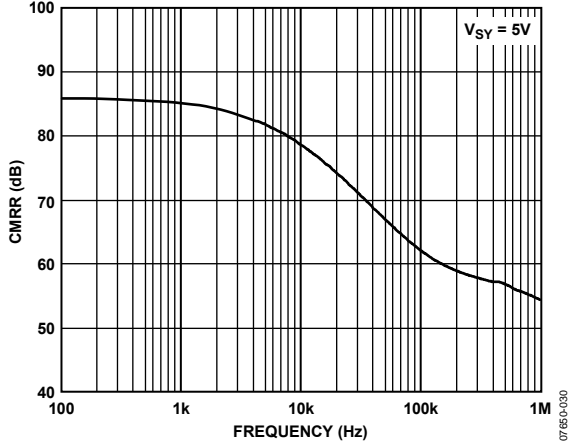


Figure 27. CMRR vs. Frequency

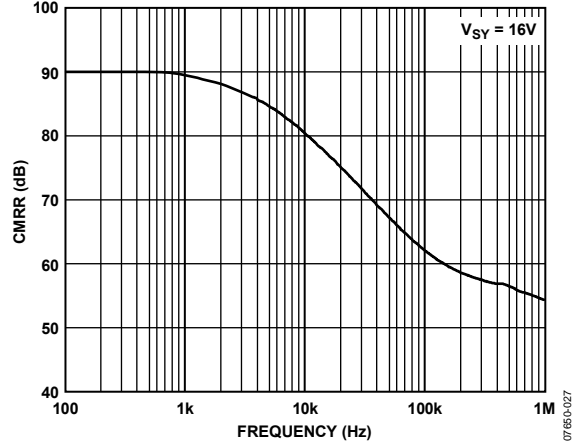


Figure 30. CMRR vs. Frequency

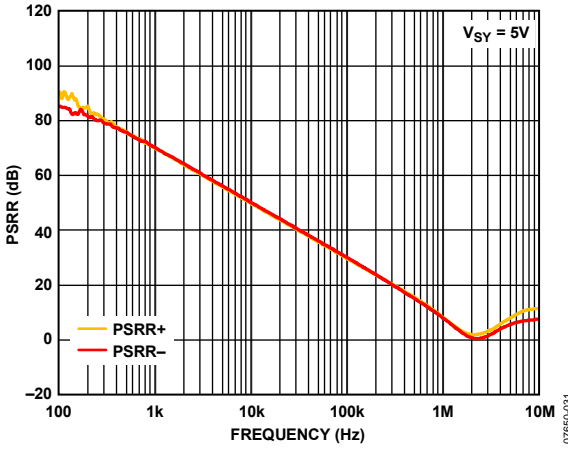


Figure 28. PSRR vs. Frequency

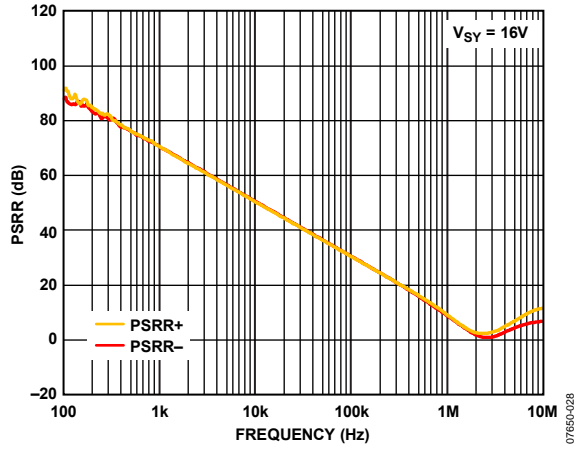


Figure 31. PSRR vs. Frequency

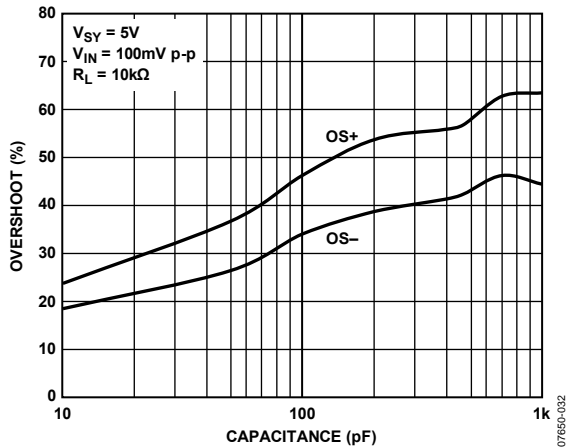


Figure 29. Small Signal Overshoot vs. Load Capacitance

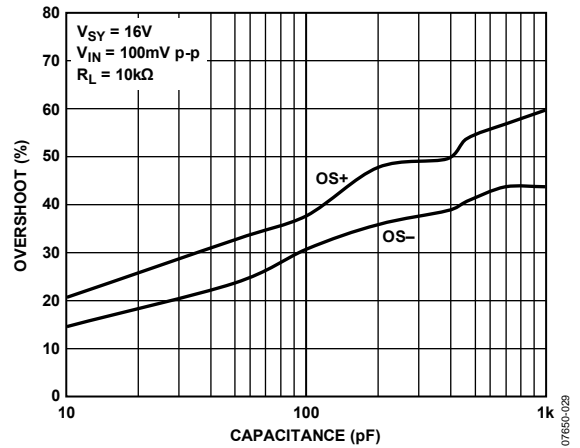


Figure 32. Small Signal Overshoot vs. Load Capacitance

T_A = 25°C, unless otherwise noted.

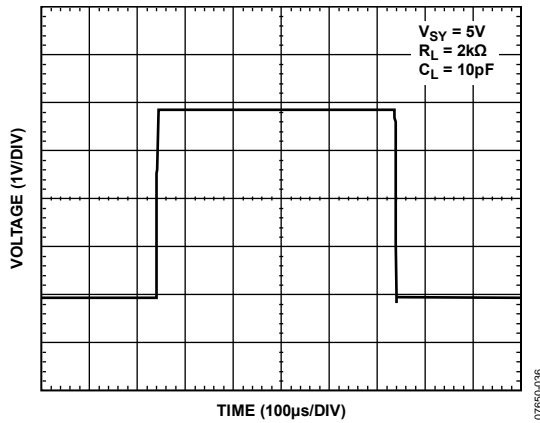


Figure 33. Large Signal Transient Response

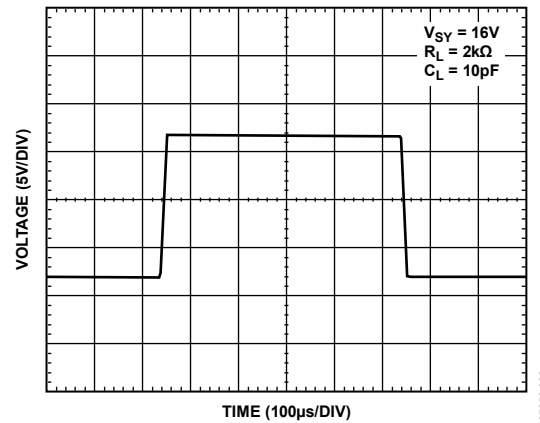


Figure 36. Large Signal Transient Response

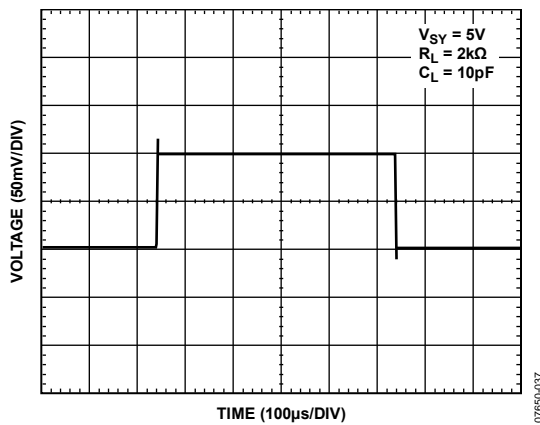


Figure 34. Small Signal Transient Response

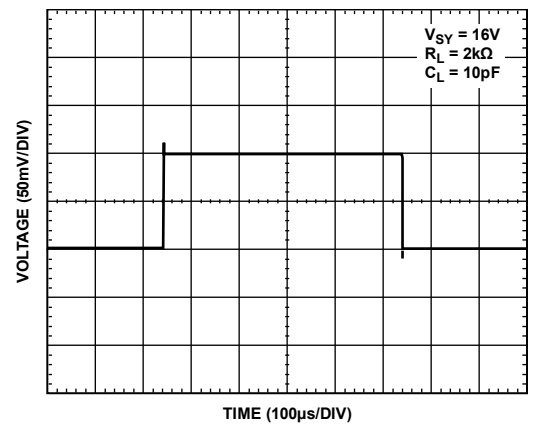


Figure 37. Small Signal Transient Response

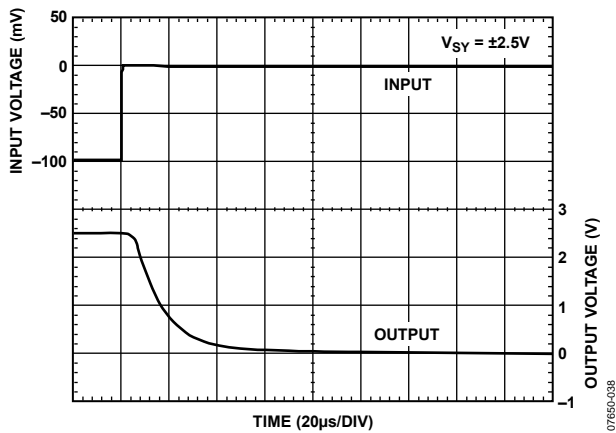


Figure 35. Positive Overload Recovery

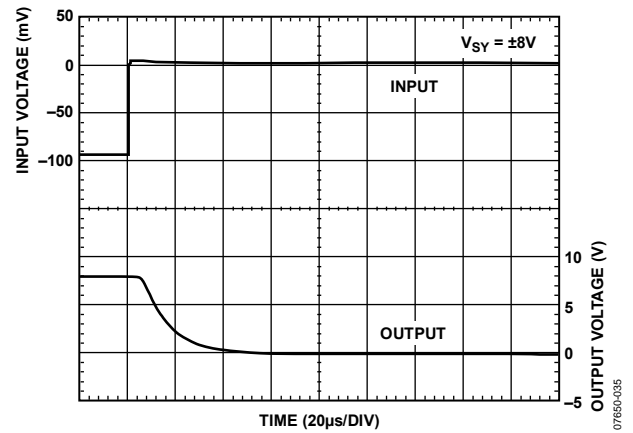


Figure 38. Positive Overload Recovery

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$T_A = 25^\circ\text{C}$, unless otherwise noted.

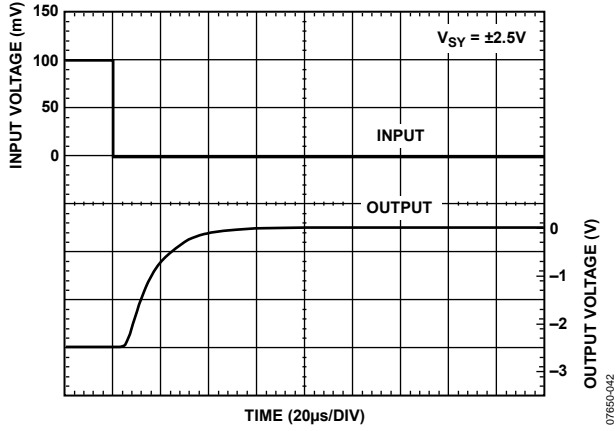


Figure 39. Negative Overload Recovery

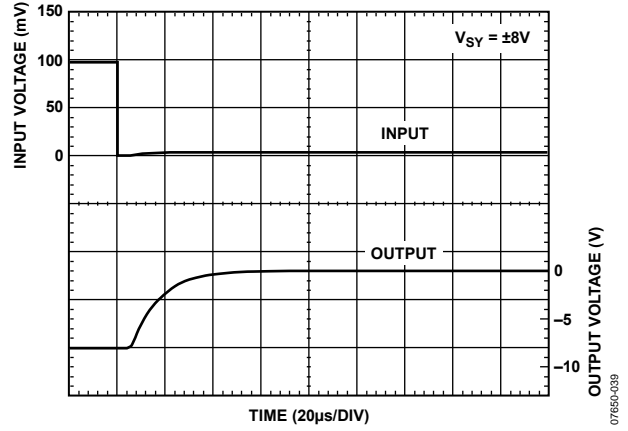


Figure 42. Negative Overload Recovery

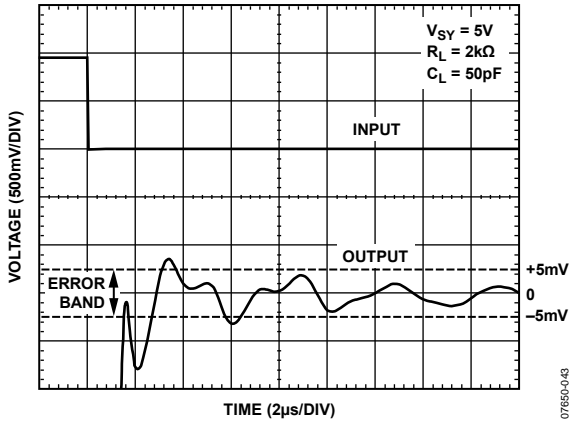


Figure 40. Negative Settling Time to 0.1%

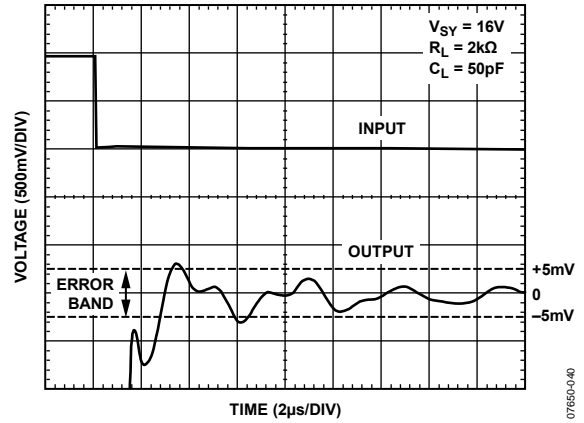


Figure 43. Negative Settling Time to 0.1%

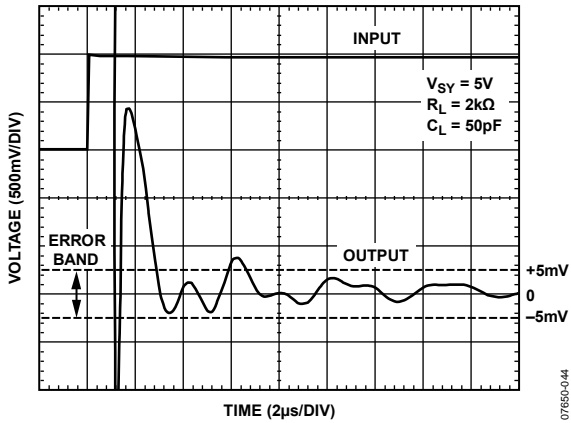


Figure 41. Positive Settling Time to 0.1%

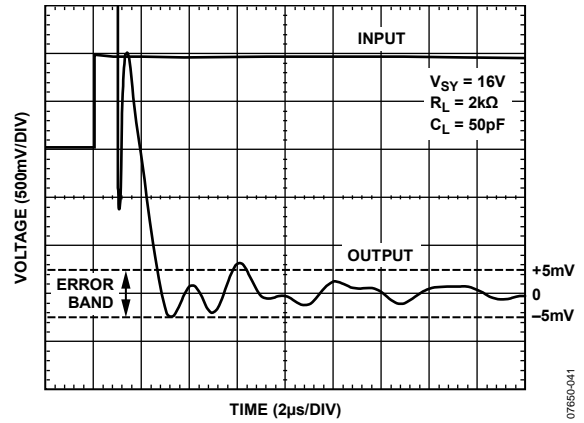


Figure 44. Positive Settling Time to 0.1%

T_A = 25°C, unless otherwise noted.

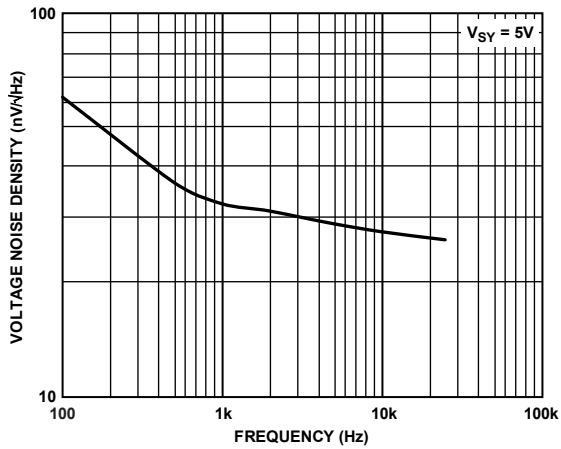


Figure 45. Voltage Noise Density vs. Frequency

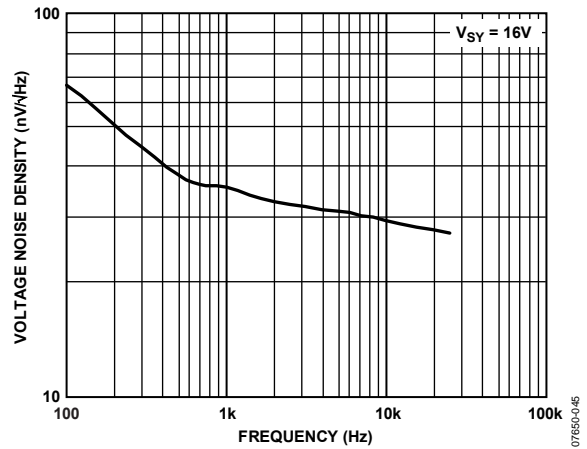


Figure 48. Voltage Noise Density vs. Frequency

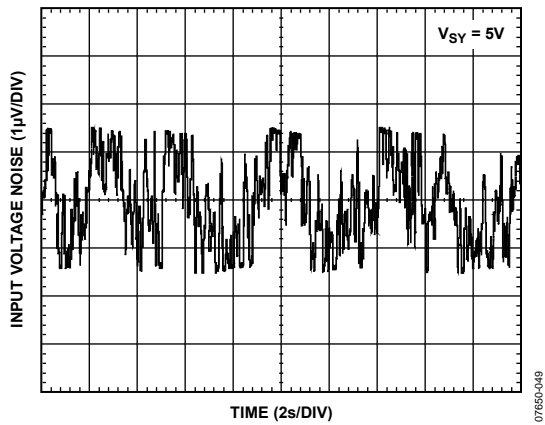


Figure 46. 0.1 Hz to 10 Hz Noise

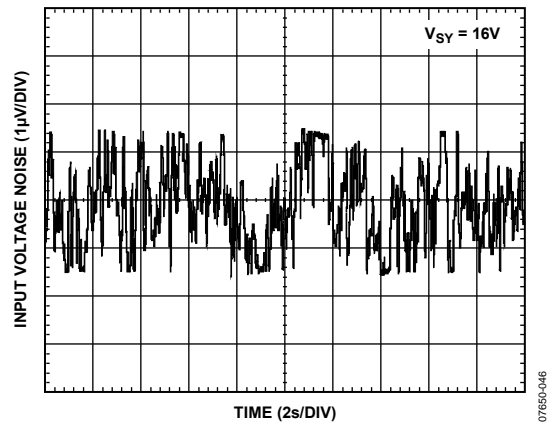


Figure 49. 0.1 Hz to 10 Hz Noise

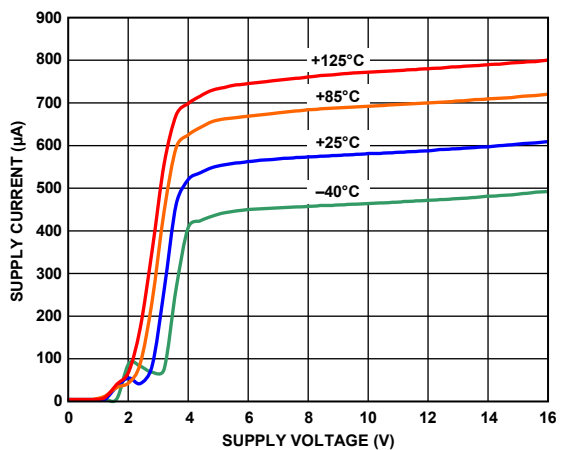


Figure 47. Supply Current vs. Supply Voltage

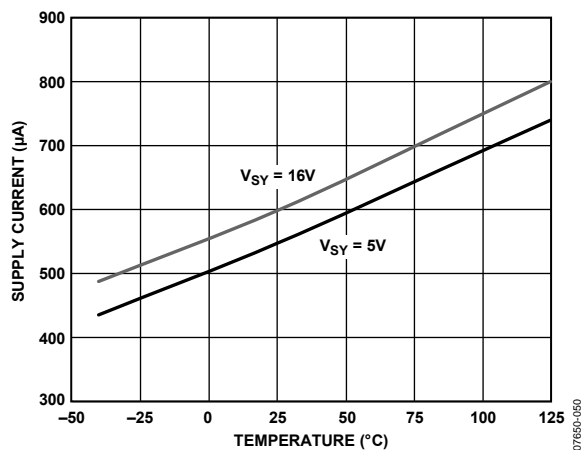


Figure 50. Supply Current vs. Temperature

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T_A = 25°C, unless otherwise noted.

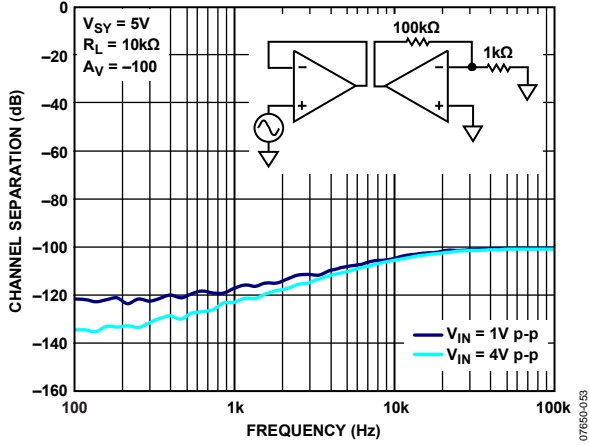


Figure 51. Channel Separation vs. Frequency

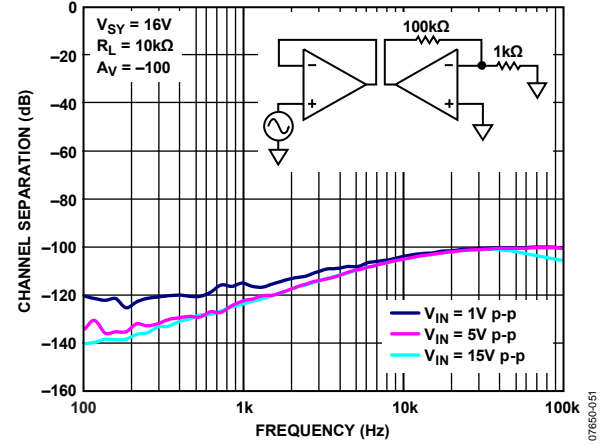


Figure 53. Channel Separation vs. Frequency

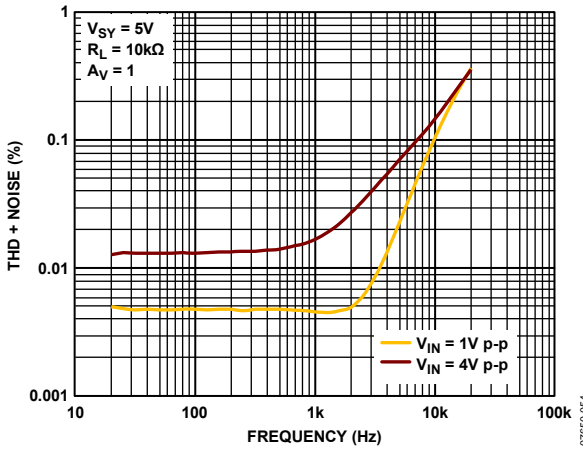


Figure 52. THD + Noise vs. Frequency

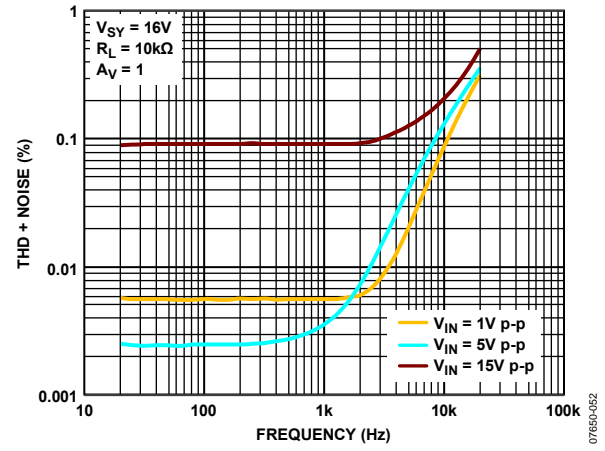


Figure 54. THD + Noise vs. Frequency

APPLICATIONS INFORMATION

RAIL-TO-RAIL INPUT OPERATION

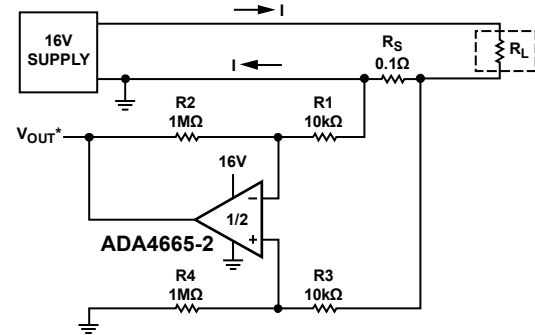
The ADA4665-2 is a unity-gain stable CMOS operational amplifier designed with rail-to-rail input/output swing capability to optimize performance. The rail-to-rail input feature is vital to maintain the wide dynamic input voltage range and to maximize signal swing to both supply rails. For example, the rail-to-rail input feature is extremely useful in buffer applications where the input voltage must cover both the supply rails.

The input stage has two input differential pairs, nMOS and pMOS. When the input common-mode voltage is at the low end of the input voltage range, the pMOS input differential pair is active and amplifies the input signal. As the input common-mode voltage is slowly increased, the pMOS differential pair gradually turns off while the nMOS input differential pair turns on. This transition is inherent to all rail-to-rail input amplifiers that use the dual differential pairs topology. For the ADA4665-2, this transition occurs approximately 1 V away from the positive rail and results in a change in offset voltage due to the different offset voltages of the differential pairs (see Figure 5 and Figure 8).

CURRENT SHUNT SENSOR

Many applications require the sensing of signals near the positive or the negative rails. Current shunt sensors are one such application and are mostly used for feedback control systems. They are also used in a variety of other applications, including power metering, battery fuel gauging, and feedback controls in electrical power steering. In such applications, it is desirable to use a shunt with very low resistance to minimize the series voltage drop. This not only minimizes wasted power, but also allows the measurement of high currents while saving power. The ADA4665-2 provides a low cost solution for implementing current shunt sensors.

Figure 55 shows a low-side current sensing circuit, and Figure 56 shows a high-side current sensing circuit using the ADA4665-2. A typical shunt resistor of 0.1 Ω is used. In these circuits, the difference amplifier amplifies the voltage drop across the shunt resistor by a factor of 100. For true difference amplification, matching of the resistor ratio is very important, where $R1/R2 = R3/R4$. The rail-to-rail feature of the ADA4665-2 allows the output of the op amp to almost reach 16 V (the power supply of the op amp). This allows the current shunt sensor to sense up to approximately 1.6 A of current.

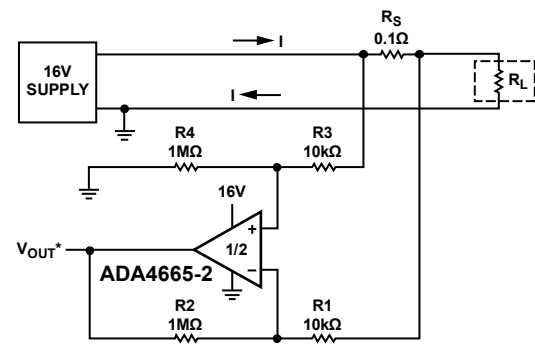


$$*V_{OUT} = \text{AMPLIFIER GAIN} \times \text{VOLTAGE ACROSS } R_S$$

$$= 100 \times R_S \times I$$

$$= 10 \times I$$

Figure 55. Low-Side Current Sensing Circuit



$$*V_{OUT} = \text{AMPLIFIER GAIN} \times \text{VOLTAGE ACROSS } R_S$$

$$= 100 \times R_S \times I$$

$$= 10 \times I$$

Figure 56. High-Side Current Sensing Circuit

ACTIVE FILTERS

The ADA4665-2 is well suited for active filter designs. An active filter requires an op amp with a unity-gain bandwidth at least 100 times greater than the product of the corner frequency, f_c , and the quality factor, Q . An example of an active filter is the Sallen-Key, one of the most widely used filter topologies. This topology gives the user the flexibility of implementing either a low-pass or a high-pass filter by simply interchanging the resistors and capacitors. To achieve the desired performance, 1% or better component tolerances are usually required.

Figure 57 shows a two-pole low-pass filter. It is configured as a unity-gain filter with cutoff frequency at 10 kHz. Resistor and capacitor values are chosen to give a quality factor, Q , of $1/\sqrt{2}$ for a Butterworth filter, which has maximally flat pass-band frequency response. Figure 58 shows the frequency response of the low-pass Sallen-Key filter. The response falls off at a rate of 40 dB per decade after the cutoff frequency of 10 kHz.

ADA4665-2

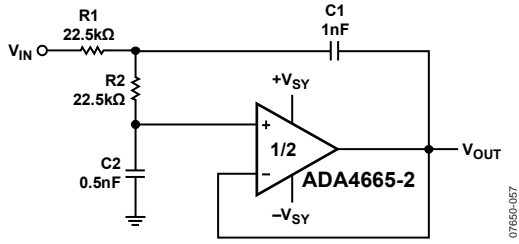


Figure 57. Two-Pole Low-Pass Filter

When $R1 = R2$ and $C1 = 2C2$, the values of Q and the cutoff frequency are calculated as follows:

$$Q = \frac{\sqrt{R1R2C1C2}}{C2(R1 + R2)}$$

$$f_c = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

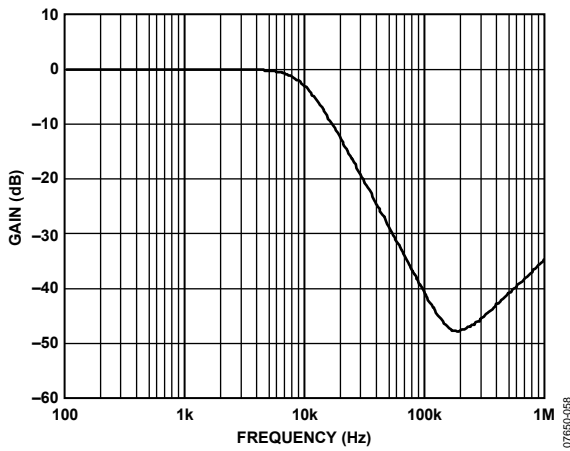


Figure 58. Low-Pass Filter: Gain vs. Frequency

Figure 59 shows a two-pole high-pass filter, with cutoff frequency at 10 kHz and quality factor, Q , of $1/\sqrt{2}$.

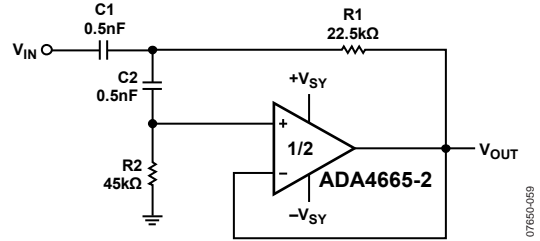


Figure 59. Two-Pole High-Pass Filter

When $R2 = 2R1$ and $C1 = C2$, the values of Q and the cutoff frequency are calculated as follows:

$$Q = \frac{\sqrt{R1R2C1C2}}{R1(C1 + C2)}$$

$$f_c = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

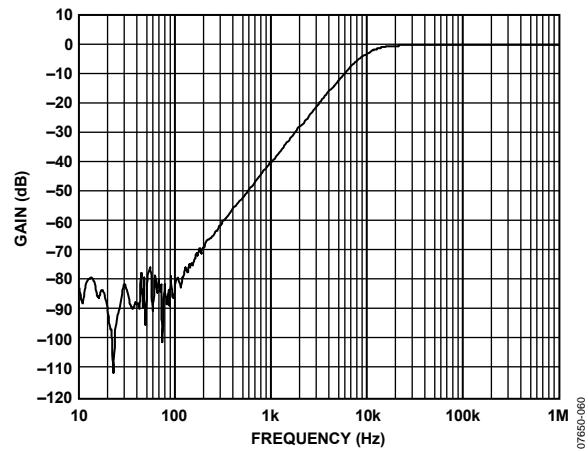
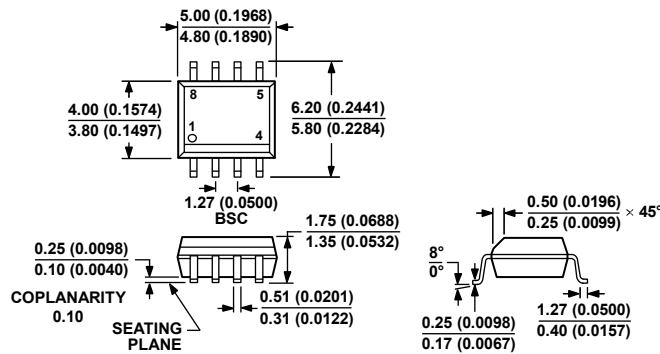


Figure 60. High-Pass Filter: Gain vs. Frequency

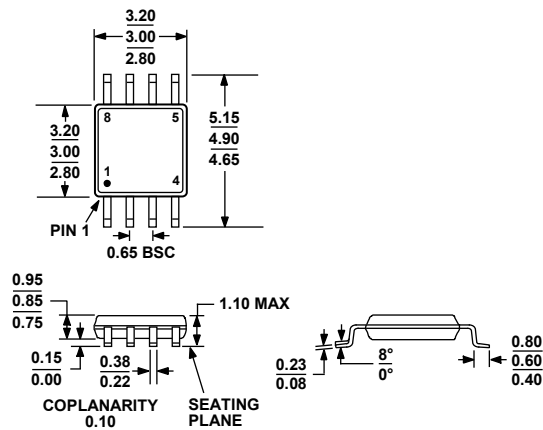
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 61. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 62. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding |
|-------------------------------|-------------------|---------------------|----------------|----------|
| ADA4665-2ARZ ¹ | -40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADA4665-2ARZ-RL ¹ | -40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADA4665-2ARZ-R7 ¹ | -40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADA4665-2ARMZ ¹ | -40°C to +125°C | 8-Lead MSOP | RM-8 | A26 |
| ADA4665-2ARMZ-R7 ¹ | -40°C to +125°C | 8-Lead MSOP | RM-8 | A26 |
| ADA4665-2ARMZ-RL ¹ | -40°C to +125°C | 8-Lead MSOP | RM-8 | A26 |

¹ Z = RoHS Compliant Part.

NOTES

NOTES