3.1 nV/√Hz, 1 mA, 180 MHz, Rail-to-Rail Input/Output Amplifiers

Data Sheet

ADA4807-1/ADA4807-2/ADA4807-4

FEATURES

Low input noise
- **3.1 nV/√Hz at f = 100 kHz with 29 Hz 1/f corner**
- **0.7 pA/√Hz at f = 100 kHz with 2 kHz 1/f corner**

High speed performance with dc precision
- **180 MHz, −3 dB bandwidth (G = +1, V_{OUT} = 20 mV p-p)**
- **225 V/µs slew rate for 5 V step (rise)**
- **47 ns settling time to 0.1% for 4 V step**
- **±125 µV and 3.7 µV/°C maximum input offset voltage and drift**
- **100 nA and 250 pA/°C maximum input offset current and drift**

Low distortion (HD2/HD3), V_S = ±5 V, V_{OUT} = 2 V p-p
- **−141 dBc/−144 dBc at 1 kHz**
- **−112 dBc/−115 dBc at 100 kHz**
- **−95 dBc/−79 dBc at 1 MHz**

Low power operation
- **1.0 mA quiescent supply current per amplifier at ±5 V**
- **Dynamic power scaling**
- **Fully specified at +3 V, +5 V, and ±5 V supplies**

Rail-to-rail inputs and outputs

APPLICATIONS

High resolution analog-to-digital converter (ADC) drivers
Portable and battery-powered instruments and systems
High component density data acquisition systems
Audio signal conditioning
Active filters

PIN CONNECTION DIAGRAMS

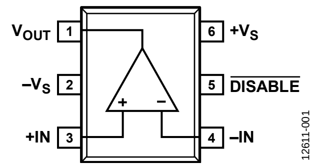

Figure 1. 6-Lead SC70 and 6-Lead SOT-23 Pin Configuration (ADA4807-1)

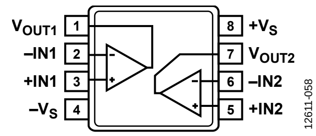

Figure 2. 8-Lead MSOP Pin Configuration (ADA4807-2)

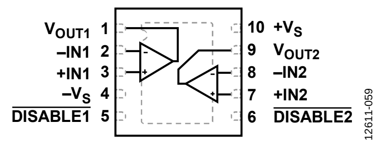

Figure 3. 10-Lead LFCSP Pin Configuration (ADA4807-2)

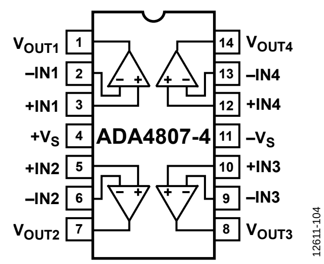

Figure 4. 14-Lead TSSOP Pin Configuration (ADA4807-4)

GENERAL DESCRIPTION

The ADA4807-1 (single), ADA4807-2 (dual), and ADA4807-4 (quad) are low noise, rail-to-rail input and output, voltage feedback amplifiers. These amplifiers combine low power, low noise, high speed, and dc precision to provide an attractive solution for a wide range of applications from high resolution data acquisition instrumentation to high performance battery-powered and high component density systems where power consumption is of key importance.

With only 1.0 mA of supply current per amplifier, the ADA4807-1/ADA4807-2/ADA4807-4 feature the lowest input voltage noise among high speed, rail-to-rail input/output amplifiers in the industry and offer a wide bandwidth, high slew rate, fast settling time, and excellent distortion performance. Additionally, these amplifiers offer very low input offset voltage and drift performance, making them ideal for driving multiplexed and high throughput precision 16-/18-bit successive approximation registers (SARs) and 24-bit Δ-Σ ADCs.

These amplifiers are fully specified at +3 V, +5 V, and ±5 V supplies and can operate over the industrial −40°C to +125°C temperature range.

The ADA4807-1 is available in 6-lead SOT-23 and space-saving 6-lead SC70 packages. The ADA4807-2 is available in an 8-lead MSOP and a compact, 3 mm × 3 mm, 10-lead LFCSP. The ADA4807-4 is available in a 14-lead TSSOP package.

Table 1. Other Rail-to-Rail Amplifiers

Device	Bandwidth (MHz)	Slew Rate (V/µs)	Voltage Noise (nV/√Hz)	Max. V_{OS} (mV)
AD8031/AD8032	80	35	15	±1.5
AD8027/AD8028	190	90	4.3	0.8
AD8029/AD8030/ AD8040	125	62	16.5	5

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Pin Connection Diagrams ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
±5 V Supply ... 3
5 V Supply ... 5
3 V Supply ... 7
Absolute Maximum Ratings ... 9
Maximum Power Dissipation ... 9
Thermal Resistance ... 9
ESD Caution ... 9
Pin Configurations and Function Descriptions ... 10
Typical Performance Characteristics ... 13
Frequency Response ... 13
Frequency and Supply Current ... 15
DC and Input Common-Mode Performance ... 16
Slew, Transient, Settling Time, and Crosstalk ... 18
Distortion and Noise ... 20
Output Characteristics ... 22
Overdrive Recovery and Turn On/Turn Off Times ... 23
Theory of Operation ... 24
Disable Circuitry ... 25
Input Protection ... 25
Noise Considerations ... 25
Applications Information ... 26
Capacitive Load Drive ... 26
Low Noise FET Operational Amplifier ... 26
Power Mode ADC Driver ... 27
ADC Driving ... 28
ADC Driving with Dynamic Power Scaling ... 29
Layout, Grounding, and Bypassing ... 30
Outline Dimensions ... 31
Ordering Guide ... 33

REVISION HISTORY

9/15—Rev. A to Rev. B

Added ADA4807-4 ... Universal
Changes to Features Section, General Description Section, and Table 1 ... 1
Added Figure 4, Renumbered Sequentially ... 1
Changes to Table 2 ... 3
Changes to Table 3 ... 5
Changes to Table 4 ... 7
Deleted Figure 6, Renumbered Sequentially ... 10
Changes to Figure 6 ... 10
Added Figure 9 and Table 9, Renumbered Sequentially ... 12
Changes to Figure 20 ... 14
Added Figure 21 ... 14
Added Figure 31 and Figure 32 ... 16
Added Figure 35 ... 17
Changes to Figure 39 ... 18
Added Figure 42 ... 19
Deleted Figure 50, Figure 51, Figure 53, and Figure 54 ... 19
Added Figure 46 ... 20
Added Figure 49 and Figure 51 ... 21
Added Figure 59 and Figure 61 ... 23
Changes to $\overline{\text{DISABLE}}$ Circuitry Section ... 25
Added Low Noise FET Operational Amplifier Section ... 26
Added Figure 70, Figure 71, Figure 72, and Power Mode ADC Driver Section ... 27
Added ADC Driving Section and Figure 73 through Figure 77 ... 28
Added ADC Driving with Dynamic Power Scaling Section, Figure 78, Figure 79, and Figure 80 ... 29
Added Figure 58 ... 33
Changes to Ordering Guide ... 33

4/15—Rev. 0 to Rev. A

Added ADA4807-2 ... Universal
Changes to Features Section, General Description Section, and Pin Connection Diagrams Heading ... 1
Added Figure 2 and Figure 3; Renumbered Sequentially ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 5
Changes to Table 3 ... 7
Changes to Table 6 and Figure 4 ... 9
Added Figure 7, Figure 8, and Table 8; Renumbered Sequentially ... 11
Reorganized Layout, Typical Performance Characteristics Section ... 12
Added Figure 36 ... 16
Changes to Figure 37 Caption, Figure 38 Caption, Figure 39 Caption, and Figure 40 Caption ... 17
Changes to Figure 44 and Figure 47 ... 18
Change to Theory of Operation Section ... 20
Changes to $\overline{\text{DISABLE}}$ Circuitry Section, Table 9, and Noise Considerations Section ... 21
Added Figure 65 and Figure 66 ... 23
Changes to Ordering Guide ... 25

12/14—Revision 0: Initial Version

SPECIFICATIONS

±5 V SUPPLY

T_A = 25°C, V_S = ±5 V, R_{LOAD} = 1 kΩ to midsupply, R_F = 0 Ω, G = +1, $-V_S \le V_{ICM} \le +V_S - 1.5$ V, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 20 mV p-p		180		MHz
	G = +1, V_{OUT} = 2 V p-p		28		MHz
Slew Rate	G = +1, V_{OUT} = 5 V step, 20% to 80%, rise/fall		225/250		V/µs
Settling Time to 0.1%	G = +1, V_{OUT} = 4 V step		47		ns
DISTORTION/NOISE PERFORMANCE					
Second Harmonic (HD2)	f_C = 1 kHz, V_{OUT} = 2 V p-p		−141		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−112		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p, ADA4807-1		−95		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p, ADA4807-2, ADA4807-4		−84		dBc
Third Harmonic (HD3)	f_C = 1 kHz, V_{OUT} = 2 V p-p		−144		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−115		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p		−79		dBc
Peak-to-Peak Noise	f = 0.1 Hz to 10 Hz		160		nV p-p
Input Voltage Noise	f = 100 kHz		3.1		nV/√Hz
	f = 1 kHz		3.3		nV/√Hz
	f = 10 Hz		5.8		nV/√Hz
Input Voltage Noise 1/f Corner			29		Hz
Input Current Noise	f = 100 kHz		0.7		pA/√Hz
	f = 10 Hz		10		pA/√Hz
Input Current Noise 1/f Corner			2		kHz
DC PERFORMANCE					
Input Offset Voltage					
$-V_S \le V_{ICM} \le +V_S - 1.5$ V	ADA4807-1, ADA4807-2	−125	±20	+125	µV
	ADA4807-4	−175	±20	+175	µV
$+V_S - 1.5$ V $\le V_{ICM} \le +V_S$	ADA4807-1, ADA4807-2	−750	±140	+750	µV
	ADA4807-4	−850	±140	+850	µV
Input Offset Voltage Drift	$-V_S \le V_{ICM} \le +V_S - 1.2$ V, T_{MIN} to T_{MAX}		0.7	3.7	µV/°C
Input Bias Current	$-V_S \le V_{ICM} \le +V_S - 1.5$ V		−1.2	−1.6	µA
	$+V_S - 1.5$ V $\le V_{ICM} \le +V_S$		530	1000	nA
Input Bias Current Drift	$-V_S \le V_{ICM} \le +V_S - 1.2$ V, T_{MIN} to T_{MAX}		2.5	3.6	nA/°C
Input Offset Current	$-V_S \le V_{ICM} \le +V_S - 1.5$ V		8	100	nA
	$+V_S - 1.5$ V $\le V_{ICM} \le +V_S$		25	150	nA
Input Offset Current Drift	$-V_S \le V_{ICM} \le +V_S - 1.2$ V, T_{MIN} to T_{MAX}		30	250	pA/°C
Open-Loop Gain		120	130		dB
INPUT CHARACTERISTICS					
Common-Mode Input Resistance			45		MΩ
Differential Input Resistance			35		kΩ
Common-Mode Input Capacitance			1		pF
Differential Input Capacitance			1		pF
Input Common-Mode Voltage Range		$-V_S - 0.2$		$+V_S + 0.2$	V
Common-Mode Rejection Ratio (CMRR)	V_{ICM} = −3 V to +2 V	96	110		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
$\overline{\text{DISABLE}}$ CHARACTERISTICS[1]					
$\overline{\text{DISABLE}}$ Input Voltage[2]					
Low	Disabled		<1.3		V
High	Enabled		>1.7		V
$\overline{\text{DISABLE}}$ Input Current					
Low	Disabled		−470		nA
High	Enabled		−3		nA
$\overline{\text{DISABLE}}$ On Time	$\overline{\text{DISABLE}}$ input midswing point to >90% of final V_{OUT}, $V_{PD} = +V_S$		1.3	1.8	µs
$\overline{\text{DISABLE}}$ Off Time	$\overline{\text{DISABLE}}$ input midswing point to <10% of enabled quiescent current, $V_{PD} = -V_S$		270	340	ns
OUTPUT CHARACTERISTICS					
Saturated Output Voltage Swing	$R_{LOAD} = 1\ k\Omega$				
High		$+V_S - 0.08$	$+V_S - 0.04$		V
Low		$-V_S + 0.1$	$-V_S + 0.07$		V
Linear Output Current[3]	Sourcing, G = +1, $V_{IN} = +V_S$, R_{LOAD} = varied		50		mA
	Sinking, G = +1, $V_{IN} = -V_S$, R_{LOAD} = varied		60		mA
Short-Circuit Current	Sourcing, G = +1, $V_{IN} = +V_S$, $R_{LOAD} = 0\ \Omega$ to $10\ \Omega$		80		mA
	Sinking, G= +1, $V_{IN} = -V_S$, $R_{LOAD} = 0\ \Omega$ to $10\ \Omega$		80		mA
Capacitive Load Drive	C_{LOAD} = 15 pF, V_{OUT} = 20 mV p-p		17		% overshoot
POWER SUPPLY					
Operating Range		2.7		11	V
Quiescent Current per Amplifier	Enabled, no load, T_A = 25°C		1.0	1.1	mA
	Disabled, T_A = 25°C		2.4	4.0	µA
Power Supply Rejection Ratio (PSRR)					
Positive	$+V_S$ = 3 V to 5 V, $-V_S$ = −5 V	98	107		dB
Negative	$+V_S$ = 5 V, $-V_S$ = −3 V to −5 V	98	120		dB

[1] The disable pin is $\overline{\text{DISABLE}}$ on the ADA4807-1 and $\overline{\text{DISABLE1}}$ or $\overline{\text{DISABLE2}}$ for the ADA4807-2 LFCSP package, hereafter referred to as $\overline{\text{DISABLE}}$ for the ADA4807-1/ADA4807-2.
[2] See the Disable Circuitry section.
[3] See Figure 53 and Figure 56.

5 V SUPPLY

T_A = 25°C, V_S = 5 V, R_{LOAD} = 1 kΩ to midsupply, R_F = 0 Ω, G = +1, 0 V ≤ V_{ICM} ≤ +V_S − 1.5 V, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 20 mV p-p		170		MHz
	G = +1, V_{OUT} = 2 V p-p		28		MHz
Slew Rate	G = +1, V_{OUT} = 2 V step, 20% to 80%, rise/fall		145/160		V/µs
Settling Time to 0.1%	G = +1, V_{OUT} = 2 V step		40		ns
DISTORTION/NOISE PERFORMANCE					
Second Harmonic (HD2)	f_C = 1 kHz, V_{OUT} = 2 V p-p		−141		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−111		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p, ADA4807-1		−93		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p, ADA4807-2, ADA4807-4		−83		dBc
Third Harmonic (HD3)	f_C = 1 kHz, V_{OUT} = 2 V p-p		−153		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−115		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p		−78		dBc
Peak-to-Peak Noise	f = 0.1 Hz to 10 Hz		160		nV p-p
Input Voltage Noise	f = 100 kHz		3.1		nV/√Hz
	f = 1 kHz		3.3		nV/√Hz
	f = 10 Hz		5.8		nV/√Hz
Input Voltage Noise 1/f Corner			29		Hz
Input Current Noise	f = 100 kHz		0.7		pA/√Hz
	f = 10 Hz		10		pA/√Hz
Input Current Noise 1/f Corner			2		kHz
DC PERFORMANCE					
Input Offset Voltage					
0 V ≤ V_{ICM} ≤ +V_S − 1.5 V	ADA4807-1, ADA4807-2	−125	±20	+125	µV
	ADA4807-4	−175	±20	+175	µV
+V_S − 1.5 V ≤ V_{ICM} ≤ +V_S	ADA4807-1, ADA4807-2	−720	±110	+720	µV
	ADA4807-4	−850	±110	+850	µV
Input Offset Voltage Drift	0 V ≤ V_{ICM} ≤ +V_S − 1.2 V, T_{MIN} to T_{MAX}		0.7	3.7	µV/°C
Input Bias Current	0 V ≤ V_{ICM} ≤ +V_S − 1.5 V		−1.2	−2.0	µA
	+V_S − 1.5 V ≤ V_{ICM} ≤ +V_S		500	1000	nA
Input Bias Current Drift	0 V ≤ V_{ICM} ≤ +V_S − 1.2 V, T_{MIN} to T_{MAX}		2.6	3.8	nA/°C
Input Offset Current	0 V ≤ V_{ICM} ≤ +V_S − 1.5 V		8	100	nA
	+V_S − 1.5 V ≤ V_{ICM} ≤ +V_S		25	150	nA
Input Offset Current Drift	0 V ≤ V_{ICM} ≤ +V_S − 1.2 V, T_{MIN} to T_{MAX}		30	250	pA/°C
Open-Loop Gain		113	130		dB
INPUT CHARACTERISTICS					
Common-Mode Input Resistance			45		MΩ
Differential Input Resistance			35		kΩ
Common-Mode Input Capacitance			1		pF
Differential Input Capacitance			1		pF
Input Common-Mode Voltage Range		−V_S − 0.2		+V_S + 0.2	V
CMRR	V_{ICM} = 1 V to 3 V	96	110		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
$\overline{\text{DISABLE}}$ CHARACTERISTICS[1]					
$\overline{\text{DISABLE}}$ Input Voltage[2]					
Low	Disabled		<1.3		V
High	Enabled		>1.8		V
$\overline{\text{DISABLE}}$ Input Current					
Low	Disabled		−360		nA
High	Enabled		−1.3		nA
$\overline{\text{DISABLE}}$ On Time	$\overline{\text{DISABLE}}$ input midswing point to >90% of final V_{OUT}, $V_{PD} = +V_S$		450	700	ns
$\overline{\text{DISABLE}}$ Off Time	$\overline{\text{DISABLE}}$ input midswing point to <10% of enabled quiescent current, $V_{PD} = −V_S$		270	450	ns
OUTPUT CHARACTERISTICS					
Saturated Output Voltage Swing	R_{LOAD} = 1 kΩ				
High		$+V_S − 0.05$	$+V_S − 0.03$		V
Low		$−V_S + 0.05$	$−V_S + 0.04$		V
Linear Output Current[3]	Sourcing, G = +1, $V_{IN} = +V_S$, R_{LOAD} = varied		50		mA
	Sinking, G = +1, $V_{IN} = −V_S$, R_{LOAD} = varied		60		mA
Short-Circuit Current	Sourcing, G = +1, $V_{IN} = +V_S$, R_{LOAD} = 0 Ω to 10 Ω		80		mA
	Sinking, G = +1, $V_{IN} = −V_S$, R_{LOAD} = 0 Ω to 10 Ω		80		mA
Capacitive Load Drive	C_{LOAD} = 15 pF, V_{OUT} = 20 mV p-p		24		% overshoot
POWER SUPPLY					
Operating Range		2.7		11	V
Quiescent Current per Amplifier	Enabled, no load, T_A = 25°C		950	1000	μA
	Disabled, T_A = 25°C		1.3	2.0	μA
PSRR					
Positive	$+V_S$ = 1.5 V to 3.5 V, $−V_S$ = −2.5 V	98	115		dB
Negative	$+V_S$ = 2.5 V, $−V_S$ = −1.5 V to −3.5 V	98	130		dB

[1] The disable pin is $\overline{\text{DISABLE}}$ on the ADA4807-1 and $\overline{\text{DISABLE1}}$ or $\overline{\text{DISABLE2}}$ for the ADA4807-2 LFCSP package, hereafter referred to as $\overline{\text{DISABLE}}$ for the ADA4807-1/ADA4807-2.
[2] See the Disable Circuitry section.
[3] See Figure 53 and Figure 56.

3 V SUPPLY

T_A = 25°C, V_S = 3 V, R_{LOAD} = 1 kΩ to midsupply, R_F = 0 Ω, G = +1, 0 V ≤ V_{ICM} ≤ +V_S − 1.5 V, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	G = +1, V_{OUT} = 20 mV p-p		165		MHz
	G = +1, V_{OUT} = 2 V p-p		28		MHz
Slew Rate	G = +1, V_{OUT} = 2 V step, 20% to 80%, rise/fall		118/237		V/µs
Settling Time to 0.1%	G = +1, V_{OUT} = 2 V step		40		ns
DISTORTION/NOISE PERFORMANCE					
Second Harmonic (HD2)	f_C = 1 kHz, V_{OUT} = 2 V p-p		−98		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−85		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p		−65		dBc
Third Harmonic (HD3)	f_C = 1 kHz, V_{OUT} = 2 V p-p		−94		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−91		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p		−68		dBc
Peak-to-Peak Noise	f = 0.1 Hz to 10 Hz		160		nV p-p
Input Voltage Noise	f = 100 kHz		3.1		nV/√Hz
	f = 10 kHz		3.3		nV/√Hz
	f = 10 Hz		5.8		nV/√Hz
Input Voltage Noise 1/f Corner			29		Hz
Input Current Noise	f = 100 kHz		0.7		pA/√Hz
	f = 10 Hz		10		pA/√Hz
Input Current Noise 1/f Corner			2		kHz
DC PERFORMANCE					
Input Offset Voltage					
0 V ≤ V_{ICM} ≤ +V_S − 1.5 V	ADA4807-1, ADA4807-2	−125	±20	+125	µV
	ADA4807-4	−175	±20	+175	µV
+V_S − 1.5 V ≤ V_{ICM} ≤ +V_S	ADA4807-1, ADA4807-2	−720	±125	+720	µV
	ADA4807-4	−850	±125	+850	µV
Input Offset Voltage Drift	0 V ≤ V_{ICM} ≤ +V_S − 1.2 V, T_{MIN} to T_{MAX}		0.7	3.8	µV/°C
Input Bias Current	0 V ≤ V_{ICM} ≤ +V_S − 1.5 V		−1.2	−2.0	µA
	+V_S − 1.5 V ≤ V_{ICM} ≤ +V_S		500	1000	nA
Input Bias Current Drift	0 V ≤ V_{ICM} ≤ +V_S − 1.2 V, T_{MIN} to T_{MAX}		2.7	3.8	nA/°C
Input Offset Current	0 V ≤ V_{ICM} ≤ +V_S − 1.5 V		8	130	nA
	+V_S − 1.5 V ≤ V_{ICM} ≤ +V_S		25	150	nA
Input Offset Current Drift	0 V ≤ V_{ICM} ≤ +V_S − 1.2 V, T_{MIN} to T_{MAX}		40	230	pA/°C
Open-Loop Gain		104	113		dB
INPUT CHARACTERISTICS					
Common-Mode Input Resistance			45		MΩ
Differential Input Resistance			35		kΩ
Common-Mode Input Capacitance			1		pF
Differential Input Capacitance			1		pF
Input Common-Mode Voltage Range		−V_S − 0.2		+V_S + 0.2	V
CMRR	V_{ICM} = 0.3 V to 1.3 V	92	110		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DISABLE CHARACTERISTICS[1]					
DISABLE Input Voltage[2]					
Low	Disabled		<1.1		V
High	Enabled		>1.5		V
DISABLE Input Current					
Low	Disabled		−325		nA
High	Enabled		−500		nA
DISABLE On Time	DISABLE input midswing point to >90% of final V_{OUT}, $V_{PD} = +V_S$		500	700	ns
DISABLE Off Time	DISABLE input midswing point to <10% of enabled quiescent current, $V_{PD} = -V_S$		270	460	ns
OUTPUT CHARACTERISTICS					
Saturated Output Voltage Swing	$R_{LOAD} = 1\ k\Omega$				
High		$+V_S - 0.04$	$+V_S - 0.02$		V
Low		$-V_S + 0.04$	$-V_S + 0.03$		V
Linear Output Current[3]	Sourcing, G = +1, $V_{IN} = +V_S$, R_{LOAD} = varied		50		mA
	Sinking, G = +1, $V_{IN} = -V_S$, R_{LOAD} = varied		60		mA
Short-Circuit Current	Sourcing, G = +1, $V_{IN} = +V_S$, $R_{LOAD} = 0\ \Omega$ to $10\ \Omega$		65		mA
	Sinking, G = +1, $V_{IN} = -V_S$, $R_{LOAD} = 0\ \Omega$ to $10\ \Omega$		70		mA
Capacitive Load Drive	C_{LOAD} = 15 pF, V_{OUT} = 20 mV p-p		30		% overshoot
POWER SUPPLY					
Operating Range		2.7		11	V
Quiescent Current per Amplifier	Enabled, no load, T_A = 25°C		915	1000	µA
	Disabled, T_A = 25°C		1.0	2.0	µA
PSRR					
Positive	$+V_S$ = 1.5 V to 3.5 V, $-V_S$ = −1.5 V	97	113		dB
Negative	$+V_S$ = 1.5 V, $-V_S$ = −1.5 V to −3.5 V	97	130		dB

[1] The disable pin is DISABLE on the ADA4807-1 and DISABLE1 or DISABLE2 for the ADA4807-2 LFCSP package, hereafter referred to as DISABLE for the ADA4807-1/ADA4807-2.
[2] See the Disable Circuitry section.
[3] See Figure 53 and Figure 56.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	11 V
Internal Power Dissipation	See Figure 5
Input Voltage (Common Mode)	$\pm V_S \pm 0.2$ V
Differential Input Voltage	±1.4 V
Output Short-Circuit Duration	See power derating curves in Figure 5
Storage Temperature Range (All Packages)	−65°C to +125°C
Lead Temperature (Soldering 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the ADA4807-1/ADA4807-2/ADA4807-4 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily can cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

Although the ADA4807-1/ADA4807-2/ADA4807-4 are internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the power derating curves shown in Figure 5.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
6-Lead SC70, 4-Layer Board	209	°C/W
6-Lead SOT-23, 4-Layer Board	223	°C/W
8-Lead MSOP	123	°C/W
10-Lead LFCSP	51	°C/W
14-Lead TSSOP	130	°C/W

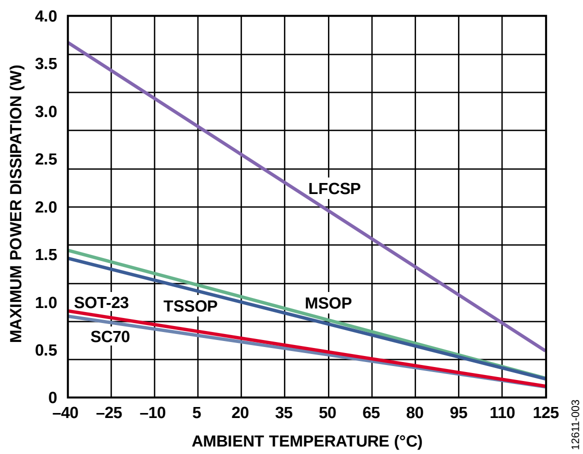

Figure 5. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

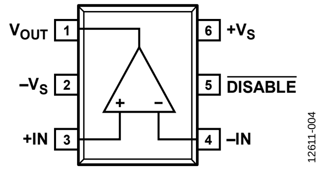

Figure 6. ADA4807-1 Pin Configuration

Table 7. ADA4807-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OUT}	Output
2	$-V_S$	Negative Supply
3	+IN	Noninverting Input
4	−IN	Inverting Input
5	$\overline{\text{DISABLE}}$	Active Low Power-Down
6	$+V_S$	Positive Supply

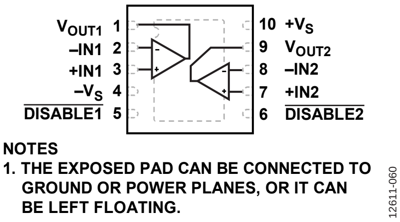

Figure 7. ADA4807-2 10-Lead LFCSP Pin Configuration

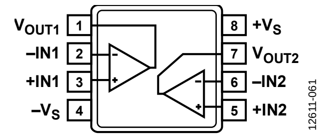

Figure 8. ADA4807-2 8-Lead MSOP Pin Configuration

Table 8. ADA4807-2 Pin Function Descriptions

Pin No.			
10-Lead LFCSP	**8-Lead MSOP**	**Mnemonic**	**Description**
1	1	V_{OUT1}	Output 1.
2	2	−IN1	Inverting Input 1.
3	3	+IN1	Noninverting Input 1.
4	4	$-V_S$	Negative Supply.
5	Not applicable	$\overline{\text{DISABLE1}}$	Active Low Power-Down 1.
6	Not applicable	$\overline{\text{DISABLE2}}$	Active Low Power-Down 2.
7	5	+IN2	Noninverting Input 2.
8	6	−IN2	Inverting Input 2.
9	7	V_{OUT2}	Output 2.
10	8	$+V_S$	Positive Supply.
	Not applicable	EPAD	Exposed Pad. For the 10-Lead LFCSP, the exposed pad can be connected to ground or power planes, or it can be left floating.

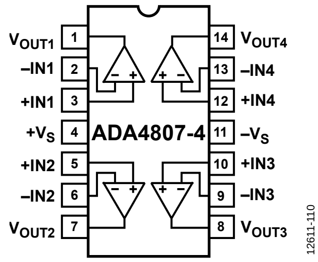

Figure 9. ADA4807-4 Pin Configuration

Table 9. ADA4807-4 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OUT1}	Output 1
2	−IN1	Inverting Input 1
3	+IN1	Noninverting Input 1
4	$+V_S$	Positive Supply
5	+IN2	Noninverting Input 2
6	−IN2	Inverting Input 2
7	V_{OUT2}	Output 2
8	V_{OUT3}	Output 3
9	−IN3	Inverting Input 3
10	+IN3	Noninverting Input 3
11	$-V_S$	Negative Supply
12	+IN4	Noninverting Input 4
13	−IN4	Inverting Input 4
14	V_{OUT4}	Output 4

TYPICAL PERFORMANCE CHARACTERISTICS

FREQUENCY RESPONSE

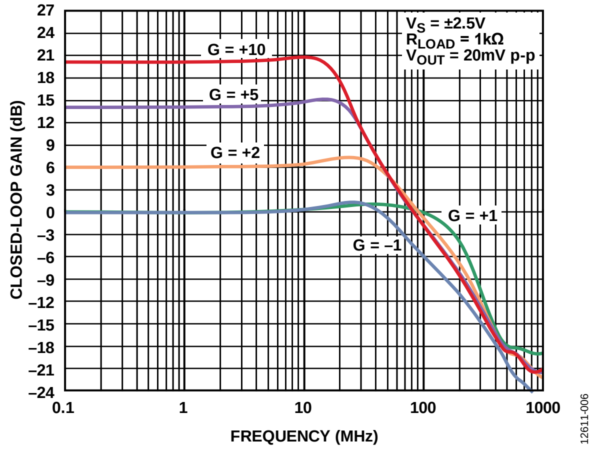

Figure 10. Small Signal Frequency Response for Various Gains, R_F = 499 Ω

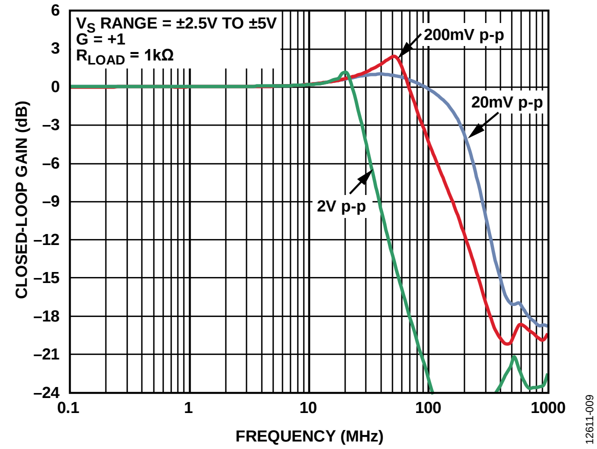

Figure 13. Frequency Response for Various Output Amplitudes, G = +1

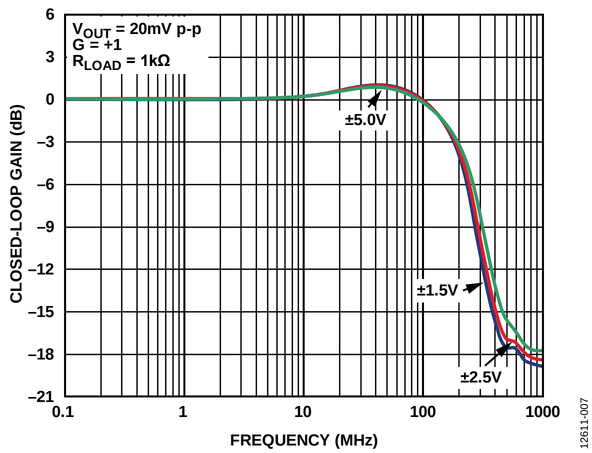

Figure 11. Small Signal Frequency Response for Various Supplies

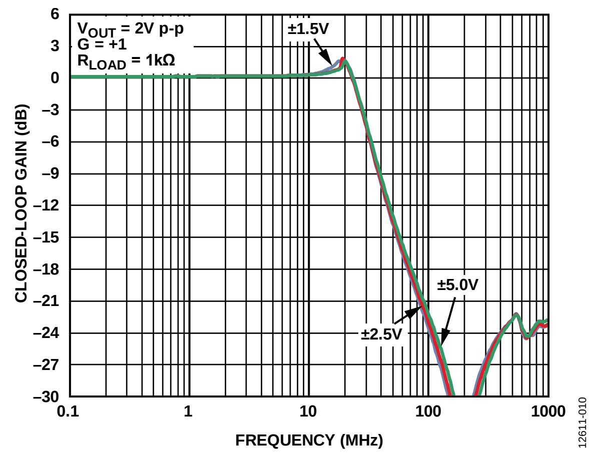

Figure 14. Large Signal Frequency Response for Various Supplies

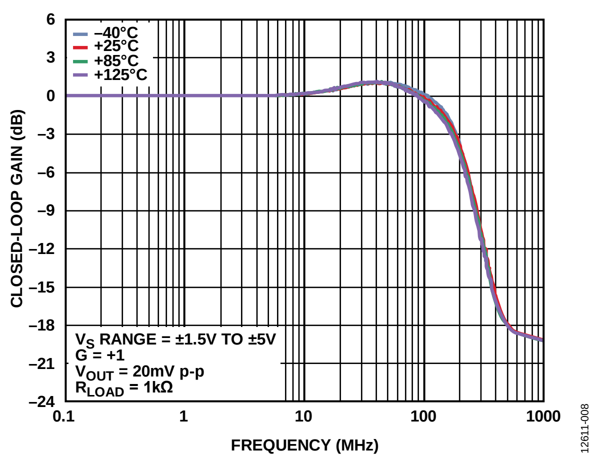

Figure 12. Small Signal Frequency Response for Various Temperatures

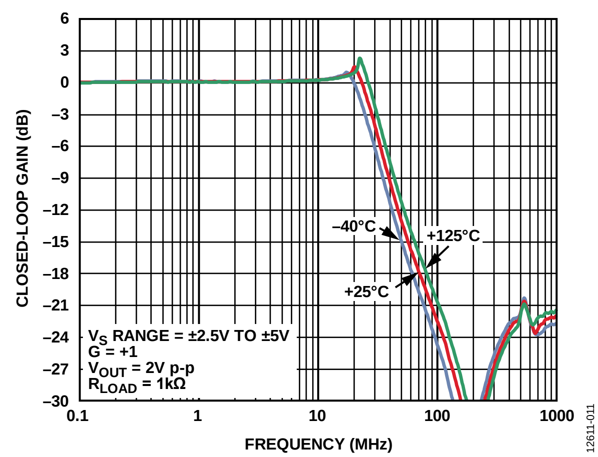

Figure 15. Large Signal Frequency Response for Various Temperatures

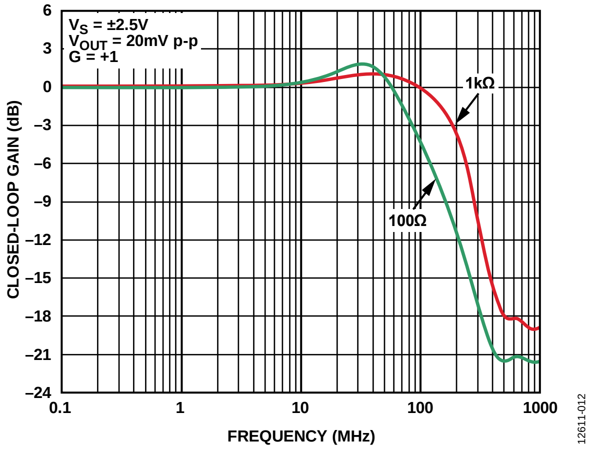

Figure 16. Small Signal Frequency Response for Various Resistive Loads

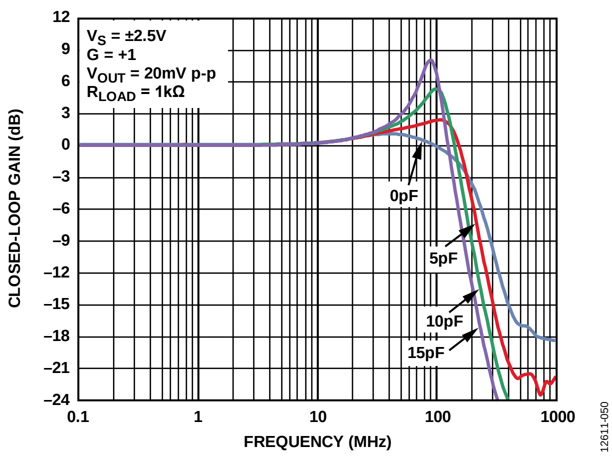

Figure 17. Small Signal Frequency Response for Various Capacitive Loads

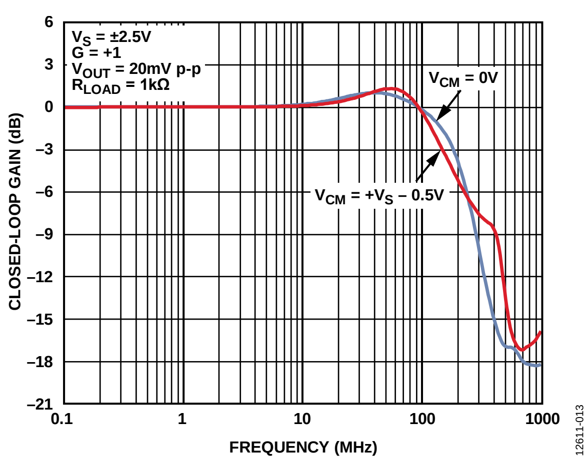

Figure 18. Small Signal Frequency Response for Various Input Common-Mode Voltages (V_{CM})

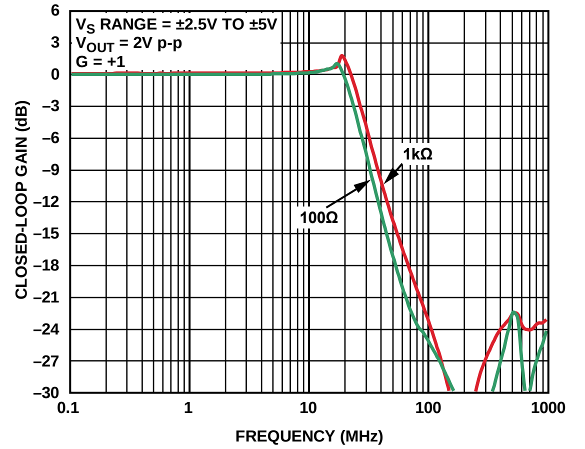

Figure 19. Large Signal Frequency Response for Various Resistive Loads

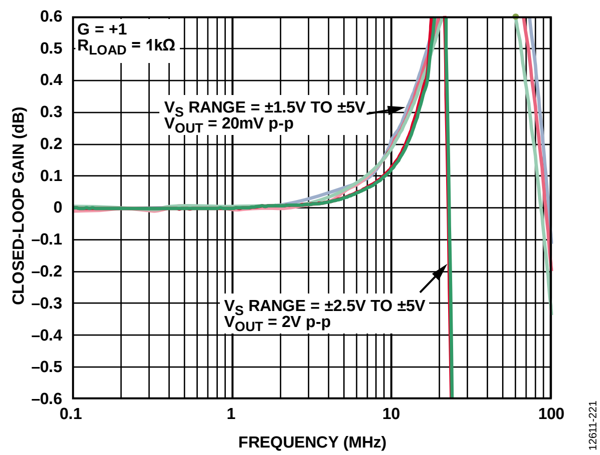

Figure 20. 0.1 dB Flatness Frequency Response for Various Output Amplitudes

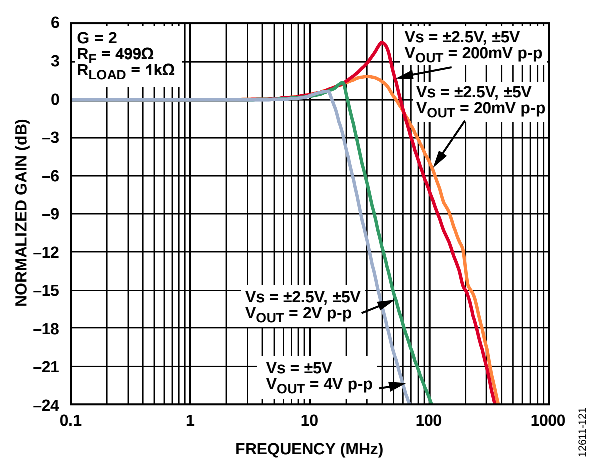

Figure 21. Frequency Response for Various Output Amplitudes, G = +2

FREQUENCY AND SUPPLY CURRENT

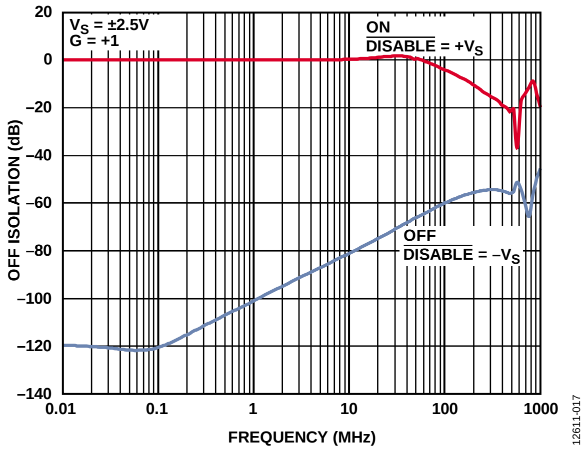

Figure 22. Off Isolation vs. Frequency

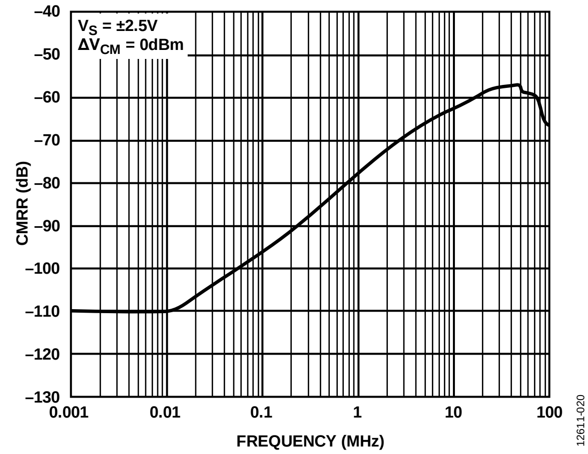

Figure 25. CMRR vs. Frequency

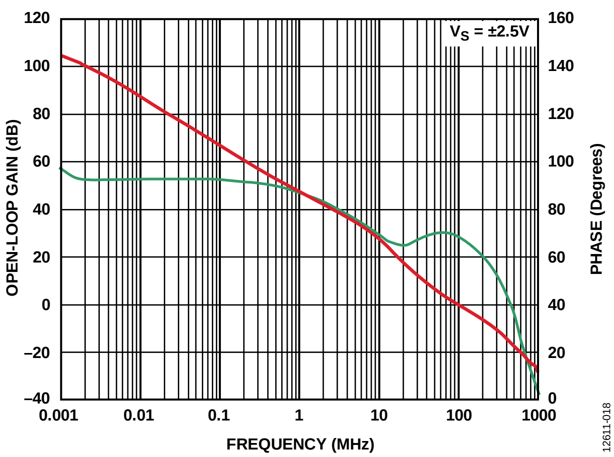

Figure 23. Open-Loop Gain and Phase vs. Frequency

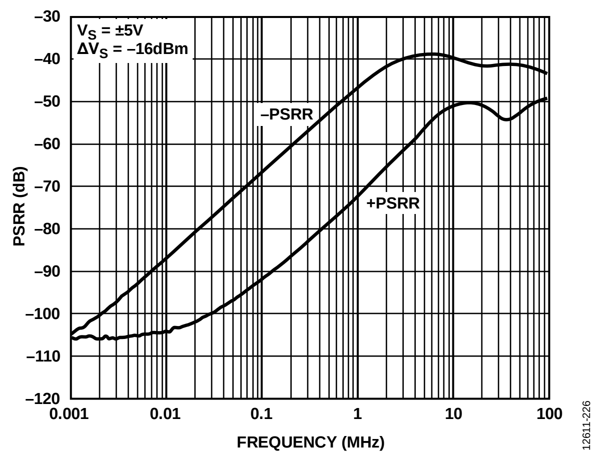

Figure 26. PSRR vs. Frequency

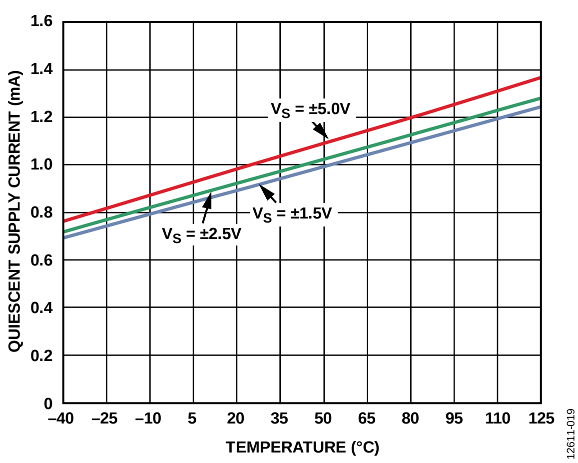

Figure 24. Quiescent Supply Current vs. Temperature

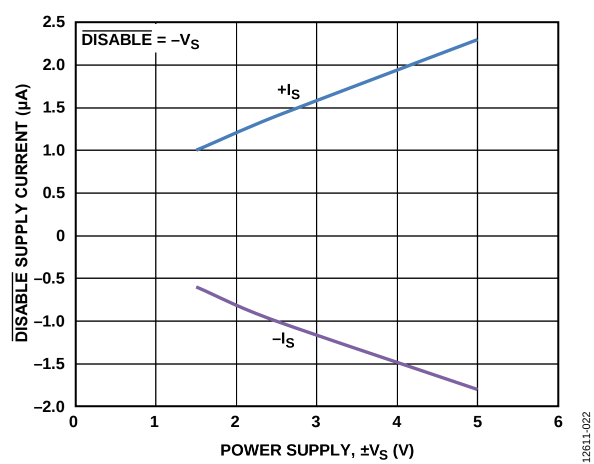

Figure 27. DISABLE Supply Current vs. Power Supply, ±V_S

DC AND INPUT COMMON-MODE PERFORMANCE

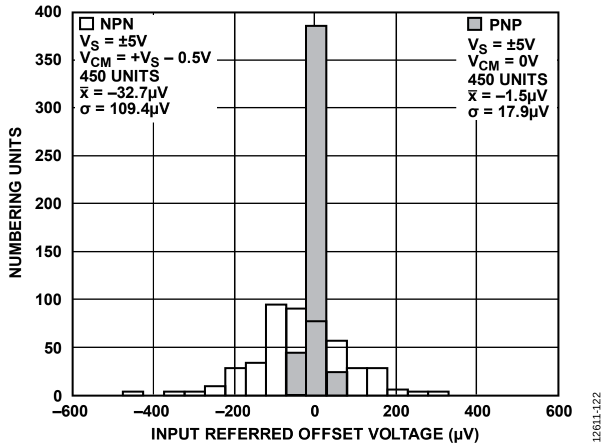

Figure 28. Input Referred Offset Voltage Distribution for the ADA4807-1 and ADA4807-2

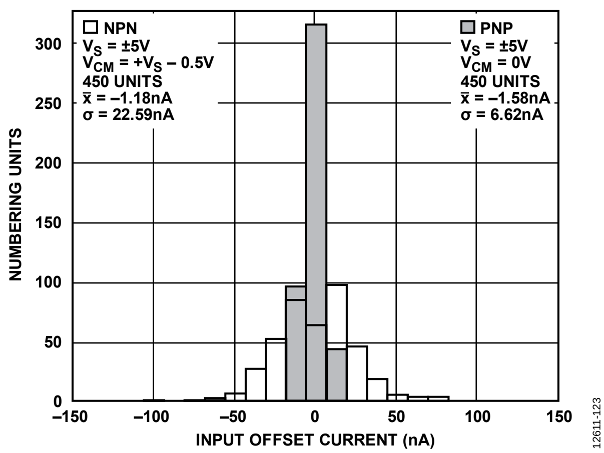

Figure 29. Input Offset Current Distribution

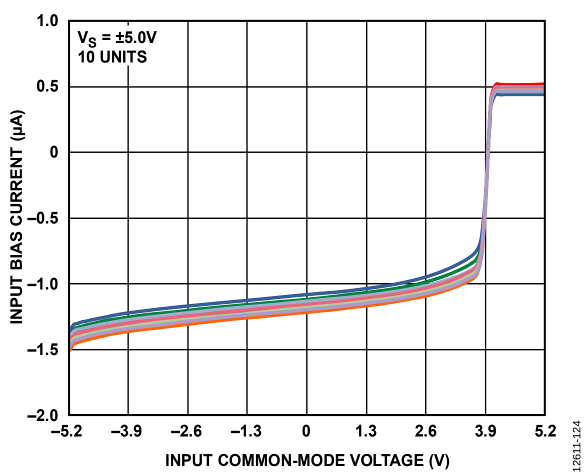

Figure 30. Input Bias Current vs. Input Common-Mode Voltage

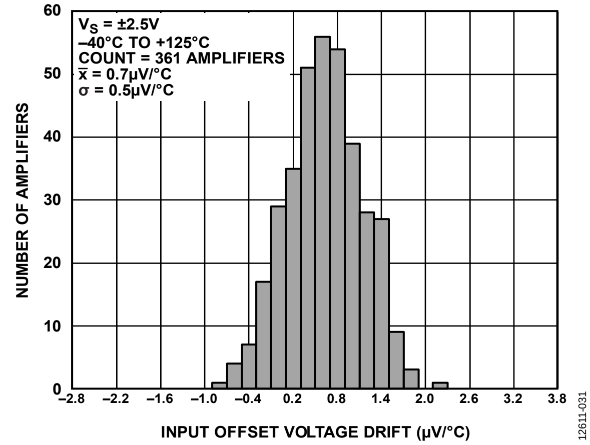

Figure 31. Input Referred Offset Voltage Drift Distribution, V_{CM} = 0 V

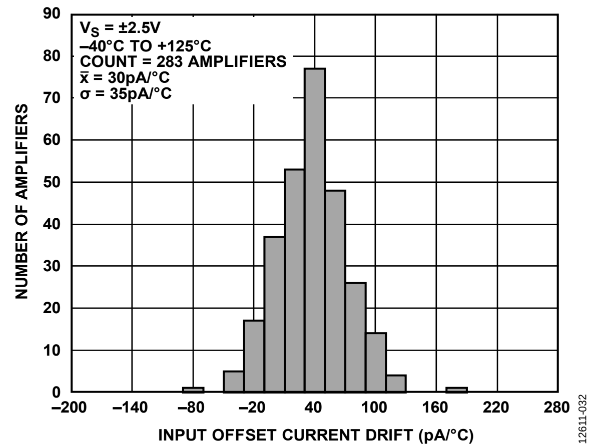

Figure 32. Input Offset Current Drift Distribution, V_{CM} = 0 V

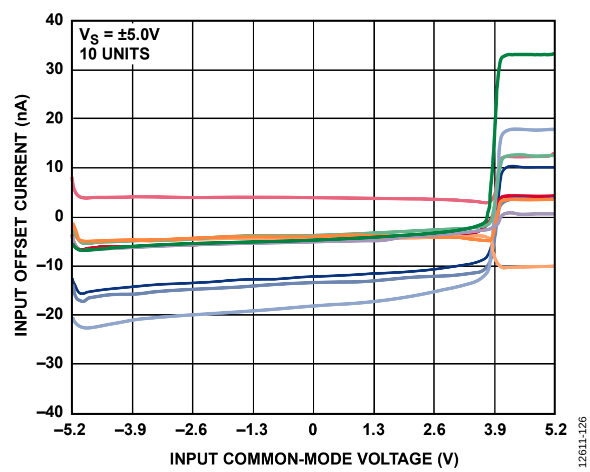

Figure 33. Input Offset Current vs. Input Common-Mode Voltage

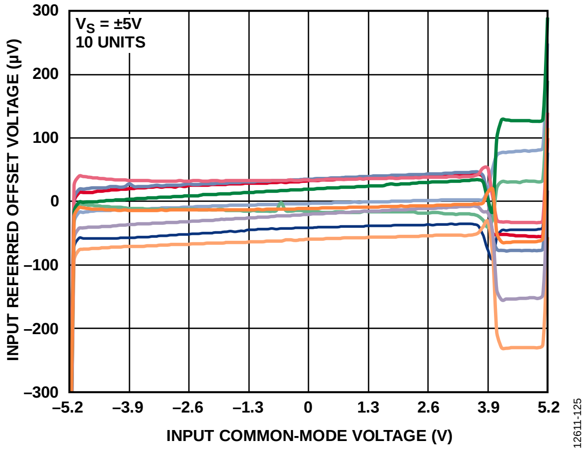

Figure 34. Input Referred Offset Voltage vs. Input Common-Mode Voltage

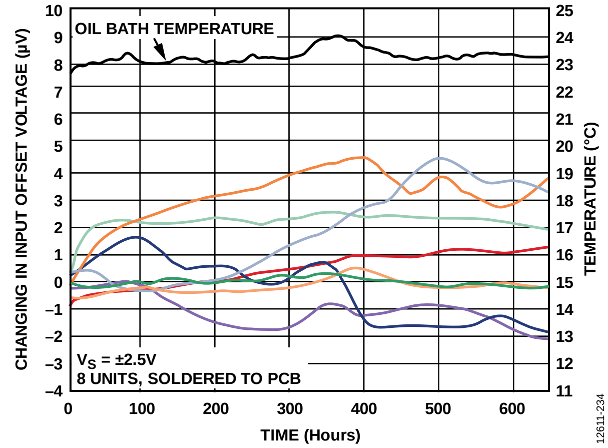

Figure 35. Long-Term Input Offset Voltage (V_{OS}) Drift

SLEW, TRANSIENT, SETTLING TIME, AND CROSSTALK

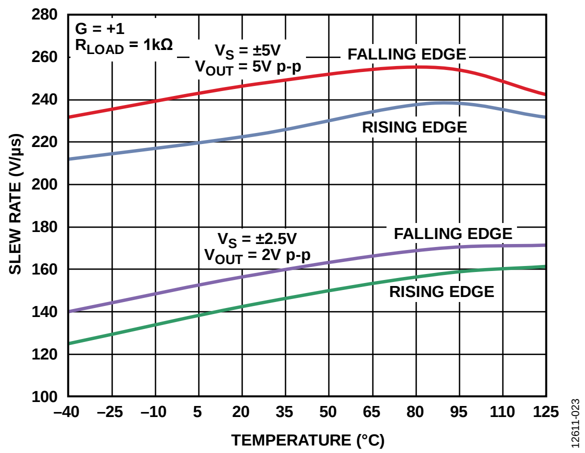

Figure 36. Slew Rate vs. Temperature

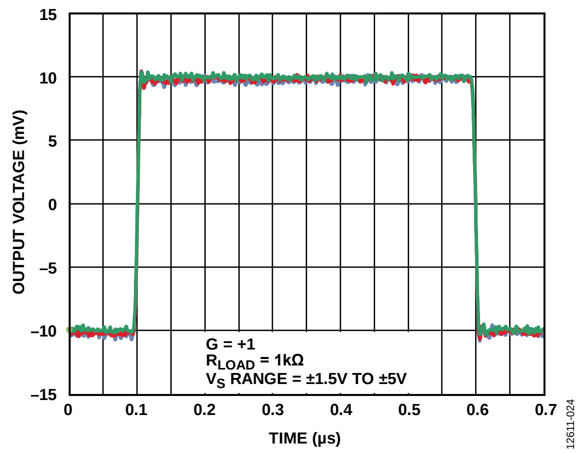

Figure 37. Small Signal Transient Response for Various Supplies

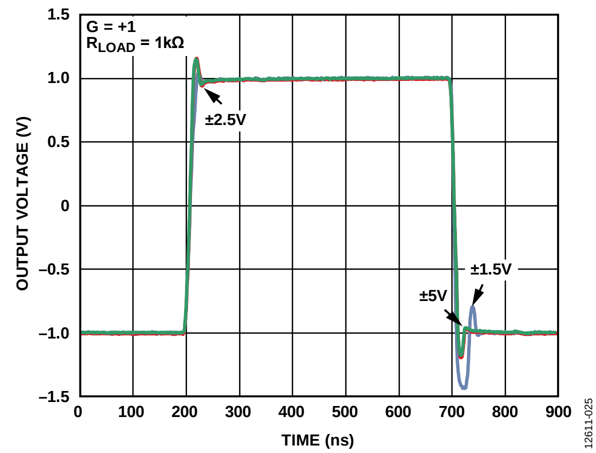

Figure 38. Large Signal Transient Response for Various Supplies

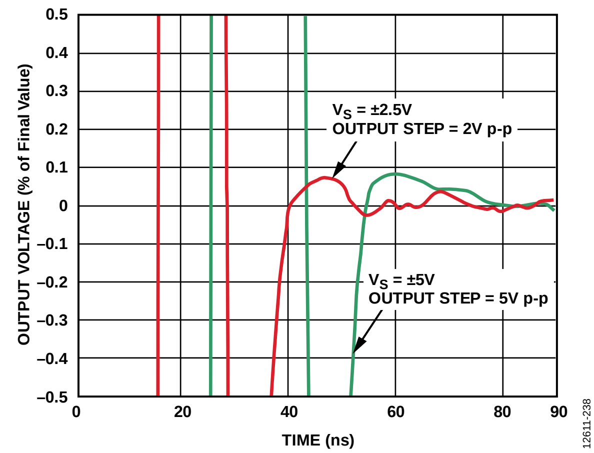

Figure 39. Settling Time to 0.1%

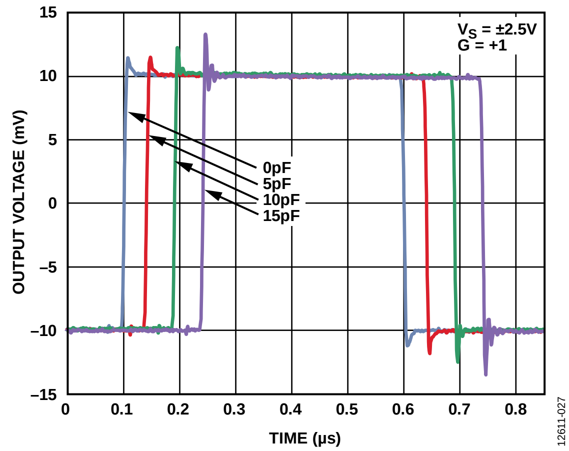

Figure 40. Small Signal Transient Response for Various Capacitive Loads

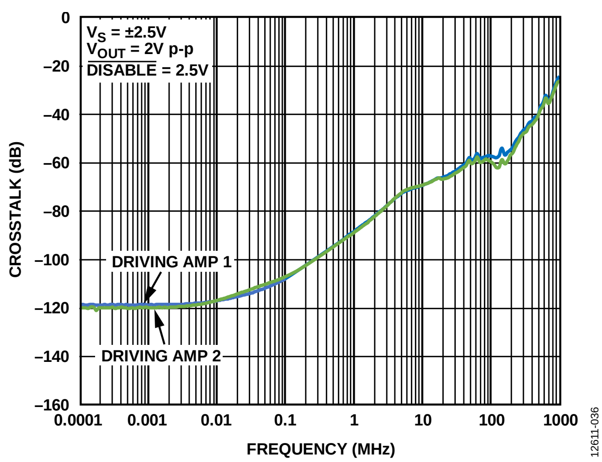

Figure 41. ADA4807-2 Crosstalk vs. Frequency

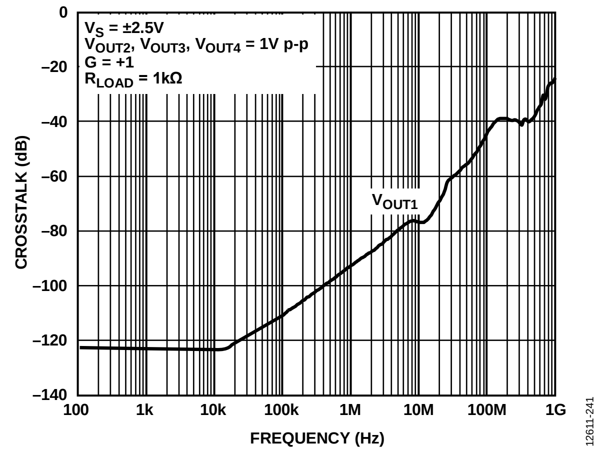

Figure 42. ADA4807-4 All Hostile Crosstalk

DISTORTION AND NOISE

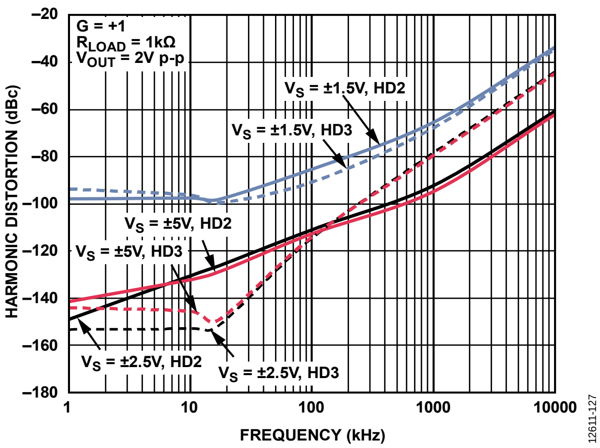

Figure 43. ADA4807-1 Harmonic Distortion vs. Frequency for Various Supplies

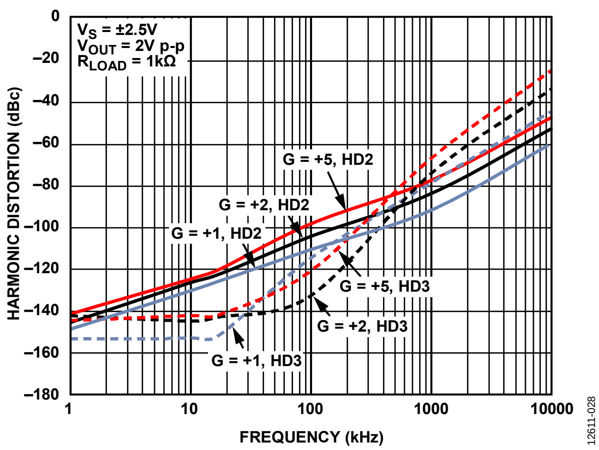

Figure 44. ADA4807-1 Harmonic Distortion vs. Frequency for Various Gains

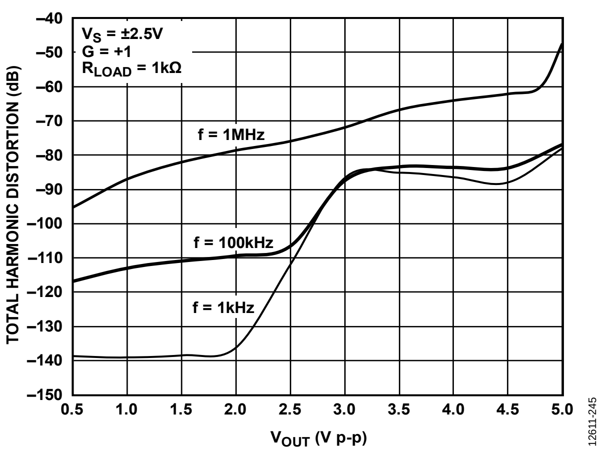

Figure 45. Total Harmonic Distortion vs. Output Voltage (V_{OUT})

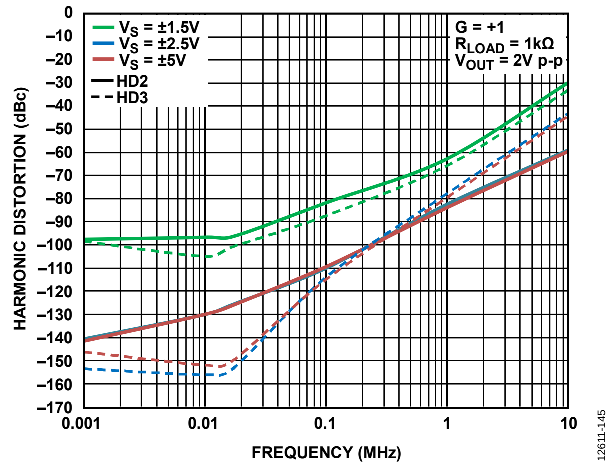

Figure 46. ADA4807-2/ADA4807-4 Harmonic Distortion vs. Frequency for Various Supplies

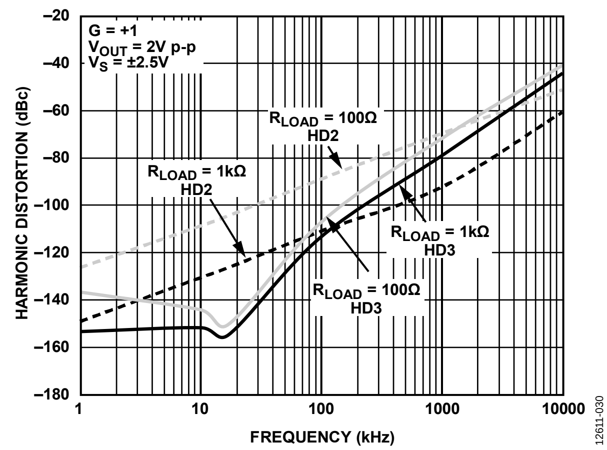

Figure 47. ADA4807-1 Harmonic Distortion vs. Frequency for Various Resistive Loads

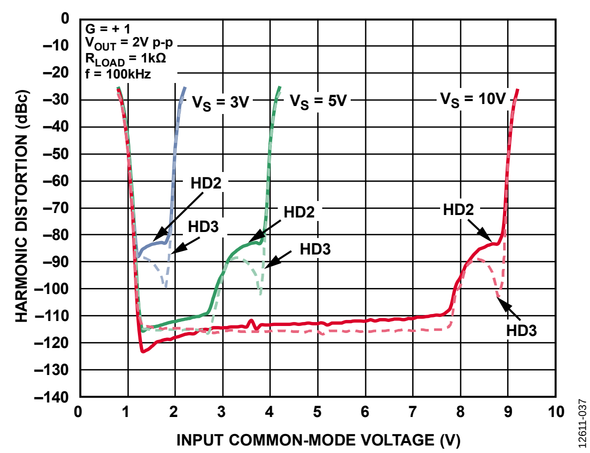

Figure 48. Harmonic Distortion vs. Input Common-Mode Voltage

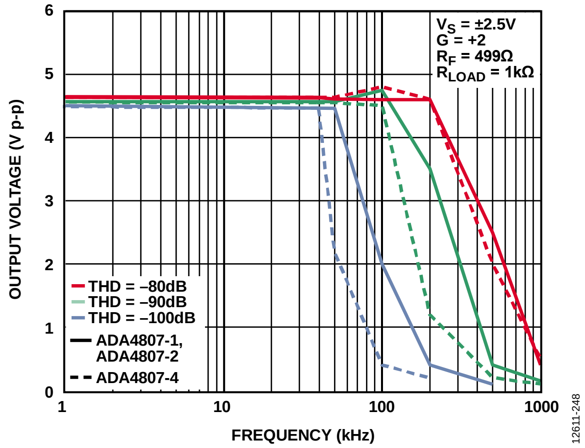

Figure 49. Output Voltage vs. Frequency for $V_S = \pm2.5$ V

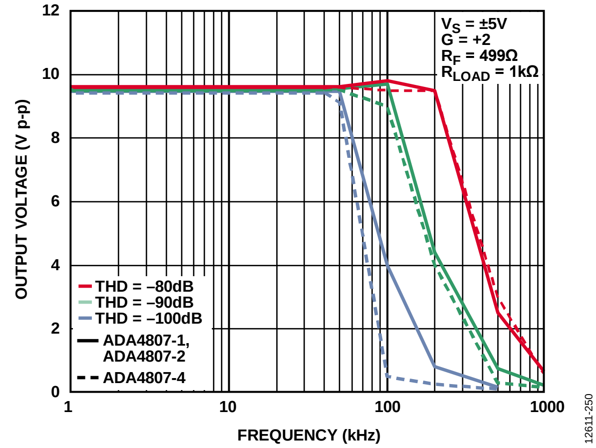

Figure 51. Output Voltage vs. Frequency for $V_S = \pm5$ V

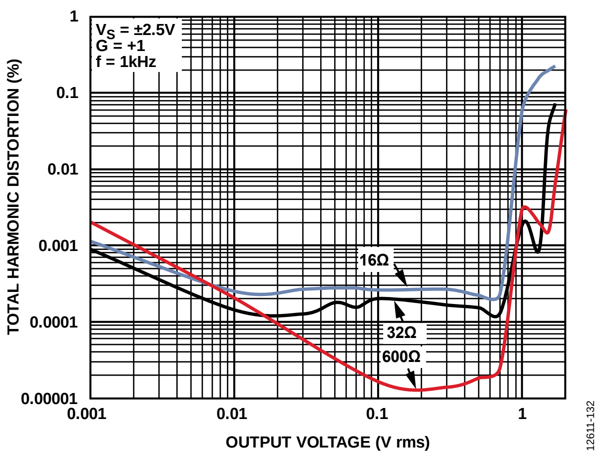

Figure 50. Total Harmonic Distortion vs. Output Voltage for Various Resistive Loads

OUTPUT CHARACTERISTICS

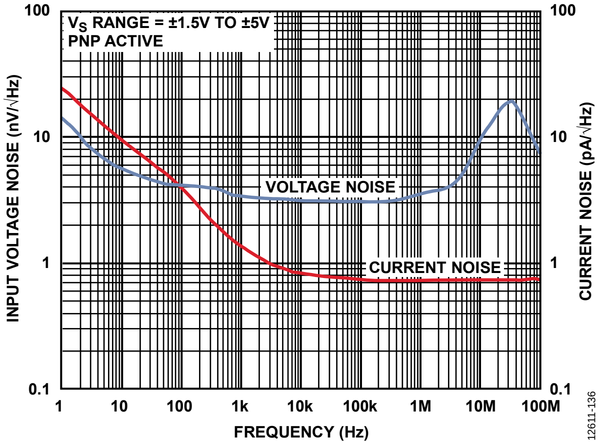

Figure 52. Input Voltage Noise and Current Noise vs. Frequency, V_{CM} = 0 V

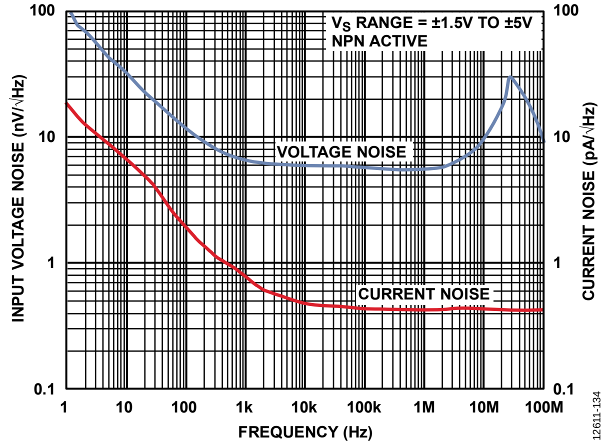

Figure 55. Input Voltage Noise and Current Noise vs. Frequency, $V_{CM} = +V_S - 0.5$ V

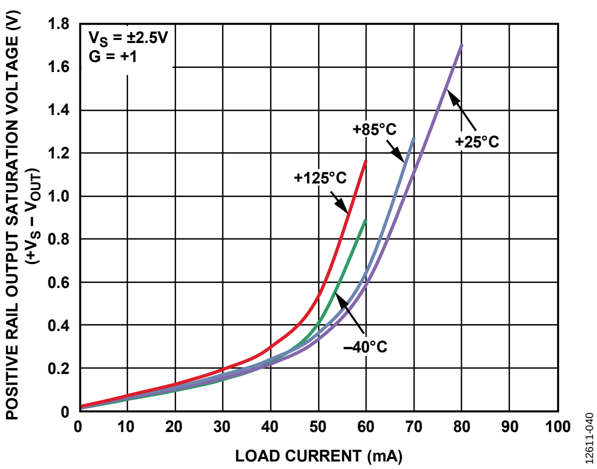

Figure 53. Positive Rail Output Saturation Voltage ($+V_S - V_{OUT}$) vs. Load Current for Various Temperatures

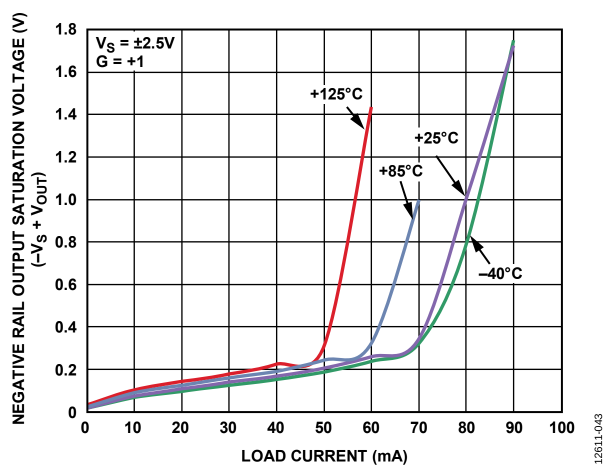

Figure 56. Negative Rail Output Saturation Voltage ($-V_S + V_{OUT}$) vs. Load Current for Various Temperatures

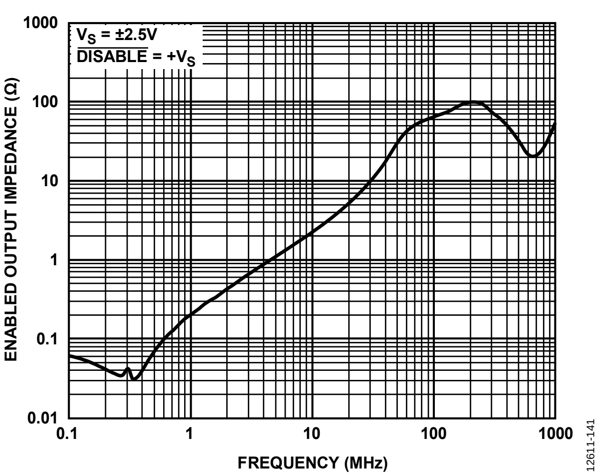

Figure 54. Enabled Output Impedance vs. Frequency

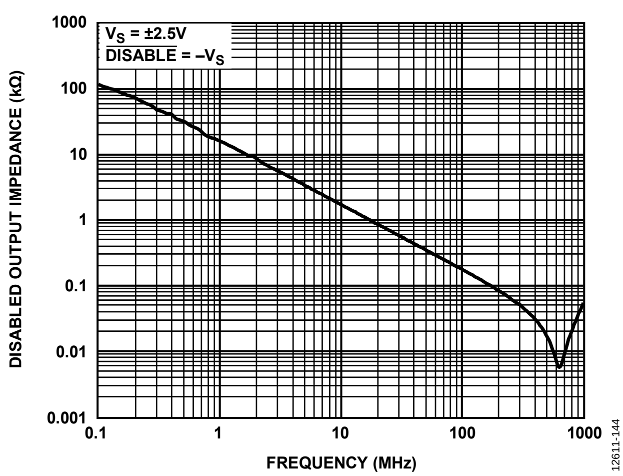

Figure 57. Disabled Output Impedance vs. Frequency

OVERDRIVE RECOVERY AND TURN ON/TURN OFF TIMES

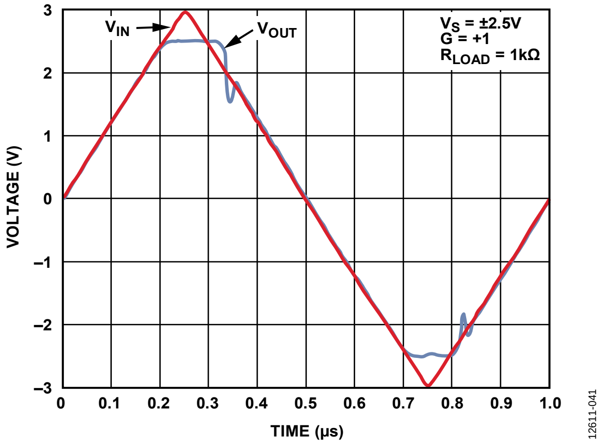

Figure 58. Input Overdrive Recovery

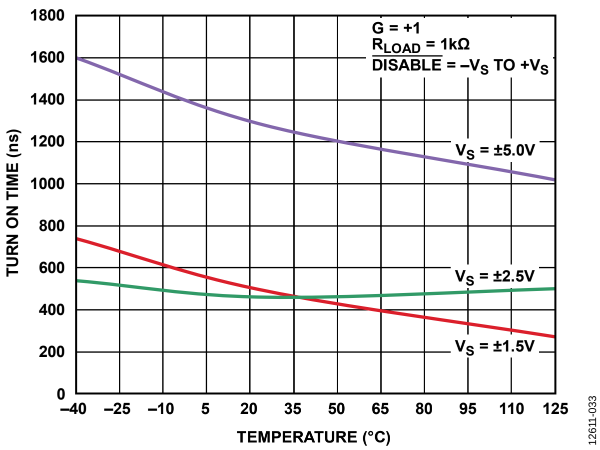

Figure 59. Turn On Time vs. Temperature and Supply

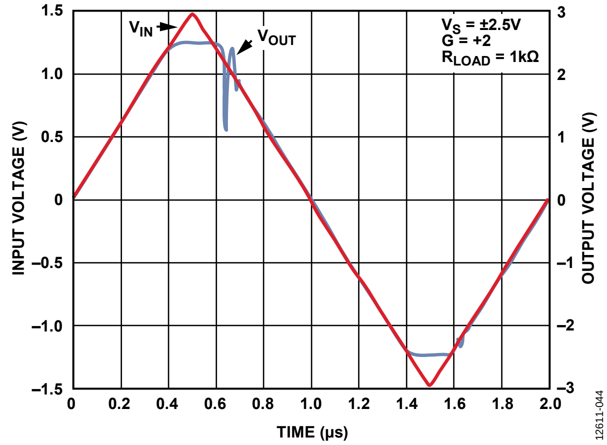

Figure 60. Output Overdrive Recovery

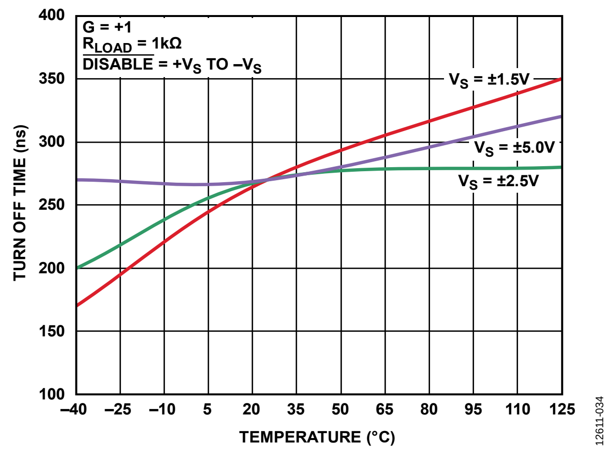

Figure 61. Turn Off Time vs. Temperature and Supply

THEORY OF OPERATION

The ADA4807-1/ADA4807-2/ADA4807-4 have a rail-to-rail input stage with an input range that goes 200 mV beyond either rail. A PNP transistor input pair is active for a majority of the input range, while an NPN transistor input pair is active for the common-mode voltages within 1.3 V of the positive rail. The ADA4807-1/ADA4807-2/ADA4807-4 are fabricated using the Analog Devices, Inc., third generation, extra fast complementary bipolar (XFCB) process resulting in exceptionally good distortion, noise, slew rate, and settling characteristics for 1 mA devices. Given traditional rail-to-rail input architecture performance, the input 1/f noise is surprisingly low, and the current noise is only 0.7 pA/√Hz for a 3 nV/√Hz voltage noise. Typical high slew rate devices suffer from increased current noise because of input pair degeneration and higher input stage current. The ADA4807-1/ADA4807-2/ADA4807-4 exceed current benchmark parameters given the performance of the XFCB process.

The multistage design of the ADA4807-1/ADA4807-2/ADA4807-4 has excellent precision specifications, such as input drift, offset, open-loop gain, CMRR, and PSRR. Typical harmonic distortion numbers fall in the range of −130 dBc for a 10 kHz fundamental (see the Distortion and Noise section). This level of performance makes the ADA4807-1/ADA4807-2/ADA4807-4 the best choices when driving 18-bit precision converters.

The ADA4807-1/ADA4807-2 are optimized for a low shutdown current (4 µA maximum), in the order of a few microamperes. In power sensitive applications, this can eliminate the use of a power FET and enable time interleaved power saving operation schemes.

The rail-to-rail input stage is useful in many different applications. Although the precision is reduced from input to input, many applications can tolerate this loss when the alternative is no functionality at all. The positive rail input range is indispensable for servo loops with a high-side input range

The ADA4807-1/ADA4807-2/ADA4807-4 input operates 200 mV beyond either rail. Internal protection circuitry prevents the output from phase inverting when the input range is exceeded. When the input exceeds a diode beyond either rail, internal electrostatic discharge (ESD) protection diodes source or sink current through the input.

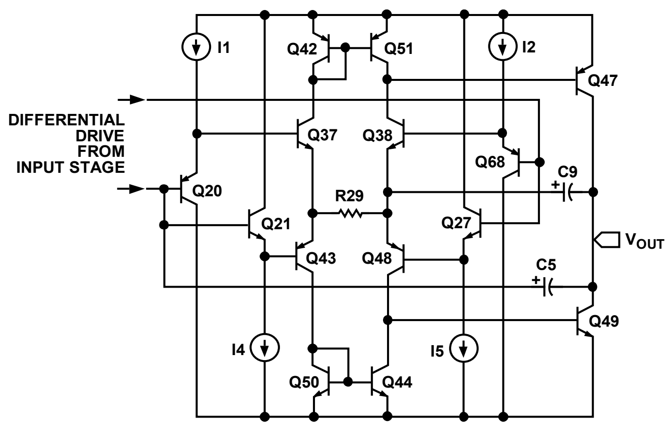

Figure 62. Differential Drive from Input Stage

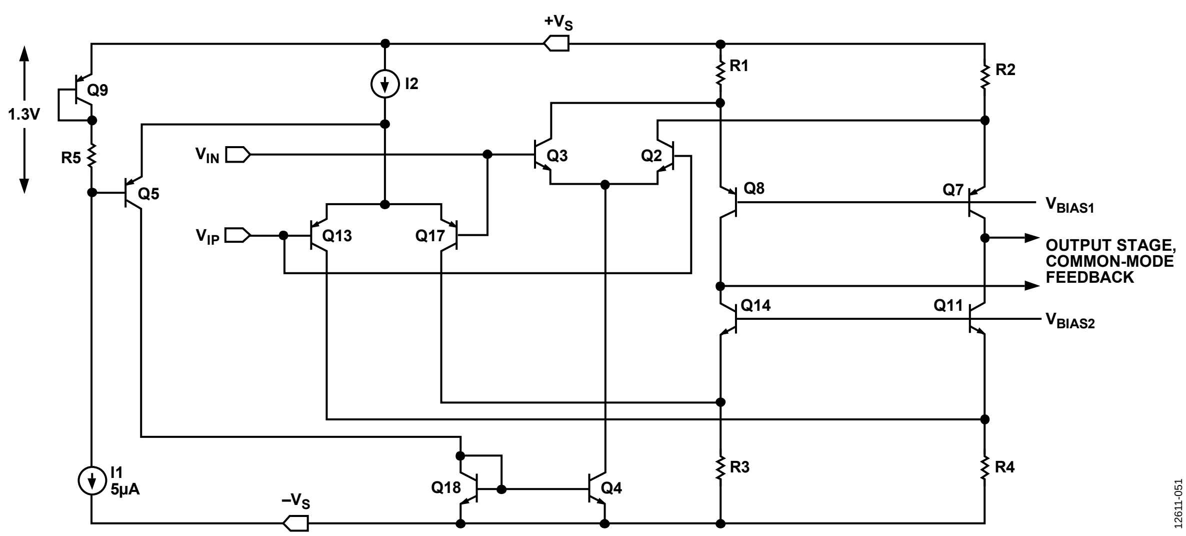

Figure 63. Simplified Schematic

DISABLE CIRCUITRY

When the DISABLE pin is an option, a pull-up resistor is required if the logic leakage currents exceed 300 nA. For a 10 V supply, pulling the DISABLE pin to below 6.3 V turns the ADA4807-1/ADA4807-2 off, which reduces the supply current to 2.4 µA. Conversely, pulling the DISABLE pin voltage to above 6.6 V enables the ADA4807-1/ADA4807-2 with a quiescent current of 1 mA. When the ADA4807-1/ADA4807-2 device is disabled, its output enters a high impedance state. Figure 64 and Table 10 show the DISABLE functionality over the complete supply range.

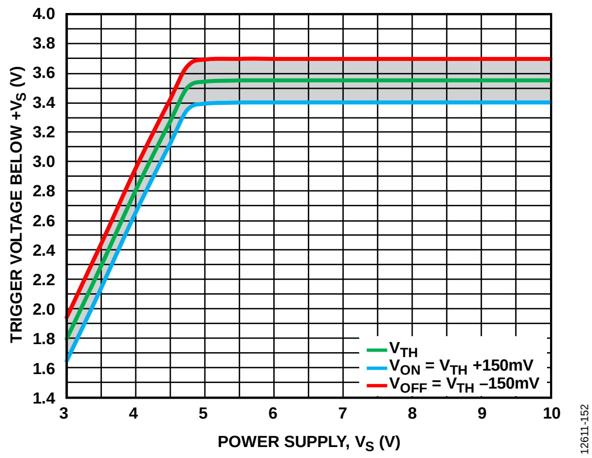

Figure 64. DISABLE Trigger Voltage

Table 10. Threshold Voltages for Disabled and Enabled Modes

Mode	+3 V	+5 V	+10 V	±5 V	+7 V/−2 V
Enabled	1.35 V	1.6 V	6.6 V	1.6 V	3.6 V
Disabled	1.05 V	1.3 V	6.3 V	1.3 V	3.3 V

The output impedance decreases as the frequency increases. When disabled, a forward isolation of 120 dB is achieved at 100 kHz (see Figure 22). ESD clamps protect the DISABLE pin, as shown in Figure 65. Voltages beyond the power supplies cause these diodes to conduct. To avoid excessive current in the ESD diodes, ensure that the voltage to the DISABLE pin is not 0.7 V greater than the positive supply or that it is not 0.7 V less than the negative supply. If an overvoltage condition is expected, limit the input current to less than 10 mA with a series resistor.

INPUT PROTECTION

The ADA4807-1/ADA4807-2/ADA4807-4 are fully protected from ESD events, withstanding human body model ESD events of ±3 kV and charged device model events of ±1.25 kV with no measured performance degradation. The precision input is protected with an ESD network between the power supplies and diode clamps across the input device pair, as shown in Figure 65.

For differential voltages above approximately 1.2 V at room temperature and 0.8 V at 125°C, the diode clamps begin to conduct. Too much current can cause damage due to excessive heating. If large differential voltages must be sustained across the input terminals, it is recommended that the current through the input clamps be limited to less than 10 mA. Series input resistors sized appropriately for the expected differential overvoltage provide the needed protection.

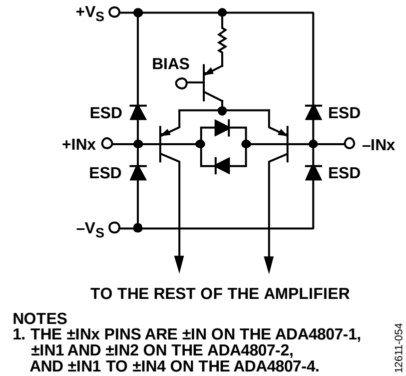

Figure 65. Input Stage and Protection Diodes

NOISE CONSIDERATIONS

Figure 66 illustrates the primary noise contributors for the typical gain configurations. The total output noise (V_{N_OUT}) is the root sum square of all the noise contributions.

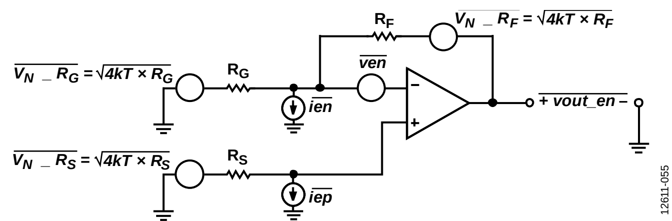

Figure 66. Noise Sources in Typical Gain Configurations

Source resistance noise, amplifier input voltage noise, and the voltage noise from the amplifier input current noise ($I_{N+} \times R_S$) are all subject to the noise gain term ($1 + R_F/R_G$).

Calculate the output noise spectral density using the following equation:

$$V_{N\_OUT} = \sqrt{4kTR_F + \left(1+\frac{R_F}{R_G}\right)^2 \left[4kTRs + I_{N+}^2 R_S^2 + V_N^2\right] + \left(\frac{R_F}{R_G}\right)^2 4kTR_G + I_{N-}^2 R_F^2}$$

where:
k is Boltzmann's constant.
T is the absolute temperature in degrees Kelvin.
R_F and R_G are the feedback network resistances, as shown in Figure 66.
R_S is the source resistance, as shown in Figure 66.
I_{N+} and I_{N-} represent the amplifier input current noise spectral density in pA/√Hz.
V_N is the amplifier input voltage noise spectral density in nV/√Hz.

APPLICATIONS INFORMATION

CAPACITIVE LOAD DRIVE

Figure 67 shows the schematic for driving large capacitive loads, and Figure 68 shows the frequency response for a gain of +2. Note that the bandwidth decreases with larger capacitive loads (see Figure 68).

Figure 69 shows the required series resistor (R_{SERIES}) when limiting the peaking to 3 dB for a range of load capacitors (C_{LOAD}) at a gain of +2. From Figure 69, no series resistors are necessary to maintain stability for larger capacitors.

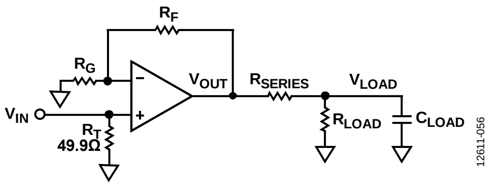

Figure 67. Schematic for Driving Large Capacitive Loads

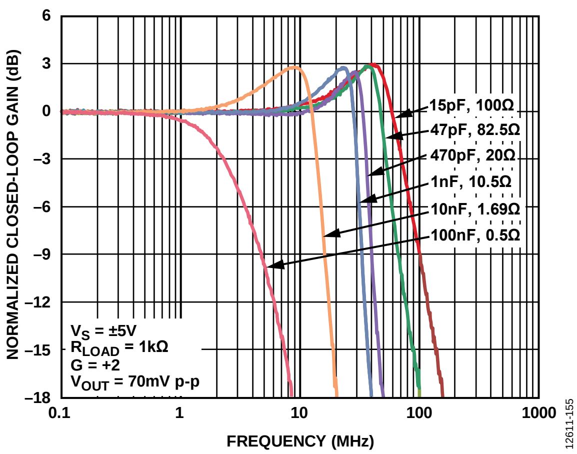

Figure 68. Frequency Response for Driving Large Capacitive Loads, $R_F = R_G = 249\ \Omega$

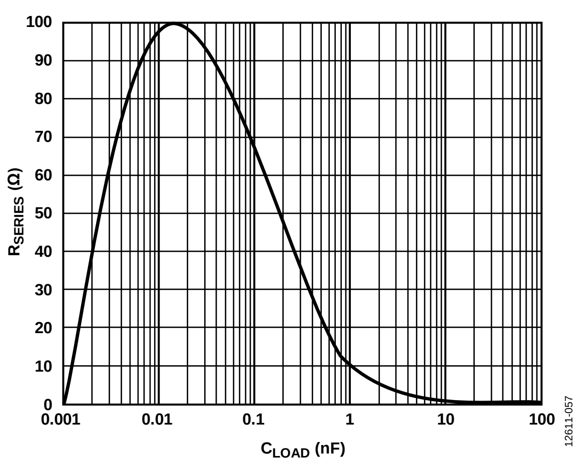

Figure 69. Required Series Resistor (R_{SERIES}) vs. Capacitive Load (C_{LOAD}) at 3 dB Peaking

LOW NOISE FET OPERATIONAL AMPLIFIER

Low noise amplifiers for photodiode, piezoelectric, and other instrumentation applications typically call for circuit parameters such as extremely high input impedance, low 1/f noise, or sub-picoamp bias currents that can be met only with a discrete amplifier design.

The discrete amplifier shown in Figure 70 uses a high-speed op amp preceded by a differential amplifier stage. This discrete configuration is implemented with dual matched JFETs, which provide high input impedance and some initial gain, reducing the noise and precision specifications of the second stage. The low current consumption of the ADA4807-1/ADA4807-2/ADA4807-4, in addition to their precision and low noise characteristics, results in a composite design with 7 mA of total supply current, 1.5 nV/√Hz noise at 1 kHz, and 4 nV/√Hz noise at 10 Hz.

The unbalanced output impedance of the FETs is negated by the use of an inverting amplifier cascode. The ADA4807-1/ADA4807-2/ADA4807-4 are ideally suited for the cascode due to their rail-to-rail input structure, which results in excellent overload behavior of the overall discrete amplifier. Using this cascode structure, the CMRR is greater than 100 dB.

A high output impedance current source is also needed to maintain the CMRR of the discrete amplifier. An ADR510 maintains a precise current over the supply voltage, and the low collector capacitance of the PMP4201 results in a balanced and predictable slew rate behavior. This is shown in Figure 71 with a 0.4 V p-p input and a 4 V p-p output with a gain of 10. Figure 72 shows output referred total harmonic distortion plus noise (THD + N) for a gain of 10.

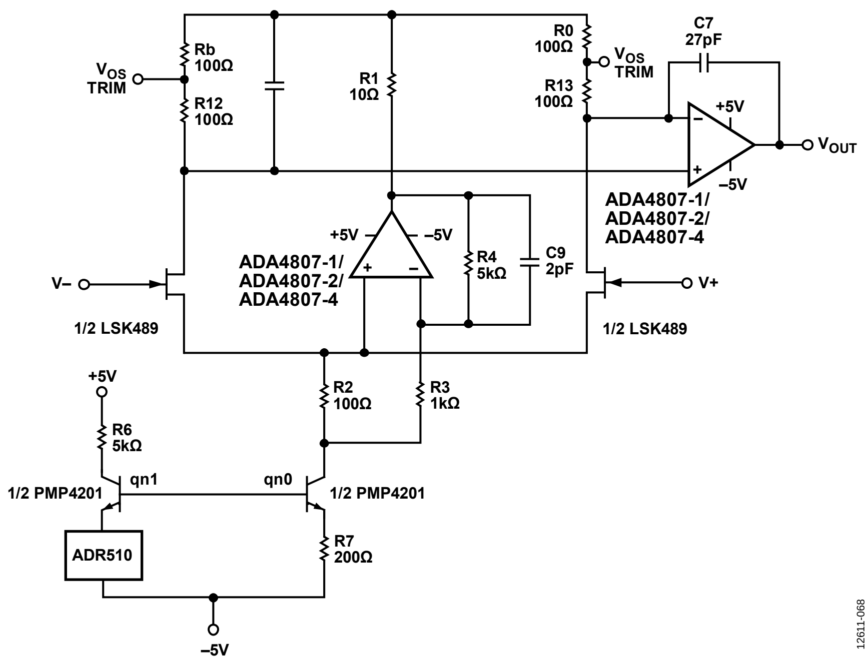

Figure 70. Low Noise FET Operational Amplifier Schematic

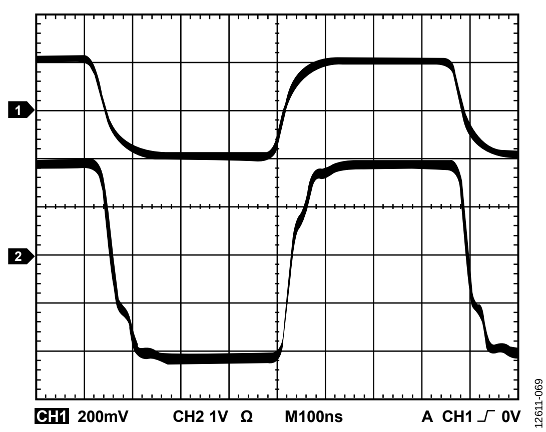

Figure 71. Pulse Response, G = 10, 4 V p-p Output

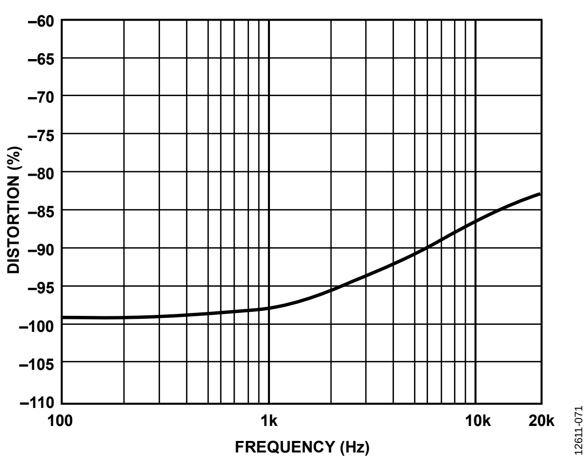

Figure 72. 8 V p-p Output, THD + N for G = 10, R_{LOAD} = 600 Ω

POWER MODE ADC DRIVER

One of the merits of a SAR ADC, such as the AD7980, is that its power scales with the sampling rate. This power scaling makes SAR ADCs very power efficient, especially when running at a low sampling frequency. However, the ADC driver used with the SAR ADC traditionally consumes constant power regardless of the sampling frequency.

Figure 73 illustrates a method by which the quiescent power of the ADC driver can be reduced by 95% while still maintaining the input signal to the ADC. Both the ADA4807-1/ADA4807-2/ ADA4807-4 and the AD8603 are rail-to-rail input and output (RRIO) amplifiers and can operate on a single 5 V analog supply. Connecting the AD8603 in parallel with a sharing resistor allows the ADA4807-1/ADA4807-2/ADA4807-4 to be powered down, reducing the total supply current for the driver from 1 mA to 50 µA. The sampling frequency of the AD7980 can then be reduced to match the power consumption of the AD8603. With the ADA4807-1/ADA4807-2/ADA4807-4 powered on, the SNR and THD are 84.1 dB and −100.3 dB for a 3 V p-p, 1 kHz input and a 4.096 V reference. The SNR and THD degrade to 81.4 dB and −77.3 dB for the same input signal in the low power mode when only the AD8603 is on.

One issue with this method is that the reference and reference buffer power do not scale with the ADC or the driver. This makes this configuration most useful in multichannel systems where the reference can be reused across many inputs. Alternately, the reference buffer can be scaled in the same fashion as the input driver; however, the reference itself must remain on in any of the modes.

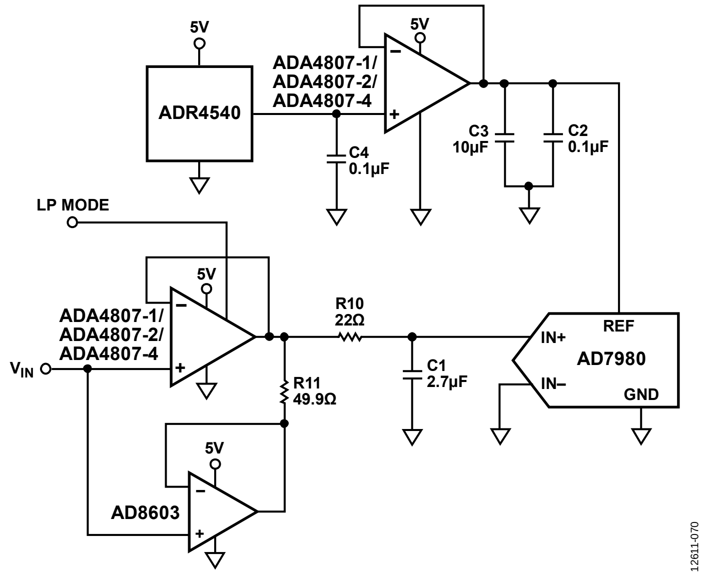

Figure 73. Dual Power Mode ADC Driver

ADC DRIVING

The ADA4807-1/ADA4807-2/ADA4807-4 can be used in ADC driving applications. Figure 74 is a simplified schematic of the ADA4807-1/ADA4807-2/ADA4807-4 driving an 18-bit differential ADC, the AD7982, in a fully differential signal chain. This configuration results in an effective number of bits (ENOB) of 15.7; results are shown in Figure 75.

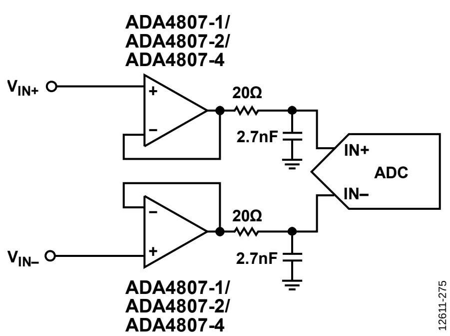

Figure 74. Schematic for Driving the AD7982, $+V_S = +7$ V, $-V_S = -1$ V

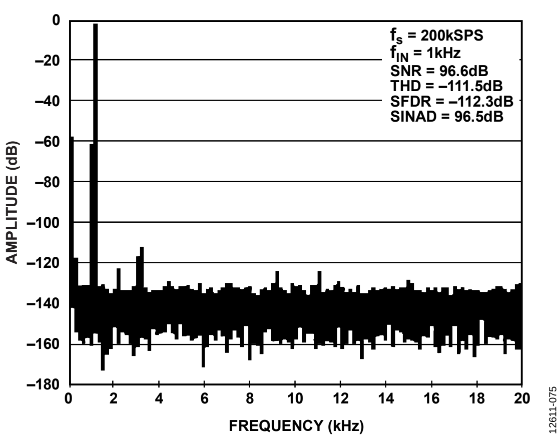

Figure 75. FFT for Driving a Differential Converter, −0.5 dBFS

Figure 76 shows the ADA4807-1/ADA4807-2/ADA4807-4 configured to convert a single-ended to differential signal and drive an 18-bit ADC. This configuration results in an ENOB of 15.3. The FFT is shown in Figure 77.

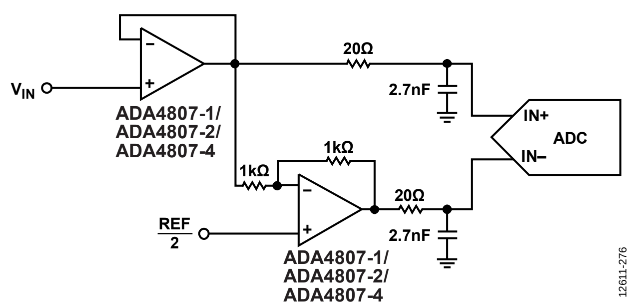

Figure 76. Schematic for Driving the AD7982 Differential Converter from a Single-Ended Input Signal, $+V_S = +7$ V, $-V_S = -1$ V

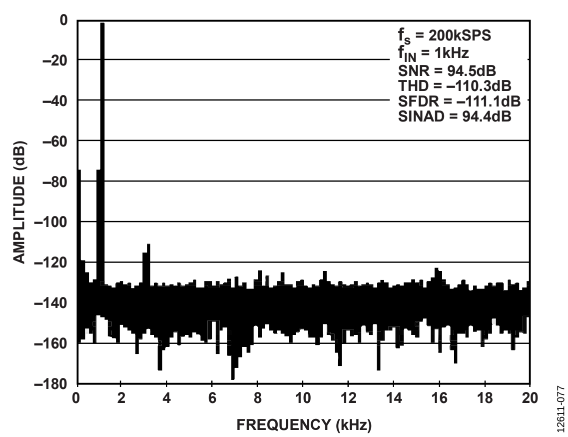

Figure 77. FFT for Driving a Single-Ended Input Signal into a Differential Converter

ADC DRIVING WITH DYNAMIC POWER SCALING

In power sensitive applications, the ADA4807-1/ADA4807-2 can be switched on prior to the ADC turning on. Figure 78 shows the timing diagram for dynamically power scaling the ADA4807-1/ADA4807-2 with the AD7982 configuration shown in Figure 79. The falling edge of the DISABLE signal must align with the rising edge of the CONV signal of the ADC to obtain a clean data acquisition. Figure 79 gives the FFT for driving a fully differential signal chain with a 1.2 µs on time as shown in Figure 78. With this method, the ADA4807-1/ADA4807-2 quiescent current (per amplifier) is reduced from 2 mA to 0.25 mA. Figure 81 gives the FFT for dynamically power scaling a single-ended input signal chain into a differential ADC with a 4 µs on time as shown in Figure 80. This configuration results in a quiescent current reduction of 20%.

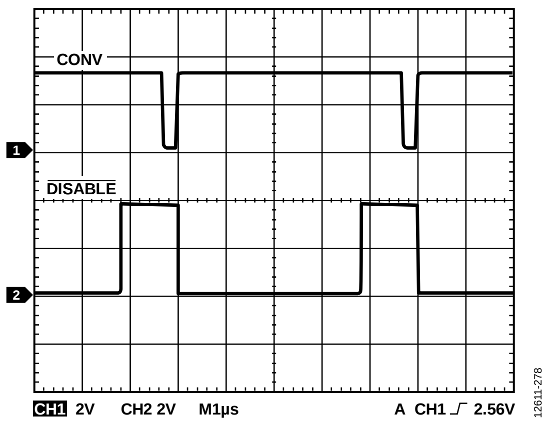

Figure 78. Dynamic Power Scaling Timing Diagram for Driving a Fully Differential Signal Chain into a Differential ADC (AD7982)

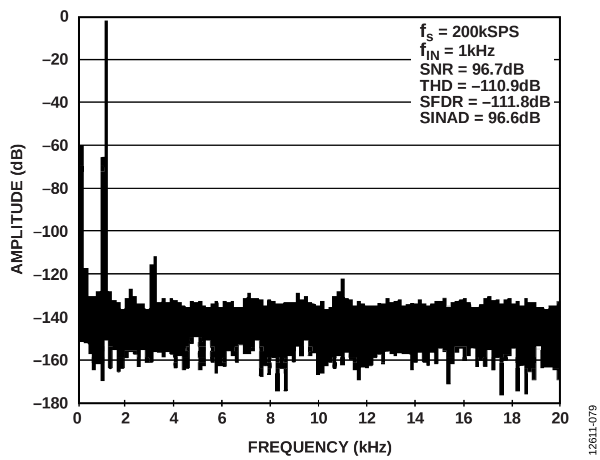

Figure 79. FFT for Driving a Differential Converter using Dynamic Power Scaling, –0.5 dBFS, On Time of 1.2 µs, for the Schematic Shown in Figure 74

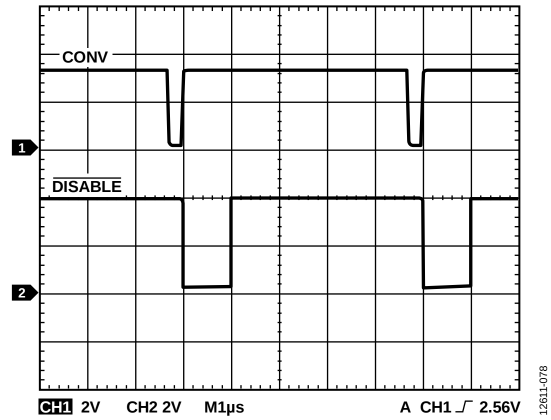

Figure 80. Dynamic Power Scaling Timing Diagram for Driving a Single-Ended Input Signal Chain into a Differential ADC (AD7982)

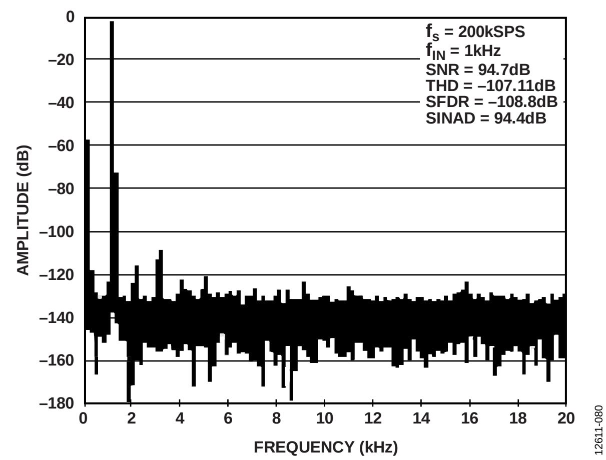

Figure 81. FFT for Driving a Single-Ended to Differential Converter Using Dynamic Power Scaling, –0.5 dBFS, On Time of 4 µs, for the Schematic Shown in Figure 76

LAYOUT, GROUNDING, AND BYPASSING

The ADA4807-1/ADA4807-2/ADA4807-4 are high speed devices. Realizing their superior performance requires attention to the details of high speed printed circuit board (PCB) design.

The first requirement is to use a multilayer PCB with solid ground and power planes that cover as much of the board area as possible.

Bypass each power supply pin directly to a nearby ground plane, as close to the device as possible. Use 0.1 μF high frequency ceramic chip capacitors.

Provide low frequency bulk bypassing using 10 μF tantalum capacitors from each supply to ground.

Stray transmission line capacitance in combination with package parasitics can potentially form a resonant circuit at high frequencies, resulting in excessive gain peaking or possible oscillation. Signal routing must be short and direct to avoid such parasitic effects. Provide symmetrical layout for complementary signals to maximize balanced performance.

Use radio frequency transmission lines to connect the driver and receiver to the amplifier.

Minimize stray capacitance at the input and output pins by clearing the underlying ground and low impedance planes near these pins.

If the driver and receiver are more than one-eighth of the wavelength from the amplifier, minimize the signal trace widths. This nontransmission line configuration requires clearing of the underlying and adjacent ground and low impedance planes near the signal lines.

OUTLINE DIMENSIONS

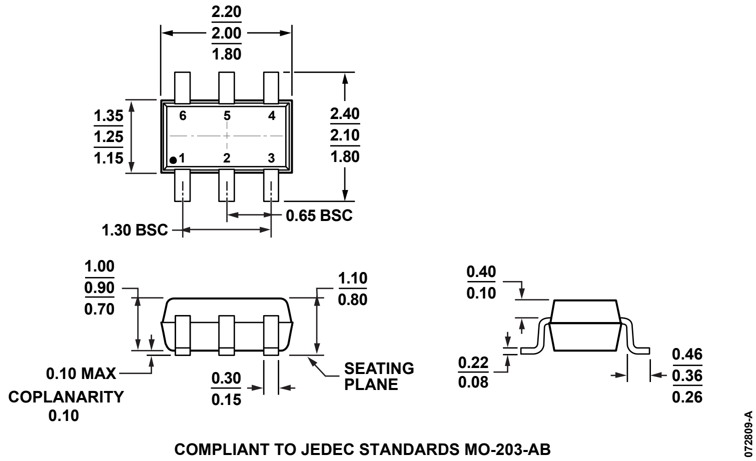

Figure 82. 6-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-6)
Dimensions shown in millimeters

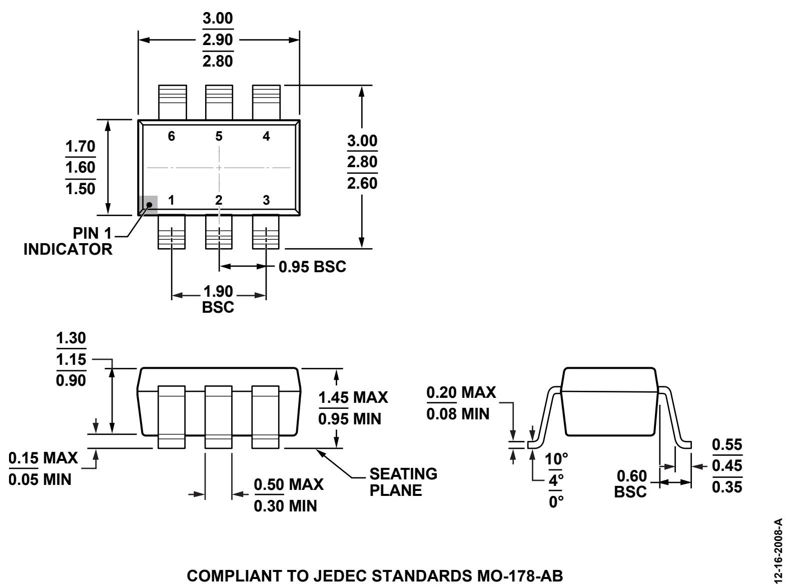

Figure 83. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters

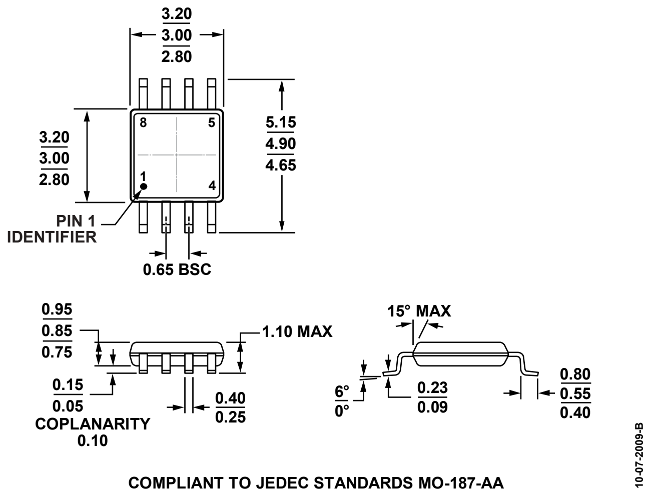

Figure 84. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

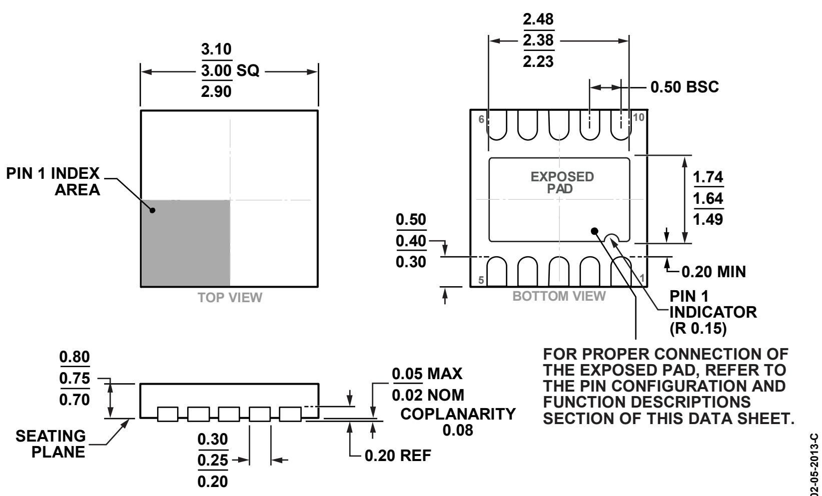

Figure 85. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters