Three ADCs, One DAC, Low Power Codec with Audio DSPs

FEATURES

- Programmable FastDSP audio processing engine
  - Up to 768 kHz sample rate
  - Biquad filters, limiters, volume controls, mixing
- Tensilica HiFi 3z DSP core
  - Quad MAC per cycle: 24 × 24-bit multiplier and 64-bit accumulator
  - Flexible power operation mode: 24.576 MHz, 49.152 MHz, 73.728 MHz, and 98.304 MHz
  - 336 kB total memory
  - JTAG debug and trace
- Low latency, 24-bit ADCs, and DAC
  - 106 dB SNR (signal through ADC with A-weighted filter)
  - 110 dB combined SNR (signal through DAC and headphone with A-weighted filter)
- Programmable double precision MAC engine for maximum 24-stage equalizer
- Serial-port sample rates from 8 kHz to 768 kHz
- 5 µs group delay (f_S = 768 kHz) analog in to analog out with FastDSP bypass (zero instructions)
- 3 differential or single-ended analog inputs, configurable as microphone or line inputs
- 8 digital microphone inputs
- Analog differential audio output, configurable as either line output or headphone driver
- 2 PDM output channels
- PLL supporting any input clock rate from 30 kHz to 36 MHz
- 4 channel asynchronous sample rate converters (ASRCs)
- 2, 16-channel serial audio ports supporting I^2S, left-justified, right-justified, or up to TDM16 (TDM12 in turbo mode)
- 8 interpolators and 8 decimators with flexible routing
- Power supplies
  - Analog AVDD at 1.8 V typical
  - Digital I/O IOVDD at 1.1 V to 1.98 V
  - Digital DVDD at 0.85 V to 1.21 V
  - Headphone HPVDD_L at 1.2 V to AVDD
- Control/communication interfaces
  - I^2C, SPI, or UART control ports
  - Main quad SPI (QSPI)
  - UART communication port
- Self-boot from QSPI flash
- Flexible GPIO and IRQ
- AEC-Q100 qualified for automotive applications
- 64-lead lead frame chip scale package [LFCSP], 9 mm × 9 mm and 0.75 mm package height

APPLICATIONS

- Automotive audio systems
- Digital audio effects processors

GENERAL DESCRIPTION

The ADAU1861 is a codec with three inputs and one output that incorporates two digital-signal processors (DSPs). The path from the analog input to the DSP core to the analog output is optimized for low latency.

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REVISION HISTORY

10/2023—Rev. 0 to Rev. A

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1/2023—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

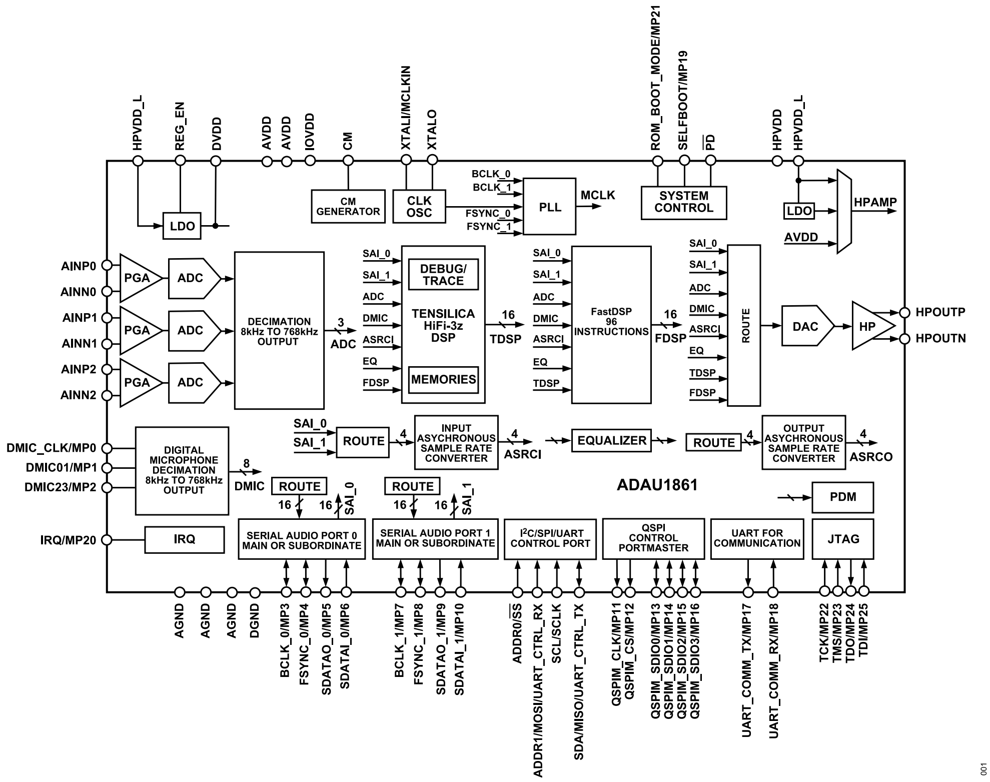

Figure 1. Functional Block Diagram

SPECIFICATIONS

Main clock = 24.576 MHz, Hibernate 1 mode, serial input sample rate = 48 kHz, measurement bandwidth = 20 Hz to 20 kHz, word width = 24 bits, ambient temperature = 25°C, and outputs line loaded with 10 kΩ, unless otherwise noted.

ANALOG PERFORMANCE SPECIFICATIONS

Supply voltages: AVDD = IOVDD = 1.8 V, and DVDD = 0.9 V, unless otherwise noted.

Table 1. Analog Performance Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTERS (ADCs)					
ADC Resolution	All ADCs		24		Bits
Digital Gain Step			0.375		dB
Digital Gain Range		−71.25		+24	dB
INPUT RESISTANCE (R_{IN})					
Single-Ended Line Input	Nonvoice wake-up mode		9		kΩ
	Voice wake-up mode		18		kΩ
Differential Line Input	Nonvoice wake-up mode		36		kΩ
	Voice wake-up mode		36		kΩ
Programmable-Gain Amplifier (PGA) Single-Ended Inputs	PGA high R_{IN}, normal, 0 dB gain		20.6		kΩ
	PGA high R_{IN}, normal, 24 dB gain		2.4		kΩ
	PGA low R_{IN}, enhanced, 0 dB gain		10.3		kΩ
	PGA low R_{IN}, enhanced, 24 dB gain		1.2		kΩ
	PGA high R_{IN}, enhanced, 0 dB gain		20.6		kΩ
	PGA high R_{IN}, enhanced, 24 dB gain		2.4		kΩ
PGA Differential Inputs	PGA high R_{IN}, normal, 0 dB gain		41.2		kΩ
	PGA high R_{IN}, normal, 24 dB gain		4.8		kΩ
	PGA low R_{IN}, enhanced, 0 dB gain		20.6		kΩ
	PGA low R_{IN}, enhanced, 24 dB gain		2.4		kΩ
	PGA high R_{IN}, enhanced, 0 dB gain		41.2		kΩ
	PGA high R_{IN}, enhanced, 24 dB gain		4.8		kΩ
SINGLE-ENDED LINE INPUT	PGAx_EN = 0 and PGAx_SLEW_DIS = 1				
Full-Scale Input Voltage	0 dBFS		0.49		V rms
	0 dBFS		1.39		V p-p
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	Enhanced performance		103		dB
	Normal performance		103		dB
	Power saving		102		dB
	Voice wake-up		99		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		98		dB
	Normal performance		98		dB
	Power saving		98		dB
	Voice wake-up		96		dB
Signal-to-Noise Ratio (SNR)[2]					
With A-Weighted Filter (RMS)	Enhanced performance		102		dB
	Normal performance		102		dB
	Power saving		102		dB
	Voice wake-up		98		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		98		dB
	Normal performance		98		dB
	Power saving		98		dB
	Voice wake-up		95		dB

SPECIFICATIONS

Table 1. Analog Performance Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Interchannel Gain Mismatch			40		mdB
Total Harmonic Distortion + Noise (THD + N)	20 Hz to 20 kHz, −1 dB full-scale output				
	Enhanced performance		–78		dBFS
	Normal performance		–78		dBFS
	Power saving		–78		dBFS
	Voice wake-up		–78		dBFS
Offset Error			±0.3		mV
Gain Error			±0.2		dB
Interchannel Isolation	CM capacitor = 1 µF		100		dB
Power-Supply Rejection Ratio (PSRR)	CM capacitor = 1 µF				
	100 mV p-p at 1 kHz		60		dB
	100 mV p-p at 10 kHz		40		dB
DIFFERENTIAL LINE INPUT	PGAx_EN = 0, PGAx_SLEW_DIS = 1				
Full-Scale Input Voltage	0 dBFS		0.98		V rms
	0 dBFS		2.78		V p-p
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	Enhanced performance		106		dB
	Normal performance		106		dB
	Power saving		105		dB
	Voice wake-up		100		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		104		dB
	Normal performance		104		dB
	Power saving		103		dB
	Voice wake-up		98		dB
SNR[2]					
With A-Weighted Filter (RMS)	Enhanced performance		106		dB
	Normal performance		106		dB
	Power saving		104		dB
	Voice wake-up		99		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		103		dB
	Normal performance		103		dB
	Power saving		102		dB
	Voice wake-up		98		dB
Interchannel Gain Mismatch			40		mdB
THD + N	20 Hz to 20 kHz, −1 dB full-scale output				
	Enhanced performance		–95		dBFS
	Normal performance		–95		dBFS
	Power saving		–95		dBFS
	Voice wake-up		–95		dBFS
Offset Error			±0.2		mV
Gain Error			±0.2		dB
Interchannel Isolation	CM capacitor = 1 µF		100		dB
PSRR	CM capacitor = 1 µF				
	100 mV p-p at 1 kHz		70		dB
	100 mV p-p at 10 kHz		70		dB
SINGLE-ENDED PGA INPUT	PGAx_EN = 1				
Full-Scale Input Voltage	0 dBFS		0.49		V rms
	0 dBFS		1.39		V p-p

SPECIFICATIONS

Table 1. Analog Performance Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	Enhanced performance		100		dB
	Normal performance		100		dB
	Power saving		99		dB
	Voice wake-up		97		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		96		dB
	Normal performance		96		dB
	Power saving		96		dB
	Voice wake-up		94		dB
SNR[2]					
With A-Weighted Filter (RMS)	Enhanced performance		100		dB
	Normal performance		100		dB
	Power saving		99		dB
	Voice wake-up		97		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		96		dB
	Normal performance		96		dB
	Power saving		96		dB
	Voice wake-up		94		dB
THD + N	20 Hz to 20 kHz, −1 dBFS				
	Enhanced performance		−78		dBFS
	Normal performance		−78		dBFS
	Power saving		−78		dBFS
	Voice wake-up		−78		dBFS
PGA Gain Range		0		24	dB
PGA Gain Variation					
With 0 dB Setting	Standard deviation		0.05		dB
With 24 dB Setting	Standard deviation		0.15		dB
Interchannel Gain Mismatch			40		mdB
Offset Error			0.3		mV
Gain Error			±0.2		dB
Interchannel Isolation	CM capacitor = 1 µF		83		dB
PSRR	CM capacitor = 1 µF				
	100 mV p-p at 1 kHz		70		dB
	100 mV p-p at 10 kHz		50		dB
DIFFERENTIAL PGA INPUT	PGAx_EN = 1				
Full-Scale Input Voltage	0 dBFS		0.98		V rms
	0 dBFS		2.78		V p-p
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	Enhanced performance		103		dB
	Normal performance		103		dB
	Power saving		103		dB
	Voice wake-up		97		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		101		dB
	Normal performance		101		dB
	Power saving		100		dB
	Voice wake-up		96		dB
SNR[2]					
With A-Weighted Filter (RMS)	Enhanced performance		102		dB
	Normal performance		102		dB

SPECIFICATIONS

Table 1. Analog Performance Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	Power saving		102		dB
	Voice wake-up		97		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		100		dB
	Normal performance		100		dB
	Power saving		100		dB
	Voice wake-up		95		dB
THD + N	20 Hz to 20 kHz, −1 dBFS				
	Enhanced performance		–95		dBFS
	Normal performance		–95		dBFS
	Power saving		–95		dBFS
	Voice wake-up		–95		dBFS
PGA Gain Range		0		24	dB
PGA Gain Variation					
With 0 dB Setting	Standard deviation		0.05		dB
With 24 dB Setting	Standard deviation		0.15		dB
Interchannel Gain Mismatch			40		mdB
Offset Error			±0.2		mV
Gain Error			±0.2		dB
Interchannel Isolation	CM capacitor = 1 µF		100		dB
PSRR	CM capacitor = 1 µF				
	100 mV p-p at 1 kHz		70		dB
	100 mV p-p at 10 kHz		70		dB
DIGITAL-TO-ANALOG CONVERTERS (DACs)					
Internal Converter Resolution	All DACs		24		Bits
Digital Gain					
Step			0.375		dB
Range		–71.25		+24	dB
Ramp Rate			4.5		dB/ms
DAC DIFFERENTIAL OUTPUT	Differential operation				
Full-Scale Output Voltage	0 dBFS to DAC		1.0		V rms
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	Enhanced performance		110		dB
	Normal performance		106		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		107		dB
	Normal performance		103		dB
SNR[2]	20 Hz to 20 kHz				
With A-Weighted Filter (RMS)	Enhanced performance		110		dB
	Normal performance		106		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		106		dB
	Normal performance		103		dB
Output Noise	20 Hz to 20 kHz				
With A-Weighted Filter (RMS)			3.15		µV
THD + N Level	Line out mode				
10 kΩ Load	−1 dBFS input, normal performance		−93		dBV
	Headphone mode				
32 Ω Load	–15 dBFS input, output power (P_{OUT}) = 1 mW, enhanced performance		–96		dBV
	–15 dBFS input, P_{OUT} = 1 mW, normal performance		–85		dBV
	−1 dBFS input, enhanced performance		–82		dBV

SPECIFICATIONS

Table 1. Analog Performance Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	−1 dBFS input, normal performance		−80		dBV
24 Ω Load	−2 dBFS input, enhanced performance		−82		dBV
	−2 dBFS input, normal performance		−80		dBV
16 Ω Load	−3 dBFS input, enhanced performance		−82		dBV
	−3 dBFS input, normal performance		−80		dBV
Headphone Output Power					
32 Ω Load	AVDD = 1.8 V, <0.1% THD + N		30		mW
24 Ω Load	AVDD = 1.8 V, <0.1% THD + N		40		mW
16 Ω Load	AVDD = 1.8 V, <0.1% THD + N		50		mW
Gain Error			±2.5		%
DC Offset			±0.1		mV
PSRR	CM capacitor = 1 μF				
AVDD	100 mV p-p at 1 kHz		85		dB
	100 mV p-p at 10 kHz		85		dB
HPVDD_L (Low-Dropout (LDO) Bypass)	100 mV p-p at 1 kHz		90		dB
	100 mV p-p at 10 kHz		90		dB
AVDD Undervoltage Trip Point			1.5		V
CM REFERENCE	CM pin				
Output			0.85		V
Source Impedance			5		kΩ
PHASED-LOCKED LOOP (PLL)					
Input Frequency	After input prescale	0.03		36	MHz
Output Frequency		24	49.152	100	MHz
Fractional Limits	Fractional mode, fraction part (numerator (N)/denominator (M))	0.1		0.9	
Integer Limits	Fractional mode, integer part	2		3072	
Lock Time	32 kHz input		6.5		ms
	24.576 MHz input		0.46	0.55	ms
REGULATOR					
Line Regulation			1		mV/V
Load Regulation			0.5		mV/mA

[1] Dynamic range is the ratio of the sum of noise and harmonic power in the band of interest with a −60 dBFS signal present to the full-scale power level in decibels.

[2] SNR is the ratio of the sum of all noise power in the band of interest with no signal present to the full-scale power level in decibels.

CRYSTAL AMPLIFIER SPECIFICATIONS

Supply voltages: AVDD = IOVDD = 1.8 V, and DVDD = 0.9 V, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
JITTER		270	500	ps
FREQUENCY RANGE	1		36	MHz
LOAD CAPACITANCE			20	pF

SPECIFICATIONS

DIGITAL INPUT AND OUTPUT SPECIFICATIONS

–40°C < T_A < +105°C, and IOVDD = 1.1 V to 1.98 V, unless otherwise noted.

Table 3.

Parameter	Symbols	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE						
High	V_{IH}		0.7 × IOVDD			V
Low	V_{IL}				0.3 × IOVDD	V
	I_{IH}	IOVDD = 1.8 V, input high current (I_{IH}) at V_{IH} = 1.1 V			10	µA
	I_{IL}	Input low current (I_{IL}) at V_{IL} = 0.45 V			10	µA
OUTPUT VOLTAGE HIGH	V_{OH}					
Drive Strength						
Low		Output high current (I_{OH}) = 1 mA	0.7 × IOVDD	0.83 × IOVDD		V
High		Output high current (I_{OH}) = 2 mA	0.7 × IOVDD	0.83 × IOVDD		V
OUTPUT VOLTAGE LOW	V_{OL}					
Drive Strength						
Low		Output low current (I_{OL}) = 1 mA		0.1 × IOVDD	0.3 × IOVDD	V
High		Output low current (I_{OL}) = 2 mA		0.1 × IOVDD	0.3 × IOVDD	V
INPUT CAPACITANCE					5	pF

POWER SUPPLY SPECIFICATIONS

Supply voltages: AVDD = IOVDD = 1.8 V and DVDD = 0.9 V, unless otherwise noted. PLL disabled, direct main clock. Digital input/output (I/O) lines loaded with 25 pF.

Table 4. Power Supply Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLIES					
AVDD Voltage		1.7	1.8	1.98	V
DVDD Voltage		0.85	0.9	1.21	V
IOVDD Voltage		1.1	1.8	1.98	V
HPVDD_L Voltage		1.2		AVDD	V

POWER-DOWN CURRENT

Supply voltages: AVDD = IOVDD = 1.8 V and DVDD = 0.9 V and was externally supplied. PLL and crystal oscillator was disabled and bypassed.

Table 5. Power-Down Current

	AVDD Current			DVDD Current			IOVDD Current			HPVDD_L Current			
Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
POWER-DOWN CURRENT													
$\overline{PD}$ Pin Low (Hardware Power Down)		6.6			56.9			2.6			3		µA
PWR_MODE = 00													
CM_KEEP_ALIVE = 0		11			258			21			3		µA
CM_KEEP_ALIVE = 1		588			258			21			3		µA

SPECIFICATIONS

TYPICAL POWER CONSUMPTION

PLL bypassed with a main clock = 24.576 MHz (external oscillator). DVDD = 0.9 V, and AVDD = IOVDD = 1.8 V was supplied externally. Where applicable, ADC0 and ADC1 were run at 192 kHz, and ADC2 was run at 48 kHz. FastDSP™ was run at 192 kHz (biquad filters with 27-bit precision), and Tensilica DSP was run at 48 kHz. DAC was run at 192 kHz, and DAC_LPM = 0. One serial port input and output, configured as a subordinate, with a headphone load of 32 Ω was used. The DAC headphone amplifier (HPAMP) was in normal voltage mode. Quiescent current had no signal.

In Table 6, ASRCI and ASRCO are the input and output ports of the asynchronous sample rate converters, FIFO is first in, first out, DMIC is the digital microphone, and PDM is the pulse density modulation.

Table 6. Typical Power Consumption

ADC + PGA Channels	DAC Channels	ASRCI/ ASRCO Channels	FIFO and SRAM2	FastDSP Instructions	Equalizer Filters	DMIC/PDM Channels	Interpolator /Decimator Channels	AVDD Current (mA)	DVDD Current (mA)	IOVDD Current (mA)	HPVDD_L Current (mA)
0	1	1/0	N	0	13	0	0	0.99	1.09	0.15	0.003
2	1	0	N	32	13	0	0	2.18	1.87	0.15	0.003
2	1	1/0	N	32	13	0	0	2.18	2.54	0.15	0.003
1	1	1/1	N	0	13	0	0	1.76	1.30	0.22	0.003
3	1	1/3	N	32	13	0	0	2.58	3.04	0.315	0.003
1 (Voice Wake Up)	0	0	Y	0	0	0	0	1.46	1.56	0.15	0.003

Typical active noise canceling (ANC) settings (phone call with ANC). Main clock = 24.576 MHz (external oscillator and PLL bypassed). DVDD = 0.9 V, and AVDD = IOVDD = 1.8 V was supplied externally. The three ADCs were PGA enabled and configured for headphone input. The DAC was configured for differential headphone operation, and the DAC output was loaded with 32 Ω, and DAC_LPM = 0. One serial port input and output, configured as subordinate, was used. One input and three output ASRCs were used. FastDSP was run at 24.576 MHz, 32 instructions (biquad filters with 27-bit precision) at 192 kHz. Tensilica DSP was bypassed, quiescent current had no signal, and the input signal level was –15 dBFS.

Table 7. Typical ANC Power Consumption

			Typical Current (mA)						
Operating Voltage	Performance Setting	Power Mode	AVDD	DVDD	IOVDD	HPVDD_L	Total Power Consumption (mW)	Typical ADC THD + N, Differential Mode (dB FS)	Typical Headphone Output THD + N (dBV), 1 mW Output
AVDD = IOVDD = 1.8 V, DVDD = 0.9 V	High	Normal voltage	3.04	3.06	0.316	0.003	8.8	–95	Not applicable No load
			7.87	3.06	0.315	0.003	17.49	–95	–96
		Low voltage	2.76	3.06	0.316	0.286	8.63	–95	Not applicable No load
			2.76	3.06	0.316	5.093	14.4	–95	–96
	Normal	Normal voltage	2.58	3.06	0.316	0.003	7.97	–95	Not applicable No load
			7.41	3.06	0.316	0.003	16.66	–95	–85
		Low voltage	2.32	3.06	0.316	0.257	7.8	–95	Not applicable No load
			2.32	3.06	0.316	5.071	13.58	–95	–85

SPECIFICATIONS

DIGITAL FILTERS

Table 8. Digital Filters

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC INPUT TO DAC OUTPUT PATH					
Pass-Band Ripple	DC to 20 kHz, sampling frequency (f_S) = 192 kHz (ADCx_FCOMP = 1, and DAC_FCOMP = 1)			±0.02	dB
Group Delay	f_S = 192 kHz		12.9		µs
	f_S = 384 kHz		7.5		µs
	f_S = 768 kHz		5		µs
SAMPLE RATE CONVERTER					
Pass Band	FSYNC_x < 63 kHz			0.475 × f_S	kHz
	63 kHz < FSYNC_x < 112 kHz			0.4286 × f_S	kHz
	FSYNC_x > 112 kHz		0.2383 × f_S		kHz
Audio Band Ripple	20 Hz to 20 kHz	–0.1		+0.1	dB
Input and Output Sample Frequency Range		7		224	kHz
Dynamic Range	ASRCx_LPM = 0		130		dB
	ASRCx_LPM = 1		130		dB
	ASRCx_LPM_II = 1		130		dB
THD + Noise	20 Hz to 20 kHz, input is typical at 1 kHz and maximum at 20 kHz				
	ASCRx_LPM = 0		–130	–120	dBFS
	ASCRx_LPM = 1		–120	–110	dBFS
	ASCRx_LPM_II = 1		–115	–90	
Start-Up Time to Lock				25	ms
PDM OUTPUTS					
Dynamic Range	20 Hz to 20 kHz, with A-weighted filter		126		dBFS
THD + N	20 Hz to 20 kHz, –6 dBFS input		–125		dBFS

DIGITAL TIMING SPECIFICATIONS

−40°C < T_A < +105°C, IOVDD = 1.1 V to 1.8 V, and DVDD = 0.9 V to 1.1 V, unless otherwise noted.

Table 9. Digital Timing Specifications

	Limit			
Parameter	Min	Max	Unit	Description
MAIN CLOCK				MCLKIN period
t_{MPI}	0.037	33.3	µs	30 kHz to 36 MHz input clock using PLL in integer mode
t_{MPF}	0.037	1.0	µs	30 kHz to 36 MHz input clock using PLL in fractional mode
SERIAL PORT				
t_{BL}	18		ns	BCLK_x low pulse width (main and subordinate modes)
t_{BH}	18		ns	BCLK_x high pulse width (main and subordinate modes)
f_{BCLK}	0.512	24.576	MHz	BCLK_x frequency
t_{LS}	3		ns	FSYNC_x setup, time to BCLK_x rising (subordinate mode)
t_{LH}	5		ns	FSYNC_x hold, time from BCLK_x rising (subordinate mode)
f_{SYNC}	8	768[1]	kHz	FSYNC_x frequency
t_{SS}	3		ns	SDATAI_x setup, time to BCLK_x rising (main and subordinate modes)
t_{SH}	10		ns	SDATAI_x hold, time from BCLK_x rising (main and subordinate modes)
t_{TS}		6	ns	BCLK_x falling to FSYNC_x timing skew (main mode)
t_{SOD}	0	16	ns	SDATAO_x delay, time from BCLK_x falling (main and subordinate modes), IOVDD at 1.62 V minimum

SPECIFICATIONS

Table 9. Digital Timing Specifications (Continued)

Parameter	Limit Min	Limit Max	Unit	Description
	0	32	ns	SDATAO_x delay, time from BCLK_x falling (main and subordinate modes), IOVDD at 1.1 V minimum
t_{SOTD}	0	16	ns	BCLK_x falling to SDATAO_x driven in three-state mode
t_{SOTX}	0	16	ns	BCLK_x falling to SDATAO_x three-stated in three-state mode
SERIAL-PERIPHERAL INTERFACE (SPI) PORT				
f_{SCLK}		24	MHz	SCLK frequency
t_{CCPL}	15		ns	SCLK pulse width low
t_{CCPH}	15		ns	SCLK pulse width high
t_{CLS}	4		ns	$\overline{SS}$ setup, time to SCLK rising
t_{CLH}	18		ns	$\overline{SS}$ hold, time from SCLK rising
t_{CLPH}	10		ns	$\overline{SS}$ pulse width high
t_{CDS}	8		ns	MOSI setup, time to SCLK rising
t_{CDH}	6		ns	MOSI hold, time from SCLK rising
t_{COD}		17	ns	MISO delay, time from SCLK falling
t_{COTS}		24	ns	MISO high-Z, time from $\overline{SS}$ rising
I^2C PORT				
f_{SCL}		1	MHz	SCL frequency
t_{SCLH}	0.26		µs	SCL high
t_{SCLL}	0.5		µs	SCL low
t_{SCS}	0.26		µs	SCL rise setup time (to SDA falling), relevant for repeated START condition
t_{SCR}		120	ns	SCL and SDA rise time, C_{LOAD} = 400 pF
t_{SCH}	0.26		µs	SCL fall hold time (from SDA falling), relevant for START condition
t_{DS}	50		ns	SDA setup time (to SCL rising)
t_{SCF}		120	ns	SCL and SDA fall time, C_{LOAD} = 400 pF
t_{BFT}	0.5		µs	SCL rise setup time (to SDA rising), relevant for STOP condition
QSPI				
f_{QCLK}		50[2]	MHz	QSPIM_CLK frequency
UART				
		1.152	Mbps	Baud rate
GENERAL-PURPOSE INPUT/OUTPUT (GPIO) PINS				
t_{GIL}		1.5 × $1/f_S$	µs	MPx input latency, time until high or low value is read by core
t_{RLPW}	20		ns	$\overline{PD}$ low pulse width
DIGITAL MICROPHONE				
t_{CF}[3]		12	ns	Digital microphone clock fall time
t_{CR}[3]		14	ns	Digital microphone clock rise time
t_{SETUP}	10		ns	Digital microphone data-setup time
t_{HOLD}	3		ns	Digital microphone data-hold time
PDM OUTPUT				
f_{PDM_CLK}				PDM clock frequency
		3.072	MHz	3 MHz setting
		6.144	MHz	6 MHz setting
t_{CF}[3]		12	ns	Digital PDM clock output fall time
t_{CR}[3]		14	ns	Digital PDM clock output rise time
t_{HOLD}	35	46	ns	PDM data-hold time

SPECIFICATIONS

[1] Stereo, 16 bit per channel only at 768 kHz.

[2] Measured when IOVDD = 1.8 V house temperature.

[3] Digital microphone clock rise and fall times are measured at 2 mA drive strength with 25 pF load.

Digital Timing Diagrams

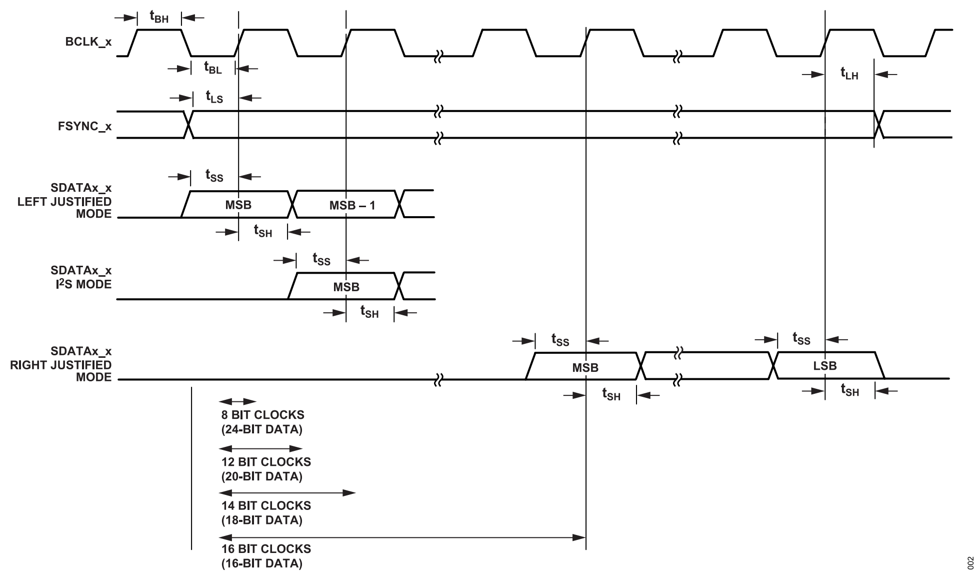

Figure 2. Serial Input Port Timing Diagram

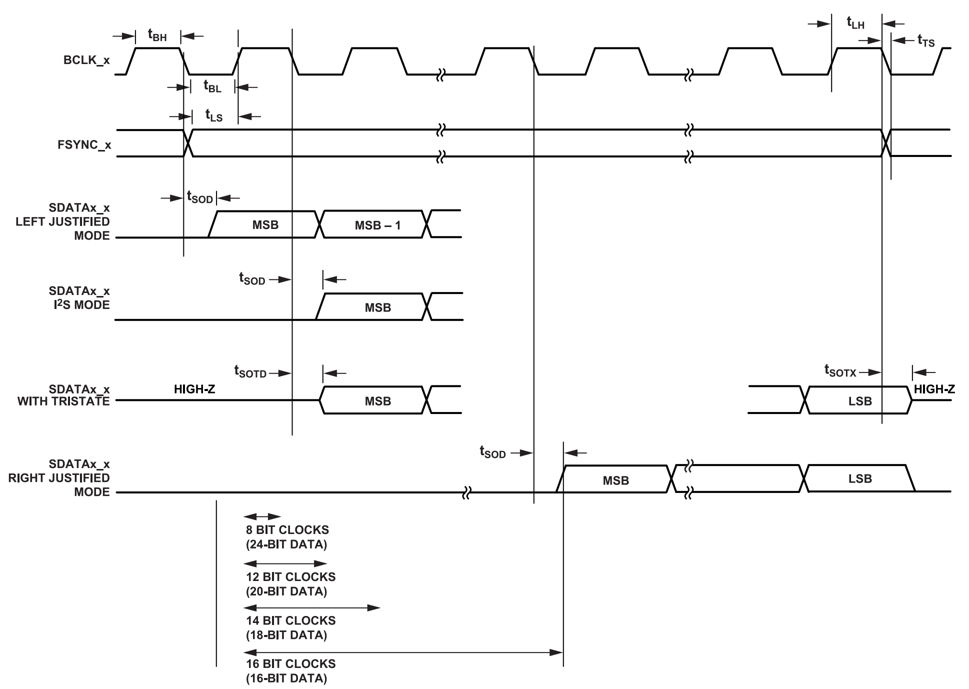

Figure 3. Serial Output Port Timing Diagram

SPECIFICATIONS

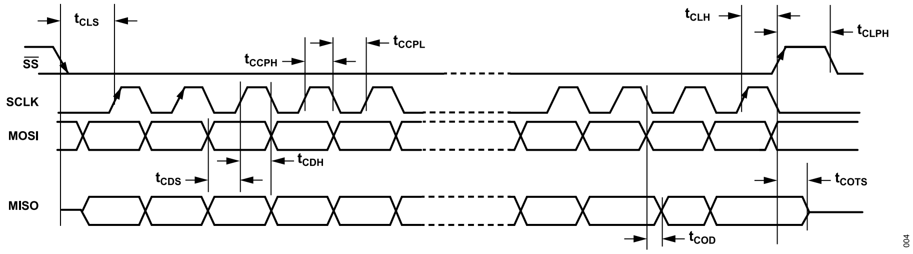

Figure 4. SPI Port Timing Diagram

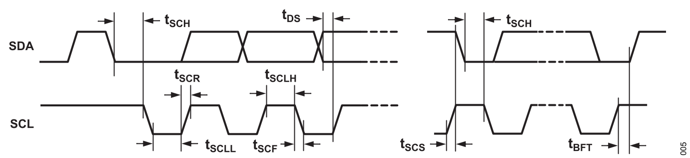

Figure 5. I²C Port Timing Diagram

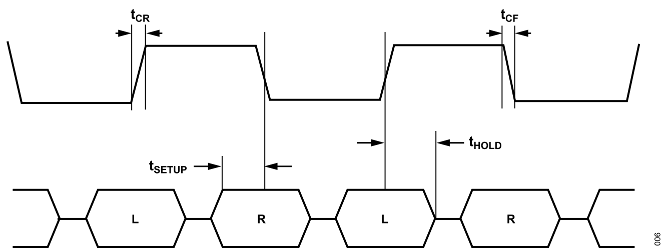

Figure 6. Digital Microphone Timing Diagram

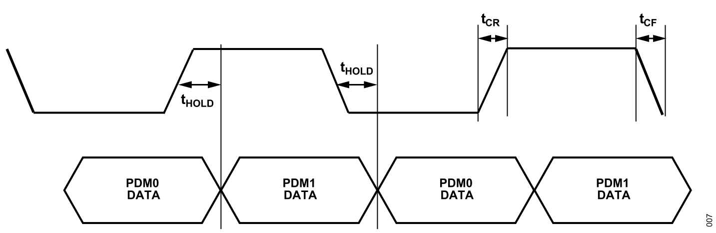

Figure 7. PDM Output Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 10. Absolute Maximum Ratings

Parameter	Rating
Power Supply (AVDD, IOVDD, and HPVDD_L)	−0.3 V to +1.98 V
Digital Supply (DVDD)	−0.3 V to +1.21 V
Input Current (Except Supply Pins)	±20 mA
Analog Input Voltage (Signal Pins)	−0.3 V to AVDD + 0.3 V
Digital Input Voltage (Signal Pins)	−0.3 to IOVDD + 0.3 V
Temperature	
Operating Range (Case)	−40°C to +105°C
Storage Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} and θ_{JC} are determined according to JESD-51-9 on a 4-layer PCB with natural convection cooling.

Table 11. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[1]	Unit
CS-64-2	38.5	8.7	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with two thermal vias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADAU1861

Table 12. ADAU1861, 64-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	1000	1C
CDM	500	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

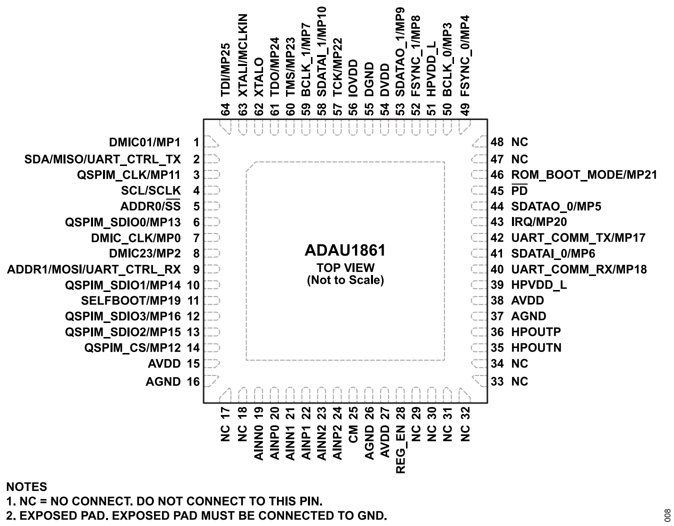

Figure 8. Pin Configuration (Top View)

Table 13. Pin Function Descriptions

Ball No.	Mnemonic	Type[1]	Description
1	DMIC01/MP1	D_IO	Digital Microphone Stereo Input 0 and Digital Microphone Stereo Input 1 (DMIC01). Multipurpose I/O 1 (MP1).
2	SDA/MISO/ UART_CTRL_TX	D_IO	I²C Data (SDA). The SDA pin is a bidirectional open-collector. The line connected to SDA must have a 2.0 kΩ pull-up resistor. SPI Data Output (MISO). This SPI data output is used for reading back registers and memory locations. MISO is three-stated when an SPI read is not active. UART Control Port Data Transmit and Output (UART_CTRL_TX).
3	QSPIM_CLK/MP11	D_IO	Quad Main SPI Clock (QSPIM_CLK). Multipurpose I/O 11 (MP11).
4	SCL/SCLK	D_IO	I²C Clock (SCL). The SCL pin is always an open-collector input when the device is in I²C control mode. The line connected to the SCL pin must have a 2.0 kΩ pull-up resistor. SPI Clock (SCLK). The SCLK pin can either run continuously or be gated off between SPI transactions.
5	ADDR0/$\overline{SS}$	D_IN	I²C Address 0 (ADDR0). SPI Latch Signal ($\overline{SS}$). $\overline{SS}$ must go low at the beginning of an SPI transaction and high at the end of a transaction. Each SPI transaction can take a different number of SCLK cycles to complete, depending on the address and read/write bit that are sent at the beginning of the SPI transaction.
6	QSPIM_SDIO0/MP13	D_IO	Quad Main SPI Data I/O 0 (QSPIM_SDIO0). Multipurpose I/O 13 (MP13).
7	DMIC_CLK/MP0	D_IO	Digital Microphone Clock Output (DMIC_CLK). Multipurpose I/O 0 (MP0).
8	DMIC23/MP2	D_IO	Digital Microphone Stereo Input 2 and Digital Microphone Stereo Input 3 (DMIC23). Multipurpose I/O 2 (MP2).
9	ADDR1/MOSI/ UART_CTRL_RX	D_IN	I²C Address 1 (ADDR1). SPI Data Input (MOSI). UART Control Port Data Receiver/Input (UART_CTRL_RX).
10	QSPIM_SDIO1/MP14	D_IO	Quad Main SPI Data Input/Output 1 (QSPIM_SDIO1). Multipurpose I/O 14 (MP14).
11	SELFBOOT/MP19	D_IO	Self Boot (SELFBOOT). Set SELFBOOT up to IOVDD at power-up to enable self-boot mode. Otherwise, set SELFBOOT to GND at start-up. Multipurpose I/O 19 (MP19).
12	QSPIM_SDIO3/MP16	D_IO	Quad Main SPI Data Input/Output 3 (QSPIM_SDIO3). Multipurpose I/O 16 (MP16).

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 13. Pin Function Descriptions (Continued)

Ball No.	Mnemonic	Type[1]	Description
13	QSPIM_SDIO2/MP15	D_IO	Quad Main SPI Data Input/Output 2 (QSPIM_SDIO2). Multipurpose I/O 15 (MP15).
14	QSPIM_CS/MP12	D_IO	Quad Main SPI Chip Select (QSPIM_CS). Multipurpose I/O 12 (MP12).
15	AVDD	PWR	1.8 V Analog Supply. Decouple AVDD to AGND with a 10 μF capacitor.
16	AGND	PWR	Analog Ground. The AGND and DGND pins can be tied together in a common ground plane.
17, 18, 29 to 34, 47, 48	NC		No Connect. Do not connect to this pin.
19	AINN0	A_IN	ADC0 Inverting Input.
20	AINP0	A_IN	ADC0 Noninverting Input.
21	AINN1	A_IN	ADC1 Inverting Input.
22	AINP1	A_IN	ADC1 Noninverting Input.
23	AINN2	A_IN	ADC2 Inverting Input.
24	AINP2	A_IN	ADC2 Noninverting Input.
25	CM	A_OUT	Common-Mode Reference Fixed at 0.85 V Nominal. A 1 μF decoupling capacitor must be connected between CM and ground to reduce crosstalk between the ADCs and DACs. The material of the capacitors is not critical. CM can be used to bias external analog circuits as long as these circuits are not drawing current from CM (for example, the noninverting input of an op amp).
26	AGND	PWR	Analog Ground. The AGND and DGND pins can be tied together in a common ground plane.
27	AVDD	PWR	1.8 V Analog Supply. Decouple AVDD to AGND with a 10 μF capacitor.
28	REG_EN	A_IN	Regulator Enable. Tie to AVDD to enable the internal regulator, and tie to ground to disable.
35	HPOUTN	A_OUT	Headphone Output Inverted.
36	HPOUTP	A_OUT	Headphone Output Noninverted.
37	AGND	PWR	Analog Ground. The AGND and DGND pins can be tied together in a common ground plane.
38	AVDD	PWR	1.8 V Analog Supply. Decouple AVDD to AGND with a 10 μF capacitor.
39	HPVDD_L	PWR	Power Supply for the Internal LDO Regulator and Headphone Amplifier Power. Decouple HPVDD_L to HPGND with a 10 μF capacitor.
40	UART_COMM_RX/MP18	D_IO	Communication UART Port Data Receiver/Input (UART_COMM_RX). Multipurpose I/O 18 (MP18).
41	SDATAI_0/MP6	D_IO	Serial Audio Port 0 Input Data (SDATAI_0). Multipurpose I/O 6 (MP6).
42	UART_COMM_TX/MP17	D_IO	Communication UART Port Data Transmit/Output (UART_COMM_TX). Multipurpose I/O 17 (MP17).
43	IRQ/MP20	D_IO	Interrupt Input/Output (IRQ). Multipurpose I/O 20 (MP20).
44	SDATAO_0/MP5	D_IO	Serial Audio Port 0 Output Data (SDATAO_0). Multipurpose I/O 5 (MP5).
45	$\overline{\text{PD}}$	D_IO	Active-Low Power Down. All digital and analog circuits are powered down. There is an internal pull-down resistor on the $\overline{\text{PD}}$ pin; therefore, the ADAU1861 is held in power-down mode if its input signal is floating while power is applied to the supply pins.
46	ROM_BOOT_MODE/MP21	D_IO	ROM Boot_Up Mode (ROM_BOOT_MODE). Use Boot-Up Mode 1 when connecting to IOVDD and use Boot-Up Mode 2 when connecting to ground. Multipurpose IO 21 (MP21).
49	FSYNC_0/MP4	D_IO	Serial Audio Port 0 Frame Sync/Left Right Clock (FSYNC_0). Multipurpose I/O 4 (MP4).
50	BCLK_0/MP3	D_IO	Serial Audio Port 0 Bit Clock (BCLK_0). Multipurpose I/O 3 (MP3).
51	HPVDD_L	PWR	Power Supply for the Internal LDO Regulator and Headphone Amplifier Power. Decouple HPVDD_L to HPGND with a 10 μF capacitor.
52	FSYNC_1/MP8	D_IO	Serial Audio Port 1 Frame Sync/Left Right Clock (FSYNC_1).

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 13. Pin Function Descriptions (Continued)

Ball No.	Mnemonic	Type[1]	Description
			Multipurpose I/O 8 (MP8).
53	SDATAO_1/MP9	D_IO	Serial Audio Port 1 Output Data (SDATAO_1).
			Multipurpose I/O 9 (MP9).
54	DVDD	PWR	Digital Core Supply. The digital supply can be generated from an on-board regulator or supplied directly from an external supply. In each case, decouple DVDD to DGND with a 1 uF and 0.1 µF capacitor.
55	DGND	PWR	Digital Ground. The AGND and DGND pins can be tied together in a common ground plane.
56	IOVDD	PWR	Supply for Digital Input and Output Pins. The digital output pins are supplied from IOVDD, and this sets the highest input voltage that can be seen on the digital-input pins. The current draw of IOVDD is variable because it is dependent on the loads of the digital outputs. Decouple IOVDD to DGND with a 0.1 µF capacitor at least.
57	TCK/MP22	D_IO	JTAG Port Clock Input (TCK).
			Multipurpose I/O 22 (MP22).
58	SDATAI_1/MP10	D_IO	Serial Audio Port 1 Input Data (SDATAI_1).
			Multipurpose I/O 10 (MP10).
59	BCLK_1/MP7	D_IO	Serial Audio Port 1 Bit Clock (BCLK_1).
			Multipurpose I/O 7 (MP7).
60	TMS/MP23	D_IO	JTAG Port Mode Selection (TMS).
			Multipurpose I/O 23 (MP23).
61	TDO/MP24	D_IO	JTAG Port Data Output (TDO).
			Multipurpose I/O 24 (MP24).
62	XTALO	A_OUT	Crystal Clock Output. The XTALO pin is the output of the crystal amplifier and must not be used to provide a clock to other ICs in the system.
63	XTALI/MCLKIN	A_IN	Crystal Clock Input (XTALI).
			Main Clock Input (MCLKIN).
64	TDI/MP25	D_IO	JTAG Port Data Input (TDI).
			Multipurpose I/O 25 (MP25).
	EPAD		Exposed Pad. Exposed pad must be connected to GND.

[1] D_IO means digital input/output, D_IN means digital input, PWR means power, A_IN means analog input, and A_OUT means analog output.

TYPICAL PERFORMANCE CHARACTERISTICS

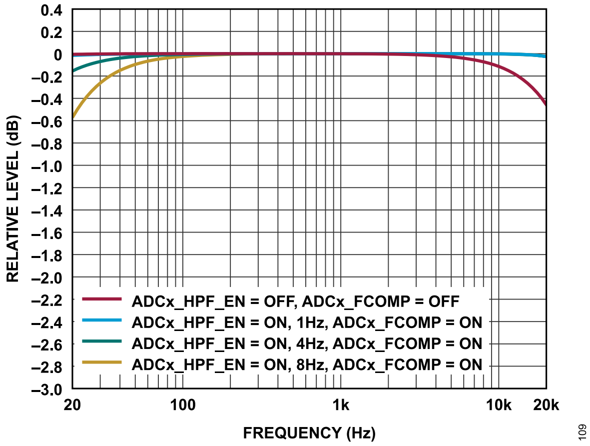

Figure 9. Frequency Response, f_S = 48 kHz, −20 dBV Input, Signal Path = AINxx to SDATAO_x, Differential Mode, No PGA

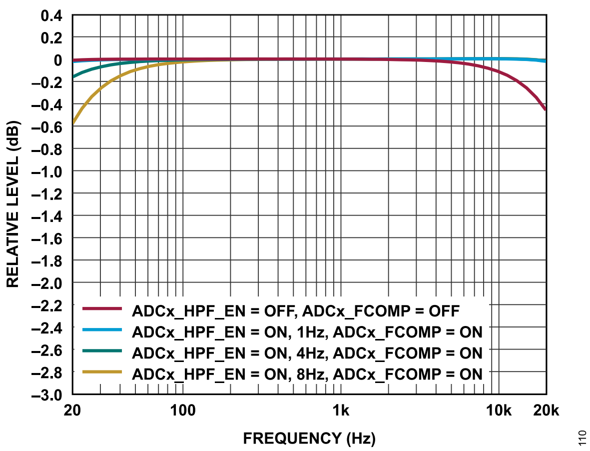

Figure 10. Frequency Response, f_S = 48 kHz, −20 dBV Input, Signal Path = AINxx to SDATAO_x, Single-End Mode, No PGA

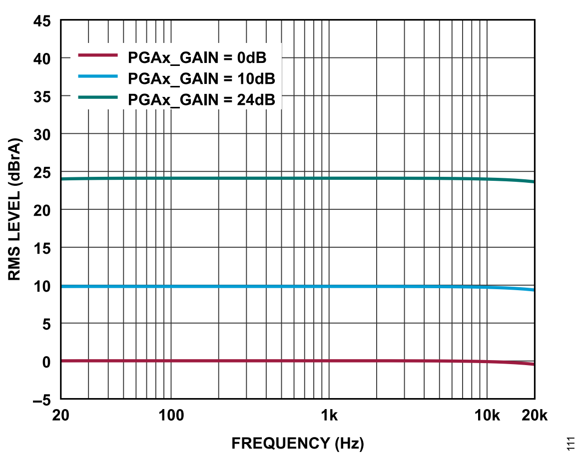

Figure 11. Frequency Response, f_S = 48 kHz, Signal Path = AINxx to SDATAO_x, Differential Mode, Output Relative to PGA Gain Settings (0 dB, 10 dB, and 24 dB), ADCx_FCOMP Off

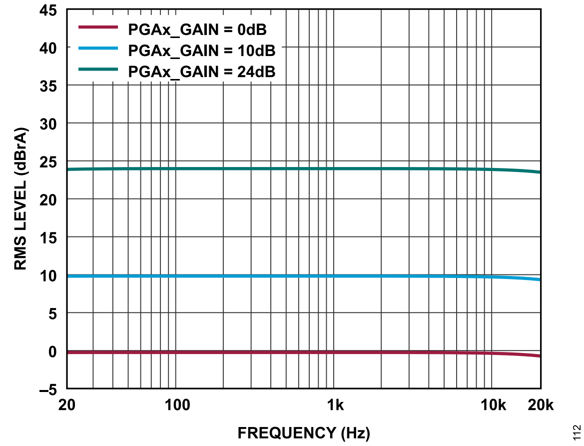

Figure 12. Frequency Response, f_S = 48 kHz, Signal Path = AINxx to SDATAO_x, Single-End Mode, Output Relative to PGA Gain Settings (0 dB, 10 dB, and 24 dB), ADCx_FCOMP Off

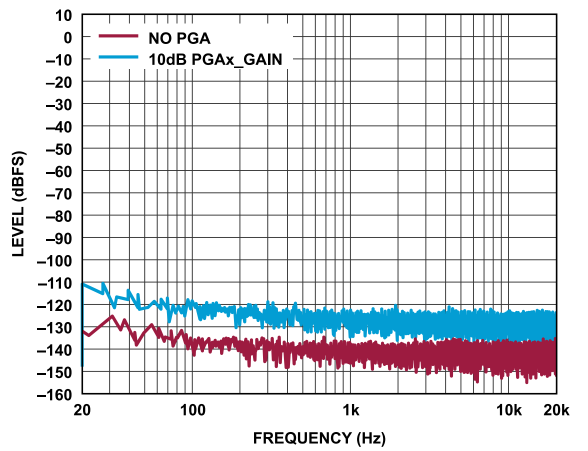

Figure 13. Fast Fourier Transform (FFT), No Signal, f_S = 48 kHz, Signal Path = AINxx to SDATAO_x, Differential Mode, No PGA, and 10 dB PGAx_GAIN

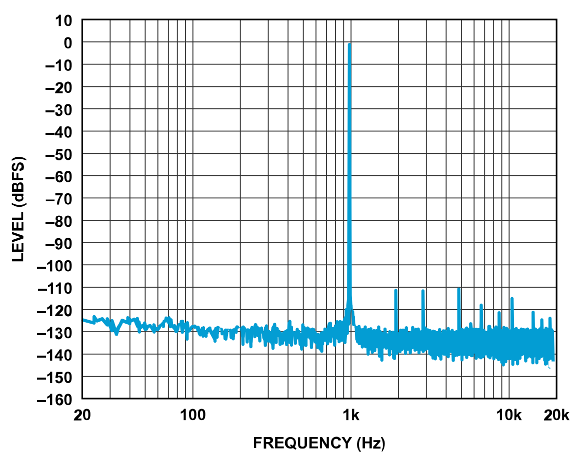

Figure 14. FFT, −1 dBV Input, −1 dBFS Output, f_S = 48 kHz, Signal Path = AINxx to SDATAO_x, Differential Mode, No PGA

TYPICAL PERFORMANCE CHARACTERISTICS

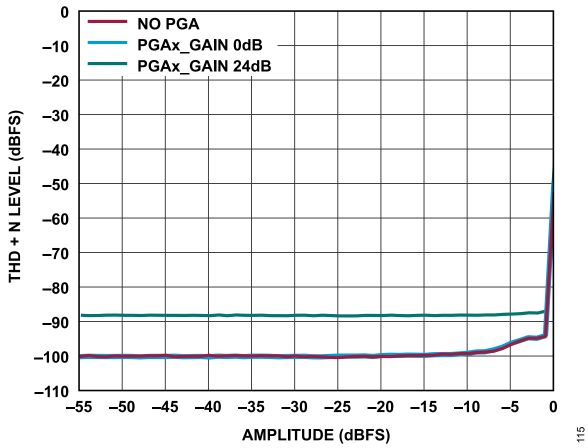

Figure 15. THD + N Level vs. Amplitude, f_S = 48 kHz, Signal Path = AINxx to SDATAO_x

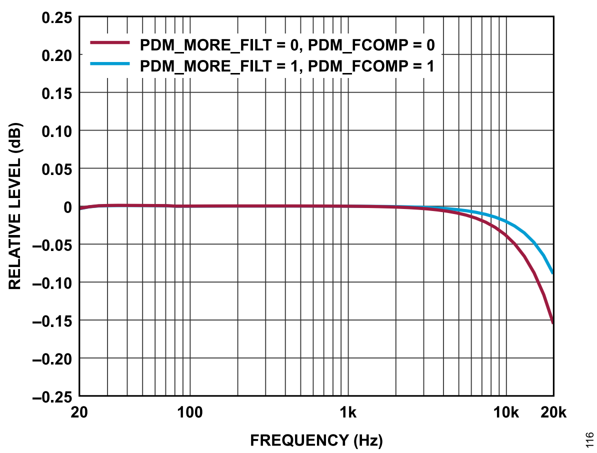

Figure 16. Frequency Response, f_S = 48 kHz, Signal Path = SDATAI_x to PDM Output

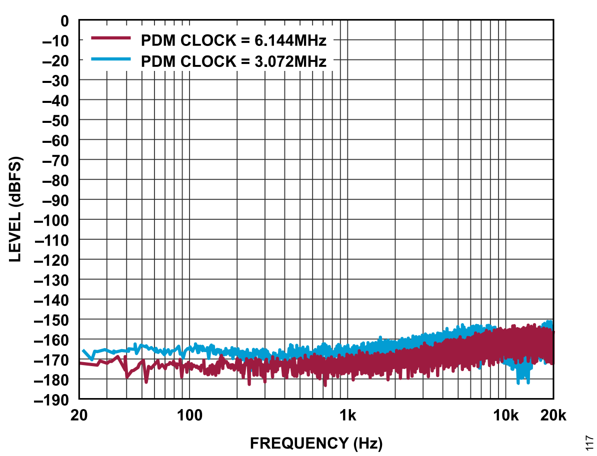

Figure 17. FFT, No Signal, f_S = 48 kHz Throughout, Signal Path = SDATAI_x to FastDSP to PDM Output

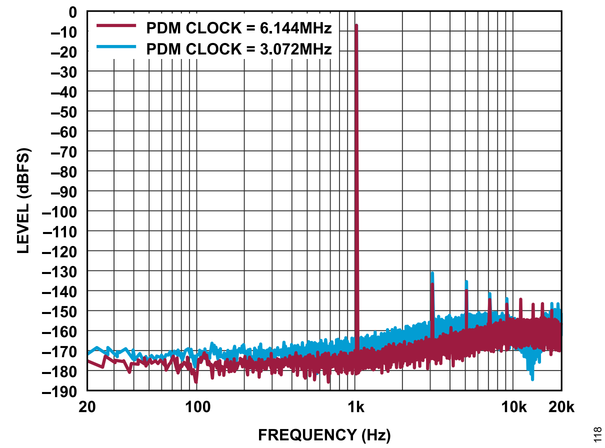

Figure 18. FFT, −7 dBFS, f_S = 48 kHz Throughout, Signal Path = SDATAI_x to FastDSP to PDM Output

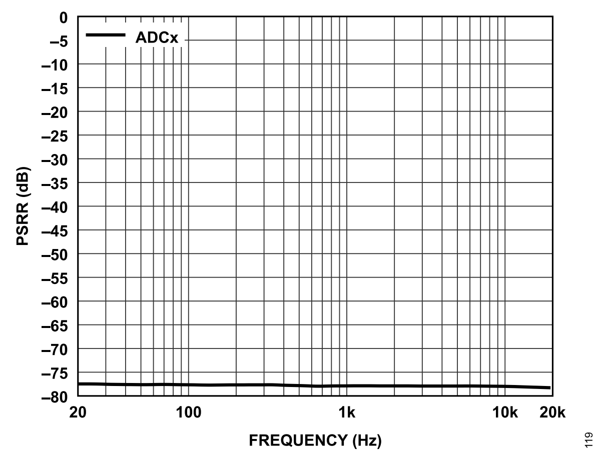

Figure 19. PSRR, Signal Path = AINxx to SDATAO_x, f_S = 48 kHz, 100 mV p-p Ripple Input on AVDD, No PGA

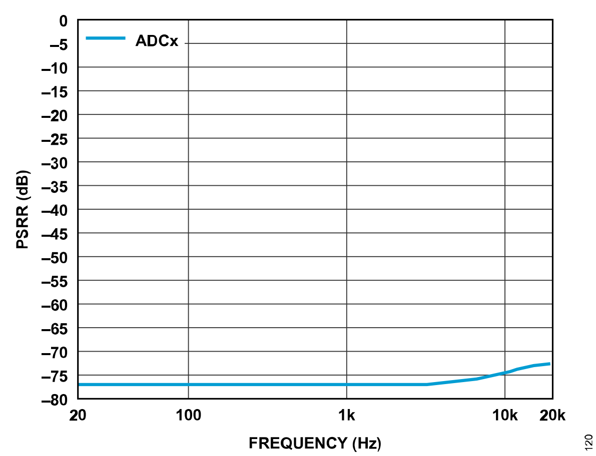

Figure 20. PSRR, Signal Path = AINxx to SDATAO_x, f_S = 48 kHz, 100 mV p-p Ripple Input on AVDD, PGA = 0 dB

TYPICAL PERFORMANCE CHARACTERISTICS

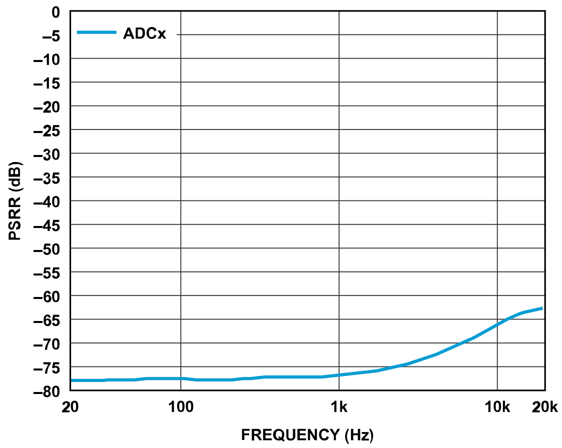

Figure 21. PSRR, Signal Path = AINxx to SDATAO_x, f_S = 48 kHz, 100 mV p-p Ripple Input on AVDD, PGA = 10 dB

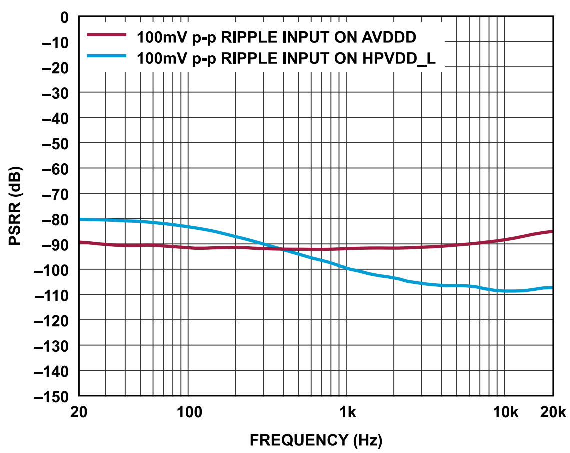

Figure 22. PSRR, Signal Path = SDATAI_x to HPOUT, f_S = 48 kHz, 100 mV p-p Ripple Input on AVDD or HPVDD_L (LDO Bypass)

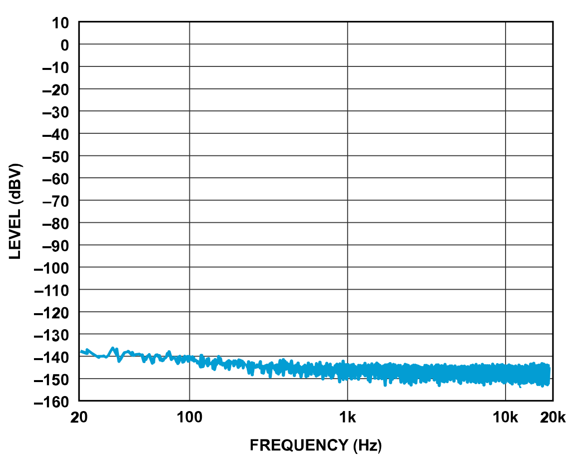

Figure 23. FFT, No Signal, f_S = 48 kHz, Signal Path = SDATAI_x to HPOUT, Headphone Mode, Load = 32 Ω

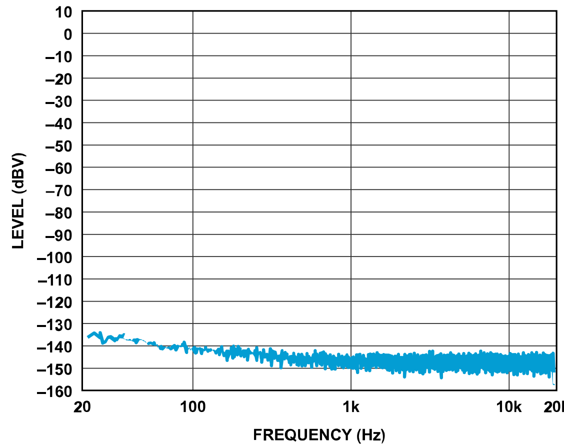

Figure 24. FFT, No Signal, f_S = 48 kHz, Signal Path = SDATAI_x to the Output of the DAC Working in Line Output Mode (LOUT), Load = 10 kΩ

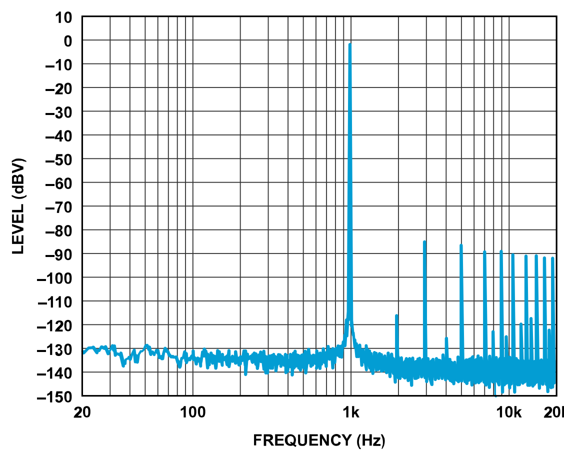

Figure 25. FFT, −1 dBFS, f_S = 48 kHz, Signal Path = SDATAI_x to the Output of the DAC Working in Headphone Mode (HPOUT), Load = 32 Ω

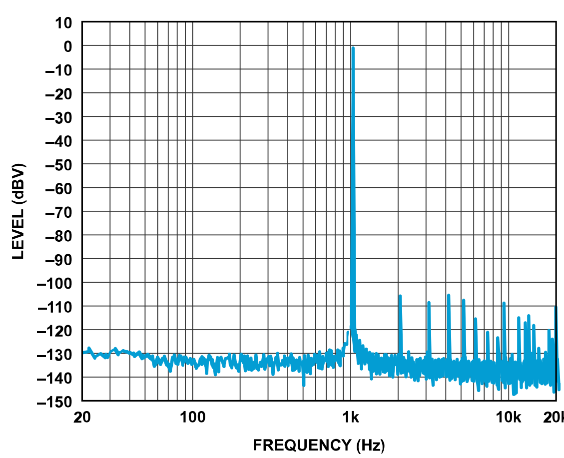

Figure 26. FFT, −1 dBFS, f_S = 48 kHz, Signal Path = SDATAI_x to LOUT Line Output Mode, Load = 10 kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

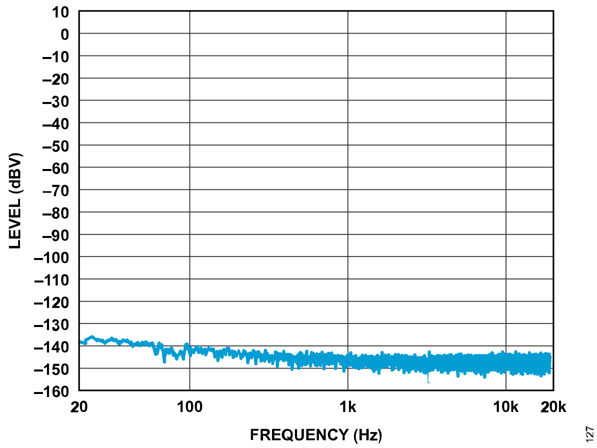

Figure 27. FFT, No Signal, f_S = 768 kHz, Signal Path = SDATAI_x to Interpolator to FastDSP to HPOUT, Headphone Mode, Load = 32 Ω

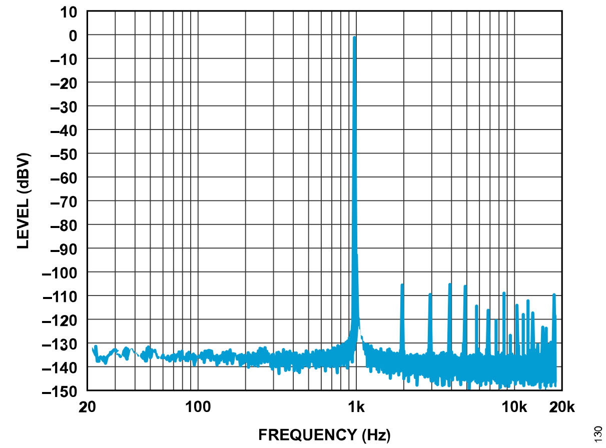

Figure 30. FFT, −1 dBFS, f_S = 768 kHz, Signal Path = SDATAI_x to Interpolator to FastDSP to LOUT, Line Output Mode, Load = 10 kΩ

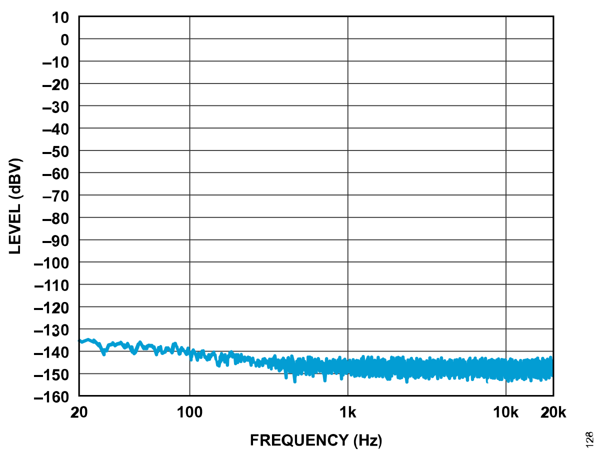

Figure 28. FFT, No Signal, f_S = 768 kHz, Signal Path = SDATAI_x to Interpolator to FastDSP to LOUT, Line Output Mode, Load = 32 Ω

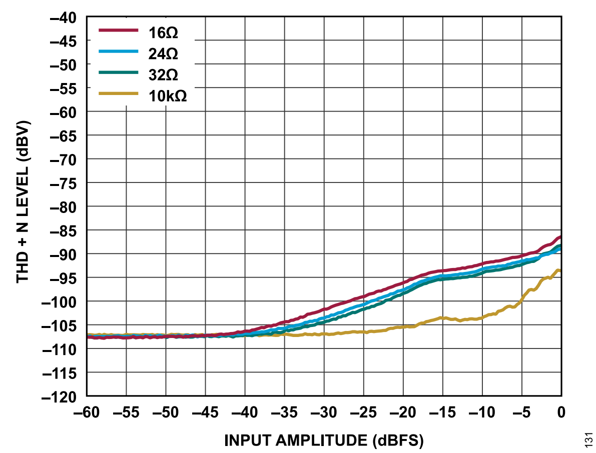

Figure 31. THD + N Level vs. Input Amplitude, f_S = 48 kHz, 16 Ω, 24 Ω, 32 Ω, or 10 kΩ (Normal), Signal Path = SDATAI_x to HPOUT/LOUT

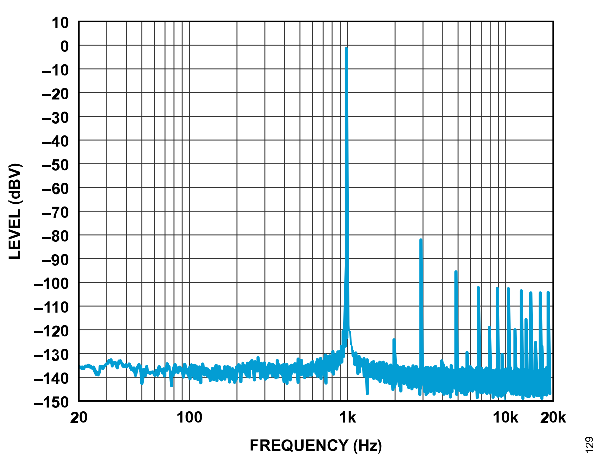

Figure 29. FFT, −1 dBFS, f_S = 768 kHz, Signal Path = SDATAI_x to Interpolator to FastDSP to HPOUT, Headphone Mode, Load = 32 Ω

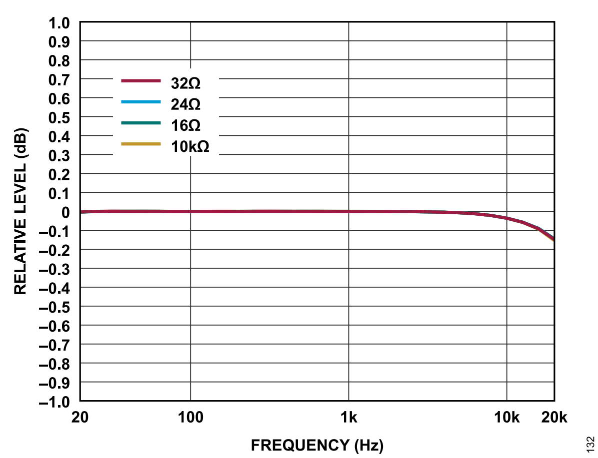

Figure 32. Relative Level vs. Frequency, f_S = 48 kHz, Signal Path = SDATAI_x to HPOUT/LOUT, 16 Ω, 24 Ω, 32 Ω, or 10 kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

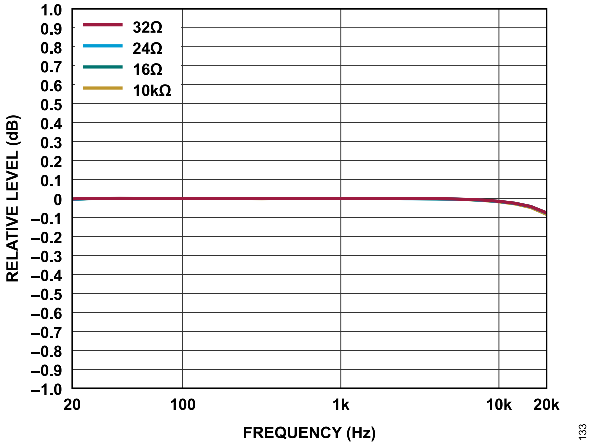

Figure 33. Relative Level vs. Frequency, f_S = 768 kHz, Signal Path = SDATAI_x to Interpolator to FastDSP to HPOUT/LOUT, 16 Ω to 10 kΩ

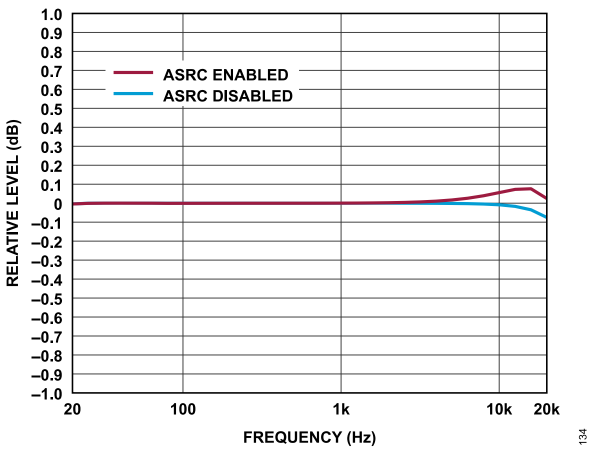

Figure 34. Relative Level vs. Frequency, f_S = 48 kHz Throughout Except FastDSP = 768 kHz, Signal Path = SDATAI_x to ASRCI to Equalizer to Interpolator to FastDSP to Decimator to ASRCO to SDATAO_x

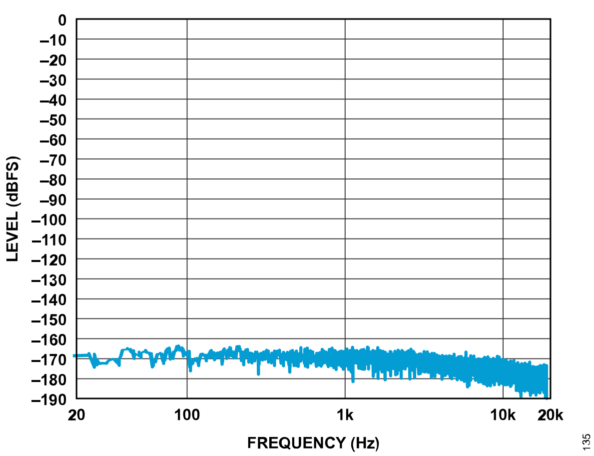

Figure 35. FFT, No Signal, f_S = 48 kHz Throughout Except FastDSP = 768 kHz, Signal Path = SDATAI_x to ASRCI to Equalizer to Interpolator to FastDSP to Decimator to ASRCO to SDATAO_x

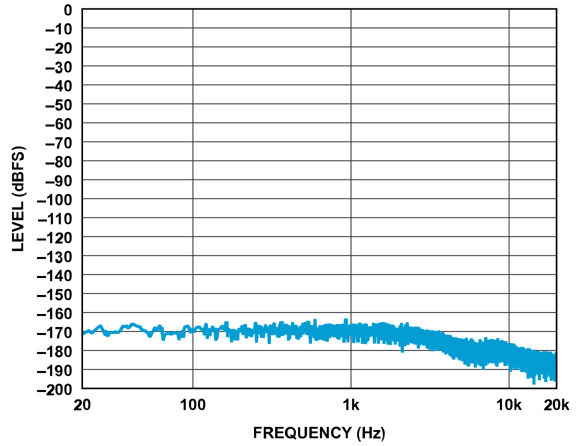

Figure 36. FFT, No Signal, f_S = 48 kHz Throughout Except FastDSP = 768 kHz, Signal Path = SDATAI_x to Equalizer to Interpolator to FastDSP to Decimator to SDATAO_x

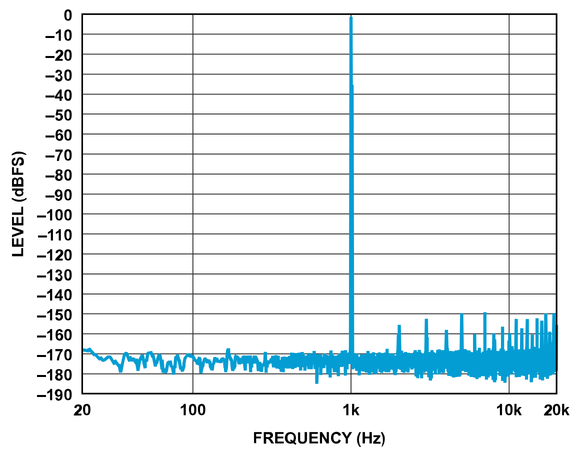

Figure 37. FFT, –1 dBFS Input, f_S = 48 kHz Throughout Except FastDSP = 768 kHz, Signal Path = SDATAI_x to ASRCI to Equalizer to Interpolator to FastDSP to Decimator to ASRCO to SDATAO_x

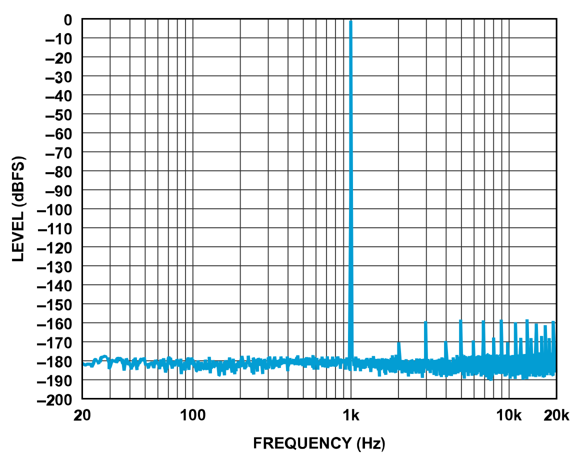

Figure 38. FFT, –1 dBFS Input, f_S = 48 kHz Throughout Except FastDSP = 768 kHz, Signal Path = SDATAI_x to Equalizer to Interpolator to FastDSP to Decimator to SDATAO_x

TYPICAL PERFORMANCE CHARACTERISTICS

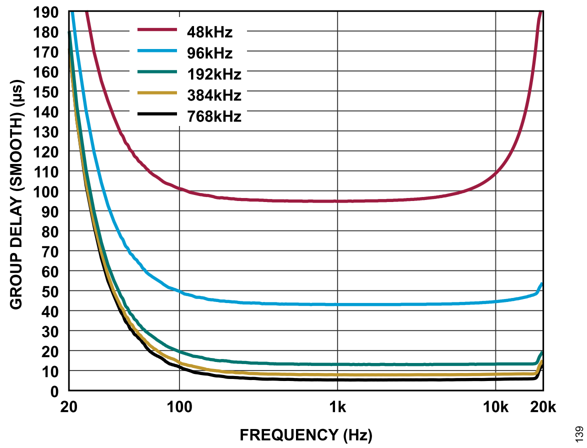

Figure 39. Group Delay (Smooth) vs. Frequency, f_S = 48 kHz to 768 kHz, Differential Mode, Signal Path = AINxx to FastDSP to HPOUT/LOUT

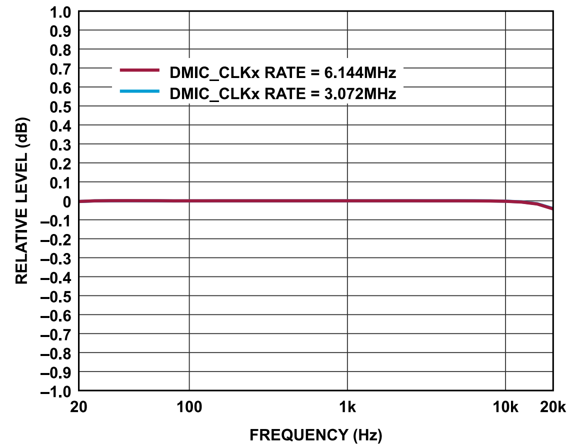

Figure 42. Relative Level vs. Frequency, DMIC_CLK_RATE = 3.072 MHz and 6.144 MHz, Signal Path = DMICxx to SDATAO_x, FCOMP = EN

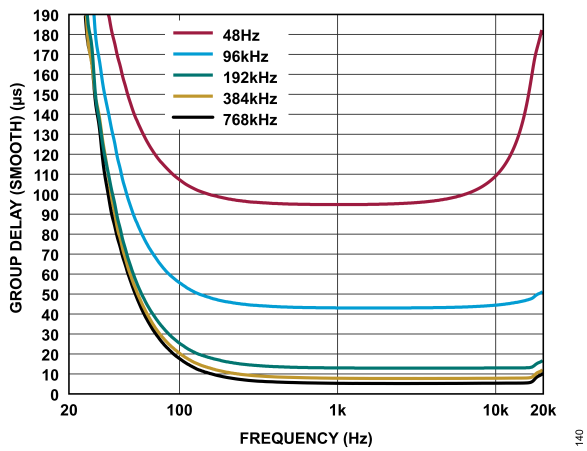

Figure 40. Group Delay (Smooth) vs. Frequency, f_S = 48 kHz to 768 kHz, Single-End Mode, Signal Path = AINxx to FastDSP to HPOUT/LOUT

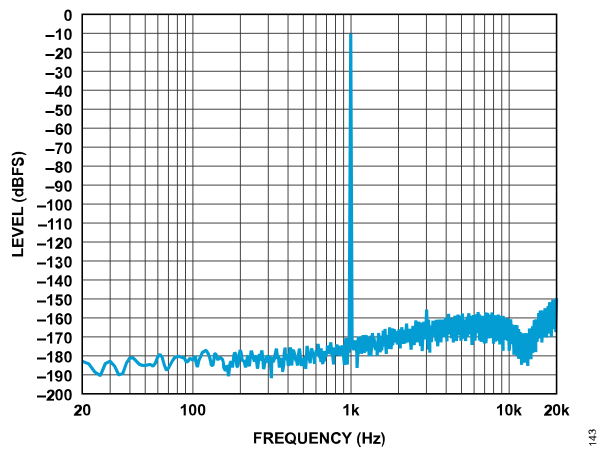

Figure 43. FFT, −10 dBFS Input, DMIC_CLK_RATE = 3.072 MHz, Signal Path = DMICxx to SDATAO_x

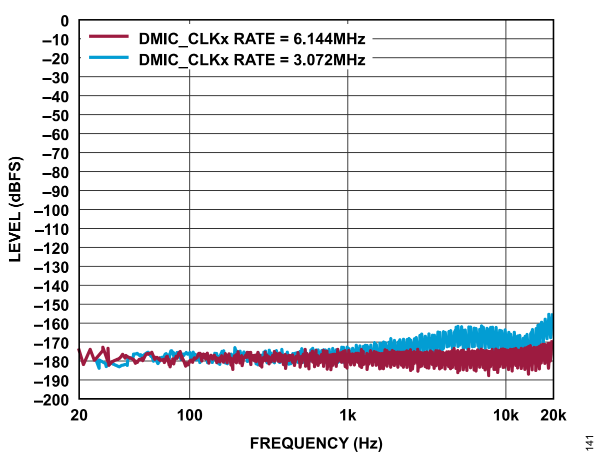

Figure 41. FFT, No Signal, DMIC_CLK_RATE = 3.072 MHz and 6.144 MHz, Signal Path = DMICxx to SDATAO_x

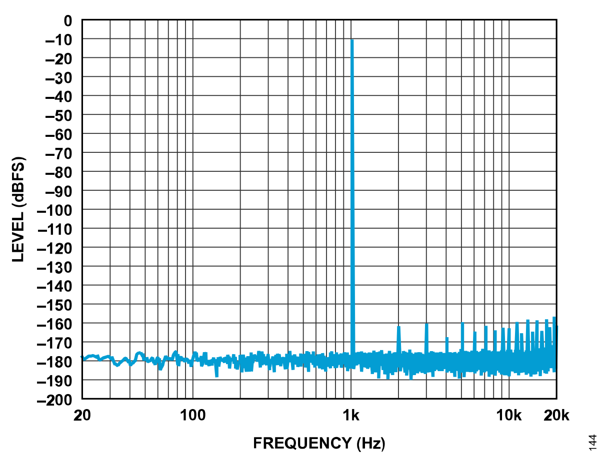

Figure 44. FFT, −10 dBFS Input, DMIC_CLK_RATE = 6.144 MHz, Signal Path = DMICxx to SDATAO_x

TYPICAL PERFORMANCE CHARACTERISTICS

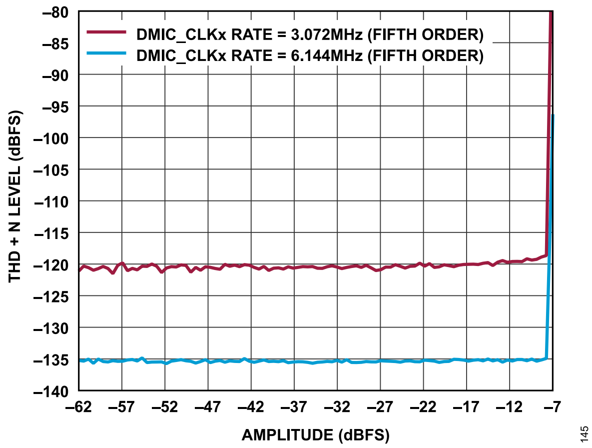

Figure 45. THD + N Level vs. Amplitude, −10 dBFS, DMIC_CLK_RATE = 3.072 MHz and 6.144 MHz (Fifth-Order), Signal Path = DMICxx to SDATAO_x

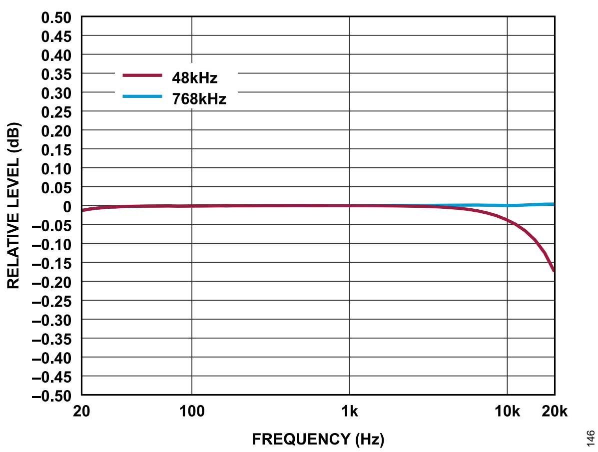

Figure 46. Relative Level vs. Frequency, Differential and Single-End Mode, Headphone and Line Output Mode, Load = 16 Ω to 10 kΩ, f_S = 48 kHz and 768 kHz, Signal Path = AIN0 to DAC

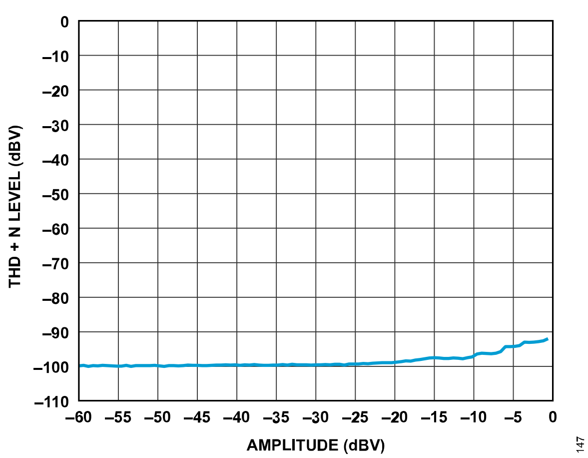

Figure 47. THD + N Level vs. Amplitude, f_S = 48 kHz to 768 kHz, Load = 10 kΩ, Signal Path = AINx to HPOUT/LOUT

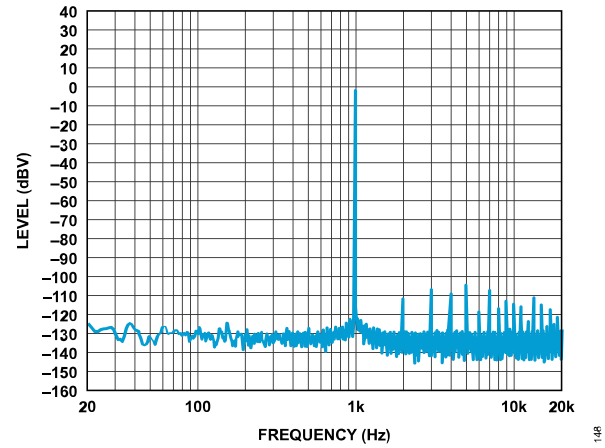

Figure 48. FFT, −1 dBV Input, Differential Mode, Line Output Mode, Load = 10 kΩ, f_S = 48 kHz to 768 kHz, Signal Path = AINx to LOUT

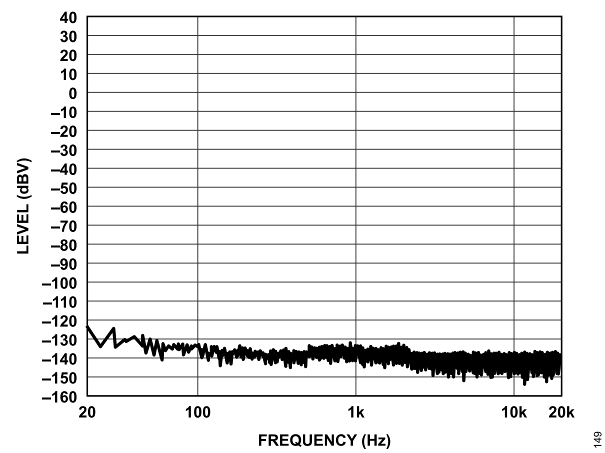

Figure 49. FFT, No Signal, Differential Mode, Load = 32 Ω to 10 kΩ, f_S = 48 kHz to 768 kHz, Signal Path = AINx to HPOUT/LOUT

THEORY OF OPERATION

The ADAU1861 is a low-power audio codec with an optimized audio processing core, making it ideal for noise canceling applications that require high quality audio, low-power, small size, and low latency. The two serial audio ports are compatible with I^2S, left-justified, right-justified, and time division multiplexing (TDM) modes, with three-state for interfacing to digital audio data. The analog operating voltage is 1.8 V, and an optional internal regulator can be used to generate the digital supply voltage. If required, the regulator can be powered down, and the digital supply voltage can be supplied externally, which is determined by the REG_EN pin.

The input signal path includes flexible configurations that can accept differential or single-ended analog microphone inputs as well as up to eight digital microphone inputs. Each input signal has its own PGA for volume adjustment.

The ADCs and DAC are high quality, 24-bit Σ-Δ converters that operate at a selectable sampling rate, and the ADCs also support an 8 kHz or a 16 kHz sampling rate in voice wake-up mode. The ADCs and DAC have an optional high-pass filter with a cutoff frequency and fine step digital soft volume controls.

The DAC output is capable of differentially driving a headphone earpiece speaker with 16 Ω impedance or higher. There is also the option to change to LOUT mode when the output is lightly loaded.

The Tensilica HiFi 3z DSP core is optimized for low-power audio processing. In addition, the Tensilica HiFi 3z DSP core allows the ADAU1861 to provide flexible solutions to meet more complicated applications.

The FastDSP core has a reduced instruction set that optimizes this codec for noise cancellation. The program and parameter random access memories (RAMs) can be loaded with custom audio processing signal flow built using the Lark Studio graphical user interface (GUI). The values stored in the parameter RAM control individual signal processing blocks.

The ADAU1861 also has a self boot function that can load the program and parameter RAMs of both cores along with the register settings on power-up using an external flash memory over the quad SPI. The external flash memory is fully memory mapped to the HiFi 3z DSP core bus fabric.

Use the Lark Studio GUI to program and control the cores through the control port. Along with designing and tuning a signal flow, the GUI can configure all of the ADAU1861 registers. The GUI allows anyone with digital or analog audio processing knowledge to design the DSP signal flow and export the flow to a target application. The interface also provides enough flexibility and programmability for an experienced DSP programmer to have control of the design. In the Lark Studio GUI, the user can connect graphical blocks (such as biquad filters, volume controls, and arithmetic operations), compile the design, and load the program and parameter files into the ADAU1861 memory through the control port. The tool also allows the user to download the design to an external flash memory for self boot operation.

The ADAU1861 can generate the internal clocks from a wide range of input clocks by using the on-board bypassable fractional PLL. The PLL accepts inputs from 30 kHz to 36 MHz. For standalone operation, the clock can be generated using the on-board crystal oscillator.

The ADAU1861 is provided in Figure 51.

APPLICATIONS INFORMATION

POWER-SUPPLY BYPASS CAPACITORS

Bypass each analog and digital power-supply pin to its nearest appropriate ground pin with a single 0.1 µF capacitor. In Figure 50, VDD refers to all power supplies (DVDD, IOVDD, AVDD, and HPVDD_L). Keep the connections to each side of the capacitor as short as possible, and route the trace on a single layer with no vias. For maximum effectiveness, place the capacitor equidistant from the power and ground pins or slightly closer to the power pin if equidistant placement is not possible. Make thermal connections to the ground planes on the far side of the capacitor.

Bypass each supply signal on the PCB with a single bulk capacitor (10 µF to 47 µF).

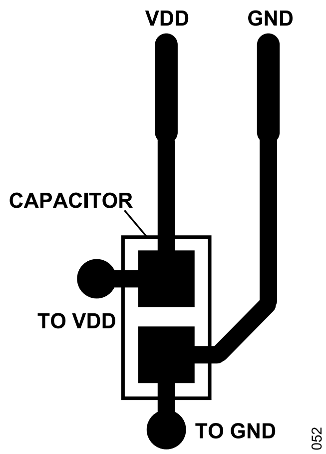

Figure 50. Recommended Power-Supply Bypass Capacitor Layout

LAYOUT

The AVDD and HPVDD_L supplies are for the headphone amplifiers. If the headphone amplifiers are enabled, the PCB traces to the AVDD and HPVDD_L pins must be wider than the traces to the other pins to increase the current carrying capacity. Use a wider trace for the headphone output lines.

GROUNDING

Use a single ground plane in the application layout. Place components in an analog signal path away from digital signals.

OUTLINE DIMENSIONS

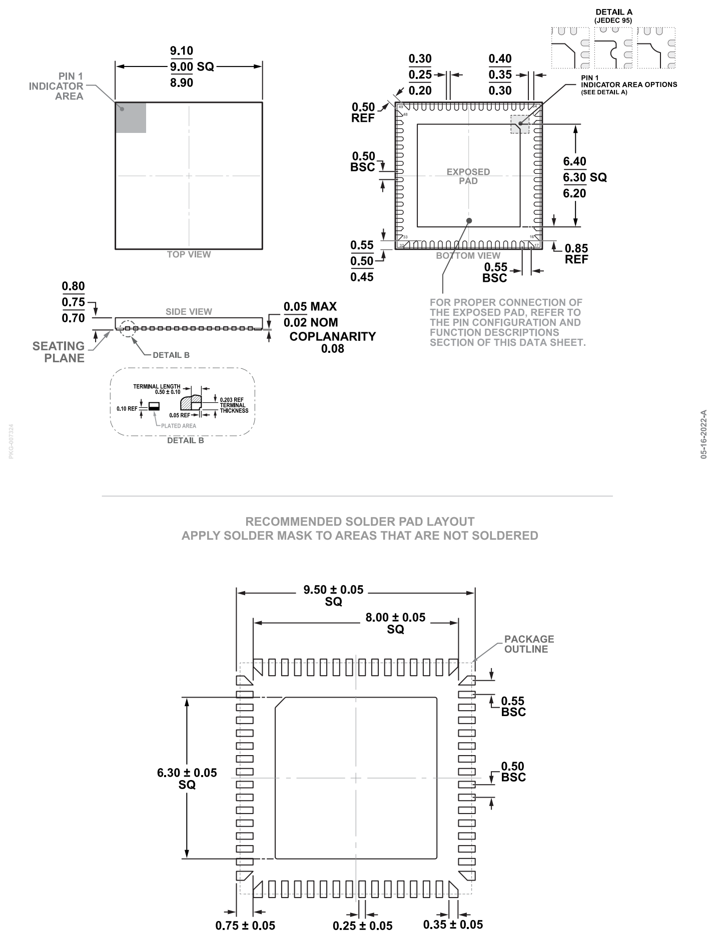

Figure 51. 64-Lead Lead Frame Chip Scale Package [LFCSP_SS]
9 mm × 9 mm Body, With Side Solderable Leads
(CS-64-2)
Dimensions shown in millimeters

Updated: October 18, 2023

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADAU1861BCSZ-RL	-40°C to +105°C	64-lead LFCSP-SS (Side Solderable) (9 mm x 9 mm x 0.75 mm)	Reel, 2500	CS-64-2
ADAU1861WBCSZ-RL	-40°C to +105°C	64-lead LFCSP-SS (Side Solderable) (9 mm x 9 mm x 0.75 mm)	Reel, 2500	CS-64-2

1 Z = RoHS Compliant Part.

2 W = Qualified for Automotive Applications.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADAU1861EBZ	Evaluation Board

1 Z = RoHS Compliant Part.