Stereo PDM to I²S/TDM Converter

Data Sheet

ADAU7112

FEATURES

- 2 channels of PDM audio inputs from digital microphones
- 64× decimation ratio of PDM to PCM audio data
- 24-bit resolution to support high sound pressure level (SPL) microphones
- 126 dB A-weighted SNR
- 4 kHz to 96 kHz output sampling rate
- Bit clock rates of 64×, 128×, 192×, 256×, 384×, or 512× the output sampling rate
- Automatic PDM clock generation
- Automatic power-down when BCLK is removed
- 0.36 mA DVDD operating current at 48 kHz sampling rate and 1.8 V supply
- Slave I²S or TDM output interface
- Up to TDM-16 supported
- Configurable TDM slots
- I/O supply voltage from 1.70 V to 3.63 V
- DVDD core supply voltage from 1.10 V to 1.98 V
- 4 µA typical DVDD shutdown current
- 9-ball, 1.26 mm × 1.26 mm, 0.4 mm pitch WLCSP
- Power-on reset

APPLICATIONS

- Mobile computing
- Portable electronics
- Consumer electronics
- Professional electronics

FUNCTIONAL BLOCK DIAGRAM

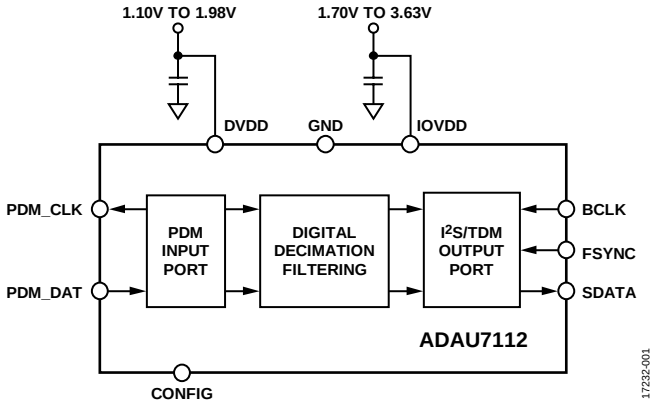

Figure 1.

GENERAL DESCRIPTION

The ADAU7112 converts stereo pulse density modulation (PDM) bit streams into one pulse code modulation (PCM) output stream. The source for the PDM data can be two microphones or other PDM sources. The PCM audio data is output on a serial audio interface port in either inter-IC serial (I²S) or time domain multiplexed (TDM) format.

The ADAU7112 is specified over a commercial temperature range of −40°C to +85°C. The ADAU7112 is available in a halide-free, 9-ball, 1.26 mm × 1.26 mm, 0.4 mm pitch, wafer level chip scale package (WLCSP).

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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REVISION HISTORY

6/2019—Revision 0: Initial Version

SPECIFICATIONS

DVDD = 1.10 V to 1.98 V, IOVDD = 1.70 V to 3.63 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUT					
Input Voltage					
High Level (V_{IH})	0.7 × IOVDD			V	
Low Level (V_{IL})			0.3 × IOVDD	V	
Input Leakage					Digital input pins with pull-down resistor
High Level (I_{IH})			2.5	µA	
Low Level (I_{IL}) at 0 V			1	µA	
Input Capacitance (C_I)		2		pF	Guaranteed by design
DIGITAL OUTPUT					
Output Voltage					
High Level (V_{OH})	0.85 × IOVDD			V	Source current when output is high (I_{OH}) = 1 mA
Low Level (V_{OL})			0.1 × IOVDD	V	Source current when output is low (I_{OL}) = 1 mA
Digital Output Pins, Output Drive					The digital output pins are driving low impedance printed circuit board (PCB) traces to a high impedance digital input buffer
IOVDD = 1.8 V Nominal					
Drive Strength	2.8			mA	
IOVDD = 3.3 V Nominal					
Drive Strength	10			mA	
PERFORMANCE					
Dynamic Range		126		dB	20 Hz to 20 kHz, −60 dB input, A-weighted filter (rms), relative to 0 dBFS output
Signal-to-Noise Ratio (SNR)		126		dB	A-weighted filter, fifth-order input, relative to 0 dBFS output
Decimation Ratio		64×			Only 64× is supported
Frequency Response	−0.1		+0.01	dB	DC to 0.45 × output sampling rate
Stop Band		0.566 × output sampling rate (f_S)		Hz	
Stop Band Attenuation	75			dB	
Group Delay	4.47	4.47	4.47	FSYNC cycles	0.02 f_S input signal
Gain	0	0	0	dB	PDM to PCM
Start-Up Time	63	64	64	FSYNC cycles	After power-up reset and initialization code is run
Bit Resolution		24		Bits	Internal and output
Interchannel Phase	0	0	0	Degrees	
CLOCKING					
Output Sampling Rate (f_S)	4	48	96	kHz	FSYNC pulse rate
Bit Clock Frequency (f_{BCLK})	0.256	12.288	24.576	MHz	
PDM_CLK Frequency (f_{PDM_CLK})	0.256	3.072	6.144	MHz	
POWER					
Supply Voltage					
Digital Core Voltage (DVDD Pin)	1.10		1.98	V	Supply for digital circuitry
Input/Output (I/O) Supply Voltage (IOVDD Pin)	1.70		3.63	V	Supply for I/O circuitry, including pads and level shifters

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Supply Current					
I/O Current (IOVDD Pin)					Dependent on the clock rates and characteristics of external loads
Operation State		1.6		mA	IOVDD = 3.3 V, f_S = 48 kHz, TDM-8 format, 25 pF capacitance
		0.86		mA	IOVDD = 1.8 V, f_S = 48 kHz, TDM-8 format, 25 pF capacitance
Shutdown Current		16		µA	Power applied, frame and bit clocks applied, then clocks removed. This specification is highly dependent on the external loads.
Digital Current (DVDD Pin)					
Operation State		0.4		mA	Over all temperatures, full voltage range, and silicon skews, f_S = 48 kHz, I²S format
		0.36		mA	DVDD = 1.8 V, f_S = 48 kHz
		0.21		mA	DVDD = 1.2 V, f_S = 48 kHz
Shutdown Current		4		µA	Power applied, frame and bit clocks applied, then clocks removed

SERIAL PORT TIMING SPECIFICATIONS

T_A = −40°C to +85°C, DVDD = 1.10 V to 1.98 V, IOVDD = 1.70 V to 3.63 V, unless otherwise noted.

Table 2.

Parameter	Min	Max	Unit	Description
SERIAL PORT				
f_{FSYNC}		96	kHz	FSYNC frequency, 1/t_{FSYNC}, not included in Figure 2
t_{FSYNC}	10.42		µs	FSYNC period
f_{BCLK}		24.576	MHz	BCLK frequency, sample rate ranging from 4 kHz to 96 kHz, 1/t_{BCLK}, not included in Figure 2
t_{BCLK}	40.7		ns	BCLK period
t_{BIL}	18		ns	BCLK low pulse width, slave mode, BCLK frequency = 24.576 MHz, BCLK period = 40.7 ns
t_{BIH}	18		ns	BCLK high pulse width, slave mode, BCLK frequency = 24.576 MHz, BCLK period = 40.7 ns
t_{LIS}	10		ns	FSYNC setup to BCLK input rising edge, slave mode, FSYNC frequency = 96 kHz
t_{LIH}	10		ns	FSYNC hold from BCLK input rising edge, slave mode, FSYNC frequency = 96 kHz
t_{SOD}		20.63	ns	SDATA delay from BCLK output falling edge, 25 pf load over entire range of IOVDD, all temperatures and skews
		9.03	ns	IOVDD = 3.3 V ± 10%, with 25 pf load
		20.63	ns	IOVDD = 1.7 V to 1.89 V, with 25 pf load

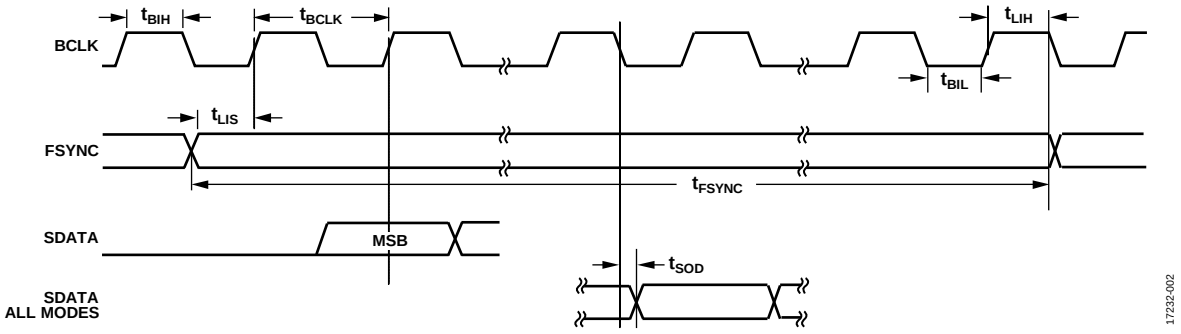

Figure 2. Serial Port Timing Diagram

PDM INPUT TIMING SPECIFICATIONS

T_A = −40°C to +85°C, DVDD = 1.10 V to 1.98 V, IOVDD = 1.70 V to 3.63 V, PDM data is latched on both edges of the clock (see Figure 3), unless otherwise noted.

Table 3.

Parameter	t_{MIN}	t_{MAX}	Unit	Description
t_{SETUP}	9		ns	Data setup time
t_{HOLD}	3		ns	Data hold time

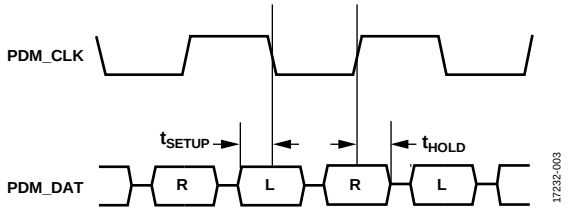

Figure 3. PDM Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
DVDD to GND	1.98 V
IOVDD to GND	3.63 V
Digital Inputs	DGND − 0.3 V to IOVDD + 0.3 V
Maximum Operating Ambient Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Storage Temperature Range	−65°C to +150°C
Soldering Temperature (60 sec)	300°C
Electrostatic Discharge (ESD) Susceptibility	4.5 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Table 5. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CB-9-8	57.1	0.5	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 1S0P thermal test board. See JEDEC JESD-51.
[2] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD-51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

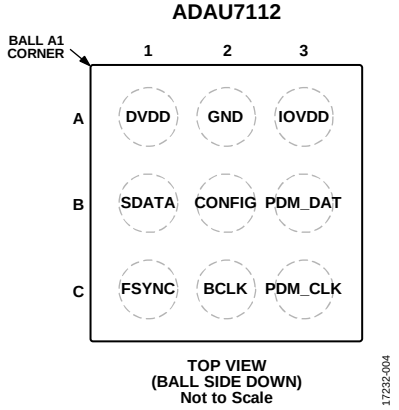

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	DVDD	Internal Core Digital Power Supply.
A2	GND	Ground.
A3	IOVDD	Digital I/O Power Supply.
B1	SDATA	I²S/TDM Serial Data Output.
B2	CONFIG	Configuration Pin.
B3	PDM_DAT	PDM Input Data.
C1	FSYNC	I²S/TDM Frame Synchronization or Left/Right Clock.
C2	BCLK	I²S/TDM Bit Clock.
C3	PDM_CLK	PDM Output Clock.

TYPICAL PERFORMANCE CHARACTERISTICS

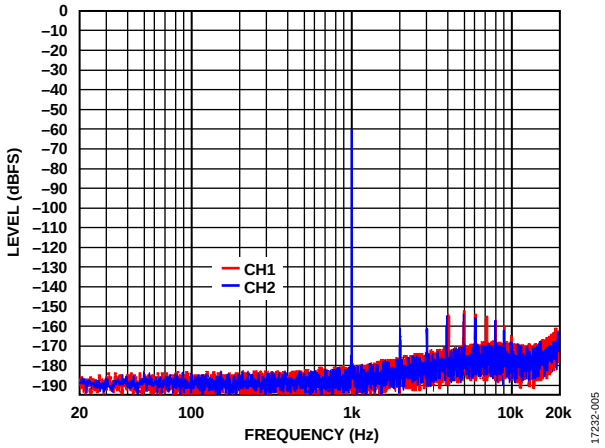

Figure 5. Fast Fourier Transform (FFT), f_S = 48 kHz, −60 dBFS Input, 64× Decimation, Fifth Order

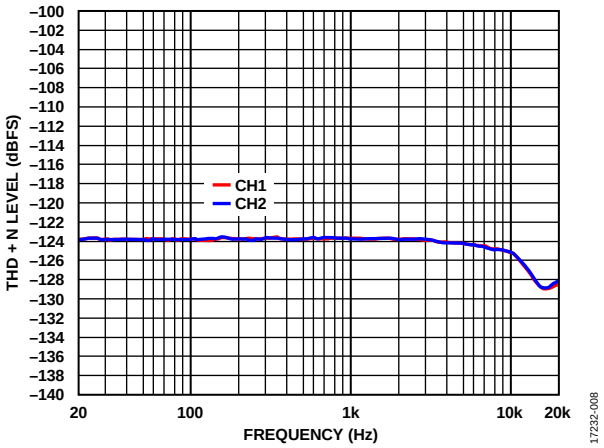

Figure 8. Total Harmonic Distortion + Noise (THD + N) Level vs. Frequency at −10 dBFS Unweighted, f_S = 48 kHz, 64× Decimation, Fifth Order

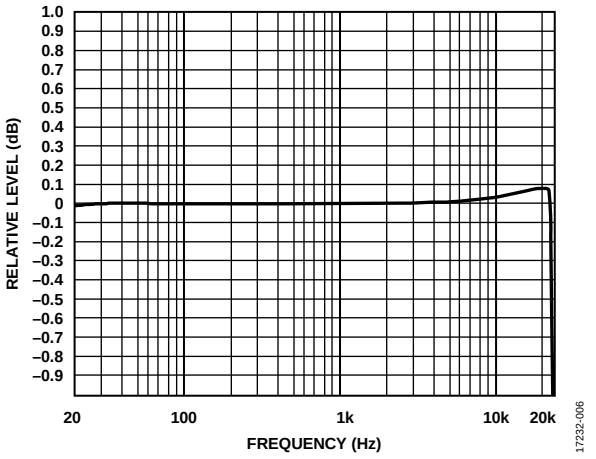

Figure 6. Relative Level vs. Frequency at −10 dBFS Normalized, 64× Decimation, f_S = 48 kHz

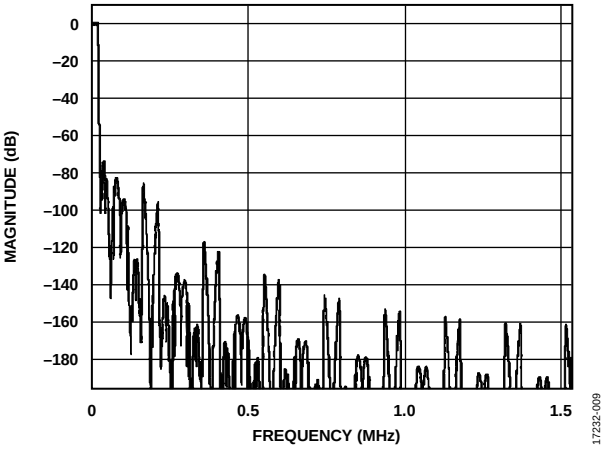

Figure 9. Magnitude vs. Frequency, 48 kHz Output, 64× Decimation

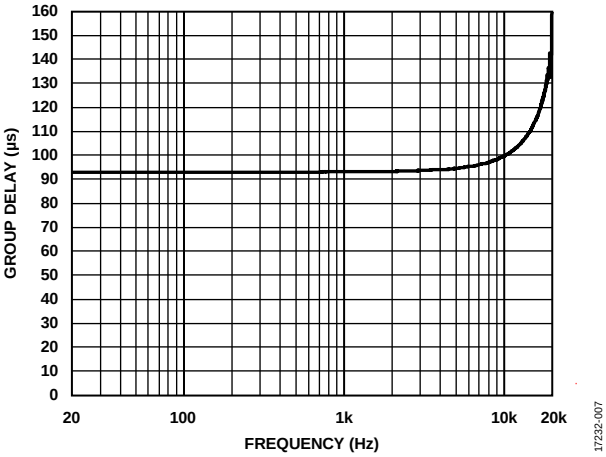

Figure 7. Group Delay vs. Frequency, f_S = 48 kHz, 64× Decimation

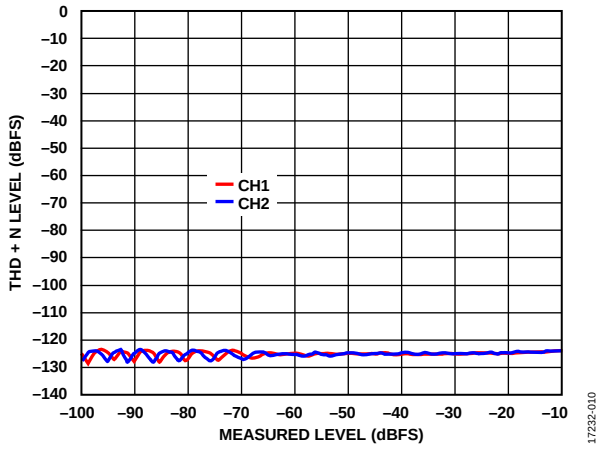

Figure 10. THD + N Level vs. Measured Level, 1 kHz, Unweighted, 64× Decimation, Fifth Order, f_S = 48 kHz

THEORY OF OPERATION

The ADAU7112 provides up to two channels of decimation from a 1-bit PDM source to a 24-bit PCM audio output. The downsampling ratio is 64 × f_S, with f_S being the PCM output sampling rate. All channels decimate at the same ratio. The 24-bit downsampled PCM audio is output via standard I²S or TDM format.

The input sources for the ADAU7112 can be any device that has a slave PDM output, such as a digital microphone. The output pins of these microphones can connect directly to the input pins of the ADAU7112.

The PDM_DAT input pin is connected to the data output of the PDM sources. Internally, there are two channels, Channel 0 and Channel 1. The mapping of the PDM_DAT input data to internal channels is shown in Table 7.

Table 7. PDM_DAT to Internal Channel Mapping

Input Pin	PDM_CLK Edge	Internal Channel
PDM_DAT	Falling	0
	Rising	1

POWER-UP AND INITIALIZATION

The ADAU7112 requires two power supplies to function: IOVDD and the DVDD. Both power supplies can be applied at the same time. If the power supplies are applied at different times, IOVDD must be applied first and then DVDD can be applied at any point after. There are no timing restrictions.

After the power supplies stabilize, the device initializes and is ready to accept incoming I²S clocks.

After the initialization is complete and I²S clocks are applied, it takes 16 full frame synchronization cycles to begin sending out PDM clocks. When the PDM clocks start, and after another 48 frame synchronization cycles, the PDM data is available on the SDATA pin. These 64 frame sync cycles are listed in Table 1.

CLOCKING

After power is applied and the power-up initialization is complete, the device is ready to accept I²S clocks. At this point, it takes 16 full frame synchronization cycles for the device to fully initialize and start sending PDM clocks. If during normal operation the bit clock or frame synchronization is removed, the ADAU7112 PDM_CLK outputs stop immediately and the ADAU7112 automatically enters a low power state. See the Power-Down State section for more details. When the clocks resume, the ADAU7112 relocks to the bit clock and the frame synchronization signals and adjusts the PDM_CLK outputs accordingly. The length of time before the PDM clock outputs resume is 4 frames ± 1 frame to lock to the incoming signal. If the format of the clock signals changes, the ADAU7112 detects this change at the end of the frame and stops the PDM clock outputs. Then, the device reconfigures and resumes sending PDM clocks with no user intervention. Again, this usually takes 4 frames ± 1 frame to lock to the incoming signal.

The ADAU7112 requires a BCLK rate that is a minimum of 64× the frame sync (FSYNC) sample rate. BCLK rates of 128×, 192×, 256×, 384×, and 512× the FSYNC rate are also supported. The ADAU7112 automatically detects the ratio between BCLK and FSYNC and generates a PDM clock output at 64× the FSYNC rate. The minimum sampling rate is 4 kHz, and the maximum sample rate is 96 kHz. The PDM clock range is 256 kHz to 6.144 MHz. Internally, all processing is performed at the PDM_CLK rate.

POWER-DOWN STATE

The ADAU7112 can be placed in a power-down state by stopping the frame and bit clocks that are being sent to the device.

To exit power-down mode, resume sending frame and bit clocks to the device.

SERIAL AUDIO OUTPUT INTERFACE

The ADAU7112 supports I²S and TDM serial output formats. Up to TDM-16 can be used, but the ADAU7112 can only place data in the first eight slots. The internal channel pair can be routed to one of four different pairs of output slots using the CONFIG pin.

Table 9 lists the available settings using the CONFIG pin. For the I²S configuration, the two internal channels are placed in the audio stream as shown in Figure 11.

For the TDM format, the configuration is independent of the actual number of TDM slots available. The configuration determines the slots in which the data is placed. However, if the bit clock to frame clock ratio is such that the slot can never be reached, the data is lost.

For example, if the CONFIG pin is pulled up through a 47 kΩ resistor to IOVDD, the data is placed in Slot 5 and Slot 6. Then, if the bit clock being sent is 128 × f_S, there are only four slots in each frame. Slot 5 and Slot 6 are never reached.

See Table 8 for supported bit clock to frame clock ratios and the resulting number of TDM data slots. Figure 14 through Figure 17 show the different options for placing the data in Slot 1 to Slot 8. These options also apply to any of the supported bit clock to frame clock ratios.

For the TDM-12 and TDM-16 clock rates, the data can only be placed in Slot 1 to Slot 8.

The SDATA pin is in tristate high impedance mode, except when the port is driving serial data.

With the CONFIG pin tied to IOVDD, the serial port is in I²S stereo mode with a 50/50 duty cycle frame clock expected. In this mode, the frame starts with the falling edge of the frame synchronization, and the expected duty cycle is 50% high and 50% low. Channel 0 sends out data when the clock is low, and as soon as the frame synchronization goes high, the data from Channel 0 is stopped and Channel 1 begins sending data. Both edges of the frame synchronization clock are used. If the duty

cycle is not 50/50, there may be errors in the resulting data. In this mode, there must be 64 bit clock cycles per frame.

The ADAU7112 can support six different bit clock rates of 64×, 128×, 192×, 256×, 384×, or 512× the output sample rate. These bit clock rates result in five different TDM formats that are supported. A ratio of 64 × f_S changes the ADAU7112 to I²S mode. See Table 8 for details.

In TDM mode, the frame synchronization is expected to be a positive going pulse that is at least one bit clock period wide. The falling edge is not important and is not considered as long as it is low long enough to meet the timing specification to be read as a low before going back high. The frame starts with the rising edge of this pulse.

Table 8. Supported TDM Bit Clock Rates

Bit Clock Rate	Number of Data Slots	Notes
64 × f_S	2	I²S mode see (Figure 11)
128 × f_S	4	See Figure 12
192 × f_S	6	See Figure 13
256 × f_S	8	See Figure 14
384 × f_S	12	See Figure 18
512 × f_S	16	See Figure 19

Table 9. CONFIG Pin Options

Device Setting	CONFIG Pin Configuration
I²S Format	Tie to IOVDD
TDM Slot 1 to Slot 2 Driven, 32-Bit Slots	Tie to GND
TDM Slot 3 to Slot 4 Driven, 32-Bit Slots	Open
TDM Slot 5 to Slot 6 Driven, 32-Bit Slots	Tie to IOVDD through a 47 kΩ resistor
TDM Slot 7 to Slot 8 Driven, 32-Bit Slots	Tie to GND through a 47 kΩ resistor

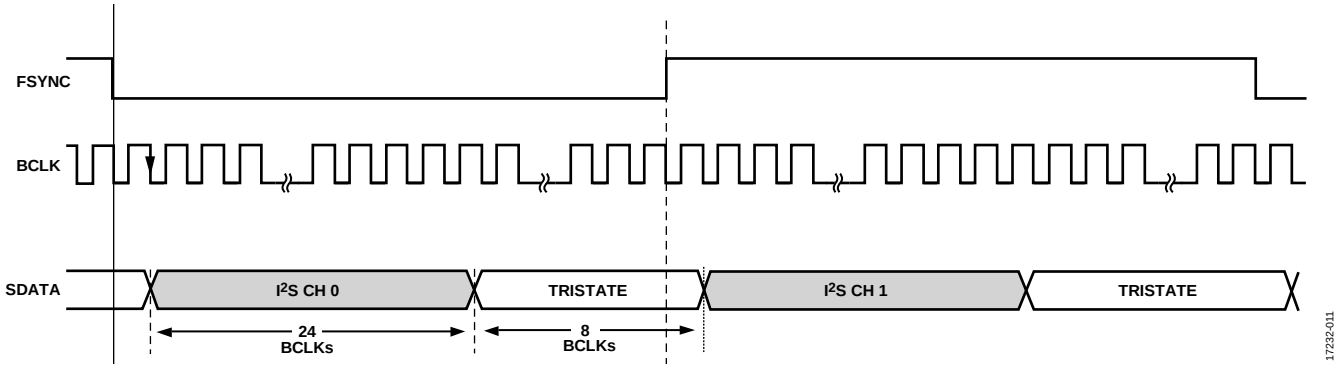

Figure 11. I²S Mode, BCLK = 64 × f_S, CONFIG Pin Tied to IOVDD

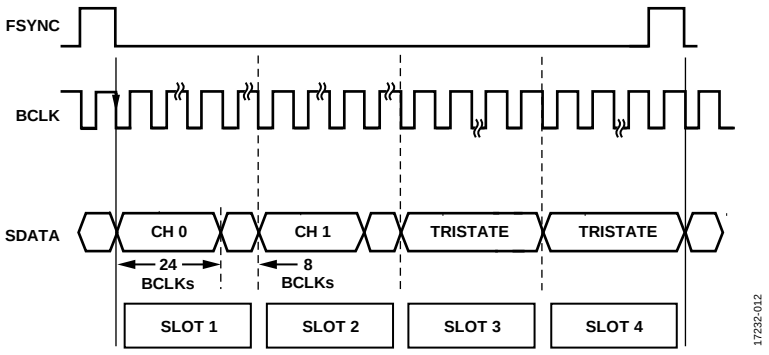

Figure 12. TDM-4, BCLK = 128 × f_S, CONFIG Pin Tied to GND

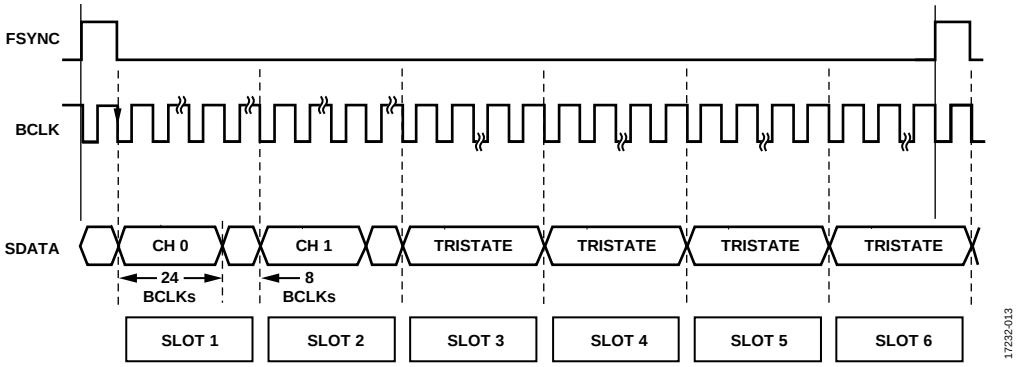

Figure 13. TDM-6, BCLK = 192 × f_S, CONFIG Pin Tied to GND

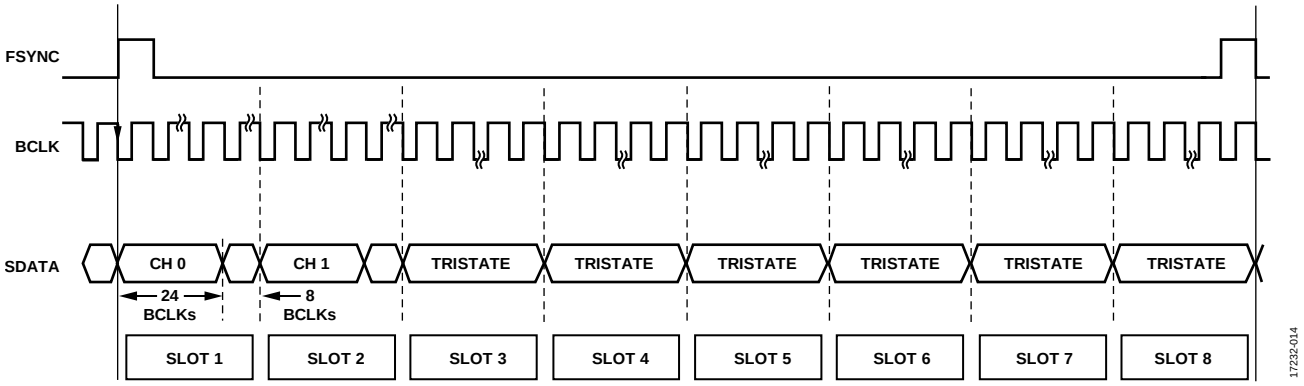

Figure 14. TDM-8, BCLK = 256 × f_S, CONFIG Pin Tied to GND

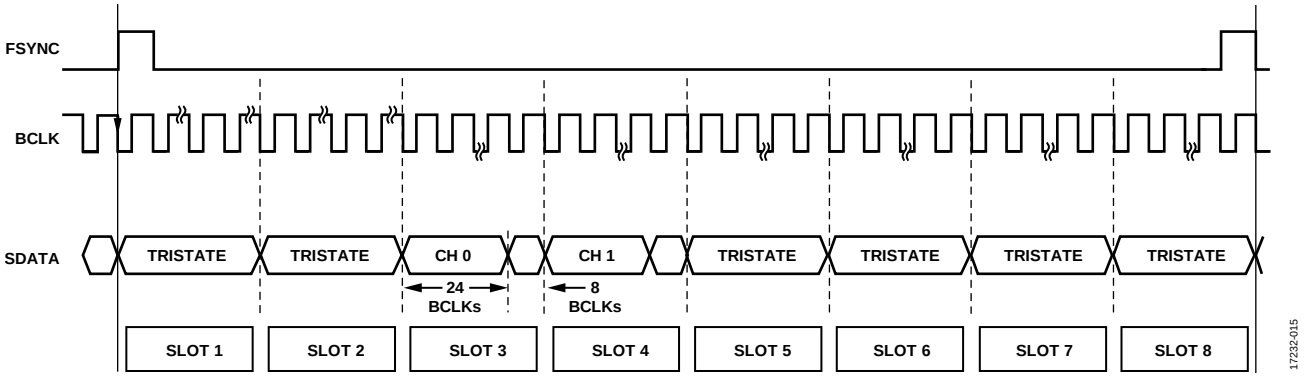

Figure 15. TDM-8, BCLK = 256 × f_S, CONFIG Pin Open

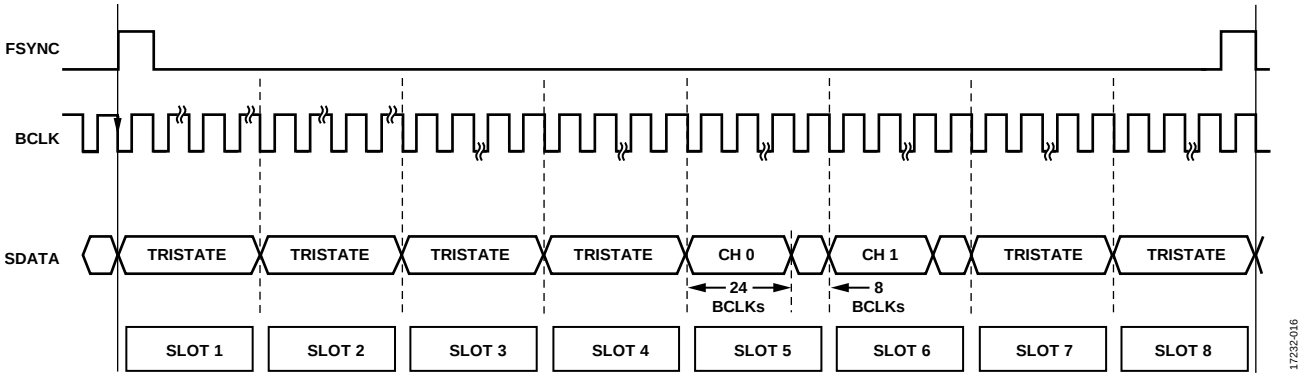

Figure 16. TDM-8, BCLK = 256 × f_S, CONFIG Pin Tied to IOVDD Through a 47 kΩ Resistor

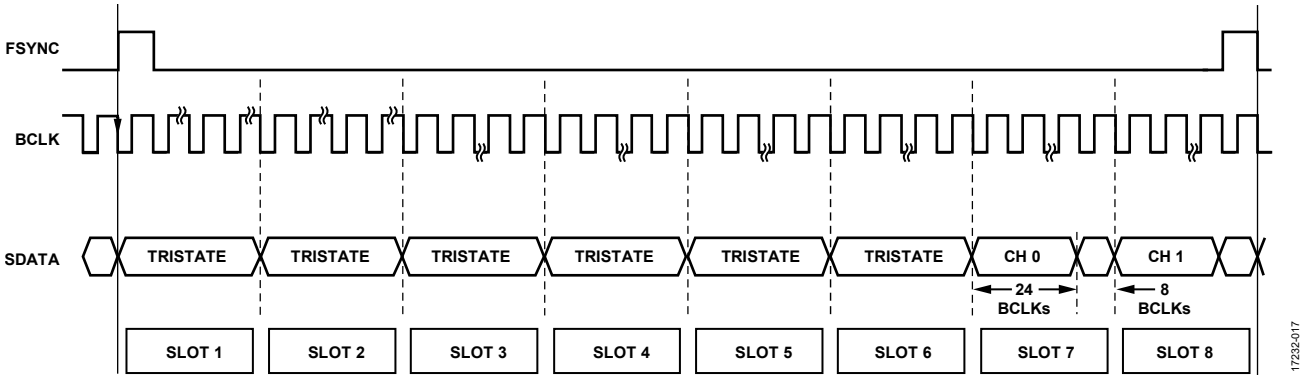

Figure 17. TDM-8, BCLK = 256 × f_S, CONFIG Pin Tied to GND Through a 47 kΩ Resistor

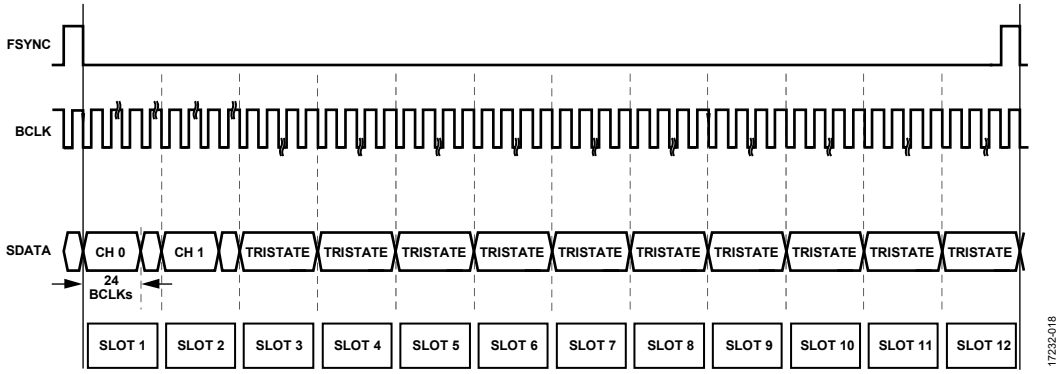

Figure 18. TDM-12, BCLK = 384 × f_S, CONFIG Pin Tied to GND

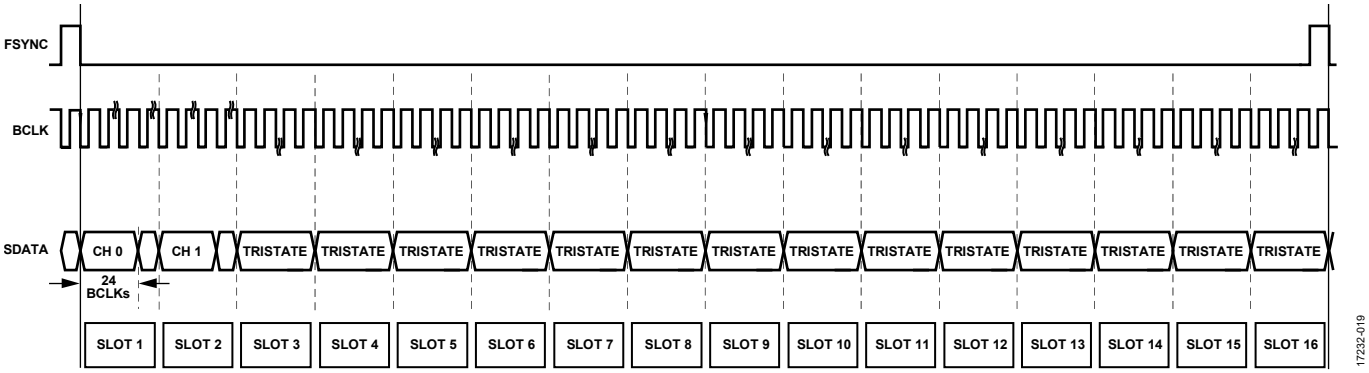

Figure 19. TDM-16, BCLK = 512 × f_S, CONFIG Pin Tied to GND

APPLICATIONS INFORMATION

Figure 20 details an example application circuit using two PDM sources and details how to set the CONFIG pin for the optional data formats.

To keep PCB manufacturing costs low, a via-in-pad is not required for most common configurations. The CONFIG pin can be left floating or a PCB trace on the top layer can connect the CONFIG pin to the nearby IOVDD pin or GND pin. A via-in-pad is only required when a pull-up or pull-down resistor is required.

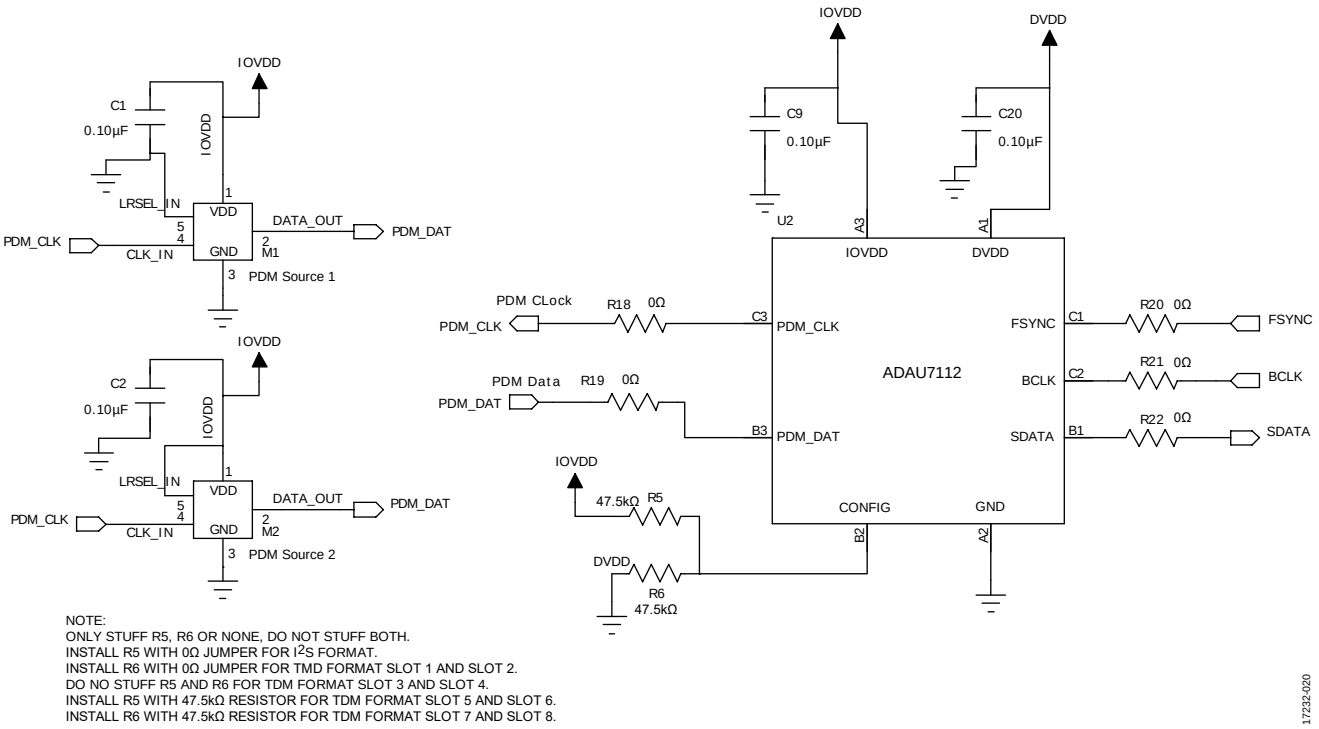

Figure 20. Example Application Circuit