3-Channel, Sigma-Delta ADC with SPI

Data Sheet **ADE7903**

FEATURES

- One (ADE7903) 24-bit, Σ-Δ ADC (simultaneously sampling with three ADE7912/ADE7913 ADCs)
- On-chip temperature sensor
- 4-wire SPI serial interface
- Standalone 24-bit, Σ-Δ ADC
- Up to four ADE7903 and ADE7912/ADE7913 devices clocked from a single crystal or an external clock
- Synchronization of multiple ADE7903 and ADE7912/ADE7913 devices
- ±31.25 mV peak input range for current channel
- ±500 mV peak input range for voltage channels
- Single 3.3 V supply
- 20-lead, wide body SOIC package
- Operating temperature: −40°C to +85°C

APPLICATIONS

- 3-phase shunt-based polyphase meters with neutral channel measurement
- Single-phase meters
- Power quality monitoring
- Solar inverters
- Process monitoring
- Standalone ADCs
- Protective devices
- Isolated sensor interfaces
- Industrial programmable logic controllers (PLCs)

TYPICAL APPLICATION CIRCUIT

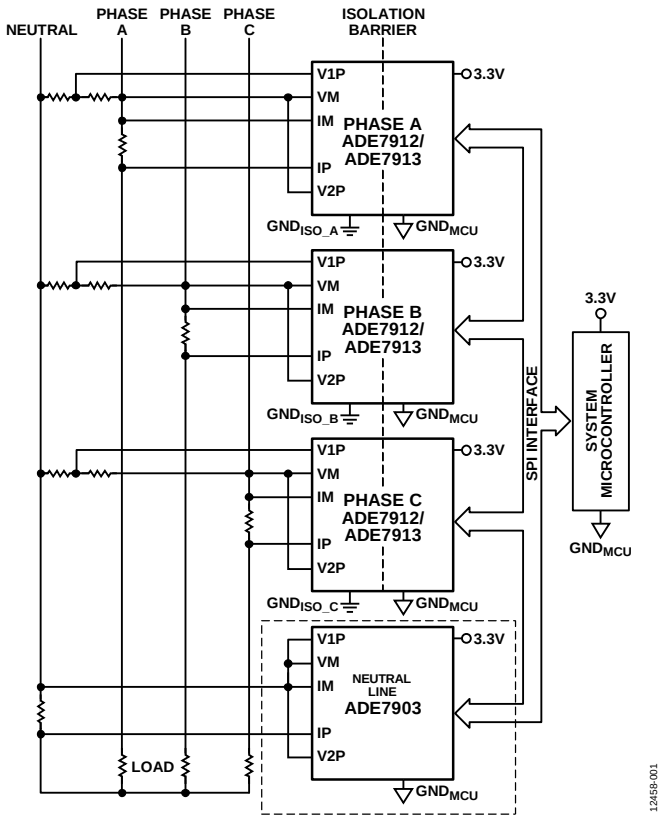


Figure 1.

GENERAL DESCRIPTION

The ADE7903 is a nonisolated, 3-channel, Σ-Δ analog-to-digital converter (ADC) for the neutral line of polyphase energy metering applications using shunt current sensors. The ADE7903 can also be used for single-phase energy metering and other standalone ADC applications. The ADE7903 features three 24-bit ADCs. The current ADC provides a 67 dBFS signal-to-noise ratio (SNR) over a 3.3 kHz signal bandwidth, whereas the voltage ADCs provide an SNR of 72 dBFS over the same bandwidth. One channel is dedicated to measuring the voltage across a shunt when the shunt is used for current sensing. Up to two additional channels are dedicated to measuring voltages, which are usually sensed using resistor dividers. One voltage channel can be used to measure the temperature of the die via an internal sensor. The ADE7903 includes three channels: one current channel and two voltage channels.

Together with the ADE7912/ADE7913, the ADE7903 provides a small form factor, 3-phase isolated solution with a neutral measurement. The three phases are isolated with ADE7912/ADE7913 devices, while the neutral line is not isolated with the ADE7903.

The ADE7903 configuration and status registers are accessed via a bidirectional SPI serial port for easy interfacing with microcontrollers.

The ADE7903 can be clocked from a crystal or an external clock signal. To minimize the system bill of materials, the master ADE7912/ADE7913 can drive the clocks of up to three additional ADE7912/ADE7913 or ADE7903 devices.

Multiple ADE7912/ADE7913 and ADE7903 devices can be synchronized to sample at the same moment and provide coherent outputs. The ADE7903 can also be used individually as a standalone ADC.

The ADE7903 is available in a 20-lead, Pb-free, wide body SOIC package.

Rev. 0 **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

12/14—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

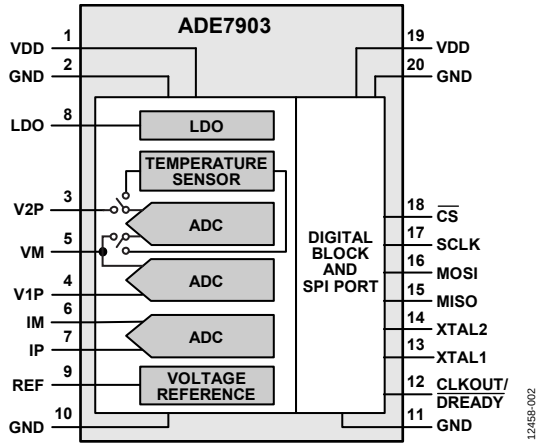


Figure 2.

SPECIFICATIONS

VDD = 3.3 V ± 10%, GND = 0 V, on-chip reference, XTAL1 = 4.096 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_A = 25°C (typical), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG INPUTS[1]					
Pseudo Differential Signal Voltage Range Between IP and IM Pins	−31.25		+31.25	mV peak	IM pin connected to GND
Pseudo Differential Signal Voltage Range Between V1P and VM Pins and Between V2P and VM Pins	−500		+500	mV peak	Pseudo differential inputs between V1P and VM pins and between V2P and VM pins; VM pin connected to GND
Maximum VM and IM Voltage	−25		+25	mV	
Crosstalk		−90		dB	IP and IM inputs set to 0 V (GND) when V1P and V2P inputs at full scale
		−105		dB	V2P and VM inputs set to 0 V (GND) when IP and V1P inputs at full scale; V1P and VM inputs set to 0 V (GND) when IP and V2P inputs at full scale
Input Impedance to Ground (DC)					
IP, IM, V1P, and V2P Pins	480			kΩ	
VM Pin	240			kΩ	
Current Channel ADC Offset Error		−2		mV	
Voltage Channels ADC Offset Error		−35		mV	
ADC Offset Drift over Temperature		±200		ppm/°C	V1 channel only
Gain Error	−4		+4	%	
Gain Drift over Temperature	−135		+135	ppm/°C	Current channel
	−85		+85	ppm/°C	V1 and V2 channels
AC Power Supply Rejection, PSR		−90		dB	VDD = 3.3 V + 120 mV rms (50 Hz/100 Hz), IP = V1P = V2P = GND
DC Power Supply Rejection, PSR		−80		dB	VDD = 3.3 V ± 330 mV dc, IP = 6.25 mV rms, V1P = V2P = 100 mV rms
TEMPERATURE SENSOR					
Accuracy		±5		°C	
WAVEFORM SAMPLING—CURRENT CHANNEL[1]					
Signal-to-Noise Ratio, SNR		67		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		68		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		72		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		74		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Signal-to-Noise-and-Distortion Ratio, SINAD		66		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		68		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		72		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		73		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Total Harmonic Distortion, THD		−79		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		−78		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		−82		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		−82		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Spurious-Free Dynamic Range, SFDR		83		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		83		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		85		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		85		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE CHANNELS[1]					
Signal-to-Noise Ratio, SNR		72		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		74		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		77		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		79		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Signal-to-Noise-and-Distortion Ratio, SINAD		72		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		74		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		77		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		78		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Total Harmonic Distortion, THD		−83		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		−83		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		−85		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		−85		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Spurious-Free Dynamic Range, SFDR		86		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		86		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		87		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		87		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
CLKIN[2]					All specifications for CLKIN = 4.096 MHz
Input Clock Frequency	3.6	4.096	4.21	MHz	
CLKIN Duty Cycle	45	50	55	%	
XTAL1 Logic Inputs					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	
XTAL1 Total Capacitance[3]		40		pF	
XTAL2 Total Capacitance[3]		40		pF	
CLKOUT Delay from XTAL1[4]			100	ns	
LOGIC INPUTS—MOSI, SCLK, $\overline{CS}$					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}		0.015	1	µA	
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS—CLKOUT/$\overline{DREADY}$ AND MISO					
Output High Voltage, V_{OH}	2.5			V	I_{SOURCE} = 800 µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 2 mA
POWER SUPPLY					For specified performance
VDD Pin	2.97		3.63	V	Minimum = 3.3 V − 10%; maximum = 3.3 V + 10%
Supply Current (I_{DD}) [5]		5.1	6.2	mA	
		2		mA	No CLKIN signal at XTAL1 pin

[1] See the Terminology section for a definition of the parameters.
[2] CLKIN is the internal clock of the ADE7903. It is the frequency at which the device is clocked at the XTAL1 pin.
[3] XTAL1/XTAL2 total capacitances refer to the net capacitances on each pin. Each capacitance is the sum of the parasitic capacitance at the pin and the capacitance of the ceramic capacitor connected between the pin and GND. See the ADE7903 Clock section for more details.
[4] CLKOUT delay from XTAL1 is the delay that occurs from a high to low transition at the XTAL1 pin to a synchronous high to low transition at the CLKOUT/$\overline{DREADY}$ pin when CLKOUT functionality is enabled.
[5] Supply current specified with the two VDD pins connected externally from the same power supply (see the Pin Configuration and Function Descriptions section).

TIMING CHARACTERISTICS

VDD = 3.3 V ± 10%, GND = 0 V, on-chip reference, CLKIN = 4.096 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 2. SPI Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit
$\overline{CS}$ to SCLK Positive Edge	t_{SS}	50		ns
SCLK Frequency[1]		250	5600	kHz
SCLK Low Pulse Width	t_{SL}	80		ns
SCLK High Pulse Width	t_{SH}	80		ns
Data Output Valid After SCLK Edge	t_{DAV}		80	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	70		ns
Data Input Hold Time After SCLK Edge	t_{DHD}	20		ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
SCLK Rise Time	t_{SR}		20	ns
SCLK Fall Time	t_{SF}		20	ns
MISO Disable After $\overline{CS}$ Rising Edge	t_{DIS}	5	40	ns
$\overline{CS}$ High After SCLK Edge	t_{SFS}	0		ns

[1] Minimum and maximum specifications are guaranteed by design.

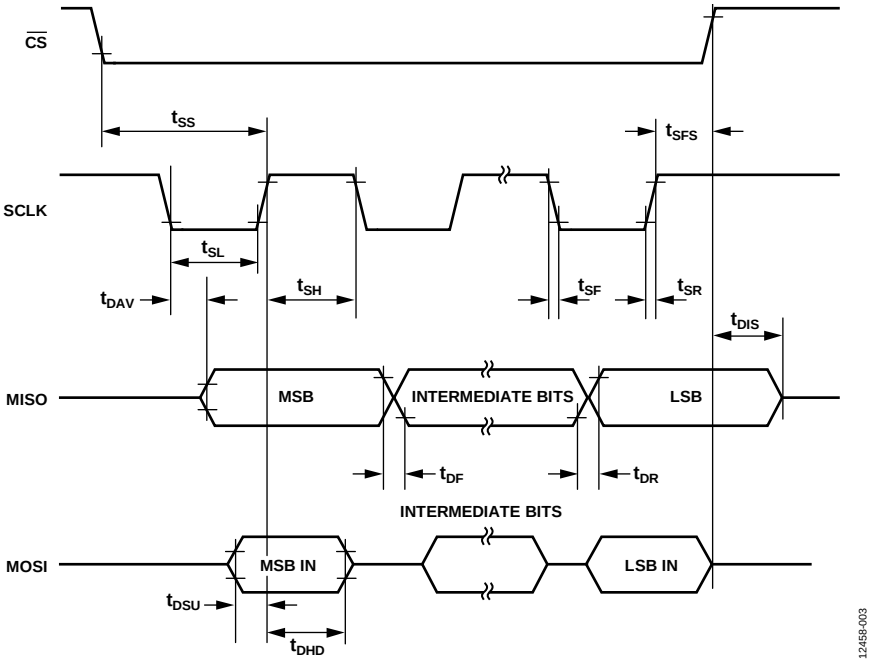


Figure 3. SPI Interface Timing

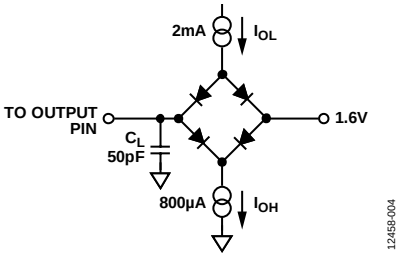


Figure 4. Load Circuit for Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
VDD to GND	−0.3 V to +3.7 V
Analog Input Voltage to GND, IP, IM, V1P, V2P, VM	−2 V to +2 V
Reference Input Voltage to GND	−0.3 V to VDD + 0.3 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.3 V
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)[1]	260°C

[1] Analog Devices, Inc., recommends that reflow profiles used in soldering RoHS compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for the latest revision of this standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} and θ_{JC} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead SOIC_W	79	24.7	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

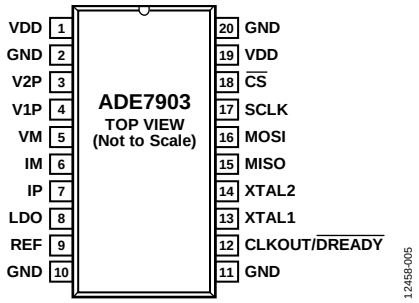


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 19	VDD	Supply Voltage. These pins provide the supply voltage for the ADE7903. Maintain the supply voltage at 3.3 V ± 10% for specified operation. Decouple each VDD pin to GND with a ceramic 100 nF capacitor and a single 10 µF capacitor in parallel. Connect the VDD pins externally.
2, 10, 11, 20	GND	Ground Reference. Connect the GND pins externally.
3, 4, 5	V2P, V1P, VM	Analog Inputs for the Voltage Channels. The voltage channels are used with the voltage transducers. V2P and V1P are pseudo differential voltage inputs with a maximum signal level of ±500 mV with respect to VM for specified operation. Use these pins with the related input circuitry, as shown in Figure 18. If V1P or V2P is not used, connect it to the VM pin.
6, 7	IM, IP	Analog Inputs for the Current Channel. The current channel is used with shunts. IM and IP are pseudo differential voltage inputs with a maximum differential level of ±31.25 mV. Use these pins with the related input circuitry, as shown in Figure 18.
8	LDO	2.5 V Output of the Analog Low Dropout (LDO) Regulator. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor to GND. Do not connect external load circuitry to this pin.
9	REF	Voltage Reference. This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V. Decouple this pin to GND with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor.
12	CLKOUT/$\overline{\text{DREADY}}$	Clock Output (CLKOUT). When CLKOUT functionality is selected (see the Synchronizing Multiple ADE7912/ADE7913 and ADE7903 Devices section for details), the ADE7903 generates a digital signal synchronous to the master clock at the XTAL1 pin. Use CLKOUT to provide a clock to other ADE7912/ADE7913 and ADE7903 devices on the board. Data Ready, Active Low ($\overline{\text{DREADY}}$). When the $\overline{\text{DREADY}}$ functionality is selected (see the Synchronizing Multiple ADE7912/ADE7913 and ADE7903 Devices section for details), the ADE7903 generates an active low signal synchronous to the ADC output frequency. Use this signal to start reading the ADC outputs of the ADE7903.
13	XTAL1	Master Clock Input. An external clock can be provided at this logic input. The CLKOUT/$\overline{\text{DREADY}}$ signal of another appropriately configured ADE7903 (see the Synchronizing Multiple ADE7912/ADE7913 and ADE7903 Devices section for details) can be provided at this pin. Alternatively, a crystal with a maximum drive level of 0.5 mW and an equivalent series resistance (ESR) of 20 Ω can be connected across XTAL1 and XTAL2 to provide a clock source for the ADE7903. The clock frequency for specified operation is 4.096 MHz, but lower frequencies down to 3.6 MHz can be used. See the ADE7903 Clock section for more details.
14	XTAL2	Crystal, Second Input. A crystal with a maximum drive level of 0.5 mW and an ESR of 20 Ω can be connected across XTAL2 and XTAL1 to provide a clock source for the ADE7903.
15	MISO	Data Output for SPI Port. Pull up this pin with a 10 kΩ resistor (see the ADE7903 Clock section for details).
16	MOSI	Data Input for SPI Port.
17	SCLK	Serial Clock Input for SPI Port. All serial data transfers are synchronized to this clock (see the ADE7903 Clock section).
18	$\overline{\text{CS}}$	Chip Select for SPI Port.

TYPICAL PERFORMANCE CHARACTERISTICS

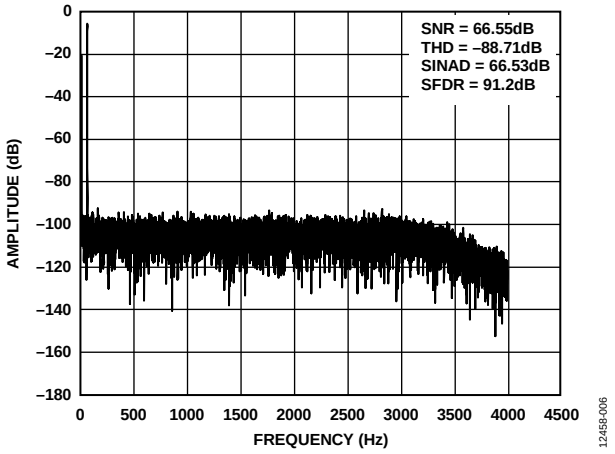


Figure 6. Current Channel Fast Fourier Transform (FFT), ±31.25 mV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz

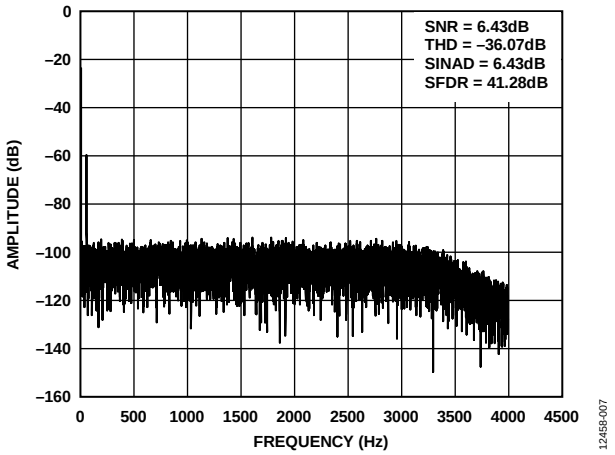


Figure 7. Current Channel FFT, ±31.25 µV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz

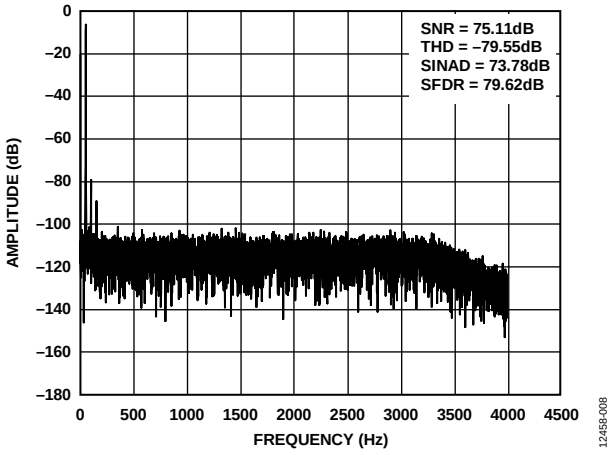


Figure 8. Voltage Channel V1 FFT, ±500 mV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz

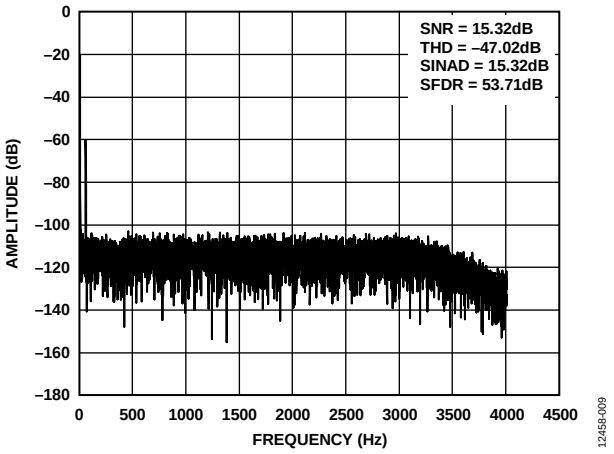


Figure 9. Voltage Channel V1 FFT, ±500 µV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz

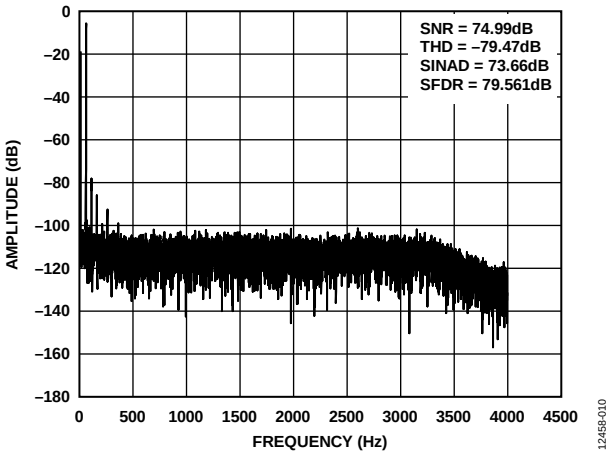


Figure 10. Voltage Channel V2 FFT, ±500 mV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz

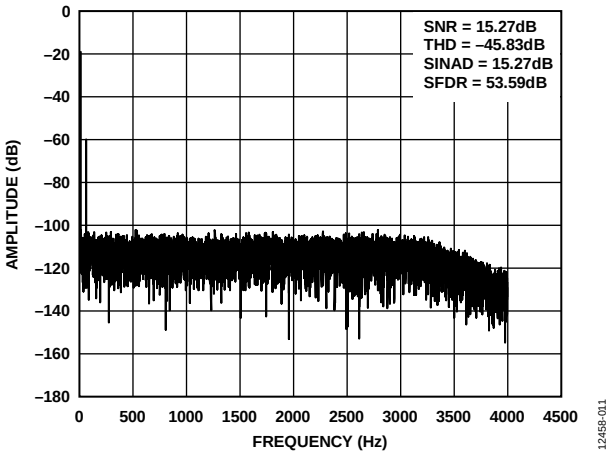


Figure 11. Voltage Channel V2 FFT, ±500 µV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz

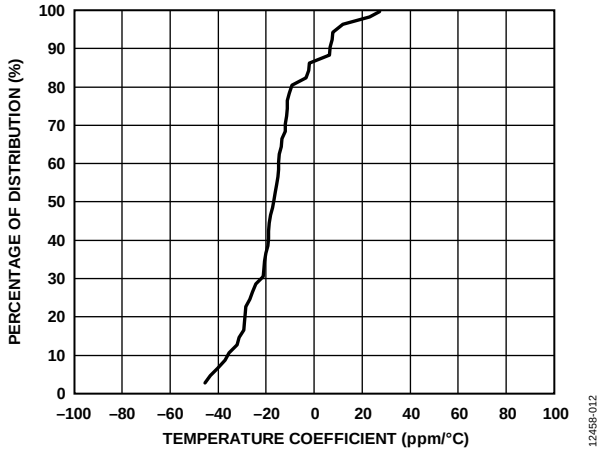


Figure 12. Cumulative Histogram of the Current Channel ADC Gain Temperature Coefficient for Temperatures Between −40°C and +25°C

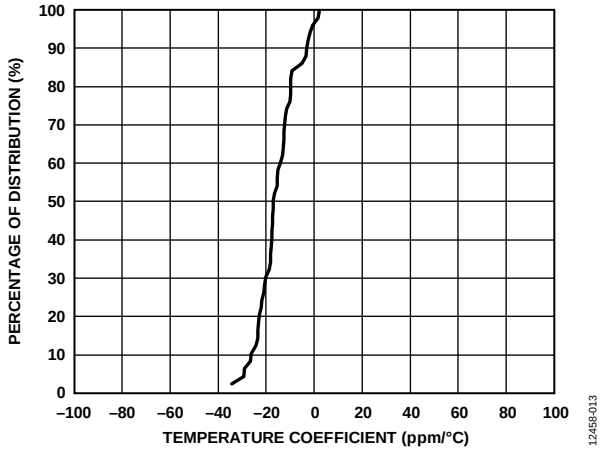


Figure 13. Cumulative Histogram of the Current Channel ADC Gain Temperature Coefficient for Temperatures Between 25°C and 85°C

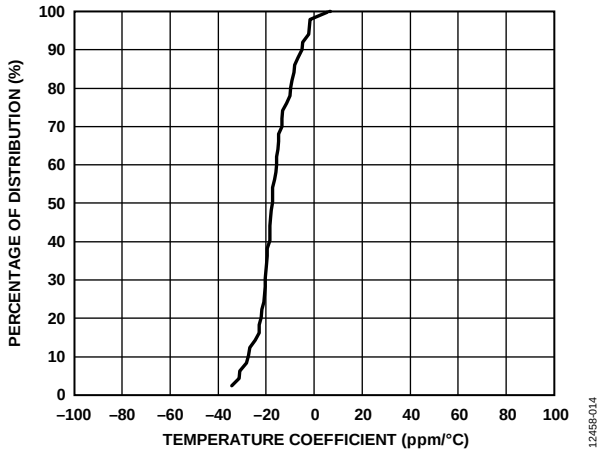


Figure 14. Cumulative Histogram of the Voltage Channel V1 ADC Gain Temperature Coefficient for Temperatures Between −40°C and +25°C

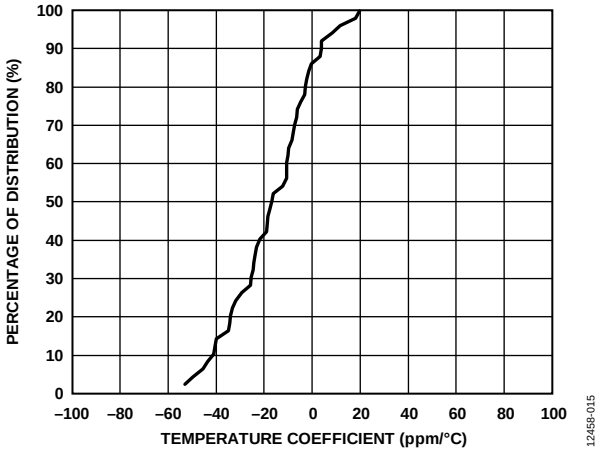


Figure 15. Cumulative Histogram of the Voltage Channel V1 ADC Gain Temperature Coefficient for Temperatures Between 25°C and 85°C

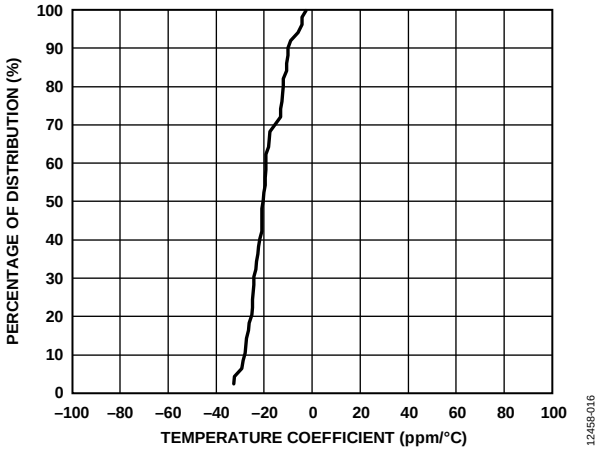


Figure 16. Cumulative Histogram of the Voltage Channel V2 ADC Gain Temperature Coefficient for Temperatures Between −40°C and +25°C

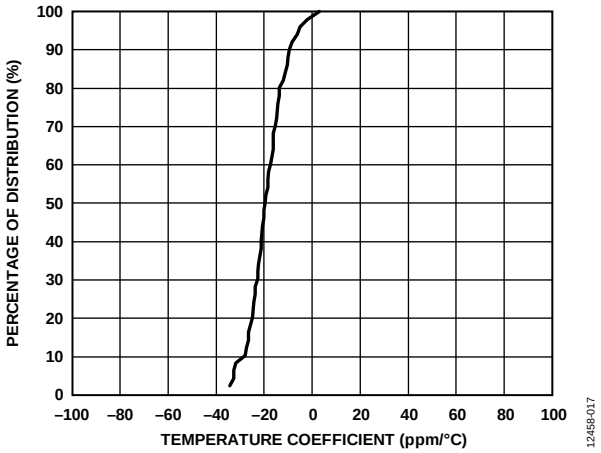
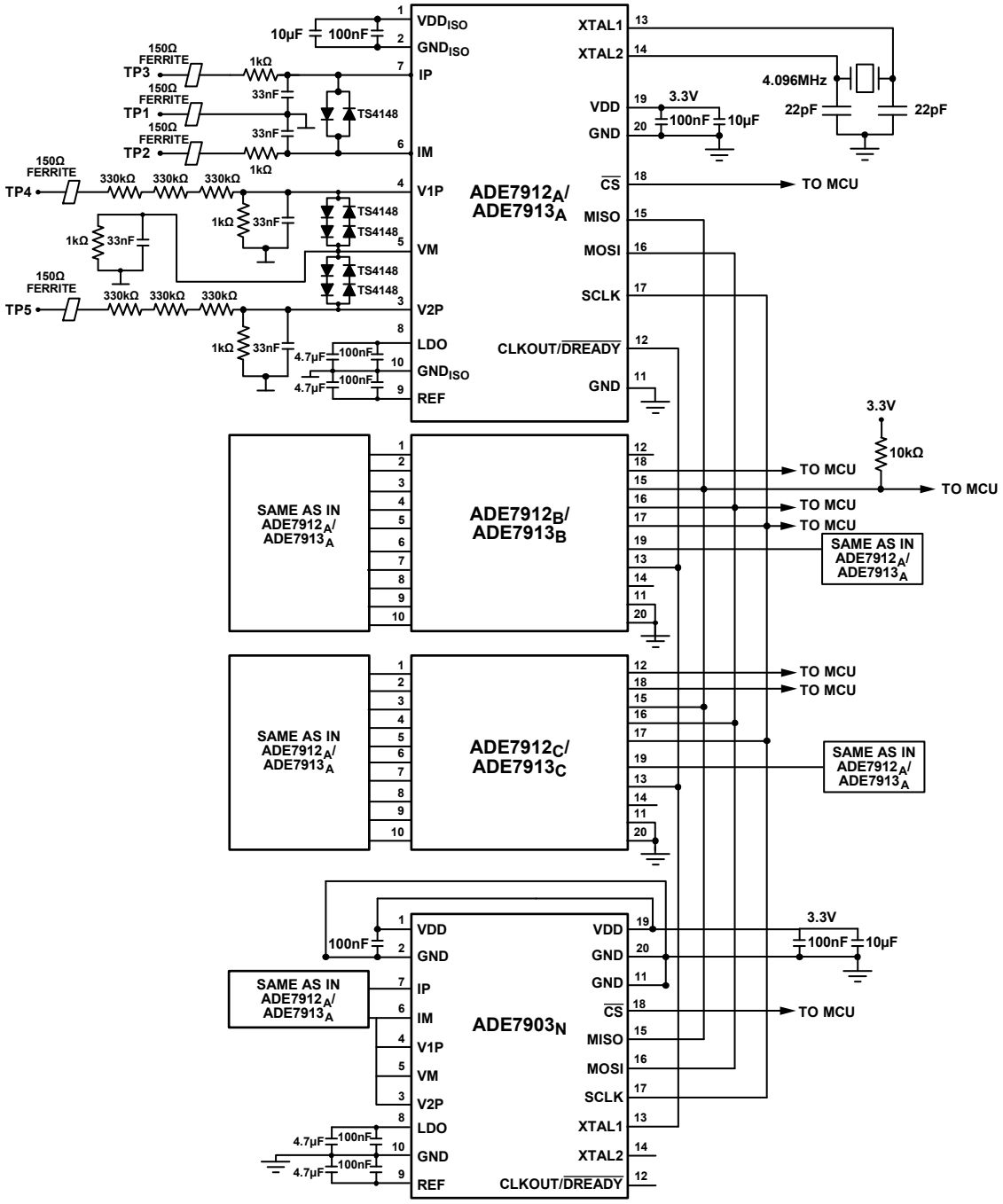


Figure 17. Cumulative Histogram of the Voltage Channel V2 ADC Gain Temperature Coefficient for Temperatures Between 25°C and 85°C

TEST CIRCUIT



NOTES
1. ADE7912$_X$/ADE7913$_X$ = PHASE X ADE7912/ADE7913, WHERE X = A, B, OR C.

12458-018

Figure 18. Test Circuit

TERMINOLOGY

Pseudo Differential Signal Voltage Range Between IP and IM, V1P and VM, and V2P and VM Pins

This range represents the peak-to-peak pseudo differential voltage that must be applied to the ADCs to generate a full-scale response when the IM and VM pins are connected to GND. The IM and VM pins are connected to GND using antialiasing filters (see Figure 18). Figure 19 illustrates the input voltage range between IP and IM. Figure 20 illustrates the input voltage range between V1P and VM and between V2P and VM.

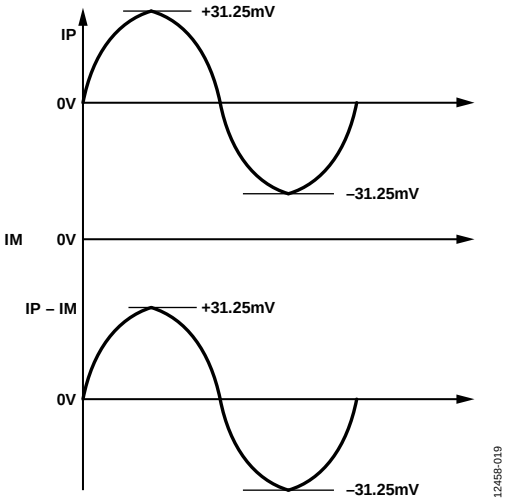


Figure 19. Pseudo Differential Input Voltage Range Between IP and IM Pins

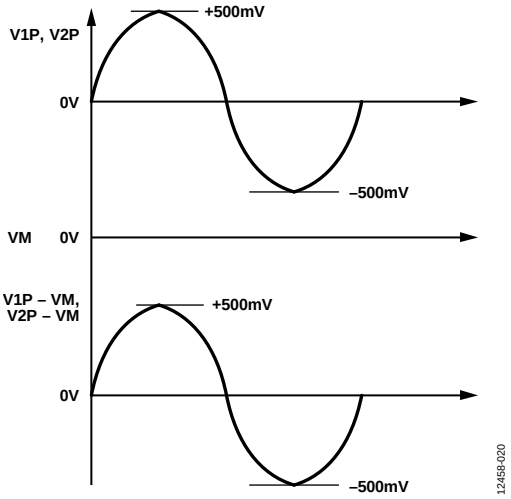


Figure 20. Pseudo Differential Input Voltage Range Between V1P and VM Pins and Between V2P and VM Pins

Maximum VM and IM Voltage Range

This range represents the maximum allowed voltage at the VM and IM pins relative to GND.

Crosstalk

Crosstalk represents leakage of signals, usually via capacitance between circuits. Crosstalk is measured in the current channel by setting the IP and IM pins to GND, supplying a full-scale alternate differential voltage between the V1P and VM pins and between the V2P and VM pins of the voltage channel, and measuring the output of the current channel. It is measured in the V1P voltage channel by setting the V1P and VM pins to GND, supplying a full-scale alternate differential voltage at the IP and V2P pins, and measuring the output of the V1P channel. Crosstalk is measured in the V2P voltage channel by setting the V2P and VM pins to GND, supplying a full-scale alternate differential voltage at the IP and V1P pins, and measuring the output of the V2P channel. The crosstalk is equal to the ratio between the grounded ADC output value and its ADC full-scale output value. The ADC outputs are acquired for 2 sec. Crosstalk is expressed in decibels.

Input Impedance to Ground (DC)

The input impedance to ground represents the impedance measured at each ADC input pin (IP, IM, V1P, V2P, and VM) with respect to GND.

ADC Offset Error

ADC offset error is the difference between the average measured ADC output code with both inputs connected to GND and the ideal ADC output code. The magnitude of the offset depends on the input range of each channel.

ADC Offset Drift over Temperature

The ADC offset drift is the change in offset over temperature. It is measured at −40°C, +25°C, and +85°C. The offset drift over temperature is computed as follows:

$$Drift = \max\left[\left|\frac{Offset(-40) - Offset(25)}{Offset(25) \times (-40 - 25)}\right|, \left|\frac{Offset(85) - Offset(25)}{Offset(25) \times (85 - 25)}\right|\right]$$

Offset drift is expressed in ppm/°C.

Gain Error

The gain error in the ADCs represents the difference between the measured ADC output code (minus the offset) and the ideal output code when the internal voltage reference is used (see the Analog-to-Digital Conversion section). The difference is expressed as a percentage of the ideal code. It represents the overall gain error of one current or voltage channel.

Gain Drift over Temperature
This temperature coefficient includes the temperature variation of the ADC gain and of the internal voltage reference. It represents the overall temperature coefficient of one current or voltage channel. With the internal voltage reference in use, the ADC gain is measured at −40°C, +25°C, and +85°C. Then, the temperature coefficient is computed as follows:

$$Drift = \max\left[\left|\frac{Gain(-40) - Gain(25)}{Gain(25) \times (-40 - 25)}\right|, \left|\frac{Gain(85) - Gain(25)}{Gain(25) \times (85 - 25)}\right|\right]$$

Gain drift is measured in ppm/°C.

Power Supply Rejection (PSR)
PSR quantifies the measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken when the voltage at the input pins is 0 V. A second reading is obtained with the same input signal levels when an ac signal (120 mV rms at 50 Hz or 100 Hz) is introduced onto the supply. Any error introduced by this ac signal is expressed as a percentage of the reading (power supply rejection ratio, PSRR). PSR = $20\log_{10}$ (PSRR).

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken when the voltage between the IP and IM pins is 6.25 mV rms, and the voltages between the V1P and VM pins and between the V2P and VM pins are 100 mV rms. A second reading is obtained with the same input signal levels when the power supplies are varied by ±10%. Any error introduced is expressed as a percentage of the reading (PSRR). Then PSR = $20\log_{10}$ (PSRR).

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The spectral components are calculated over a 2 sec window. The value for SNR is expressed in decibels relative to full scale (dBFS).

Signal-to-Noise-and-Distortion (SINAD) Ratio
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The spectral components are calculated over a 2 sec window. The value for SINAD is expressed in decibels relative to full scale (dBFS).

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of all harmonics (excluding the noise components) to the rms value of the fundamental. The spectral components are calculated over a 2 sec window. The value for THD is expressed in decibels relative to full scale (dBFS).

Spurious-Free Dynamic Range (SFDR)
SFDR is the ratio of the rms value of the actual input signal to the rms value of the peak spurious component over the measurement bandwidth of the waveform samples. The spectral components are calculated over a 2 sec window. The value of SFDR is expressed in decibels relative to full scale (dBFS).

THEORY OF OPERATION

ANALOG INPUTS

The ADE7903 has three analog inputs: one current channel and two voltage channels. The current channel has two fully differential voltage input pins, IP and IM, that accept a maximum differential signal of ±31.25 mV.

The maximum V_{IP} signal level is also ±31.25 mV. The maximum V_{IM} signal level allowed at the IM input is ±25 mV. Figure 21 shows a schematic of the input for the current channel and its relation to the maximum IM pin voltage.

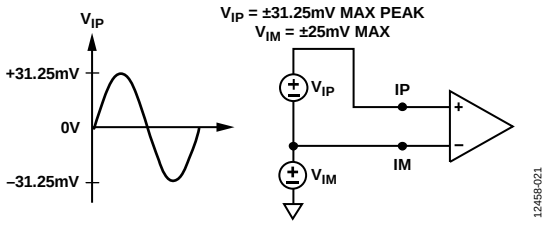


Figure 21. Maximum Input Level, Current Channel

Note that the current channel is used to sense the voltage across a shunt. In this case, one pole of the shunt becomes the ground of the meter (see Figure 28) and, therefore, the current channel is used in a pseudo differential configuration, similar to the voltage channel configuration (see Figure 22).

The voltage channel has two pseudo differential, single-ended voltage input pins: V1P and V2P. These single-ended voltage inputs have a maximum input voltage of ±500 mV with respect to VM. The maximum signal allowed at the VM input is ±25 mV. Figure 22 shows a schematic of the voltage channel inputs and their relation to the maximum VM voltage.

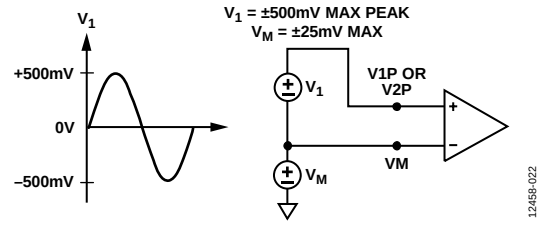


Figure 22. Maximum Input Level, Voltage Channels

ANALOG-TO-DIGITAL CONVERSION

The ADE7903 has three second-order Σ-Δ ADCs. For simplicity, the block diagram in Figure 23 shows a first-order Σ-Δ ADC. The converter is composed of the Σ-Δ modulator and the digital low-pass filter (LPF).

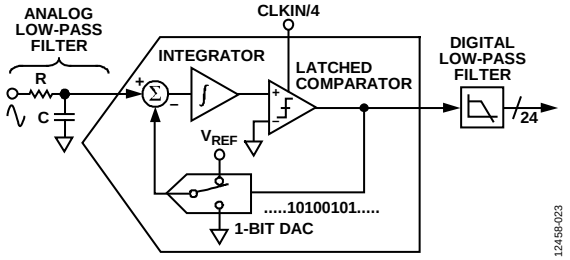


Figure 23. First-Order Σ-Δ ADC

A Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7903, the sampling clock is equal to CLKIN/4 (1.024 MHz when CLKIN = 4.096 MHz). The 1-bit digital-to-analog converter (DAC) in the feedback loop is driven by the serial stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and, therefore, the bit stream) can approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. A meaningful result is obtained only when a large number of samples is averaged. This averaging is completed in the second part of the ADC, the digital low-pass filter, after the data is passed through the digital isolators. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first technique is oversampling. Oversampling means that the signal is sampled at a rate (frequency) that is many times higher than the bandwidth of interest. For example, when CLKIN = 4.096 MHz, the sampling rate in the ADE7903 is 1.024 MHz, and the bandwidth of interest is 40 Hz to 3.3 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the bandwidth of interest is lowered, as shown in Figure 24.

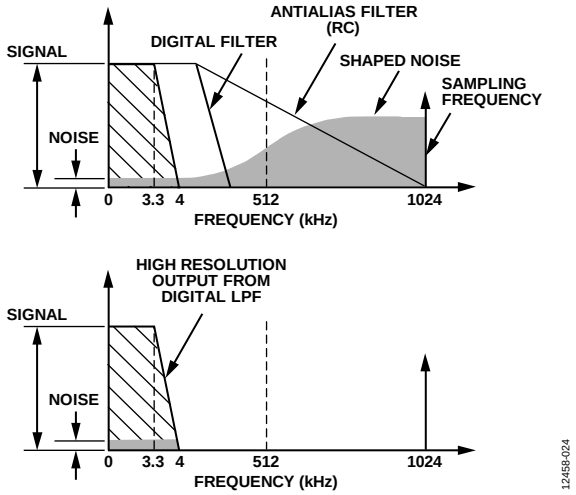


Figure 24. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

However, oversampling alone is not sufficient to improve the SNR in the band of interest. For example, an oversampling factor of four is required to increase the SNR by a mere 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. Noise shaping is the second technique used to achieve high resolution. In the Σ-Δ modulator,

the noise is shaped by the integrator, which has a high-pass type response for the quantization noise. The result is that most of the noise is at higher frequencies where it can be removed by the digital low-pass filter. This noise shaping is shown in Figure 24.

The bandwidth of interest is a function of the input clock frequency, the ADC output frequency (selectable by Bits[5:4] (ADC_FREQ) in the CONFIG register; see the ADC Output Values section for details), and Bit 7 (BW) of the CONFIG register. When CLKIN is 4.096 MHz and the ADC output frequency is 8 kHz, if BW is cleared to 0 (the default value), the ADC bandwidth is 3.3 kHz. If BW is set to 1, the ADC bandwidth is 2 kHz. Table 6 shows the ADC output frequencies and the ADC bandwidth as a function of the input clock (CLKIN) frequency. Three cases are shown: one for CLKIN = 4.096 MHz, the typical clock input frequency value; one for CLKIN = 4.21 MHz, the maximum clock input frequency; and one for CLKIN = 3.6 MHz, the minimum clock input frequency.

Antialiasing Filter

Figure 23 also shows an analog low-pass filter (RC) on the input to the ADC. This filter is placed outside the ADE7903, and its role is to prevent aliasing. Aliasing is an artifact of all sampled systems, as shown in Figure 25. Aliasing refers to the frequency components in the input signal to the ADC that are higher than half the sampling rate of the ADC and appear in the sampled signal at a frequency below half the sampling rate. Frequency components above half the sampling frequency (also known as the Nyquist frequency, that is, 512 kHz) are imaged or folded back down below 512 kHz. This folding happens with all ADCs, regardless of the architecture. In Figure 25, only frequencies near the sampling frequency of 1.024 MHz move into the bandwidth of interest for metering, that is, 40 Hz to 3.3 kHz or 40 Hz to 2 kHz. To attenuate the high frequency noise (near 1.024 MHz) and prevent the distortion of the bandwidth of interest, a low-pass filter must be introduced. It is recommended that one RC filter with a corner frequency of 5 kHz be used for the attenuation to be sufficiently high at the sampling frequency of 1.024 MHz. The 20 dB per decade attenuation of this filter is usually sufficient to eliminate the effects of aliasing.

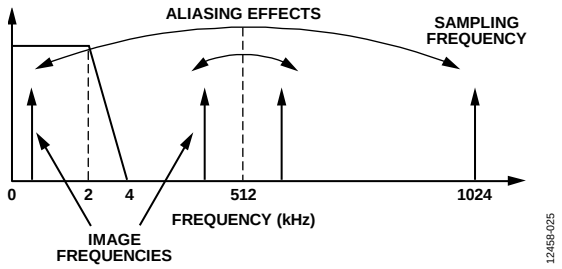


Figure 25. Aliasing Effects

ADC Transfer Function

All ADCs in the ADE7903 produce 24-bit signed output codes. With a full-scale input signal of 31.25 mV on the current channel and 0.5 V on the voltage channels, and with an internal reference of 1.2 V, the ADC output code is nominally 5,320,000 and usually varies for each ADE7903 around this value. The code from the ADC can vary between 0x800000 (−8,388,608) and 0x7FFFFF (+8,388,607), which is equivalent to an input signal level of ±49.27 mV on the current channel and ±0.788 V on the voltage channels. However, for specified performance, do not exceed the nominal range of ±31.25 mV for the current channel and ±500 mV for the voltage channels; ADC performance is guaranteed only for input signals within these limits.

ADC Output Values

The ADC output values are stored in three 24-bit signed registers, IWV, V1WV, and V2WV, at a rate defined by Bits[5:4] (ADC_FREQ) in the CONFIG register. The output frequency is 8 kHz (CLKIN/512), 4 kHz (CLKIN/1024), 2 kHz (CLKIN/2048), or 1 kHz (CLKIN/4096) based on ADC_FREQ being equal to 00, 01, 10, or 11, respectively, when CLKIN is 4.096 MHz.

The microcontroller reads the ADC output registers one at a time or in burst mode. See the SPI Read Operation section and the SPI Read Operation in Burst Mode section for more information.

Table 6. ADC Output Frequency and ADC Bandwidth as a Function of CLKIN Frequency

CLKIN (MHz)	ADC_FREQ Bits in CONFIG Register	ADC Output Frequency (Hz)	ADC Bandwidth When BW Bit in CONFIG Register Cleared to 0 (Hz)	ADC Bandwidth When BW Bit in CONFIG Register Set to 1 (Hz)
4.096	00	8000	3300	2000
	01	4000	1650	1000
	10	2000	825	500
	11	1000	412	250
4.21	00	8222	3391	2055
	01	4111	1695	1027
	10	2055	847	513
	11	1027	423	256
3.6	00	7031	2900	1757
	01	3515	1450	878
	10	1757	725	439
	11	878	362	219

REFERENCE CIRCUIT

The nominal reference voltage at the REF pin is 1.2 V. This reference voltage is used for the ADCs in the ADE7903. Because the on-chip dc-to-dc converter cannot supply external loads, the REF pin cannot be overdriven by a standalone external voltage reference.

The voltage of the ADE7903 reference drifts slightly with temperature. Table 1 lists the gain drift over temperature specification of each ADC channel. This value includes the temperature variation of the ADC gain, together with the temperature variation of the internal voltage reference.

CRC OF ADC OUTPUT VALUES

Every output cycle, the ADE7903 computes the cyclic redundancy check (CRC) of the ADC output values stored in the IWV, V1WV, and V2WV registers. Bits[5:4] (ADC_FREQ) in the CONFIG register determine the ADC output frequency and, therefore, the update rate of the CRC. The CRC algorithm is based on the CRC-16-CCITT algorithm. The registers are introduced into a linear feedback shift register (LFSR) based generator one byte at a time, least significant byte first, as shown in Figure 26. Each byte is then used with the MSB first. The 16-bit result is written in the ADC_CRC register.

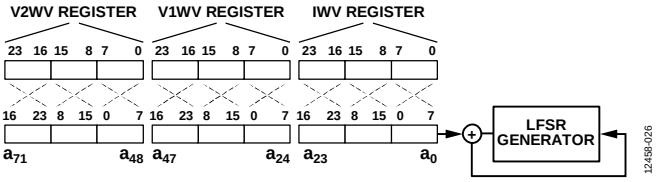


Figure 26. CRC Calculation of ADC Output Values

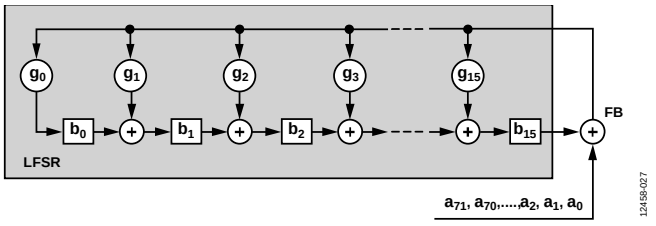


Figure 27. LFSR Generator Used for ADC_CRC Calculation

Figure 27 shows how the LFSR works. The IWV, V1WV, and V2WV registers form the [a_{71}, a_{70},…, a_0] bits used by the LFSR. Bit a_0 is Bit 7 of the first register to enter the LFSR; Bit a_{71} is Bit 16 of V2WV, the last register to enter the LFSR. The formulas that govern the LFSR are as follows:

$b_i(0) = 1$, where i = 0, 1, 2, …, 15, the initial state of the bits that form the CRC. Bit b_0 is the LSB, and Bit b_{15} is the MSB.

g_i, where i = 0, 1, 2, …, 15 are the coefficients of the generating polynomial defined by the CRC-16-CCITT algorithm as follows:

$$G(x) = x^{16} + x^{12} + x^5 + 1 \quad (1)$$

$$g_0 = g_5 = g_{12} = 1 \quad (2)$$

All other g_i coefficients are equal to 0.

$$FB(j) = a_{j-1} \text{ XOR } b_{15}(j-1) \quad (3)$$

$$b_0(j) = FB(j) \text{ AND } g_0 \quad (4)$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1),\ i = 1, 2, 3, \ldots, 15 \quad (5)$$

Equation 3, Equation 4, and Equation 5 must be repeated for j = 1, 2, …, 72. The value written into the ADC_CRC register contains Bit $b_i(72)$, i = 0, 1, …, 15.

The ADC_CRC register can be read by executing an SPI register read access or as part of the SPI burst mode read operation. See the SPI Read Operation and the SPI Read Operation in Burst Mode sections for more details.

TEMPERATURE SENSOR

The ADE7903 contains a temperature sensor that is multiplexed with the V2P input of the voltage channel. Bit 3 (TEMP_EN) of the CONFIG register selects what the third ADC of the ADE7903 measures. If the TEMP_EN bit is 0, its default value, the ADC measures the voltage between the V2P and VM pins. If the TEMP_EN bit is 1, the ADC measures the temperature sensor. In the ADE7903, the conversion result is stored in the V2WV register. The time it takes for the temperature sensor measurement to settle after the TEMP_EN bit is set to 1 is 5 ms.

The expression used to calculate the temperature in the microcontroller, when Bit 7 (BW) in the CONFIG register is set to the default value of 0, is

$$temp = 8.72101 \times 10^{-5} \times (V2WV + TEMPOS \times 2^{11}) - 306.47$$

where *temp* is the temperature value measured in degrees Celsius.

The gain value is different depending on the value of Bit 7 (BW) in the CONFIG register. When Bit 7 (BW) is set to 0, the gain used to convert the bit information provided by the ADE7903 into degrees Celsius has a default value of 8.72101×10^{-5}°C/LSB; when Bit 7 (BW) is set to 1, this gain value is 9.26171×10^{-5}°C/LSB. The temperature measurement accuracy is ±5°C. TEMPOS is the 8-bit, signed, read-only register in which the temperature sensor offset is stored. The offset information is calculated during the manufacturing process, and it is stored with the opposite sign. For example, if the offset is 5, −5 is written into the ADE7903. One LSB of the TEMPOS register is equivalent to 2^{11} LSBs of the V2WV register.

Instead of using the default gain value, the gain can be calibrated as part of the overall meter calibration process. Measure the temperature, TEMP, of the ADE7903, read the V2WV register containing the temperature sensor reading of the ADE7903, and compute the gain as follows:

$$Temperature\ gain = \frac{TEMP}{V2WV + TEMPOS \times 2^{11}} \quad (6)$$

PROTECTING THE INTEGRITY OF CONFIGURATION REGISTERS

The configuration registers of the ADE7903 are either user accessible registers (CONFIG, SYNC_SNAP, COUNTER0, and COUNTER1) or internal registers. The internal registers are not user accessible, and they must remain at their default values. To protect the integrity of all configuration registers, a write protection mechanism is available.

By default, the write protection is disabled and the user accessible configuration registers can be written without restriction. When the protection is enabled, no writes to any configuration register are allowed. The registers can always be read, without restriction, independent of the write protection state.

To enable the protection, write 0xCA to the 8-bit lock register (Address 0xA). To disable the protection, write 0x9C to the 8-bit lock register. It is recommended that the write protection be enabled after the CONFIG register is initialized. If any user accessible register must be changed, for example, during the synchronization process of multiple ADE7912/ADE7913 and ADE7903 devices, disable the protection, change the value of the register, and then reenable the protection.

CRC OF CONFIGURATION REGISTERS

Every output cycle, the ADE7903 computes the CRC of the CONFIG and TEMPOS registers, as well as Bit 2 (IC_PROT) of the STATUS0 register, and Bit 7 of the STATUS1 register. The CRC algorithm is called CRC-16-CCITT. The 16-bit result is written in the CTRL_CRC register.

The input registers to the CRC circuit form a 64-bit array that is introduced bit by bit into an LFSR-based generator, similar to Figure 26 and Figure 27, one byte at a time, least significant byte first. Each byte is then processed with the MSB first.

The formulas that govern the LFSR are as follows:

$b_i(0) = 1$, where i = 0, 1, 2, …, 15, the initial state of the bits that form the CRC. Bit b_0 is the LSB, and Bit b_{15} is the MSB.

g_i, where i = 0, 1, 2, …, 15 are the coefficients of the generating polynomial defined by the CRC-16-CCITT algorithm in Equation 1 and Equation 2.

$$FB(j) = a_{j-1} \text{ XOR } b_{15}(j-1) \quad (7)$$

$$b_0(j) = FB(j) \text{ AND } g_0 \quad (8)$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1),\ i = 1, 2, 3, \ldots, 15 \quad (9)$$

Equation 7, Equation 8, and Equation 9 must be repeated for j = 1, 2, … , 64. The value written into the CTRL_CRC register contains Bit $b_i(64)$, i = 0, 1, …, 15. Because each ADE7903 has a particular TEMPOS register value, each ADE7903 has a different CTRL_CRC register default value.

ADE7903 STATUS

The bits in the STATUS0 and STATUS1 registers of the ADE7903 characterize the state of the device.

If the value of the CTRL_CRC register changes, Bit 1 (CRC_STAT) in the STATUS0 register is set to 1. This bit clears to 0 when the STATUS0 register is read.

After the configuration registers are protected by writing 0xCA into the lock register, Bit 2 (IC_PROT) in the STATUS0 register is set to 1. It clears to 0 when the STATUS0 register is read, and it is set back to 1 at the next ADC output cycle.

At power-up, or after a hardware or software reset, the ADE7903 signals the end of the reset period by clearing Bit 0 (RESET_ON) in the STATUS0 register to 0.

If the ADC output values of IWV, V1WV, and V2WV are not read during an output cycle, Bit 3 (ADC_NA) in the STATUS1 register becomes 1. It clears to 0 when the STATUS1 register is read.

The STATUS0 and STATUS1 registers can be read by executing an SPI register read. STATUS0 can also be read as part of the SPI burst mode read operation. See the SPI Read Operation and the SPI Read Operation in Burst Mode sections for more information.

APPLICATIONS INFORMATION

ADE7903 IN POLYPHASE ENERGY METERS

The ADE7903 is designed for use in a 3-phase energy metering systems in which three ADE7912/ADE7913 devices and one ADE7903 device are managed by a master device containing an SPI interface, usually a microcontroller.

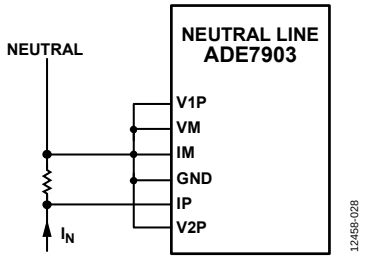


Figure 28. Neutral Line with the ADE7903

Figure 28 shows how the ADE7903 inputs are connected on the neutral line of a 3-phase system. The neutral current is sensed using a shunt, and the voltage across the shunt is measured at the fully differential inputs, IP and IM.

A pole of the shunt is connected to the IM pin of the ADE7903 and becomes the ground, GND. Pin V1P and Pin VM are connected to the IM pin if they are not in use. The V1P and V2P voltage channels are used to measure auxiliary voltages. If V1P or V2P is not used, connect it to VM.

Figure 29 shows a block diagram of a 3-phase energy meter that uses three ADE7912/ADE7913 devices, one ADE7903 on the neutral line, and a microcontroller. One 4.096 MHz crystal provides the clock to the ADE7912/ADE7913 that senses the Phase A current and voltage. The ADE7912/ADE7913 devices that sense the Phase B and Phase C currents and voltages and the ADE7903 device that senses the neutral current are clocked by a signal generated at the CLKOUT/$\overline{\text{DREADY}}$ pin of the ADE7912/ADE7913 that is placed to sense the Phase A current and voltage. As an alternative configuration, the microcontroller can generate a 4.096 MHz clock to all ADE7912/ADE7913 and ADE7903 devices at the XTAL1 pin (see Figure 30). Note that the XTAL1 pin can receive a clock with a frequency within the 3.6 MHz to 4.21 MHz range, as specified in Table 1.

The microcontroller uses the SPI port to communicate with the ADE7912/ADE7913 and ADE7903 devices. Four of its input/output pins, CS_A, CS_B, CS_C, and CS_N, are used to generate the SPI $\overline{\text{CS}}$ signals. The SCLK, MOSI, and MISO pins of the microcontroller are directly connected to the corresponding SCLK, MOSI, and MISO pins of each ADE7912/ADE7913 device (see Figure 31). To simplify Figure 29 to Figure 31, these connections are not shown.

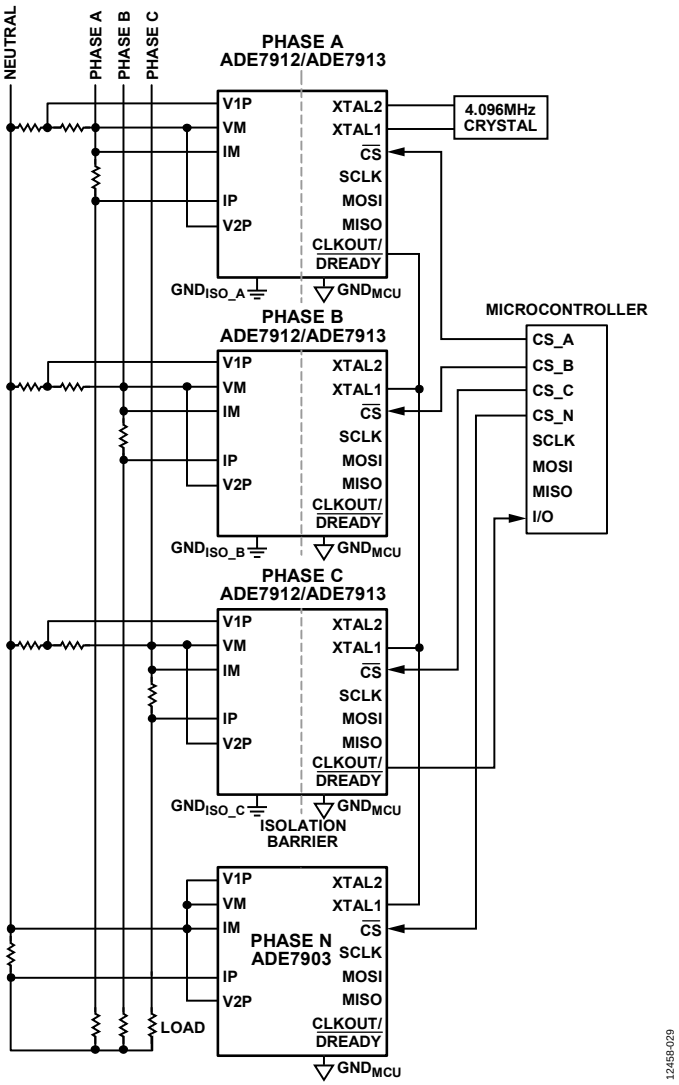


Figure 29. 3-Phase Energy Meter Using Three ADE7912/ADE7913 Devices and One ADE7903 Device

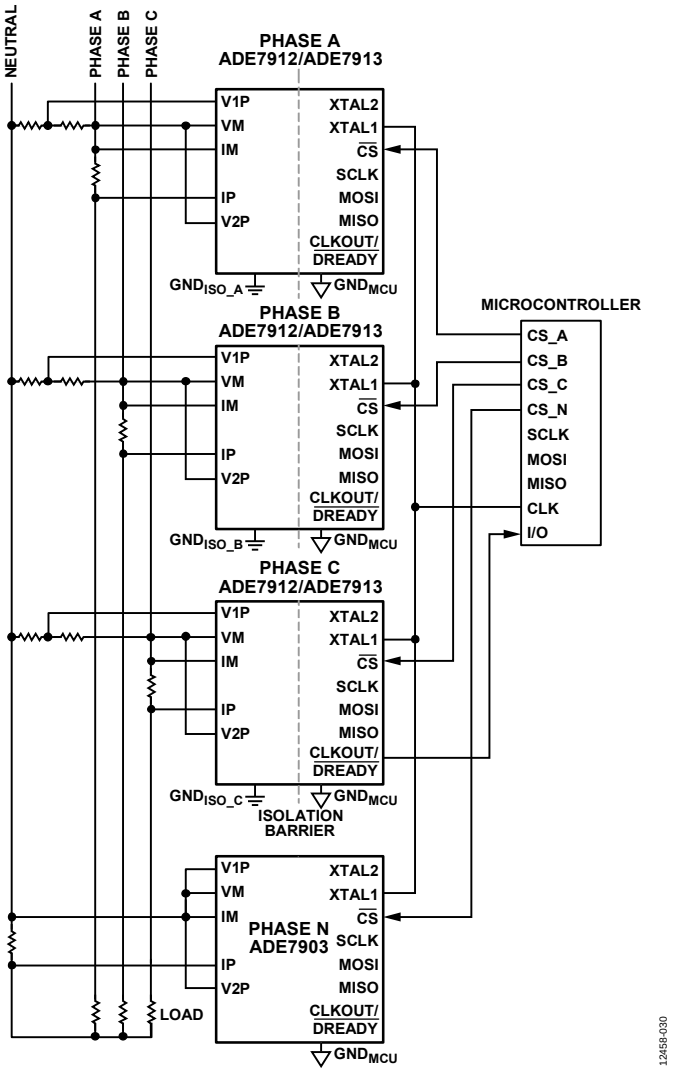


Figure 30. Microcontroller Generating Clock to Three ADE7912/ADE7913 Devices and One ADE7903 Device

In Figure 30, the CLKOUT/$\overline{\text{DREADY}}$ pin of the ADE7912/ADE7913 used to sense the Phase C current and voltage is connected to the input/output pin of the microcontroller. CLKOUT/$\overline{\text{DREADY}}$ provides an active low pulse for 64 CLKIN cycles (15.625 µs at CLKIN = 4.096 MHz) when the ADC conversion data is available. It signals when the ADC outputs of all ADE7912/ADE7913 and ADE7903 devices become available and when the microcontroller starts to read them. See the Synchronizing Multiple ADE7912/ADE7913 and ADE7903 Devices section for more information about synchronizing multiple ADE7912/ADE7913 and ADE7903 devices.

At power-up, or after a hardware or software reset, follow the procedure described in the Power-Up Procedure for Systems with Multiple Devices Using a Single Crystal section or the Power-Up Procedure for Systems with Multiple Devices Using Clock Generated from Microcontroller section to ensure that the ADE7912/ADE7913 and ADE7903 devices function appropriately.

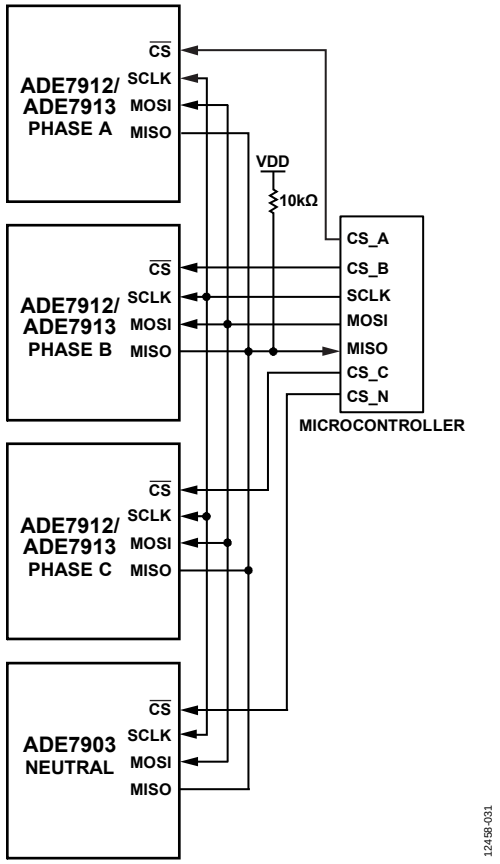


Figure 31. SPI Connections Between Three ADE7912/ADE7913 Devices, One ADE7903 Device, and a Microcontroller

ADE7903 IN SINGLE-PHASE ENERGY METERS

The ADE7903 is also designed for use in a single-phase energy metering system in which one ADE7903 device or an ADE7903 and ADE7912/ADE7913 combination is managed by a master device containing an SPI interface, usually a microcontroller.

Figure 32 shows a block diagram of a single-phase energy meter that uses an ADE7903 on the phase and a microcontroller. One 4.096 MHz crystal provides the clock to the ADE7903 that senses the phase current and voltage. Unlike the isolated solution, this setup means that the ADE7903 is floating at the line voltage. Other combinations of the ADE7903 and the ADE7912/ADE7913 are possible in a single-phase application for monitoring both the phase and the neutral.

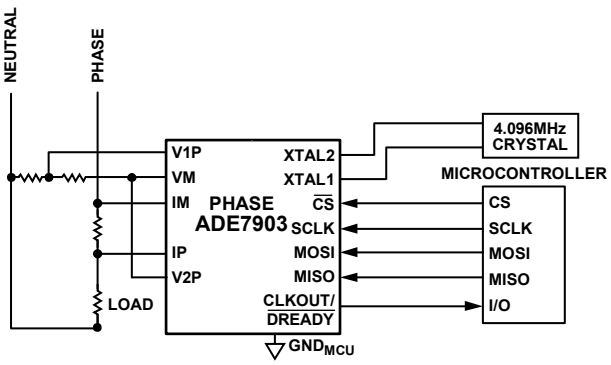


Figure 32. Single-Phase Energy Meter Using an ADE7903 Device

ADE7903 CLOCK

Provide a digital clock signal at the XTAL1 pin to clock the ADE7903. The frequency at which the ADE7903 is clocked at XTAL1 is called CLKIN. The ADE7903 is specified for CLKIN = 4.096 MHz, but frequencies between 3.6 MHz and 4.21 MHz are acceptable.

Alternatively, a 4.096 MHz crystal with a typical drive level of 0.5 mW and an ESR of 20 Ω can be connected across the XTAL1 and XTAL2 pins to provide a clock source for the ADE7903 (see Figure 33).

The total capacitance (TC) at the XTAL1 and XTAL2 pins is

$$TC = C1 + CP1 = C2 + CP2$$

where:
C1 and *C2* are the ceramic capacitors between XTAL1 and GND and between XTAL2 and GND, respectively.
CP1 and *CP2* are the parasitic capacitors of the wires connecting the crystal to the ADE7903.

The load capacitance (LC) of the crystal is equal to half the total capacitance because it is the capacitance of the series circuit composed by C1 + CP1 and C2 + CP2.

$$LC = \frac{C1 + CP1}{2} = \frac{C2 + CP2}{2} = \frac{TC}{2}$$

Therefore, the value of the C1 and C2 capacitors as a function of the load capacitance of the crystal is

$$C1 = C2 = 2 \times LC - CP1 = 2 \times LC - CP2$$

In the case of the ADE7903, the typical total capacitance of the XTAL1 and XTAL2 pins is 40 pF (see Table 1). Select a crystal with a load capacitance of

$$LC = \frac{TC}{2} = 20 \text{ pF}$$

Assuming that the parasitic capacitances, CP1 and CP2, are equal to 20 pF, select the C1 and C2 capacitors equal to 20 pF.

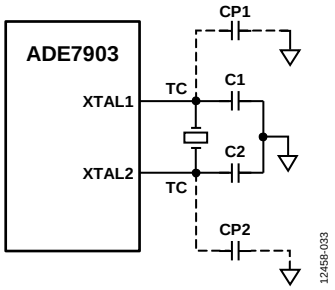


Figure 33. Crystal Circuitry

SPI-COMPATIBLE INTERFACE

The SPI of the ADE7903 is the slave of the communication and consists of four pins: SCLK, MOSI, MISO, and $\overline{CS}$. The serial clock for a data transfer is applied at the SCLK logic input. All data transfer operations synchronize to the serial clock. Data shifts into the ADE7903 at the MOSI logic input on the falling edge of SCLK, and the ADE7903 samples the data on the rising edge of SCLK. Data shifts out of the ADE7903 at the MISO logic output on the falling edge of SCLK and can be sampled by the master device on the rising edge of SCLK. The MSB of the word is shifted in and out first. The maximum and minimum serial clock frequencies supported by this interface are 5.6 MHz and 250 kHz, respectively. MISO stays in high impedance when no data is transmitted from the ADE7903. At power-up or during hardware or software reset, the microcontroller reads the STATUS0 register to detect when Bit 0 (RESET_ON) clears to 0. See Figure 31 for details of the connections between the SPI ports of three ADE7912/ADE7913 devices and one ADE7903 device, and a microcontroller containing an SPI interface.

The $\overline{CS}$ logic input is the chip select input. Drive the $\overline{CS}$ input low for the entire data transfer operation. Bringing $\overline{CS}$ high during a data transfer operation leaves the ADE7903 register that is the object of the data transfer unaffected; however, it aborts the transfer and places the serial bus in a high impedance state. A new transfer can then be initiated by returning the $\overline{CS}$ logic input to low.

SPI Read Operation

The read operation using the ADE7903 SPI interface is initiated when the master sets the $\overline{CS}$ pin low and begins sending one command byte on the MOSI line. The master places data on the MOSI line starting with the first high to low transition of SCLK.

The bit composition of the command byte is shown in Table 7. Bits[1:0] are don't care bits, and they can have any value. The examples presented throughout this section show them set to 00. Bit 2 (READ_EN) determines the type of the operation. For a read, READ_EN must be set to 1. For a write, READ_EN must be cleared to 0. Bits[7:3] (ADDR) represent the address of the register to be read or written.

Table 7. Command Byte for SPI Read/Write Operations

Bit Location	Bit Name	Description
1:0	Reserved	These bits can have any value.
2	READ_EN	Set this bit to 1 if a SPI read operation is executed. Clear this bit to 0 if a SPI write operation is executed.
7:3	ADDR	Address of the register to be read or written.

The ADE7903 SPI samples data on the low to high transitions of SCLK. After the ADE7903 device receives the last bit of the command byte on a low to high transition of SCLK, it begins to transmit its contents on the MISO line when the next SCLK high to low transition occurs; thus, the master can sample the data on a low to high SCLK transition. After the master receives the last bit, it sets the $\overline{CS}$ and SCLK lines high and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. Figure 34 shows an 8-bit register read operation; 16-bit and 32-bit registers are read in the same manner.

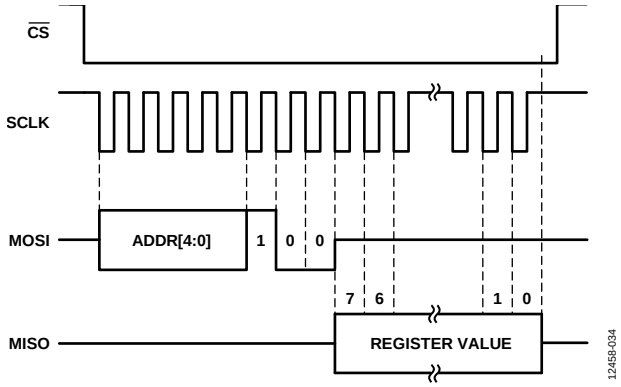


Figure 34. SPI Read Operation of an 8-Bit Register

SPI Read Operation in Burst Mode

All ADE7903 output registers (IWV, V1WV, V2WV, ADC_CRC, STATUS0, and CNT_SNAPSHOT) can be read in one of two ways: one register at a time (see the SPI Read Operation section) or by reading multiple consecutive registers simultaneously in burst mode. Burst mode is initiated when the master sets the $\overline{CS}$ pin low and begins sending the command byte (see Table 7) on the MOSI line with Bits[7:3] (ADDR) set to the IWV register address, 00000. This means a command byte set to 0x04. The master places data on the MOSI line starting with the first high to low transition of SCLK. The SPI of the ADE7903 samples data on the low to high transitions of SCLK. After the ADE7903 device receives the last bit of the command byte on a low to high transition of SCLK, it begins to transmit the 24-bit IWV register on the MISO line when the next SCLK high to low transition occurs; thus, the master can sample the data on a low to high SCLK transition. After the master receives the last bit of the IWV register, the ADE7903 device sends V1WV, which is placed at the next location, and continues in this manner until the master sets the $\overline{CS}$ and SCLK lines high and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 35 for details of the SPI read operation in burst mode.

If a register does not need to be read, for example, the 16-bit CNT_SNAPSHOT register, the master sets the $\overline{CS}$ and SCLK lines high after the STATUS0 register is received.

For example, if the IWV register is not required, but V1WV is, set the ADDR bits to the V1WV address, 00001, in the command byte, and execute the burst mode operation.

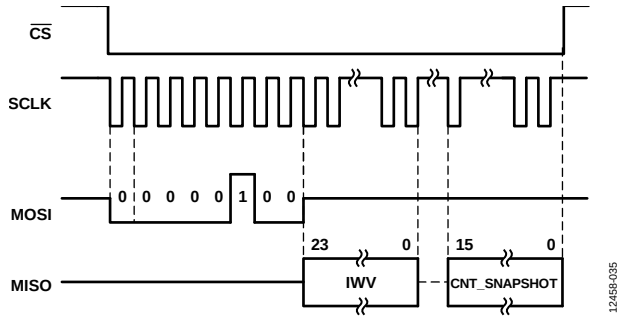


Figure 35. SPI Read Operation in Burst Mode

SPI Write Operation

The SPI write operation is initiated when the master sets the $\overline{CS}$ pin low and begins sending one command byte (see Table 7). Bit 2 (READ_EN) must be cleared to 0. The master places data on the MOSI line starting with the first high to low transition of SCLK. The SPI of the ADE7903 samples data on the low to high transitions of SCLK. Next, the master sends the 8-bit value of the register without losing any SCLK cycles. After the last bit is transmitted, at the end of the SCLK cycle, the master sets the $\overline{CS}$ and SCLK lines high, and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 36 for details of the SPI write operation.

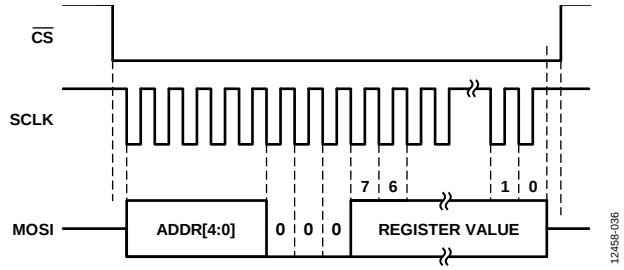


Figure 36. SPI Write Operation

Note that the SPI write operation can execute 8-bit writes only. The 16-bit synchronization counter register (composed of COUNTER0 and COUNTER1) is written by executing the write operation twice: the least significant byte is written first, followed by the most significant byte. See the Synchronizing Multiple ADE7912/ADE7913 and ADE7903 Devices section for details on the functionality controlled by the synchronization counter register.

Because the ADE7903 does not need to acknowledge a write command in any way, this operation can be broadcast to multiple ADE7912/ADE7913 and ADE7903 devices when the same register must be initialized with the same value.

After executing a write operation, it is recommended to read back the register to ensure that it was initialized correctly.

SYNCHRONIZING MULTIPLE ADE7912/ADE7913 AND ADE7903 DEVICES

The ADE7912/ADE7913 and ADE7903 allow the user to sample all currents and voltages simultaneously and to provide coherent ADC output samples, which is a highly desired feature in polyphase metering systems.

The ADE7903 in Polyphase Energy Meters section describes how a polyphase energy meter containing multiple ADE7912/ADE7913 and ADE7903 devices can use one crystal to clock all the ADE7912/ADE7913 and ADE7903 devices. At power-up, only one ADE7912/ADE7913 or ADE7903 device is clocked from the crystal, while the other devices are set to receive the clock from the CLKOUT/$\overline{\text{DREADY}}$ pin of the first ADE7912/ADE7913 device. This pin has $\overline{\text{DREADY}}$ functionality enabled by default. In Figure 29 and Figure 30, the ADE7912/ADE7913 device on Phase A is clocked from the crystal or the microcontroller, and the CLKOUT/$\overline{\text{DREADY}}$ pin generates the $\overline{\text{DREADY}}$ signal. The other ADE7912/ ADE7913 and ADE7903 devices are clocked by the $\overline{\text{DREADY}}$ signal because the CLKOUT signal has not yet been received by their XTAL1 pins. The microcontroller enables CLKOUT functionality when Bit 0 (CLKOUT_EN) in the CONFIG register is set to 1. This operation ensures that the other ADE7912/ ADE7913 and ADE7903 devices in the system receive the same clock as the ADE7912/ADE7913 on Phase A and that all ADCs within all ADE7912/ADE7913 and ADE7903 devices in the system sample data at the same exact moment.

As an alternative to using one crystal, the microcontroller can generate a clock signal to the XTAL1 pins of every ADE7912/ADE7913 and ADE7903, ensuring precise ADC sampling synchronization (see Figure 30).

To configure all ADE7912/ADE7913 and ADE7903 devices in an energy meter to provide coherent ADC output samples, that is, samples obtained in the same output cycle, all ADE7912/ADE7913 and ADE7903 devices must have the same ADC output frequency and the outputs must be synchronized. Bits[5:4] (ADC_FREQ) in the CONFIG register select the ADC output frequency; therefore, they must be initialized to the same value (see the ADC Output Values section for more details).

To synchronize the ADC outputs, that is, to set all ADE7912/ADE7913 and ADE7903 devices to generate ADC outputs at the same exact moment, after power-up, the microcontroller must broadcast a write to the 8-bit SYNC_SNAP register with the value 0x01. All ADE7912/ADE7913 and ADE7903 devices then start a new ADC output period simultaneously when Bit 0 (sync) of the SYNC_SNAP register is written. The sync bit clears itself to 0 after one CLKIN cycle.

As shown in Figure 29 and Figure 30, the CLKOUT/ $\overline{\text{DREADY}}$ pin of one ADE7912/ADE7913 or ADE7903 is connected to an I/O input of the microcontroller. This ADE7912/ADE7913 or ADE7903 device has Bit 0 (CLKOUT_EN) in the CONFIG register set to the default value, 0, to enable the $\overline{\text{DREADY}}$ functionality. When the ADC output period starts, the CLKOUT/$\overline{\text{DREADY}}$ pin goes low for 64 CLKIN cycles (15.625 µs when CLKIN = 4.096 MHz), signaling that all ADC outputs from all ADE7912/ADE7913 and ADE7903 devices are available and the microcontroller must start reading them. It is recommended that the SPI read in burst mode be used to ensure that all data is read in the shortest amount of time.

For more information on the synchronization procedure of ADE7912/ADE7913 devices, refer to the ADE7912/ADE7913 data sheet. The same synchronization procedure applies to the ADE7903.

POWER MANAGEMENT

POWER-UP AND INITIALIZATION PROCEDURES

At power-up or after a hardware or software reset, execute the following steps for a microcontroller managing a system formed by one or multiple ADE7912/ADE7913 and ADE7903 devices.

Power-Up Procedure for Systems with a Single ADE7903

For a standalone ADE7903 device managed by a microcontroller, the power-up procedure is as follows (see Figure 37):

1. Connect a crystal between the XTAL1 and XTAL2 pins.
2. Supply VDD to the ADE7903 device. To ensure that the ADE7903 device starts functioning correctly, the supply must reach 3.3 V − 10% in fewer than 23 ms from approximately a 2.6 V level. The ADE7903 device starts to function.
3. To determine when the ADE7903 device is ready to accept commands, read the STATUS0 register until Bit 0 (RESET_ON) is cleared to 0, which happens approximately 20 ms after the ADE7903 starts to function and indicates that the ADE7903 is fully functional using the default settings.
4. Initialize the CONFIG register.
5. Protect the user accessible and internal configuration registers by setting the lock register to 0xCA. See the Protecting the Integrity of Configuration Registers section.
6. When the ADC conversion data is available, the ADE7903 device begins generating a signal that is active low at the CLKOUT/$\overline{\text{DREADY}}$ pin for 64 CLKIN cycles (15.625 µs for CLKIN = 4.096 MHz). The $\overline{\text{DREADY}}$ functionality is enabled by default at the CLKOUT/$\overline{\text{DREADY}}$ pin.
7. The microcontroller reads the IWV, V1WV, V2WV, ADC_CRC, CNT_SNAPSHOT, and STATUS0 registers in SPI burst mode (see the SPI Read Operation in Burst Mode section for more information).

Note that this power-up procedure also applies in the same way to systems that have multiple ADE7903 devices, each clocked from its own crystal. Every ADE7903 device is powered up and started independently.

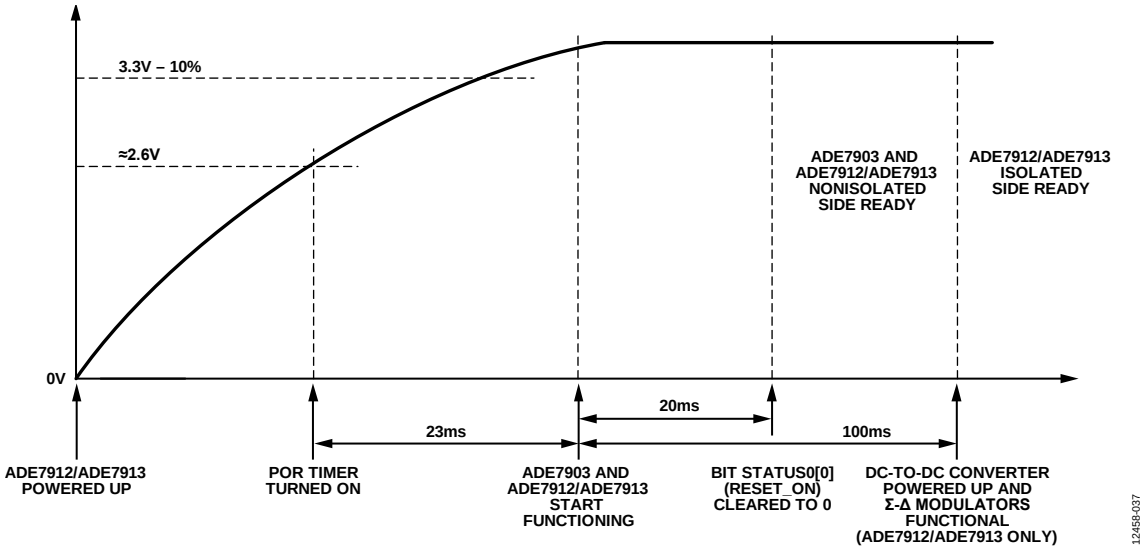


Figure 37. Power-Up Procedure for Systems with One or Multiple ADE7903 and ADE7912/ADE7913 Devices, Each Clocked from Its Own Crystal

Power-Up Procedure for Systems with Multiple Devices Using a Single Crystal

For polyphase energy meters using the ADE7912/ADE7913 and ADE7903 devices, shown in Figure 29 and Figure 30, in which a single crystal is used, see the ADE7912/ADE7913 data sheet for additional details on the power-up procedure.

Power-Up Procedure for Systems with Multiple Devices Using Clock Generated from Microcontroller

For polyphase energy meters in which the microcontroller generates the clock signal used by all ADE7912/ADE7913 and ADE7903 devices (see Figure 30), see the ADE7912/ADE7913 data sheet for additional details on the power-up procedure.

HARDWARE RESET

The ADE7903 does not have a dedicated reset pin. Instead, while the SCLK pin is receiving the serial clock, the $\overline{CS}$ and MOSI pins can be kept low by executing a SPI broadcast write operation in which the lines are kept low for 64 SCLK cycles. This is equivalent to sending eight bytes equal to 0x00 to the ADE7903 to accomplish a hardware reset.

During a hardware reset, all the registers are set to their default values. This procedure can be done simultaneously for an ADE7903 device in a polyphase or single-phase energy meter. At the end of the reset period, the ADE7903 clears Bit 0 (RESET_ON) in the STATUS0 register to 0. At this point, follow one of the procedures described in the Power-Up and Initialization Procedures section to initialize the ADE7903 correctly.

SOFTWARE RESET

Bit 6 (SWRST) in the CONFIG register manages the software reset functionality. The default value of this bit is 0. If this bit is set to 1, the ADE7903 enters the software reset state. In this state, all the internal registers are reset to their default values. When the software reset ends, Bit 6 (SWRST) in the CONFIG register clears automatically to 0, and Bit 0 (RESET_ON) in the STATUS0 register is cleared to 0. If the configuration registers are protected using a lock = 0xCA register write, first unlock the registers by writing lock = 0x9C, and then write to the CONFIG register by setting Bit 6 (SWRST) to 1 to start a software reset. At this point, follow one of the procedures described in the Power-Up and Initialization Procedures section to initialize the ADE7903 correctly.

POWER-DOWN MODE

If the microcontroller generates the clock to all ADE7912/ADE7913 and ADE7903 devices (see Figure 30), the current consumption can be reduced by shutting down the clock. The ADE7903 stops functioning. When the clock is restarted, as a good programming practice, execute a hardware reset to restart the ADE7903.

In systems in which the CLKOUT/$\overline{DREADY}$ pin of one ADE7912/ADE7913 device is used to clock other ADE7912/ADE7913 and ADE7903 devices (see Figure 29 and Figure 30), lower current consumption of the ADE7903 device can be achieved by clearing Bit 0 (CLKOUT_EN) in the CONFIG register to 0.

LAYOUT GUIDELINES

Figure 18 shows the test circuit of the ADE7903. The test circuit contains three ADE7912/ADE7913 devices and one ADE7903 device together with the surrounding circuitry required to sense the phase current and voltages in a 3-phase system. The ADE7912/ADE7913 and ADE7903 devices are managed by a microcontroller using the SPI interface. The microcontroller is not shown in the schematic. For the layout of that schematic, refer to the Layout Guidelines section of the ADE7912/ADE7913 data sheet, in addition to the guidelines in this section for the ADE7903 on the neutral channel.

Figure 38 and Figure 39 show a proposed layout of the printed circuit board (PCB) with two layers that have the components placed on the top layer of the board only. Follow these layout guidelines to create a low noise design.

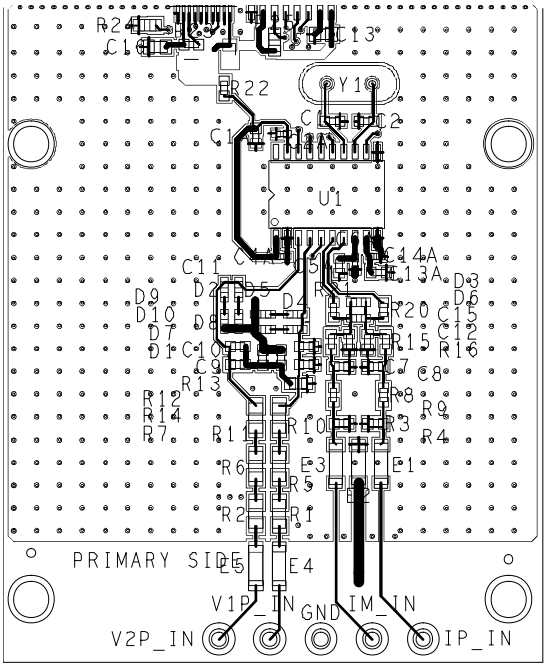


Figure 38. 2-Layer Circuit Board, Top Layer

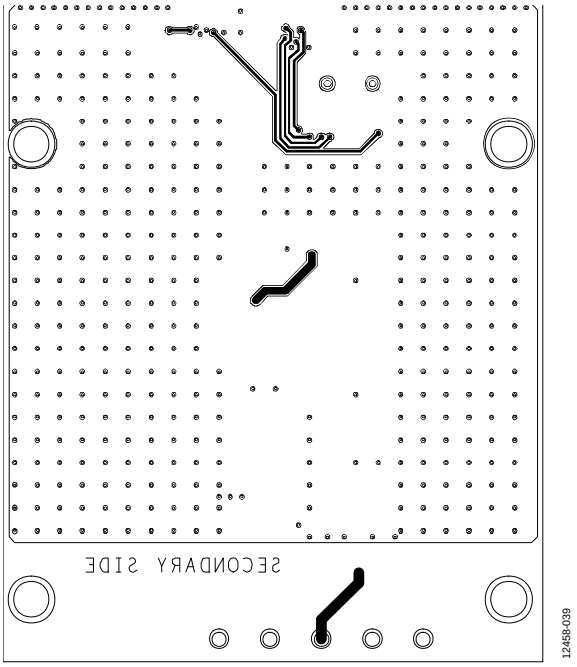


Figure 39. 2-Layer Circuit Board, Bottom Layer

ADE7903 EVALUATION BOARD

The EVAL-ADE7903EBZ evaluation board allows users to quickly evaluate the ADE7903. This evaluation board is used in conjunction with the EVAL-SDP-CB1Z system demonstration platform. Order both the EVAL-ADE7903EBZ evaluation board and the system demonstration platform to evaluate the ADE7903. See the EVAL-ADE7903EBZ product page for details.

ADE7903 VERSION

Bits[2:0] (Version) in the STATUS1 register identify the version of the ADE7903.

REGISTER LIST

In Table 8 to Table 14, R means a register can be read, and W means a register can be written. U means an unsigned register, and S means a signed register in twos complement format.

Table 8. Register List

Address	Register Name	R/W	Bit Length	Type	Default Value[1]	Description
0x0	IWV	R	24	S	0x000000	Instantaneous value of Current I.
0x1	V1WV	R	24	S	0x000000	Instantaneous value of Voltage V1.
0x2	V2WV	R	24	S	0x000000	Instantaneous value of Voltage V2.
0x3	Reserved	R	24	S	0x000000	Reserved. This location always reads 0x000000.
0x4	ADC_CRC	R	16	U	N/A	CRC value of IWV, V1WV, and V2WV registers. See the CRC of ADC Output Values section for details.
0x5	CTRL_CRC	R	16	U	N/A	CRC value of configuration registers. See the CRC of Configuration Registers section for details.
0x6	Reserved	R	16	S	0x0000	Reserved. This location always reads 0x0000.
0x7	CNT_SNAPSHOT	R	16	U	0x00	Snapshot value of the counter used in synchronization operation. See Table 9 and the Synchronizing Multiple ADE7912/ADE7913 and ADE7903 Devices section for details.
0x8	CONFIG	R/W	8	U	0	Configuration register. See Table 10 for details.
0x9	STATUS0	R	8	U	0x01	Status register. See Table 11 for details.
0xA	Lock	W	8	U	0x00	Memory protection register. See the Protecting the Integrity of Configuration Registers section and Table 12 for details.
0xB	SYNC_SNAP	W	8	U	0x00	Synchronization register. See Table 13 for details.
0xC	COUNTER0	R/W	8	U	N/A	Contains the eight LSBs of the internal synchronization counter.
0xD	COUNTER1	R/W	8	U	N/A	COUNTER1[3:0] bits contain the four MSBs of the internal synchronization counter. See the Synchronizing Multiple ADE7912/ADE7913 and ADE7903 Devices section for details.
0xE	Reserved	R/W	8	U	0xFF	Reserved registers.
0xF	STATUS1	R	8	U	0x00	Status register. See Table 14 for details.
0x10, 0x11	Reserved	R/W	8	U	0x00	For proper operation, do not write to these registers.
0x12, 0x13	Reserved	R	8	U	0x00	Reserved registers.
0x14	Reserved					No functionality assigned at this address.
0x15, 0x16, 0x17	Reserved	R	8	U	0x00	Reserved registers.
0x18	TEMPOS	R	8	S	N/A	Temperature sensor offset. See the Temperature Sensor section for more information.

[1] N/A means not applicable.

Table 9. CNT_SNAPSHOT Register (Address 0x7)

Bit(s)	Name	Default Value	Description
[11:0]	Counter	0x000	Snapshot value of the counter used in synchronization operation.
[15:12]	Reserved	0000	Reserved. These bits do not represent any functionality.

Table 10. CONFIG Register (Address 0x8)

Bit(s)	Name	Default Value	Description
0	CLKOUT_EN	0	Enables CLKOUT functionality at the CLKOUT/$\overline{\text{DREADY}}$ pin. When CLKOUT_EN = 0, the default value, $\overline{\text{DREADY}}$ functionality is enabled. When CLKOUT_EN = 1, CLKOUT functionality is enabled.
1	Reserved	0	Reserved. This bit does not represent any functionality.
2	Reserved	0	Reserved bit.
3	TEMP_EN	0	This bit selects the second voltage channel measurement. When the TEMP_EN bit is set to 0, the default value, the voltage between the V2P and VM pins is measured. When this bit is 1, the internal temperature sensor is measured (see the Temperature Sensor section for more information).
[5:4]	ADC_FREQ	00	These bits select the ADC output frequency. 00 = 8 kHz, 125 µs period. 01 = 4 kHz, 250 µs period. 10 = 2 kHz, 500 µs period. 11 = 1 kHz, 1 ms period.
6	SWRST	0	When this bit is set to 1, a software reset is initiated. This bit clears itself to 0 after one CLKIN cycle.
7	BW	0	Selects the bandwidth of the digital low-pass filter of the ADC. When BW = 0, the default value, the bandwidth is 3.3 kHz. When BW = 1, the bandwidth is 2 kHz. The bandwidth data is for CLKIN = 4.096 MHz and an ADC output frequency of 8 kHz. See the Analog-to-Digital Conversion section for details on how CLKIN and the ADC output frequency influence the bandwidth selection.

Table 11. STATUS0 Register (Address 0x9)

Bit(s)	Name	Default Value	Description
0	RESET_ON	1	During reset, the RESET_ON bit is set to 1. When the reset ends and the ADE7903 is ready to be configured, the RESET_ON bit is cleared to 0.
1	CRC_STAT	0	If the CRC of the configuration registers changes value, the CRC_STAT bit is set to 1.
2	IC_PROT	0	If the configuration registers are not protected, this bit is 0. After the configuration registers are protected (lock register = 0xCA), this bit is set to 1.
[7:3]	Reserved	0	Reserved. These bits do not represent any functionality.

Table 12. Lock Register (Address 0xA)

Bit(s)	Name	Default Value	Description
[7:0]	LOCK_KEY	00000000	When the LOCK_KEY bits are equal to 0xCA, protection of the configuration registers is enabled. When the LOCK_KEY bits are equal to 0x9C, the protection is disabled, and the configuration registers can be written. This is a write only register. If the address location is read, the value is 0x00.

Table 13. SYNC_SNAP Register (Address 0xB)

Bit(s)	Name	Default Value	Description
0	Sync	0	When the sync bit is set to 1 via a broadcast SPI write operation, the ADE7912/ADE7913 devices in the system generate ADC outputs in the same exact moment. The bit clears itself back to 0 after one CLKIN cycle. See the Synchronizing Multiple ADE7912/ADE7913 and ADE7903 Devices section for more details.
1	Snap	0	When snap is set to 1 via a broadcast SPI write operation, the internal counters of the ADE7912/ADE7913 devices in the system are latched. The bit clears itself back to 0 after one CLKIN cycle. See the Synchronizing Multiple ADE7912/ADE7913 and ADE7903 Devices section for more details.
[7:2]	Reserved	0	Reserved. These bits do not represent any functionality.

Table 14. STATUS1 Register (Address 0xF)

Bit(s)	Name	Default Value	Description
[2:0]	Version	0	The ADE7903 version number.
3	ADC_NA	0	If the ADC outputs are not accessed during one ADC output period, the ADC_NA bit is set to 1. When the STATUS1 register is read, the bit is cleared to 0.
[6:4]	Reserved	0	Reserved. These bits do not represent any functionality.
7	Reserved	0	Reserved. Internal functionality is associated with this bit.