Dual RF PLL Frequency Synthesizers

ADF4206/ADF4208

FEATURES

ADF4206: 550 MHz/550 MHz
ADF4208: 2.0 GHz/1.1 GHz
2.7 V to 5.5 V power supply
Selectable charge pump supply (V_P) allows extended tuning voltage in 3 V systems
Selectable charge pump currents
On-chip oscillator circuit
Selectable dual modulus prescaler
RF2: 32/33 or 64/65
RF1: 32/33 or 64/65
3-wire serial interface
Power-down mode

APPLICATIONS

Wireless handsets (GSM, PCS, DCS, CDMA, WCDMA)
Base stations for wireless radio (GSM, PCS, DCS, CDMA, WCDMA)
Wireless LANS
Communications test equipment
CATV equipment

GENERAL DESCRIPTION

The ADF420x family of dual frequency synthesizers are used to implement local oscillators in the upconversion and down-conversion sections of wireless receivers and transmitters. Each synthesizer consists of a low noise, digital, phase frequency detector (PFD); a precision charge pump; a programmable reference divider; programmable A and B counters; and a dual modulus prescaler (P/P + 1). The A (6-bit) and B (11-bit) counters, in conjunction with the dual modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R counter) allows selectable REFIN frequencies at the PFD input. The on-chip oscillator circuitry allows the reference input to be derived from crystal oscillators.

A complete phase-locked loop (PLL) can be implemented if the synthesizers are used with an external loop filter and voltage controlled oscillators (VCOs).

Control of all the on-chip registers is via a simple 3-wire interface. The devices operate with a power supply ranging from 2.7 V to 5.5 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

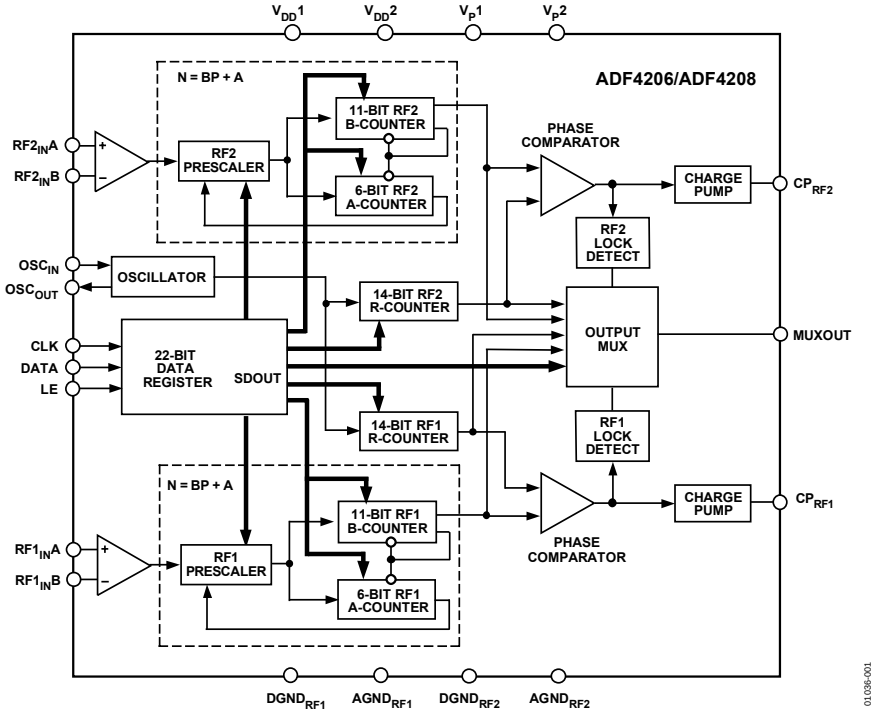

Figure 1.

Rev. A

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TABLE OF CONTENTS

REVISION HISTORY

2/06—Rev. 0 to Rev. A

Updated Format ... Universal
Deleted ADF4207 ... Universal
Changes to Table 3 ... 6
Changes to Function Description ... 7
Changes to Table 4 ... 7
Changes to Figure 22 Caption ... 12
Changes to Pulse Swallow Function ... 13
Changes to Figure 29 ... 15
Changes to Figure 31 ... 17
Updated Outline Dimensions ... 25
Changes to Ordering Guide ... 25

3/01—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD}1 = V_{DD}2 = 3$ V ± 10%, 5 V ± 10%; $V_{DD}1$, $V_{DD}2 \le V_P1$, $V_P2 \le 6.0$ V; $AGND_{RF1} = DGND_{RF1} = AGND_{RF2} = DGND_{RF2} = 0$ V;
$T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted; dBm referred to 50 Ω.

Table 1.

Parameter	B Version[1]	B Chips[2]	Unit	Test Conditions/Comments
RF/IF CHARACTERISTICS (3 V)				See Figure 22 for input circuit
RF1 Input Frequency ($RF1_{IN}$)				
ADF4206	0.05/0.55	0.05/0.55	GHz min/max	For f < 50 MHz ensure SR > 23 V/µs
ADF4208	0.08/2.0	0.08/2.0	GHz min/max	For f < 50 MHz ensure SR > 37 V/µs
RF Input Sensitivity	−15/+4	−15/+4	dBm min/max	
IF Input Frequency ($RF2_{IN}$)				
ADF4206	0.05/0.55	0.05/0.55	GHz min/max	For f < 50 MHz ensure SR > 23 V/µs
ADF4208	0.08/1.1	0.08/1.1	GHz min/max	For f < 50 MHz ensure SR > 37 V/µs
IF Input Sensitivity	−15/+4	−15/+4	dBm min/max	
Maximum Allowable Prescaler Output Frequency[3]	165	165	MHz max	
RF CHARACTERISTICS (5 V)				
RF1 Input Frequency ($RF1_{IN}$)				
ADF4206	0.05/0.55	0.05/0.55	GHz min/max	For f < 50 MHz ensure SR > 32 V/µs
ADF4208	0.08/2.0	0.08/2.0	GHz min/max	For f < 50 MHz ensure SR > 51 V/µs
RF Input Sensitivity	−10/+4	−10/+4	dBm min/max	
IF Input Frequency ($RF2_{IN}$)			MHz min/max	
ADF4206	0.05/0.55	0.05/0.55	GHz min/max	For f < 50 MHz ensure SR > 32 V/µs
ADF4208	0.08/1.1	0.08/1.1	GHz min/max	For f < 50 MHz ensure SR > 51 V/µs
IF Input Sensitivity	−10/+4	−10/+4	dBm min/max	
Maximum Allowable Prescaler Output Frequency[3]	200	200	MHz max	
REFIN CHARACTERISTICS				
REFIN Input Frequency	5/40	5/40	MHz min/max	For f < 5 MHz ensure SR > 9 V/µs
REFIN Input Sensitivity[4]	−2	−2	dBm min	
REFIN Input Capacitance	10	10	pF max	
REFIN Input Current	±100	±100	µA max	
PHASE DETECTOR				
Phase Detector Frequency[5]	55	55	MHz max	
CHARGE PUMP				
I_{CP} Sink/Source				
High Value	5	5	mA typ	
Low Value	1.25	1.25	mA typ	
Absolute Accuracy	2.5	2.5	% typ	
I_{CP} Three-State Leakage Current	1	1	nA typ	
LOGIC INPUTS				
V_{INH}, Input High Voltage	$0.8 \times V_{DD}$	$0.8 \times V_{DD}$	V min	
V_{INL}, Input Low Voltage	$0.2 \times V_{DD}$	$0.2 \times V_{DD}$	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	$V_{DD} - 0.4$	$V_{DD} - 0.4$	V min	I_{OH} = 500 µA
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 500 µA

Parameter	B Version[1]	B Chips[2]	Unit	Test Conditions/Comments
POWER SUPPLIES				
$V_{DD}1$	2.7/5.5	2.7/5.5	V min/V max	
$V_{DD}2$	$V_{DD}1$	$V_{DD}1$		
V_P	$V_{DD}1$/6.0	$V_{DD}1$/6.0	V min/V max	$V_{DD}1$, $V_{DD}2 \le V_P1$, $V_P2 \le 6.0$ V
I_{DD} ($I_{DD}1 + I_{DD}2$)[6]				
ADF4206	14	14	mA max	9.5 mA typical at V_{DD} = 3 V, T_A = 25°C
ADF4208	21	21	mA max	14 mA typical at V_{DD} = 3 V, T_A = 25°C
$I_{DD}1$				
ADF4206	8	8	mA max	5.5 mA typical at V_{DD} = 3 V, T_A = 25°C
ADF4208	14	14	mA max	9 mA typical at V_{DD} = 3 V, T_A = 25°C
$I_{DD}2$				
ADF4206	7.5	7.5	mA max	5 mA typical at V_{DD} = 3 V, T_A = 25°C
ADF4208	9	9	mA max	5.5 mA typical at V_{DD} = 3 V, T_A = 25°C
I_P ($I_P1 + I_P2$)	1	1	mA max	T_A = 25°C
Low Power Sleep Mode	0.5	0.5	µA typ	
NOISE CHARACTERISTICS				
Normalized Phase Noise Floor (RF1)[7]				
ADF4206	−213	−213	dBc/Hz typ	
ADF4208	−217	−217	dBc/Hz typ	
Phase Noise Performance[8]				@ VCO output
ADF4206 (RF1, RF2)	−92	−92	dBc/Hz typ	@ 540 MHz output, 200 kHz at PFD
ADF4208 (RF1)	−85	−85	dBc/Hz typ	@ 1750 MHz output, 200 kHz at PFD
ADF4208 (RF1)	−91	−91	dBc/Hz typ	@ 900 MHz output, 200 kHz at PFD
Spurious Signals				
RF1, RF2 (20 kHz Loop B/W)	−80/−84	−80/−84	dB typ	@ 200 kHz/400 kHz offsets and 200 kHz PFD

[1] Operating temperature range for B version: −40°C to +85°C.
[2] The B chip specifications are given as typical values.
[3] This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.
[4] AC coupling ensures $AV_{DD}/2$ bias. $V_{DD}1 = V_{DD}2$ = 3 V; For $V_{DD}1 = V_{DD}2$ = 5 V, use CMOS-compatible levels.
[5] Guaranteed by design. Sample tested to ensure compliance.
[6] Typical values apply for V_{DD} = 3 V; P = 32; $RF1_{IN}1/RF2_{IN}2$ for ADF4206 = 540 MHz; $RF1_{IN}1/RF2_{IN}2$ for ADF4208 = 900 MHz.
[7] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value) and 10 log F_{PFD}. $PN_{SYNTH} = PN_{TOT} - 10 \log F_{PFD} - 20 \log N$.
[8] The phase noise is measured at 1 kHz, unless otherwise noted. The phase noise is measured with the EVAL-ADF4206EB or the EVAL-ADF4208EB evaluation board and the HP8562E spectrum analyzer. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10 MHz @ 0 dBm).

TIMING SPECIFICATIONS

$V_{DD}1 = V_{DD}2 = 3$ V ± 10%, 5 V ± 10%; $V_{DD}1$, $V_{DD}2 \le V_P1$, $V_P2 \le 6.0$ V; $AGND_{RF1} = DGND_{RF1} = AGND_{RF2} = DGND_{RF2} = 0$ V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted; dBm referred to 50 Ω.

Table 2.

Parameter[1]	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLK setup time
t_2	10	ns min	DATA to CLK hold time
t_3	25	ns min	CLK high duration
t_4	25	ns min	CLK low duration
t_5	10	ns min	CLK to LE setup time
t_6	20	ns min	LE pulse width

[1] Guaranteed by design but not production tested.

TIMING DIAGRAM

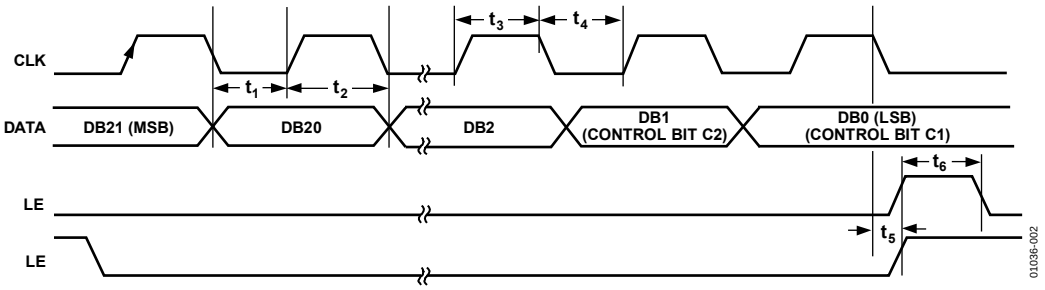


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.[1]

Table 3.

Parameter	Ratings
$V_{DD}1$ to GND[2]	−0.3 V to +7 V
$V_{DD}1$ to $V_{DD}2$	−0.3 V to +0.3 V
V_P1, V_P2 to GND	−0.3 V to +7 V
V_P1, V_P2 to $V_{DD}1$	−0.3 V to +5.5 V
Digital I/O Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to VP + 0.3 V
OSC_{IN}, OSC_{OUT}, $RF1_{IN}$ (A, B), $RF2_{IN}$ (A, B) to GND	−0.3 V to V_{DD} + 0.3 V
RF_{IN}A to RF_{IN}B (RF1, RF2)	±320 mV
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
TSSOP θ_{JA} Thermal Impedance	112°C/W
LFCSP θ_{JA} Thermal Impedance (Paddle Soldered)	30.4°C/W
Reflow Soldering	
Peak Temperature (40 sec)	260°C

[1] This device is a high performance RF integrated circuit with an ESD rating of <2 kΩ and it is ESD sensitive. Proper precautions should be taken for handling and assembly.
[2] GND = AGND = DGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TRANSISTOR COUNT

11,749 (CMOS) and 522 (Bipolar).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

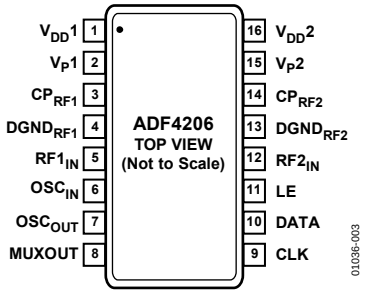


Figure 3. 16-Lead TSSOP Pin Configuration

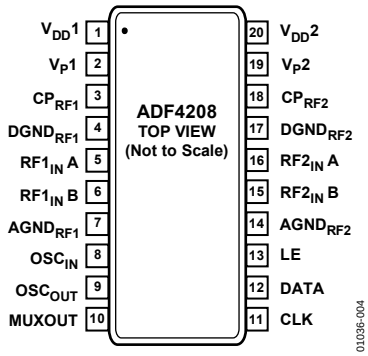


Figure 4. 20-Lead TSSOP Pin Configuration

Table 4. Pin Function Descriptions

ADF4206 Pin No.	ADF4208 Pin No.	Mnemonic	Description
1	1	$V_{DD}1$	Positive Power Supply for the RF1 Section. A 0.1 µF capacitor is connected between this pin and $DGND_{RF1}$ (the RF1 ground pin). $V_{DD}1$ should have a value of between 2.7 V and 5.5 V. $V_{DD}1$ must have the same potential as $V_{DD}2$.
2	2	V_P1	Power Supply for the RF1 Charge Pump. This is greater than or equal to V_{DD}.
3	3	CP_{RF1}	Output from the RF1 Charge Pump. This is normally connected to a loop filter that drives the input to an external VCO.
4	4	$DGND_{RF1}$	Ground Pin for the RF1 Digital Circuitry.
5	5	$RF1_{IN}$/$RF1_{IN}$A	Input to the RF1 Prescaler. This low level input signal is taken from the RF1 VCO.
6	8	OSC_{IN}	Oscillator Input. It has a $V_{DD}/2$ threshold and is driven from an external CMOS or TTL logic gate.
7	9	OSC_{OUT}	Oscillator Output.
8	10	MUXOUT	This multiplexer output allows the IF/RF lock detect, the scaled RF, or the scaled reference frequency external access. See Figure 30.
9	11	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 22-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
10	12	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs as the control bits. This input is a high impedance CMOS input.
11	13	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
12	16	$RF2_{IN}$/$RF2_{IN}$A	Input to the RF2 Prescaler. This low level input signal is normally ac-coupled to the external VCO.
13	17	$DGND_{RF2}$	Ground Pin for the RF2, Digital, Interface, and Control Circuitry.
14	18	CP_{RF2}	Output from the RF2 Charge Pump. This is normally connected to a loop filter that drives the input to an external VCO.
15	19	V_P2	Power Supply for the RF2 Charge Pump. This is greater than or equal to V_{DD}.
16	20	$V_{DD}2$	Positive Power Supply for the RF2, Interface, and Oscillator Sections. A 0.1 µF capacitor is connected between this pin and $DGND_{RF2}$ (the RF2 ground pin). $V_{DD}2$ has a value between 2.7 V and 5.5 V. $V_{DD}2$ must have the same potential as $V_{DD}1$.
N/A	6	$RF1_{IN}$B	Complementary Input to the RF1 Prescaler of the ADF4208. This point is decoupled to the ground plane with a small bypass capacitor.
N/A	7	$AGND_{RF1}$	Ground Pin for the RF1 Analog Circuitry.
N/A	14	$AGND_{RF2}$	Ground Pin for the RF2 Analog Circuitry.
N/A	15	$RF2_{IN}$B	Complementary Input to the RF2 Prescaler. This point is decoupled to the ground plane with a small bypass capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

FREQ-UNIT	PARAM-TYPE	DATA-FORMAT	KEYWORD	IMPEDANCE (Ω)
GHz	S	MA	R	50

FREQ	MAGS11	ANGS11	FREQ	MAGS11	ANGS11
0.0	0.957111193	−3.130429321	1.35	0.816886959	−51.80711782
0.15	0.963546793	−6.686426265	1.45	0.825983016	−56.20373378
0.25	0.953621785	−11.19913586	1.55	0.791737125	−61.21554647
0.35	0.953757706	−15.35637483	1.65	0.770543186	−61.88187496
0.45	0.929831379	−20.3793432	1.75	0.793897072	−65.39516615
0.55	0.908459709	−22.69144845	1.85	0.745765233	−69.24884474
0.65	0.897303634	−27.07001443	1.95	0.7517547	−71.21608147
0.75	0.876862863	−31.32240763	2.05	0.745594889	−75.93169947
0.85	0.849338092	−33.68058163	2.15	0.713387801	−78.8391674
0.95	0.858403269	−38.57674885	2.25	0.711578577	−81.71934806
1.05	0.841888714	−41.48606772	2.35	0.698487131	−85.49067481
1.15	0.840354983	−45.97597958	2.45	0.669871818	−88.41958754
1.25	0.822165839	−49.19163116	2.55	0.668353367	−91.70921678

01036-005

Figure 5. S-Parameter Data for the ADF4208 RF1 Input (Up to 2.5 GHz)

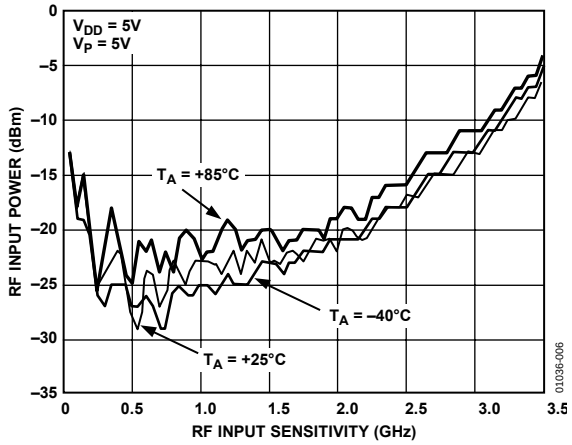


Figure 6. ADF4208 RF1 Phase Noise (900 MHz, 200 kHz, 20 kHz)

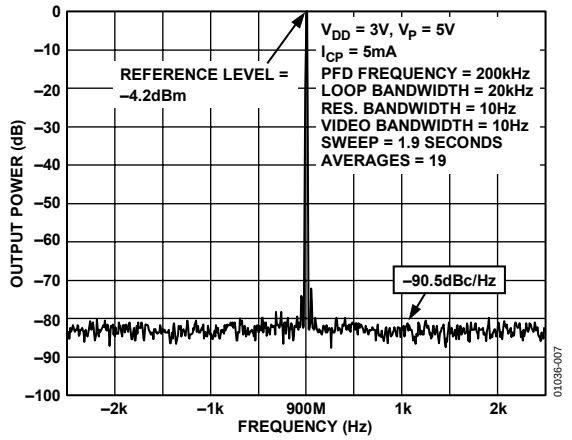


Figure 7. ADF4208 RF1 Phase Noise (900 MHz, 200 kHz, 20 kHz)

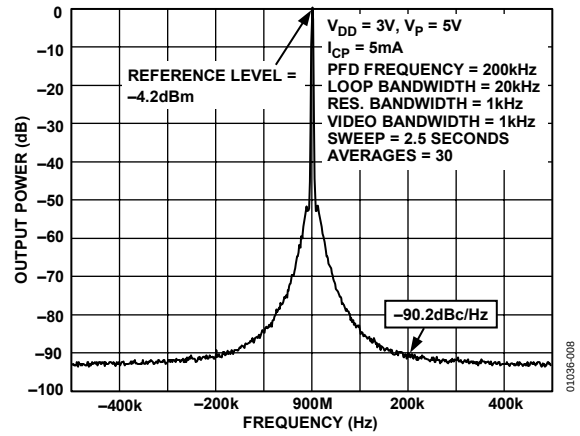


Figure 8. ADF4208 RF1 Reference Spurs (900 MHz, 200 kHz, 20 kHz)

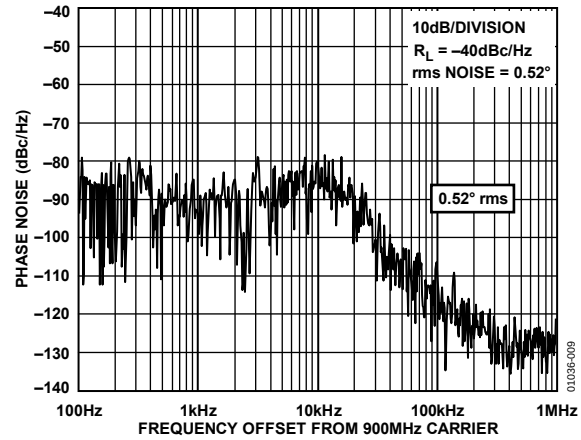


Figure 9. ADF4208 RF1 Integrated Phase Noise (900 MHz, 200 kHz, 20 kHz)

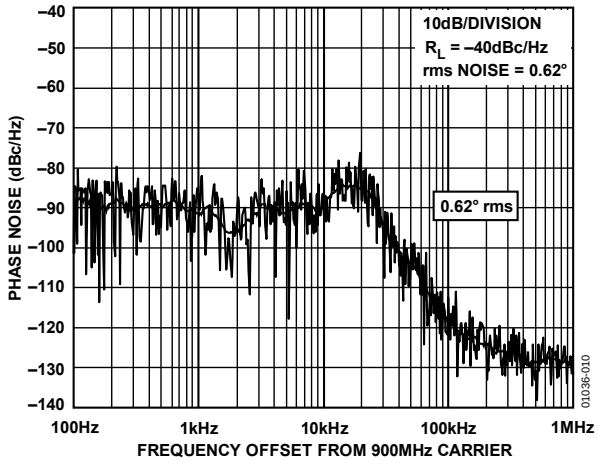


Figure 10. ADF4208 RF1 Integrated Phase Noise (900 MHz, 200 kHz, 35 kHz)

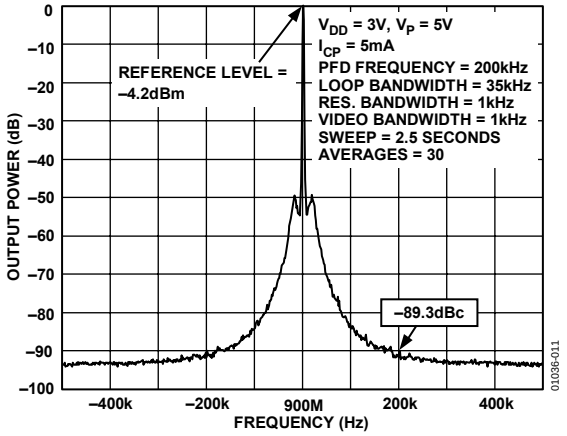


Figure 11. ADF4208 RF1 Reference Spurs (900 MHz, 200 kHz, 35 kHz)

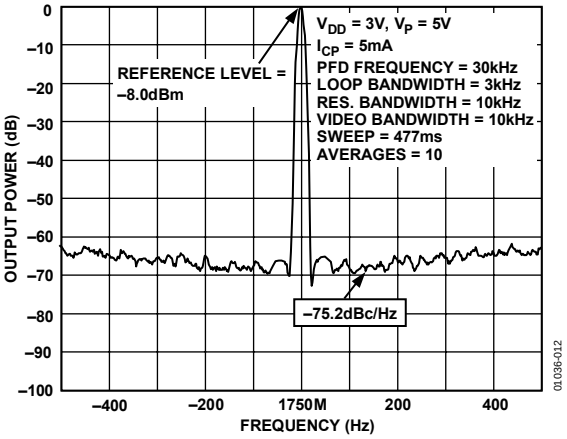


Figure 12. ADF4208 RF1 Phase Noise (1750 MHz, 30 kHz, 3 kHz)

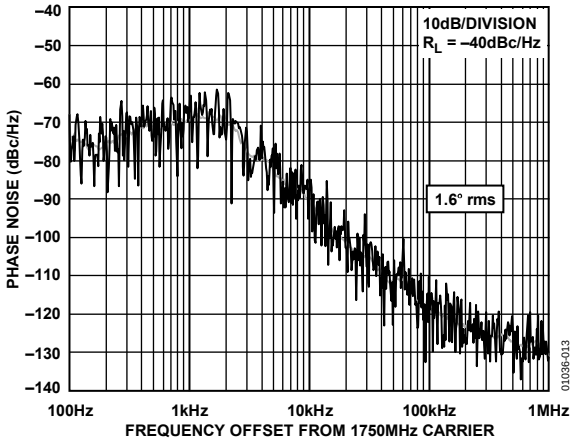


Figure 13. ADF4208 RF1 Integrated Phase Noise (1750 MHz, 30 kHz, 3 kHz)

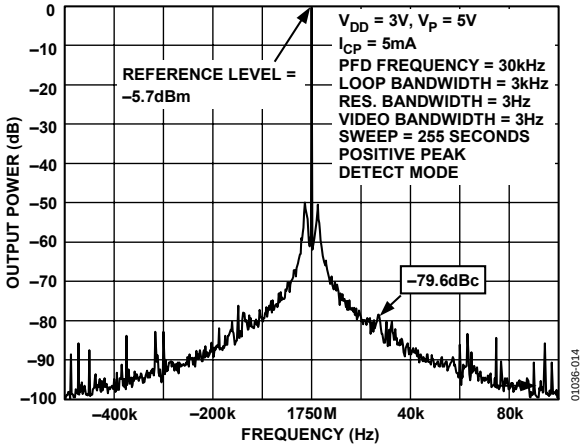


Figure 14. ADF4208 RF1 Reference Spurs (1750 MHz, 30 kHz, 3 kHz)

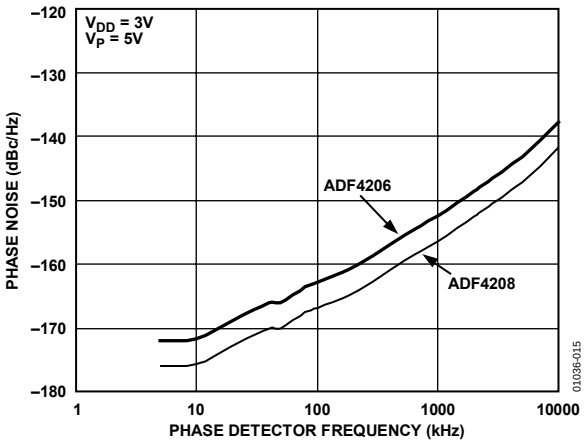


Figure 15. ADF4208 RF1 Phase Noise vs. PFD Frequency

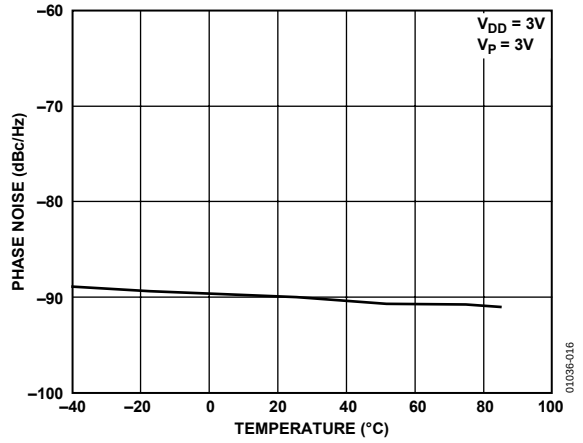


Figure 16. ADF4208 RF1 Phase Noise vs. Temperature (900 MHz, 200 kHz, 20 kHz)

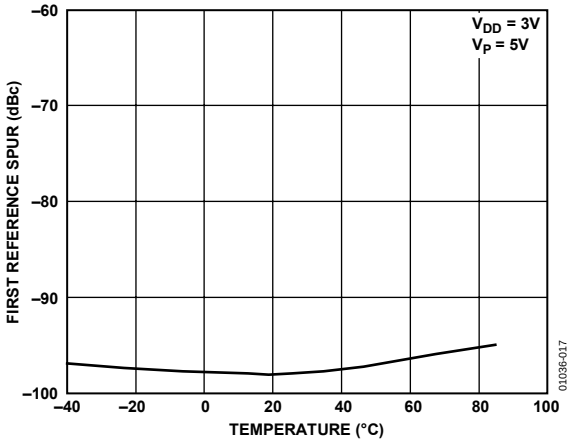


Figure 17. ADF4208 RF1 Reference Spurs vs. Temperature (900 MHz, 200 kHz, 20 kHz)

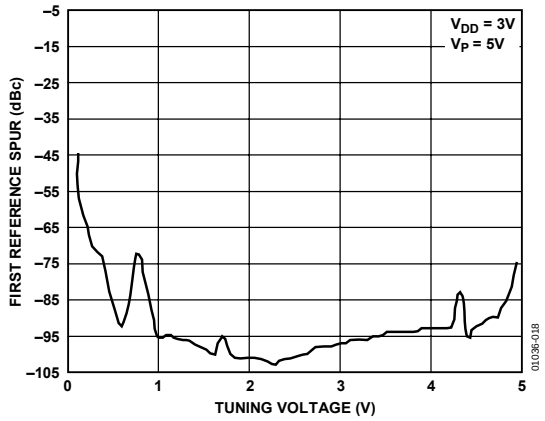


Figure 18. ADF4208 RF1 Reference Spurs vs. V_{TUNE} (900 MHz, 200 kHz, 20 kHz)

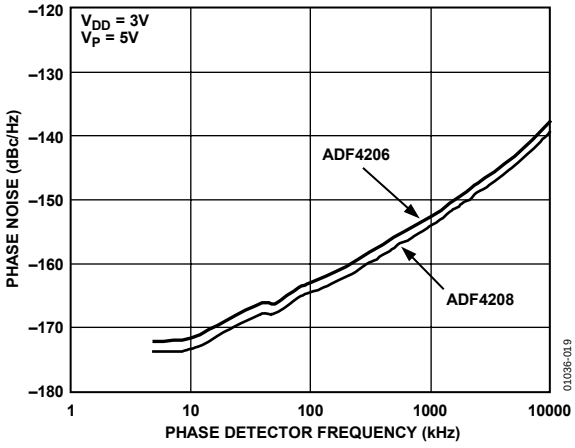


Figure 19. ADF4208 RF2 Phase Noise vs. PFD Frequency

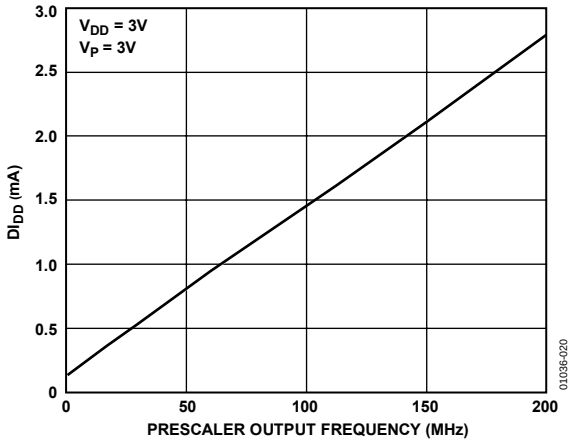


Figure 20. DI_{DD} vs. Prescaler Output Frequency RF1 and RF2 (All Models)

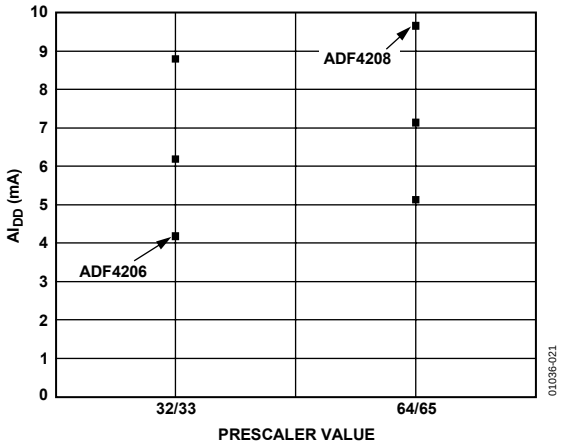


Figure 21. ADF4206/ADF4208 AI_{DD} vs. Prescaler Value (RFI)

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 22. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. Typical recommended external components are shown in Figure 22.

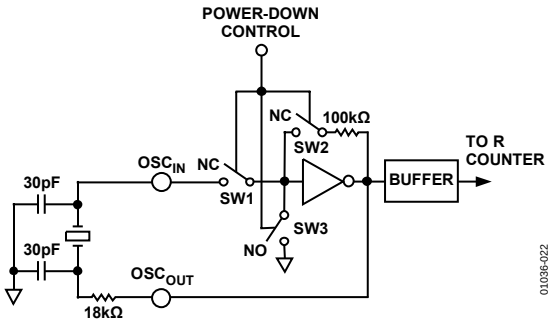


Figure 22. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 23. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

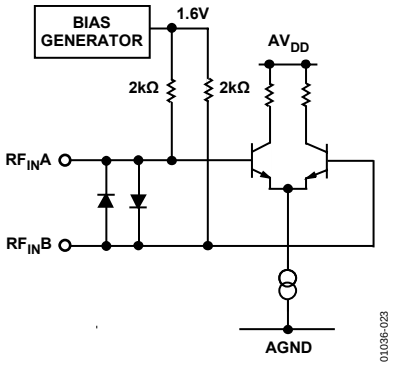


Figure 23. RF Input Stage

PRESCALER

The dual modulus prescaler (P/P + 1), along with the A and B counters, enables the large division ratio, N, to be realized (N = BP + A). This prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A and B counters. It is based on a synchronous 4/5 core.

The prescaler is selectable. Both RF1 and RF2 can be set to either 32/33 or 64/65. DB20 of the AB counter latch selects the value. See Figure 29 and Figure 31.

A AND B COUNTERS

The A and B CMOS counters combine with the dual modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The devices are guaranteed to work when the prescaler output is 200 MHz or less.

PULSE SWALLOW FUNCTION

The A and B counters, in conjunction with the dual modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The equation for the VCO frequency is

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN}/R$$

where:

f_{VCO} is the output frequency of the external voltage controlled oscillator (VCO).

P is the preset modulus of the dual modulus prescaler (32/33, 64/65).

B is the preset divide ratio of the binary 11-bit counter (2 to 2047).

A is the preset divide ratio of the binary 6-bit A counter (0 to 63).

f_{REFIN} is the output frequency of the external reference frequency oscillator.

R is the preset divide ratio of the binary 14-bit programmable reference counter (1 to 16,383).

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

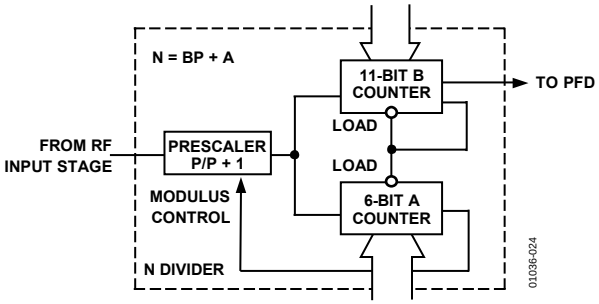


Figure 24. A and B Counters

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter (N = BP + A) and produces an output proportional to the phase and frequency difference between them. Figure 25 is a simplified schematic.

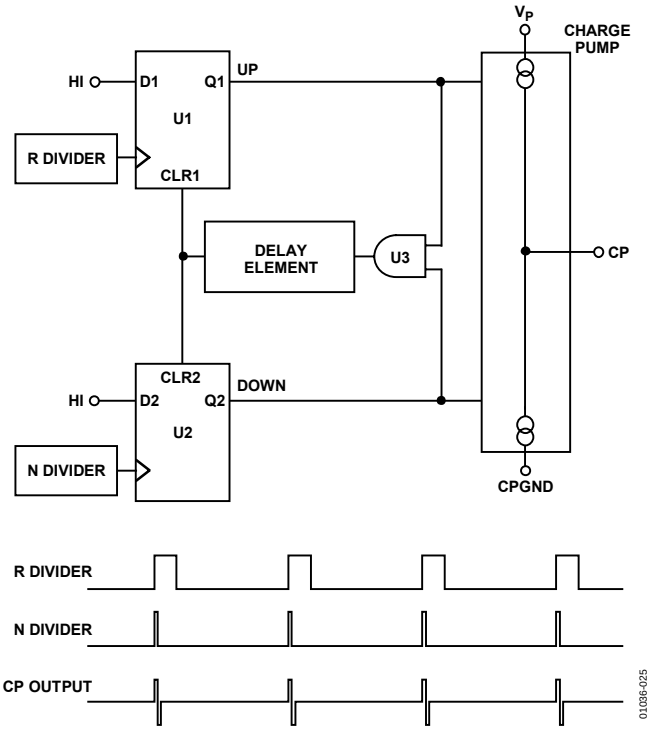


Figure 25. PFD Simplified Schematic and Timing (In Lock)

The PFD includes a delay element that sets the width of the antibacklash phase. The typical value for this in the ADF420x family is 3 ns. The pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs.

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4206 family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by P3, P4, P11, and P12. See Figure 28 and Figure 30. Figure 26 shows the MUXOUT circuit in block diagram form.

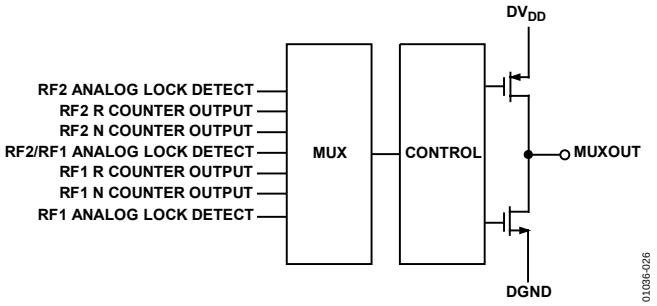


Figure 26. MUXOUT Circuit

LOCK DETECT

MUXOUT can be programmed for analog lock detect. The N-channel open-drain analog lock detect is operated with an external pull-up resistor of 10 kΩ nominal. When lock is detected, it is high with narrow, low going pulses.

INPUT SHIFT REGISTER

The functional block diagram for the ADF420x family is shown in Figure 1. The main blocks include a 22-bit input shift register, a 14-bit R counter, and a 17-bit N counter, comprising a 6-bit A counter and an 11-bit B counter. Data is clocked into the 22-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs (DB1, DB0) as shown in the timing diagram of Figure 2.

Table 5 is the truth table for these bits.

Table 5. C2, C1 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	RF2 R counter
0	1	RF2 AB counter (and prescaler select)
1	0	RF1 R counter
1	1	RF1 AB counter (and prescaler select)

RF2 REFERENCE COUNTER LATCH

RF2 F_O	RF2 LOCK DETECT	THREE-STATE CP_{RF2}	RF2 CP GAIN	RF2 PD POLARITY	NOT USED	14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P4	P3	P2	P5	P1		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

RF2 AB COUNTER LATCH

RF2 POWER-DOWN	RF2 PRESCALER	11-BIT B COUNTER											NOT USED	6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P7	P6	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (0)	C1 (0)

RF1 REFERENCE COUNTER LATCH

RF1 F_O	RF1 LOCK DETECT	THREE-STATE CP_{RF1}	RF1 CP GAIN	RF1 PD POLARITY	NOT USED	14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P12	P11	P10	P13	P9		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

RF1 AB COUNTER LATCH

RF1 POWER-DOWN	RF1 PRESCALER	11-BIT B COUNTER											NOT USED	6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	P14	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

01036-027

Figure 27. ADF4206 Family Latch Summary

RF2 REFERENCE COUNTER LATCH

RF2 F_O	RF2 LOCK DETECT	THREE-STATE CP_{RF2}	RF2 CP GAIN	RF2 PD POLARITY		14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P4	P3	P2	P5	P1		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

R14	R13	R12	.....	R3	R2	R1	DIVIDE RATIO
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16380
1	1	1	.....	1	0	1	16381
1	1	1	.....	1	1	0	16382
1	1	1	.....	1	1	1	16383

P1	PD POLARITY
0	NEGATIVE
1	POSITIVE

P5	I_{CP}
0	1.25mA
1	4.375mA

P2	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

P12 FROM RF1 R LATCH	P11	P4	P3	MUXOUT
0	0	0	0	LOGIC LOW STATE
0	0	0	1	RF2 ANALOG LOCK DETECT
0	X	1	0	RF2 REFERENCE DIVIDER OUTPUT
0	X	1	1	RF2 N DIVIDER OUTPUT
0	1	0	0	RF1 ANALOG LOCK DETECT
0	1	0	1	RF1/RF2 ANALOG LOCK DETECT
1	X	0	0	RF1 REFERENCE DIVIDER
1	X	0	1	RF1 N DIVIDER
1	0	1	0	FAST LOCK OUTPUT SWITCH ON AND CONNECTED TO MUXOUT
1	0	1	1	RF2 COUNTER RESET
1	1	1	0	RF1 COUNTER RESET
1	1	1	1	RF2 AND RF1 COUNTER RESET

01036-031

Figure 28. RF2 Reference Counter Latch Map

RF2 AB COUNTER LATCH

RF2 POWER-DOWN	RF2 PRESCALER	11-BIT B COUNTER												6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P7	P6	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

A6	A5	A4	A3	A2	A1	A COUNTER DIVIDE RATIO
X	X	0	0	0	0	0
X	X	0	0	0	1	1
X	X	0	0	1	0	2
X	X	0	0	1	1	3
.	.	.	.	.	.	
.	.	.	.	.	.	
.	.	.	.	.	.	
X	X	1	1	1	0	14
X	X	1	1	1	1	15

B11	B10	B9	.....	B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	.....	0	0	0	NOT ALLOWED
0	0	0	.....	0	0	1	NOT ALLOWED
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	2044
1	1	1	.....	1	0	1	2045
1	1	1	.....	1	1	0	2046
1	1	1	.....	1	1	1	2047

P6	RF2 PRESCALER
0	64/65
1	32/33

P7	RF2 SECTION
0	NORMAL OPERATION
1	POWER-DOWN

N = BP + A, P IS PRESCALER VALUE SET BY P6. B MUST BE GREATER THAN OR EQUAL TO A. TO ENSURE CONTINUOUSLY ADJACENT VALUES OF N × F_{REF}, N_{MIN} IS (P^2 – P).

01036-032

Figure 29. RF2 AB Counter Latch Map

RF1 REFERENCE COUNTER LATCH

RF1 F_O	RF1 LOCK DETECT	THREE-STATE CP_{RF1}	RF1 CP GAIN	RF1 PD POLARITY		14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P12	P11	P10	P13	P9		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

R14	R13	R12	.....	R3	R2	R1	DIVIDE RATIO
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16380
1	1	1	.....	1	0	1	16381
1	1	1	.....	1	1	0	16382
1	1	1	.....	1	1	1	16383

P9	PD POLARITY
0	NEGATIVE
1	POSITIVE

P13	I_{CP}
0	1.25 mA
1	4.375 mA

P10	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

P12	P11	P4 FROM RF2 R LATCH	P3	MUXOUT
0	0	0	0	LOGIC LOW STATE
0	0	0	1	RF2 ANALOG LOCK DETECT
0	X	1	0	RF2 REFERENCE DIVIDER OUTPUT
0	X	1	1	RF2 N DIVIDER OUTPUT
0	1	0	0	RF1 ANALOG LOCK DETECT
0	1	0	1	RF1/RF2 ANALOG LOCK DETECT
1	X	0	0	RF1 REFERENCE DIVIDER
1	X	0	1	RF1 N DIVIDER
1	0	1	0	FAST LOCK OUTPUT SWITCH ON AND CONNECTED TO MUXOUT
1	0	1	1	RF2 COUNTER RESET
1	1	1	0	RF1 COUNTER RESET
1	1	1	1	RF2 AND RF1 COUNTER RESET

01036-033

Figure 30. RF1 Reference Counter Latch Map

RF1 AB COUNTER LATCH

RF1 POWER-DOWN	RF1 PRESCALER	11-BIT B COUNTER												6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	P14	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

A6	A5	A4	A3	A2	A1	A COUNTER DIVIDE RATIO
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
.	.	.	.	.	.	
.	.	.	.	.	.	
.	.	.	.	.	.	
1	1	1	1	1	0	62
1	1	1	1	1	1	63

B11	B10	B9	.....	B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	.....	0	0	0	NOT ALLOWED
0	0	0	.....	0	0	1	NOT ALLOWED
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	2044
1	1	1	.....	1	0	1	2045
1	1	1	.....	1	1	0	2046
1	1	1	.....	1	1	1	2047

P14	RF1 PRESCALER
0	64/65
1	32/33

P16	RF1 SECTION
0	NORMAL OPERATION
1	POWER-DOWN

N = BP + A, P IS PRESCALER VALUE SET BY P6. B MUST BE GREATER THAN OR EQUAL TO A. FOR CONTINUOUSLY ADJACENT VALUES OF N, N_{MIN} IS (P^2 – P).

01036-034

Figure 31. RF1 AB Counter Latch Map

PROGRAM MODES

Figure 28 and Figure 30 show how to set up the program modes in the ADF420x family. Three points should be noted:

1. RF2 and RF1 analog lock detect indicate when the PLL is in lock. When the loop is locked and either RF2 or RF1 analog lock detect is selected, the MUXOUT pin shows a logic high with narrow, low going pulses. When the RF2/RF1 analog lock detect is chosen, the locked condition is indicated only when both RF2 and RF1 loops are locked.
2. The RF2 counter reset mode resets the R and AB counters in the RF2 section and also puts the RF2 charge pump into three-state. The RF1 counter reset mode resets the R and AB counters in the RF1 section and also puts the RF1 charge pump into three-state. The RF2 and RF1 counter reset mode resets the R and AB counters on both the RF1 and RF2 simultaneously.

   Upon removal of the reset bits, the AB counter resumes counting in close alignment with the R counter (maximum error is one prescaler output cycle).
3. The fast lock mode uses MUXOUT to switch a second loop filter damping resistor to ground during fast lock operation. Activation of fast lock occurs whenever the RF1 CP gain in the RF1 reference counter is set to one.

POWER-DOWN

It is possible to program the ADF420x family for either synchronous or asynchronous power-down on either the RF2 or RF1 side.

Synchronous RF2 Power-Down

Programming a 1 to P7 of the ADF420x family initiates a power-down. If P2 of the ADF420x family has been set to 0 (normal operation), a synchronous power-down is conducted. The device automatically puts the charge pump into three-state and completes the power-down.

Asynchronous RF2 Power-Down

If P2 of the ADF420x family has been set to 1 (three-state the RF2 charge pump), and P7 is subsequently set to 1, an asynchronous power-down is conducted. The device enters power-down on the rising edge of LE latching the 1 to P7 (the RF2 power-down bit).

Synchronous RF1 Power-Down

Programming a 1 to P16 of the ADF420x family initiates a power-down. If P10 of the ADF420x family is set to 0 (normal operation), a synchronous power-down is conducted. The device automatically puts the charge pump into three-state and completes the power-down.

Asynchronous RF1 Power-Down

If P10 of the ADF420x family is set to 1 (three-state the RF1 charge pump), and P16 is subsequently set to 1, an asynchronous power-down occurs. The device goes into power-down on the rising edge of LE latching the 1 to P16 (the RF1 power-down bit).

Activation of either synchronous or asynchronous power-down forces the R and N dividers of the RF2/RF1 loop to their load state conditions, and the RF2/RF1 input section is debiased to a high impedance state.

The reference oscillator circuit is only disabled if both the RF2 and RF1 power-downs are set.

The input register and latches remain active and are capable of loading and latching data during all power-down modes.

The RF2/RF1 section of the devices returns to normal powered up operation immediately upon LE latching a 0 to the appropriate power-down bit.

IF SECTION (RF2)

Programmable RF2 Reference (R) Counter

If Control Bit C2 and Control Bit C1 are 0 and 0, the data is transferred from the input shift register to the 14-bit RF2 R counter. Figure 28 shows the input shift register data format for the RF2 R counter and the divide ratios that are possible.

RF2 Phase Detector Polarity

P1 sets the RF2 phase detector polarity. When the RF2 VCO characteristics are positive, this is set to 1. When they are negative, it is set to 0. See Figure 28.

RF2 Charge Pump Three-State

P2 puts the RF2 charge pump into three-state mode when programmed to a 1. It is set to 0 for normal operation. See Figure 28.

RF2 Program Modes

Figure 28 and Figure 30 show how to set up the program modes in the ADF420x family.

RF2 Charge Pump Currents

Bit P5 programs the current setting for the RF2 charge pump. See Figure 28.

Programmable RF2 AB Counter

If Control Bit C2 and Control Bit C1 are 0 and 1, the data in the input register is used to program the RF2 AB counter. The AB counter is a 6-bit swallow counter (A counter) and an 11-bit programmable counter (B counter). Figure 29 shows the input register data format for programming the RF2 AB counter and the divide ratios that are possible.

RF2 Prescaler Value

P6 in the RF2 AB counter latch sets the RF2 prescaler value. See Figure 29.

RF2 Power-Down

P7 in Figure 29 is the power-down bit for the RF2 side.

RF SECTION (RF1)

Programmable RF1 Reference (R) Counter

If Control Bit C2 and Control Bit C1 are 1 and 0, the data is transferred from the input shift register to the 14-bit RF1 R counter. Figure 30 shows the input shift register data format for the RF1 R counter and the divide ratios that are possible.

RF1 Phase Detector Polarity

P9 sets the RF1 phase detector polarity. When the RF1 VCO characteristics are positive this is set to 1. When negative it is set to 0. See Figure 30.

RF1 Charge Pump Three-State

P10 puts the RF1 charge pump into three-state mode when programmed to a 1. It is set to 0 for normal operation. See Figure 30.

RF1 Program Modes

Figure 28 and Figure 30 show how to set up the program modes in the ADF420x family.

RF1 Charge Pump Currents

Bit P13 programs the current setting for the RF1 charge pump. See Figure 30.

Programmable RF1 AB Counter

If Control Bit C2 and Control Bit C1 are 1 and 1, then the data in the input register is used to program the RF1 AB counter. The AB counter is a 6-bit swallow counter (A counter) and 11-bit programmable counter (B counter). Figure 31 shows the input register data format for programming the RF1 AB counter and the divide ratios that are possible.

RF1 Prescaler Value

P14 in the RF1 A, B counter latch sets the RF1 prescaler value. See Figure 31.

RF1 Power-Down

Setting P16 in the RF1 AB counter high powers down RF1 side.

RF Fast Lock

The fast lock feature improves the lock time of the PLL. It increases charge pump current to a maximum for a time. Activate fast lock of the ADF420x family by setting P13 in the reference counter high and setting the fast lock switch on using MUXOUT. Switching in an external resistor using MUXOUT compensates the loop dynamics for the effect of increasing charge pump current. Setting P13 low removes the PLL from fast lock mode.

APPLICATIONS SECTION

LOCAL OSCILLATOR FOR GSM HANDSET RECEIVER

Figure 33 shows the ADF4208 used in a classic superheterodyne receiver to provide the required local oscillators (LOs).

In this circuit, the reference input signal is applied to the circuit at OSC_{IN} and is generated by a 10 MHz crystal oscillator. This is a low cost solution. For better performance over temperature, a TCXO (temperature controlled crystal oscillator) can be used instead.

To have a channel spacing of 200 kHz (the GSM standard), the reference input must be divided by 50 using the on-chip reference counter.

The RF output frequency range is 1050 MHz to 1086 MHz. Loop filter component values are chosen so that the loop bandwidth is 20 kHz. The synthesizer is set up for a charge pump current of 4.375 mA and the VCO sensitivity is 15.6 MHz/V.

The IF output is fixed at 125 MHz. The IF loop bandwidth is chosen to be 20 kHz with a channel spacing of 200 kHz. Loop filter component values are chosen accordingly.

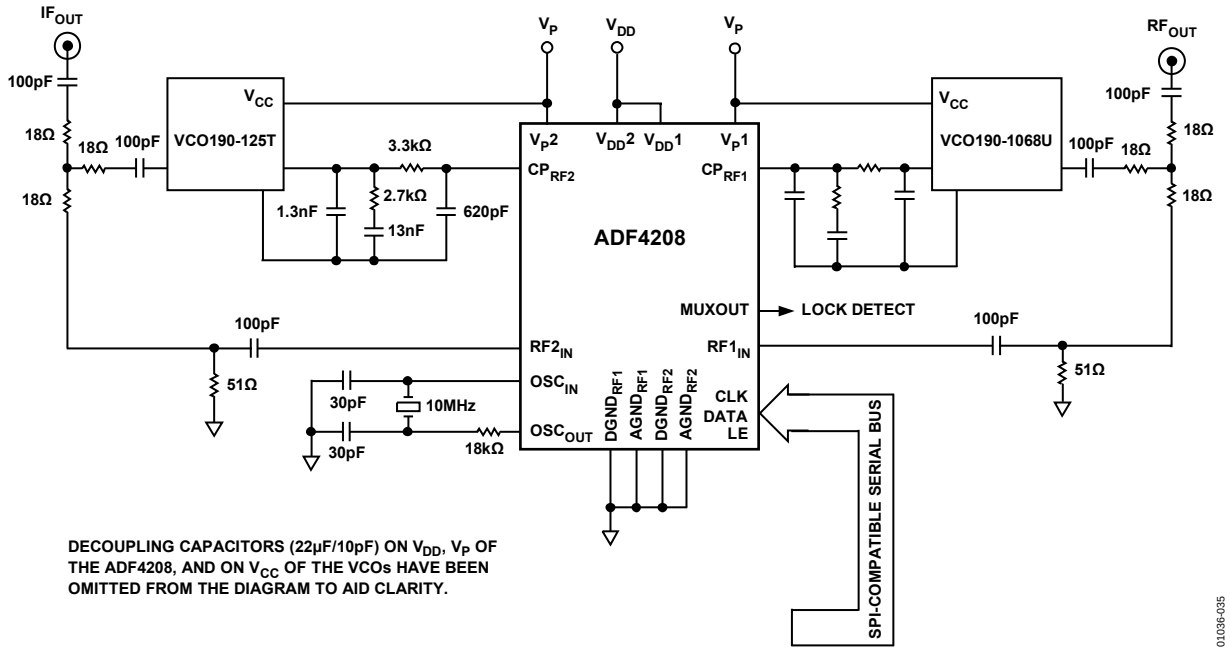


Figure 32. GSM Handset Receiver Local Oscillator Using the ADF4208

LOCAL OSCILLATOR FOR WCDMA RECEIVER

Figure 33 shows the ADF4208 used to generate the local oscillator frequencies for a wideband CDMA (WCDMA) system.

The required RF output range is 1720 MHz to 1780 MHz. The VCO190-1750T meets this requirement. Channel spacing is 200 kHz with a 20 kHz loop bandwidth. VCO sensitivity is 32 MHz/V. A charge pump current of 4.375 mA is used and the desired phase margin for the loop is 45°.

When the IF output is fixed at 200 MHz, the VCO190-200T is used. It has a sensitivity of 10 MHz/V. Channel spacing and loop bandwidth are chosen to be the same as the RF side.

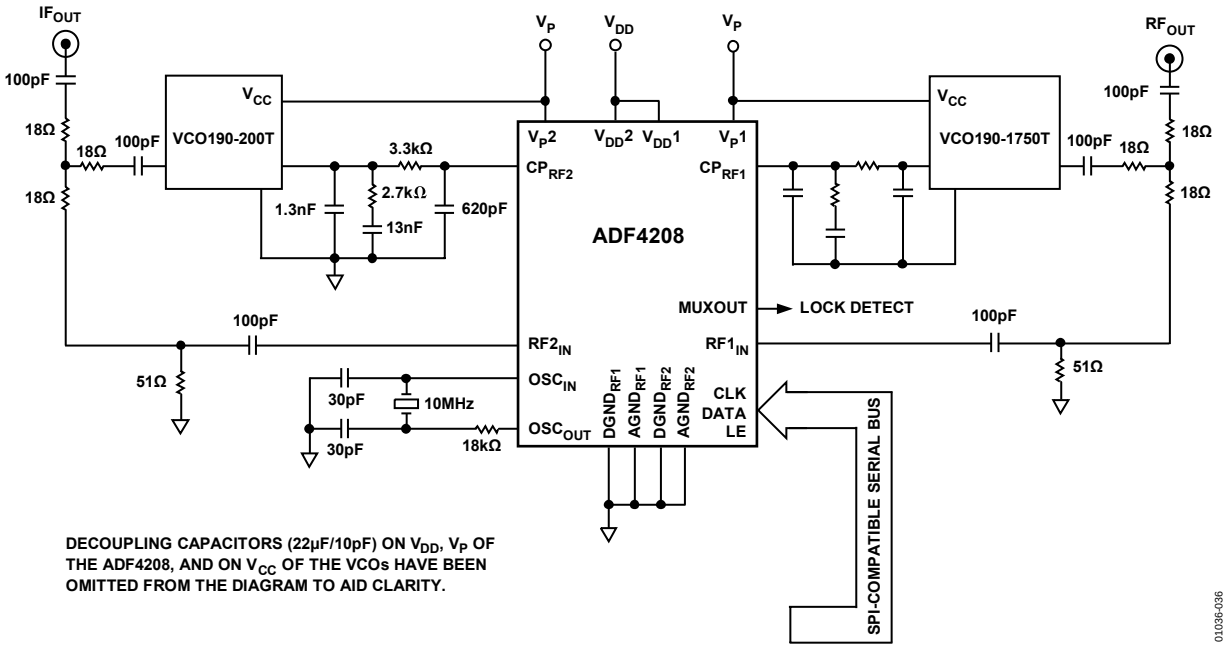


Figure 33. Local Oscillator for WCDMA Receiver Using the ADF4208

INTERFACING

The ADF420x family has a simple SPI®-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE goes high, the 22 bits clocked into the input register on each rising edge of CLK transfers to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 909 kHz or one update every 1.1 ms. This is more than adequate for systems that have typical lock times in hundreds of microseconds.

ADuC812 INTERFACE

Figure 34 shows the interface between the ADF420x family and the ADuC812 microconverter. Because the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The microconverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF420x family needs a 22-bit word. This is accomplished by writing three 8-bit bytes from the microconverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

On first applying power to the ADF420x family, it requires four writes (one each to the R counter latch and the AB counter latch for both RF1 and RF2 sides) for the output to become active.

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed will be about 180 kHz.

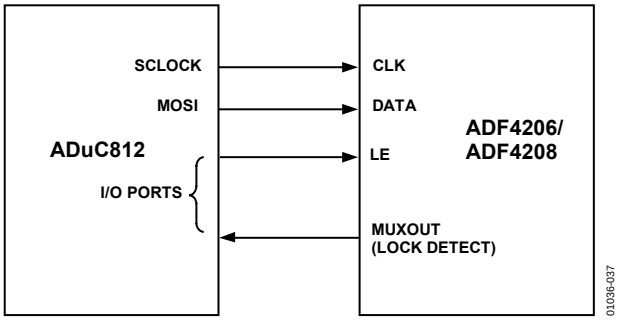


Figure 34. ADuC812 to ADF420x Family Interface

ADSP-2181 INTERFACE

Figure 35 shows the interface between the ADF420x family and the ADSP-21xx digital signal processor. The ADF420x family needs a 22-bit serial word for each latch write. The easiest way to accomplish this using the ADSP21-xx family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for eight bits and use three memory locations for each 22-bit word. To program each 22-bit latch, store the three 8-bit bytes, enable the autobuffered mode and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

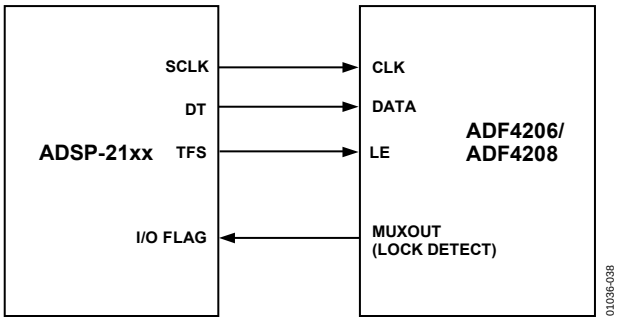
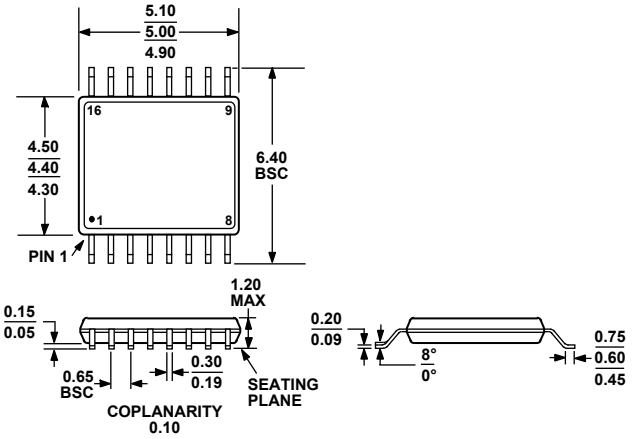


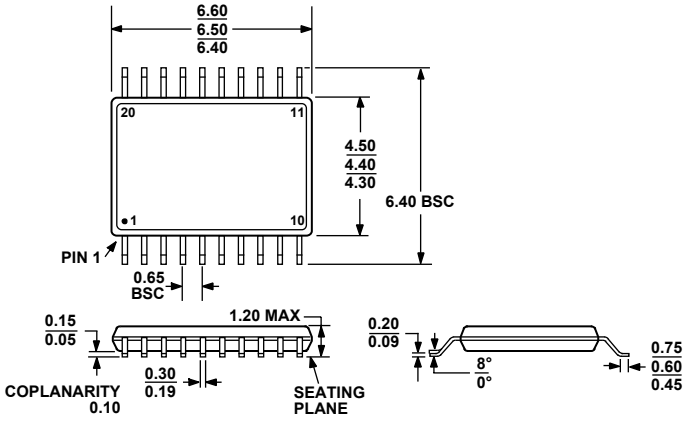
Figure 35. ADSP-21xx to ADF420x Family Interface

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 36. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 37. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters