

FEATURES

Radio frequency (RF) ranges

- 169.4 MHz to 169.6 MHz
- 426 MHz to 470 MHz
- 863 MHz to 960 MHz

Data rates

- 2FSK/2GFSK: 0.1 kbps to 300 kbps
- 4FSK/4GFSK: 1 kbps to 360 kbps (transmit only)

Dual power amplifiers (PAs)

Programmable receiver channel bandwidth

- from 2.6 kHz to 406 kHz

Receiver (Rx) performance

- Up to 97 dB blocking at ± 20 MHz offset
- Up to 72 dB adjacent channel rejection
- 134.3 dBm sensitivity at 0.1 kbps
- 121.3 dBm sensitivity at 2.4 kbps

Transmitter (Tx) performance

- 20 dBm to +17 dBm range with 0.1 dB step resolution
- Very low output power variation vs. temperature and supply

Low active current

- 50 mA Tx current at 17 dBm
- 21.2 mA Rx current at 12.5 kbps

Ultralow sleep current

- 10 nA with memory retained

Host microprocessor interface

- Easy to use programming serial peripheral interface (SPI)
- Configurable 8-bit general-purpose input/output (GPIO) bus

On-chip ARM Cortex-M0 processor for

- Radio control and calibration
- Packet management
- Clear channel assessment (CCA)

IEEE802.15.4g support

- Frame format
- Data whitening
- Dual-sync word detection
- Forward error correction (FEC) and interleaving

Suitable for systems targeting compliance with

- ETSI EN 300 220-1
- EN 54-25, EN 13757-4
- FCC Part 15, Part 22, Part 24, Part 90, and Part 101
- ARIB STD-T30, STD-T67, STD-T108, STD-T96

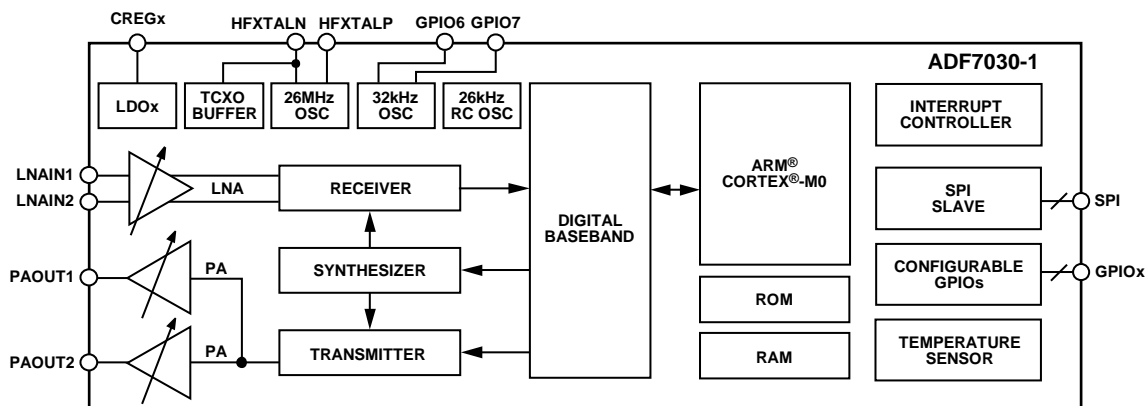
Packages

- 6 mm \times 6 mm, 40-lead LFCSP
- 7 mm \times 7 mm, 48-lead LQFP

APPLICATIONS

- IEEE 802.15.4g (MR-FSK PHY)
- Wireless M-Bus (EN 13757-4)
- Smart metering
- Security and building automation
- Active tag asset tracking
- Industrial control
- Wireless sensor networks (WSNs)

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. CREGx, GPIOx, AND SPI CONTAIN MULTIPLE PINS.

Figure 1.

14373-001

Rev. A

Document Feedback

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TABLE OF CONTENTS

| | | | |
|--|----|--------------------------------------|----|
| Features | 1 | 460 MHz—Transmit | 34 |
| Applications | 1 | 868 MHz—Receive | 36 |
| Functional Block Diagram | 1 | 868 MHz—Transmit | 38 |
| Revision History | 2 | 915 MHz—Receive | 40 |
| General Description | 3 | 915 MHz—Transmit | 42 |
| Specifications | 4 | Theory of Operation | 44 |
| Temperature and Voltage | 4 | State Machine | 44 |
| General RF | 4 | Radio Timing | 45 |
| Receive | 5 | Host Interface | 46 |
| Transmit | 6 | Receiver | 46 |
| Current Consumption | 8 | Transmitter | 48 |
| Band Specific Receive and Transmit | 9 | Calibration | 49 |
| External 26 MHz Oscillator | 19 | Packet Handling | 50 |
| Low Frequency Oscillator | 19 | Applications Information | 51 |
| Temperature Sensor | 19 | Typical Application Circuit | 51 |
| Digital Input/Output | 20 | Silicon Anomaly | 52 |
| Digital Timing | 20 | ADF7030-1 Functionality Issues | 52 |
| Absolute Maximum Ratings | 22 | Functionality Issues | 52 |
| ESD Caution | 22 | Development Support | 53 |
| Pin Configurations and Function Descriptions | 23 | Design Package | 53 |
| Typical Performance Characteristics | 27 | Reference Manuals | 53 |
| 169 MHz—Receive | 27 | Evaluation Kits | 53 |
| 169 MHz—Transmit | 28 | Evaluation Software | 53 |
| 433 MHz—Receive | 30 | Outline Dimensions | 54 |
| 433 MHz—Transmit | 31 | Ordering Guide | 55 |
| 460 MHz—Receive | 33 | | |

REVISION HISTORY

3/2020—Rev. 0 to Rev. A

| | |
|---|----|
| Changes to Features | 1 |
| Changes to General Description | 3 |
| Changes to Wideband Mode Parameter, Table 3 | 5 |
| Changes to Table 6 and Table 7 | 9 |
| Changes to Table 8 and Table 9 | 11 |
| Changes to Table 10 and Table 11 | 13 |
| Changes to Table 12 and Table 13 | 15 |
| Changes to Table 14 and Table 15 | 17 |
| Changes to Figure 7 to Figure 12 | 27 |
| Changes to Figure 23 to Figure 26 | 30 |

| | |
|--|----|
| Changes to Figure 34 to Figure 38 | 33 |
| Changes to Figure 46 to Figure 51 | 36 |
| Changes to Figure 52 to Figure 54 | 37 |
| Changes to Figure 65 to Figure 70 | 40 |
| Changes to Figure 71 | 41 |
| Deleted Figure 72 and Figure 73, Renumbered Sequentially ... | 41 |
| Changes to Table 28 | 47 |
| Updated Outline Dimensions | 54 |

6/2016—Revision 0: Initial Version

GENERAL DESCRIPTION

The [ADF7030-1](#) is a fully integrated, radio transceiver achieving high performance at very low power. The [ADF7030-1](#) is ideally suited for applications that require long range, network robustness, and long battery life. It is suitable for applications that operate in the ISM, SRD, and licensed frequency bands at 169.4 MHz to 169.6 MHz, 426 MHz to 470 MHz, and 863 MHz to 960 MHz. It provides extensive support for standards-based protocols like IEEE802.15.4g while also providing flexibility to support a wide range of proprietary protocols.

The highly configurable low intermediate frequency (IF) receiver supports a large range of receiver channel bandwidths from 2.6 kHz to 406 kHz. This range of receiver channel bandwidths allows the [ADF7030-1](#) to support ultranarrow-band, narrow-band, and wideband channel spacing.

The [ADF7030-1](#) features two independent PAs supporting output power ranges of -20 dBm to +13 dBm and -20 dBm to +17 dBm. The PAs support ultrafine adjustment of the power with a step resolution of 0.1 dB. The PA output power is exceptionally robust over temperature and voltage. The PAs have an automatic power ramp control to limit spectral splatter to meet regulatory standards.

The [ADF7030-1](#) features an on-chip ARM® Cortex®-M0 processor that performs radio control, radio calibration, and packet management. Cortex-M0 eases the processing burden of the host processor because the [ADF7030-1](#) integrates the lower layers of a typical communication protocol stack. This internal processor also permits the download and execution of Analog Devices, Inc., provided firmware modules that can extend the functionality of the ADF7030-1.

The [ADF7030-1](#) has two packet modes: generic packet mode and IEEE802.15.4g mode. In generic packet mode, the packet format is highly flexible and fully programmable, thereby ensuring its compatibility with proprietary packet formats. In IEEE802.15.4g packet mode, the packet format conforms to the

IEEE802.15.4g standard. FEC, as per the IEEE802.15.4g standard, is also supported.

The [ADF7030-1](#) operates with a power supply range of 2.2 V to 3.6 V and has very low power consumption in both Tx and Rx modes, enabling long lifetimes in battery-operated systems. An ultralow power deep sleep mode achieves a typical current of 10 nA with the configuration memory retained.

A complete wireless solution can be built using a small number of external discrete components and a host processor (typically a microcontroller). The host processor can configure the [ADF7030-1](#) using a simple command-based protocol over a standard 4-wire SPI interface. A single-byte command transitions the radio between states or performs a radio function.

The [ADF7030-1](#) is available in two package types: a 6 mm × 6 mm, 40-lead LFCSP and a 7 mm × 7 mm, 48-lead LQFP. Both package types use NiPdAu plating to mitigate against silver migration in high humidity applications. The ADF7030-1 operating temperature range is -40°C to +85°C.

For Figure 13 to Figure 19, Figure 30, Figure 42, Figure 60, Figure 61, and Figure 75 in the Typical Performance Characteristics section, PA_COARSE is a programmable value that provides a coarse adjustment of the PA output power. This value can be programmed in the range of 1 to 6 for PA1, and from 1 to 10 for PA2. PA_FINE is a programmable value that provides a fine adjustment of the PA output power. This value can be programmed in the range of 3 to 127 for both PA1 and PA2. PA_MICRO is a programmable value that provides a microadjustment (typically <0.1 dB) of the PA output power. This value can be programmed in the range of 1 to 31 for both PA1 and PA2. PAOLDO_VOUT_CON is a programmable value that configures the internal LDO voltage that provides bias for the PA. For additional information on these bit settings, see the [ADF7030-1 Software Reference Manual](#), which is the detailed programming guide for the device.

SPECIFICATIONS

$V_{DD} = V_{BAT1} = V_{BAT2} = V_{BAT3} = V_{BAT4} = V_{BAT5} = V_{BAT6} = 2.2\text{ V to }3.6\text{ V}$, exposed pad (EPAD) = 0 V (ground), $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical specifications are at $V_{DD} = 3\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted. All VBATx pins must be tied together. A one-time radio calibration is required, unless otherwise noted.

TEMPERATURE AND VOLTAGE

Table 1.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--------------------------|------------------------|-----|-----|------------------|---|
| TEMPERATURE RANGE, T_A | -40 | | +85 | $^\circ\text{C}$ | |
| VOLTAGE SUPPLY | | | | | |
| VBATx Pin Voltage | 2.2 | | 3.6 | V | Transmit power $\leq 13\text{ dBm}$ |
| | 2.85 | | 3.6 | V | Transmit power $\geq 17\text{ dBm}$, PA LDO voltage = 2.65 V |
| | PA LDO voltage + 0.2 V | | 3.6 | V | Transmit power $> 13\text{ dBm}$ and $< 17\text{ dBm}$; the PA LDO voltage is configurable |

GENERAL RF

Table 2.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|---------------------|-------|------|---|
| RF FREQUENCY | | | | | |
| Frequency Range | | 169.4 | 169.6 | MHz | |
| | | 426 | 470 | MHz | |
| | | 863 | 960 | MHz | |
| Channel Frequency Resolution | | 1.5 | | Hz | |
| DATA RATE | | | | | |
| IEEE802.15.4g Packet Mode | | | | kbps | |
| 2FSK, 2GFSK Modulation | 2.4 | | 150 | kbps | |
| Generic Packet Mode | | | | kbps | |
| 2FSK, 2GFSK Modulation | 0.1 | | 300 | kbps | |
| 4FSK, 4GFSK Modulation | 1 | | 360 | kbps | Tx only, generic packet mode only |
| On/Off Keying (OOK) Modulation | | 16.384 | | kbps | Tx only, Manchester encoded, generic packet mode only |
| Resolution | | 1 | | bps | |
| FREQUENCY DEVIATION | | | | | |
| Range | | | | | |
| 2FSK, 2GFSK Modulation | 1 | | 250 | kHz | |
| 4FSK, 4GFSK Modulation | 1 | | 250 | kHz | Tx only, generic packet mode only |
| Resolution | | 100 | | Hz | |
| GAUSSIAN FILTER BANDWIDTH TIME (BT) PRODUCT | | 0.3, 0.35, 0.4, 0.5 | | | Programmable |

RECEIVE

Table 3.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|----------|-----|------|---|
| MAXIMUM DATA RATE ERROR TOLERANCE | | ±0.1 | | % | |
| RECEIVER CHANNEL FILTER BANDWIDTH | | | | | Programmable; see Table 27 and Table 28 for a list of all supported values |
| Narrow-Band Mode | | | | | |
| Maximum | | 20.0 | | kHz | |
| Minimum | | 2.6 | | kHz | |
| Wideband Mode | | | | | |
| Maximum | | 406.25 | | kHz | |
| Minimum | | 77.38 | | kHz | |
| MAXIMUM RF INPUT LEVEL | | 10 | | dBm | |
| RECEIVER LINEARITY | | | | | Measured at maximum receiver gain |
| Input Third-Order Intercept (IIP3) | | -8.5 | | dBm | Receiver channel frequency = 169.43125 MHz, f _{SOURCE1} = 171.35 MHz, f _{SOURCE2} = 173.26875 MHz |
| Input Second-Order Intercept (IIP2) | | 53 | | dBm | Receiver channel frequency = 169.53125 MHz, f _{SOURCE1} = 171.55 MHz, f _{SOURCE2} = 171.63125 MHz |
| 1 dB Compression (P1dB) | | -18.7 | | dBm | Receiver channel frequency = 169.43125 MHz, f _{SOURCE1} = 171.43125 MHz |
| RECEIVED SIGNAL STRENGTH INDICATOR (RSSI) | | | | | Refer to the Typical Performance Characteristics section for further detail; sensitivity defined as bit error rate (BER) = 0.1% |
| Resolution | | 0.25 | | dB | |
| Calibrated Absolute Accuracy | | ±2 | | dB | -40 dBm to sensitivity + 6 dB; one-point offset calibration |
| DIFFERENTIAL LOW NOISE AMPLIFIER (LNA) INPUT IMPEDANCE, 40-LEAD LFCSP PACKAGE | | | | | |
| LNA in Rx Mode | | | | | |
| f = 169 MHz | | 78 - j20 | | Ω | |
| f = 433 MHz | | 69 - j25 | | Ω | |
| f = 460 MHz | | 68 - j25 | | Ω | |
| f = 868 MHz | | 56 - j29 | | Ω | |
| f = 915 MHz | | 55 - j30 | | Ω | |
| LNA in Tx Mode | | | | | Combined match enabled |
| f = 169 MHz | | 7 + j2 | | Ω | |
| f = 433 MHz | | 7 + j4 | | Ω | |
| f = 460 MHz | | 7 + j4 | | Ω | |
| f = 868 MHz | | 8 + j8 | | Ω | |
| f = 915 MHz | | 8 + j8 | | Ω | |
| DIFFERENTIAL LNA INPUT IMPEDANCE, 48-LEAD LQFP PACKAGE | | | | | |
| LNA in Rx Mode | | | | | |
| f = 169 MHz | | 78 - j16 | | Ω | |
| f = 433 MHz | | 71 - j18 | | Ω | |
| f = 460 MHz | | 73 - j22 | | Ω | |
| f = 868 MHz | | 58 - j20 | | Ω | |
| f = 915 MHz | | 57 - j20 | | Ω | |
| LNA in Tx Mode | | | | | Combined match enabled |
| f = 169 MHz | | 7 + j3 | | Ω | |
| f = 433 MHz | | 8 + j9 | | Ω | |
| f = 460 MHz | | 8 + j9 | | Ω | |
| f = 868 MHz | | 9 + j18 | | Ω | |
| f = 915 MHz | | 9 + j19 | | Ω | |

TRANSMIT

Table 4.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments | |
|--|-----|------------|-----|----------|---|--|
| POWER AMPLIFIER (PA) | | | | | | |
| Power Amplifier 1 (PA1) | | | | | | |
| Transmit Power Maximum | | 13 | | dBm | From -40°C to $+85^{\circ}\text{C}$, transmit power = 13 dBm, RF frequency = 169 MHz From $V_{\text{DD}} = 2.2\text{ V}$ to $V_{\text{DD}} = 3.6\text{ V}$, transmit power = 13 dBm, RF frequency = 169 MHz transmit power = 13 dBm, RF frequency = 169 MHz | |
| Transmit Power Minimum | | -20 | | dBm | | |
| Transmit Power Step Resolution | | 0.1 | | dB | | |
| Transmit Power Variation vs. Temperature | | ± 0.15 | | | | |
| Transmit Power Variation vs. V_{DD} | | ± 0.1 | | | | |
| Transmit Power Accuracy | | ± 0.3 | | | | |
| Power Amplifier 2 (PA2) | | | | | | |
| Transmit Power Maximum | | | | | The maximum output power level achievable on PA2 depends on the programmable PA CREG3 LDO voltage setting; refer to the ADF7030-1 Software Reference Manual for further details | |
| | | 17 | | dBm | $2.85\text{ V} \leq V_{\text{DD}} \leq 3.6\text{ V}$ | |
| | | 13 | | dBm | $2.2\text{ V} \leq V_{\text{DD}} \leq 3.6\text{ V}$ | |
| Transmit Power Minimum | | -20 | | dBm | From -40°C to $+85^{\circ}\text{C}$, transmit power = 17 dBm, RF frequency = 169 MHz From $V_{\text{DD}} = 3.0\text{ V}$ to $V_{\text{DD}} = 3.6\text{ V}$, transmit power = 17 dBm, RF frequency = 169 MHz Transmit power = 17 dBm, RF frequency = 169 MHz | |
| Transmit Power Step Resolution | | 0.1 | | dB | | |
| Transmit Power Variation vs. Temperature | | ± 0.1 | | dB | | |
| Transmit Power Variation vs. V_{DD} | | ± 0.1 | | dB | | |
| Transmit Power Accuracy | | ± 0.25 | | dB | | |
| PA IMPEDANCE, 40-LEAD LFCSP PACKAGE | | | | | | |
| Optimum PA Load While in Transmit | | | | | | |
| PA1 | | | | | | |
| f = 169 MHz | | 50 + j0 | | Ω | For guidance on impedance matching, refer to the ADF7030-1 Hardware Reference Manual | |
| f = 433 MHz, f = 460 MHz | | 45 + j30 | | Ω | | |
| f = 868 MHz, f = 915 MHz | | 50 + j20 | | Ω | | |
| PA2 | | | | | | |
| f = 169 MHz | | 38 + j0 | | Ω | | |
| f = 433 MHz, f = 460 MHz | | 38 + j25 | | Ω | | |
| f = 868 MHz, f = 915 MHz | | 38 + j18.5 | | Ω | | |
| PA Input Impedance While in Rx | | | | | | |
| PA1 | | | | | | |
| f = 169 MHz | | 7 - j232 | | Ω | | |
| f = 433 MHz | | 5 - j102 | | Ω | | |
| f = 460 MHz | | 5 - j96 | | Ω | | |
| f = 868 MHz | | 4 - j49 | | Ω | | |
| f = 915 MHz | | 4 - j46 | | Ω | | |
| PA2 | | | | | | |
| f = 169 MHz | | 5 - j177 | | Ω | | |
| f = 433 MHz | | 3 - j69 | | Ω | | |
| f = 460 MHz | | 3 - j65 | | Ω | | |
| f = 868 MHz | | 3 - j33 | | Ω | | |
| f = 915 MHz | | 3 - j31 | | Ω | | |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|------------------------------------|-----|----------|-----|------|--|
| PA IMPEDANCE, 48-LEAD LQFP PACKAGE | | | | | For guidance on impedance matching, refer to the ADF7030-1 Hardware Reference Manual |
| Optimum PA Load While in Transmit | | | | | |
| PA1 | | | | | |
| f = 169 MHz | | 45 + j 8 | | Ω | |
| f = 433 MHz, f = 460 MHz | | 40 + j20 | | Ω | |
| f = 868 MHz | | 40 + j20 | | Ω | |
| f = 915 MHz | | 40 + j20 | | Ω | |
| PA2 | | | | | |
| f = 169 MHz | | 37 + j 9 | | Ω | |
| f = 433 MHz, f = 460 MHz | | 30 + j25 | | Ω | |
| f = 868 MHz, f = 915 MHz | | 30 + j15 | | Ω | |
| PA Input Impedance While in Rx | | | | | |
| PA1 | | | | | |
| f = 169 MHz | | 6 – j236 | | Ω | |
| f = 433 MHz, f = 460 MHz | | 6 – j87 | | Ω | |
| f = 868 MHz | | 5 – j37 | | Ω | |
| f = 915 MHz | | 5 – j34 | | Ω | |
| PA2 | | | | | |
| f = 169 MHz | | 5 – j169 | | Ω | |
| f = 433 MHz, f = 460 MHz | | 4 – j58 | | Ω | |
| f = 868 MHz | | 3 – j22 | | Ω | |
| f = 915 MHz | | 3 – j19 | | Ω | |

CURRENT CONSUMPTION

Table 5.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|------|-----|------|---|
| TRANSMIT CURRENT CONSUMPTION | | | | | |
| In the PHY_TX state transmitting a carrier | | | | | |
| f = 169.4 MHz | | | | | |
| Tx Power = 0 dBm, PA1 | | 18 | | mA | |
| Tx Power = 10 dBm, PA1 | | 31 | | mA | |
| Tx Power = 13 dBm, PA1 | | 39 | | mA | |
| Tx Power = 17 dBm, PA2 | | 65 | | mA | |
| f = 433 MHz | | | | | |
| Tx Power = 0 dBm, PA1 | | 19 | | mA | |
| Tx Power = 10 dBm, PA1 | | 31 | | mA | |
| Tx Power = 13 dBm, PA1 | | 39 | | mA | |
| f = 460 MHz | | | | | |
| Tx Power = 17 dBm, PA2 | | 50 | | mA | |
| f = 868 MHz, f = 915 MHz | | | | | |
| Tx Power = 0 dBm, PA1 | | 20 | | mA | |
| Tx Power = 10 dBm, PA1 | | 34 | | mA | |
| Tx Power = 13 dBm, PA1 | | 43 | | mA | |
| Tx Power = 17 dBm, PA2 | | 65 | | mA | |
| RECEIVE CURRENT CONSUMPTION | | | | | |
| In the PHY_RX state, waiting for preamble | | | | | |
| f = 169.4 MHz | | | | | |
| Data Rate = 4.8 kbps | | 24.8 | | mA | Narrow-band receive path |
| f = 433 MHz, f = 460 MHz | | | | | |
| Data Rate = 4.8 kbps | | 24.5 | | mA | Narrow-band receive path |
| Data Rate = 50 kbps | | 24 | | mA | Wideband receive path |
| f = 868 MHz, f = 915 MHz | | | | | |
| Data Rate = 5 kbps | | 23.2 | | mA | Narrow-band receive path |
| Data Rate = 12.5 kbps | | 21.2 | | mA | Wideband receive path |
| Data Rate = 50 kbps | | 21.4 | | mA | Wideband receive path |
| Data Rate = 100 kbps | | 23.7 | | mA | Wideband receive path |
| Data Rate = 150 kbps | | 24 | | mA | Wideband receive path |
| Data Rate = 300 kbps | | 25.4 | | mA | Wideband receive path |
| RADIO STATE CURRENT CONSUMPTION | | | | | |
| PHY_SLEEP State | | | | | |
| | | 2 | | nA | Memory not retained, no wakeup oscillator enabled, RTC disabled |
| | | 10 | | nA | Memory retained, no wakeup oscillator enabled, RTC disabled |
| | | 1 | | µA | Memory retained, internal 26 kHz RC oscillator enabled, RTC enabled |
| | | 1 | | µA | Memory retained, external 32 kHz oscillator enabled, RTC enabled |
| PHY_OFF State | | 1.9 | | mA | First entry to PHY_OFF after wake from PHY_SLEEP or after reset event |
| PHY_OFF State | | 3.7 | | mA | Second and subsequent entries to PHY_OFF after wake from PHY_SLEEP or after reset event |
| PHY_ON State | | 3.7 | | mA | |

BAND SPECIFIC RECEIVE AND TRANSMIT**169.4 MHz to 169.6 MHz**

Unless otherwise noted, the configurations detailed in Table 6 are used to specify the performance of the ADF7030-1 in Table 7. All measurements are performed on the [EV-ADF70301-169BZ](#) evaluation board, unless otherwise noted. The [EV-ADF70301-169BZ](#) uses a separate transmit/receive match design and a 26 MHz thermally compensated crystal oscillator (TCXO) reference. N/A means not applicable.

Table 6. Configurations in the 169.4 MHz to 169.6 MHz Frequency Band

| Configuration Name | RF Frequency (MHz) | Data Rate (kbps) | Modulation | Frequency Deviation (kHz) | Channel Spacing (kHz) | IF Frequency (kHz) | Receiver Bandwidth (kHz) | Packet Setup for Packet-Based Testing |
|----------------------------|--------------------|------------------|------------|---------------------------|-----------------------|--------------------|--------------------------|---|
| 169.41875 MHz/ 0.1 kbps | 169.41875 | 0.1 | 2GFSK | 0.5 | N/A | 81.25 | 2.6 | Preamble = 0xAAAA, sync word = 0xF672, payload length = 23 bytes, cyclic redundancy check (CRC) = 2 bytes |
| 169.43125 MHz/ 2.4 kbps | 169.43125 | 2.4 | 2GFSK | 2.4 | 12.5 | 81.25 | 9.1 | Preamble = 0x55555555, sync word = 0xF672, payload length = 23 bytes, CRC = 2 bytes |
| 169.41875 MHz/ 4.8 kbps | 169.41875 | 4.8 | 2GFSK | 2.4 | 12.5 | 81.25 | 11.1 | Preamble = 0x55555555, sync word = 0xF672, payload length = 23 bytes, CRC = 2 bytes |
| 169.46875 MHz/ 6.4 kbps | 169.46875 | 6.4 | 4GFSK | 3.2 (outer deviation) | 12.5 | N/A (Tx only) | N/A (Tx only) | N/A |

Table 7. Specifications in the 169.4 MHz to 169.6 MHz Frequency Band

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|--------|-----|------|--|
| SENSITIVITY, PACKET ERROR RATE (PER) | | | | | |
| Configuration 169.41875 MHz/0.1 kbps | | -134.3 | | dBm | At PER = 5%, automatic frequency control (AFC) disabled |
| Configuration 169.43125 MHz/2.4 kbps | | -121.3 | | dBm | At PER = 5%, AFC enabled, RF frequency error range = ±11.5 ppm |
| Configuration 169.41875 MHz/4.8 kbps | | -120.0 | | dBm | At PER = 5%, AFC enabled, RF frequency error range = ±11.5 ppm |
| CHANNEL SELECTIVITY AND BLOCKING— BER-BASED TEST METHOD | | | | | Desired signal 3 dB above the input sensitivity level (BER = 0.1%), carrier wave interferer power level increased until BER = 0.1%; AFC disabled, image calibrated |
| Configuration 169.43125 MHz/2.4 kbps | | | | | |
| Adjacent Channel (±12.5 kHz) | | 72 | | dB | |
| Alternate Channel (±25 kHz) | | 72 | | dB | |
| ±2 MHz | | 93 | | dB | |
| ±10 MHz | | 92 | | dB | |
| ±20 MHz | | 97 | | dB | |
| Configuration 169.41875 MHz/4.8 kbps | | | | | |
| Adjacent Channel (±12.5 kHz) | | 70 | | dB | |
| Alternate Channel (±25 kHz) | | 70 | | dB | |
| ±2 MHz | | 92 | | dB | |
| ±10 MHz | | 95 | | dB | |
| CHANNEL SELECTIVITY AND BLOCKING— PER-BASED TEST METHOD | | | | | Desired signal 3 dB above the input sensitivity level (PER = 5%), carrier wave interferer power level increased until PER = 5%, AFC enabled, image calibrated |
| Configuration 169.43125 MHz/2.4 kbps | | | | | |
| Adjacent Channel (±12.5 kHz) | | 66 | | dB | |
| Alternate Channel (±25 kHz) | | 67 | | dB | |
| ±2 MHz | | 93 | | dB | |
| ±10 MHz | | 91 | | dB | |
| Configuration 169.41875 MHz/4.8 kbps | | | | | |
| Adjacent Channel (±12.5 kHz) | | 53 | | dB | |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|------|-----|------|---|
| Alternate Channel (± 25 kHz) | | 64 | | dB | |
| ± 2 MHz | | 91 | | dB | |
| ± 10 MHz | | 94 | | dB | |
| CHANNEL SELECTIVITY AND BLOCKING— ETSI EN 300 220-1 TEST METHOD Configuration 169.43125 MHz/2.4 kbps | | | | | Measured as per EN 300 220-1 V2.4.1, AFC disabled Desired signal level = -106.7 dBm (3 dB above the reference sensitivity level) |
| ± 2 MHz | | -15 | | dBm | |
| ± 10 MHz | | -12 | | dBm | |
| Configuration 169.41875 MHz/4.8 kbps | | | | | Desired signal level = -105.8 dBm (3 dB above the reference sensitivity level) |
| ± 2 MHz | | -16 | | dBm | |
| ± 10 MHz | | -13 | | dBm | |
| COCHANNEL REJECTION | | | | | Desired signal 3 dB above the input sensitivity level (PER = 5%), carrier wave interferer power level increased until PER = 5%, AFC enabled |
| Configuration 169.43125 MHz/2.4 kbps | | -9 | | dB | |
| Configuration 169.41875 MHz/4.8 kbps | | -11 | | dB | |
| CALIBRATED IMAGE REJECTION | | | | dB | Desired signal 3 dB above the input sensitivity level (PER = 5%), carrier wave interferer power level increased until PER = 5%, AFC enabled, image calibrated |
| Configuration 169.43125 MHz/2.4 kbps | | 60 | | dB | |
| Configuration 169.41875 MHz/4.8 kbps | | 58 | | dB | |
| ADJACENT CHANNEL POWER (ACP) | | | | | Spectrum analyzer settings: resolution bandwidth = 100 Hz, video bandwidth = 300 Hz PA1, output power = 13 dBm |
| Configuration 169.43125 MHz/2.4 kbps Adjacent Channel | | -83 | | dBc | |
| Alternate Channel | | -83 | | dBc | |
| Configuration 169.41875 MHz/4.8 kbps Adjacent Channel | | -60 | | dBc | PA2, output power = 17 dBm |
| Alternate Channel | | -84 | | dBc | |
| Configuration 169.46875 MHz/6.4 kbps Adjacent Channel | | -68 | | dBc | PA1, output power = 13 dBm |
| Alternate Channel | | -81 | | dBc | |
| OCCUPIED BANDWIDTH | | | | | Occupied bandwidth is the bandwidth containing 99% of the total integrated power; spectrum analyzer settings: resolution bandwidth = 100 Hz, video bandwidth = 300 Hz |
| Configuration 169.43125 MHz/2.4 kbps | | 6.3 | | kHz | PA1, output power = 13 dBm |
| Configuration 169.41875 MHz/4.8 kbps | | 7.8 | | kHz | PA2, output power = 17 dBm |
| Configuration 169.46875 MHz/6.4 kbps | | 8.2 | | kHz | PA1, output power = 13 dBm |
| SPURIOUS EMISSIONS (EXCLUDING HARMONICS) | | | | | Measured conductively at antenna input; RF frequency = 169.43125 MHz |
| Receive | | | | | |
| <1 GHz | | -74 | | dBm | |
| 1 GHz to 4 GHz | | -52 | | dBm | |
| Transmit | | | | | PA2, output power = 17 dBm, transmitting continuous carrier wave |
| <1 GHz | | -70 | | dBc | |
| 1 GHz to 4 GHz | | -72 | | dBc | |
| HARMONIC EMISSIONS | | | | | Measured conductively at antenna input, transmitting continuous carrier wave; RF frequency = 169.43125 MHz PA2 |
| 17 dBm Output Power Second Harmonic | | -64 | | dBc | |
| Third Harmonic | | -89 | | dBc | |
| All Other Harmonics | | <-90 | | dBc | |

433 MHz

Unless otherwise noted, the configuration detailed in Table 8 is used to specify the performance of the ADF7030-1 in Table 9. All measurements are performed on the [EV-ADF70301-460BZ](#) evaluation board, unless otherwise noted. The [EV-ADF70301-460BZ](#) uses a separate transmit/receive match design and a 26 MHz TCXO reference.

Table 8. 433 MHz Configurations

| Configuration Name | RF Frequency (MHz) | Data Rate (kbps) | Modulation | Frequency Deviation (kHz) | Channel Spacing (kHz) | IF Frequency (kHz) | Receiver Bandwidth (kHz) | Packet Setup for Packet Based Testing |
|--------------------|--------------------|------------------|------------|---------------------------|-----------------------|--------------------|--------------------------|---|
| 433 MHz/50 kbps | 433 | 50 | 2GFSK | 25 | 200 | 135.42 | 101.57 | Preamble = 0xAAAAAAAA, sync word = 0xF672, payload length = 16 bytes, CRC = 2 bytes |

Table 9. 433 MHz Specifications

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|----------------------------|-----|----------------------------|---|
| SENSITIVITY, PER Configuration 433 MHz/50 kbps | | -108.6 | | dBm | AT PER = 5%, AFC enabled, RF frequency error range = ±25 ppm |
| CHANNEL SELECTIVITY AND BLOCKING— BER-BASED TEST METHOD Configuration 433 MHz/50 kbps Adjacent Channel (±200 kHz) Alternate Channel (±400 kHz) ±2 MHz ±10 MHz ±20 MHz | | 56 62 78 83 87 | | dB dB dB dB dB | Desired signal 3 dB above the input sensitivity level (BER = 0.1%), carrier wave interferer power level increased until BER = 0.1%, image calibrated, AFC disabled |
| CHANNEL SELECTIVITY AND BLOCKING— PER BASED TEST METHOD Configuration 433 MHz/50 kbps Adjacent Channel (±200 kHz) Alternate Channel (±400 kHz) ±2 MHz ±10 MHz | | 51 58 73 79 | | dB dB dB dB | Desired signal 3 dB above the input sensitivity level (PER = 5%), carrier wave interferer power level increased until PER = 5%, image calibrated, AFC enabled |
| COCHANNEL REJECTION Configuration 433 MHz/50 kbps | | -10 | | dB | Desired signal 3 dB above the input sensitivity level (PER = 5%), carrier wave interferer power level increased until PER = 5%, AFC enabled |
| CALIBRATED IMAGE REJECTION Configuration 433 MHz/50 kbps | | 48 | | dB | Desired signal 3 dB above the input sensitivity level (PER = 5%), carrier wave interferer power level increased until PER = 5%, AFC enabled, image calibrated |
| ACP Configuration 433 MHz/50 kbps | | -60 | | dBc | Spectrum analyzer settings: resolution bandwidth = 100 Hz, video bandwidth = 300 Hz |
| OCCUPIED BANDWIDTH Configuration 433 MHz/50 kbps | | 86 | | kHz | Occupied bandwidth is the bandwidth containing 99% of the total integrated power; spectrum analyzer settings: resolution bandwidth = 100 Hz, video bandwidth = 300 Hz |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------------|------------|------------|-------------|---|
| SPURIOUS EMISSIONS (EXCLUDING HARMONICS) | | | | | Measured conductively at antenna port; RF frequency = 433 MHz PA1, output power = 13 dBm, transmitting continuous carrier wave |
| Receive | | | | | |
| <1 GHz | | -74 | | dBm | |
| 1 GHz to 4 GHz | | -51 | | dBm | |
| Transmit | | | | | |
| <1 GHz | | -46 | | dBc | |
| 1 GHz to 4 GHz | | -68 | | dBc | |
| HARMONIC EMISSIONS | | | | | Measured conductively at antenna input, transmitting continuous carrier wave; RF frequency = 433 MHz, PA1, output power = 10 dBm |
| Second Harmonic | | -64 | | dBc | |
| All Other Harmonics | | <-90 | | dBc | |

450 MHz to 470 MHz

Unless otherwise noted, the configuration detailed in Table 10 is used to specify the performance of the ADF7030-1 in Table 11. All measurements are performed on the [EV-ADF70301-460BZ](#) evaluation board, unless otherwise noted. The [EV-ADF70301-460BZ](#) uses a separate transmit/receive match design and a 26 MHz TCXO reference.

Table 10. Configurations in the 450 MHz to 470 MHz Frequency Band

| Configuration Name | RF Frequency (MHz) | Data Rate (kbps) | Modulation | Frequency Deviation (kHz) | Channel Spacing (kHz) | IF Frequency (kHz) | Receiver Bandwidth (kHz) | Packet Setup for Packet Based Testing |
|--------------------|--------------------|------------------|------------|---------------------------|-----------------------|--------------------|--------------------------|---|
| 460 MHz/7.2 kbps | 460 | 7.2 | 2GFSK | 2.0 | 12.5 | 81.25 | 11.7 | Preamble = 0xAAAAAAAA, sync word = 0xF672, payload length = 23 bytes, CRC = 2 bytes |

Table 11. Specifications in the 450 MHz to 470 MHz Frequency Band

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|----------------------------|-----|----------------------------|---|
| SENSITIVITY, PER Configuration 460 MHz/7.2 kbps | | -115.6 | | dBm | At PER = 5%, AFC enabled, RF frequency error range = ± 3.9 ppm |
| CHANNEL SELECTIVITY AND BLOCKING— BER-BASED TEST METHOD Configuration 460 MHz/7.2 kbps Adjacent Channel (± 12.5 kHz) Alternate Channel (± 25 kHz) ± 2 MHz ± 10 MHz ± 20 MHz | | 58 60 81 87 89 | | dB dB dB dB dB | Desired signal 3 dB above the input sensitivity level (BER = 0.1%), carrier wave interferer power level increased until BER = 0.1%, image calibrated, AFC disabled |
| CHANNEL SELECTIVITY AND BLOCKING— PER-BASED TEST METHOD Configuration 460 MHz/7.2 kbps Adjacent Channel (± 12.5 kHz) Alternate Channel (± 25 kHz) ± 2 MHz ± 10 MHz | | 51 58 80 87 | | dB dB dB dB | Desired signal 3 dB above the input sensitivity level (PER = 5%), carrier wave interferer power level increased until PER = 5%, image calibrated, AFC enabled |
| COCHANNEL REJECTION Configuration 460 MHz/7.2 kbps | | -13 | | dB | Desired signal 3 dB above the input sensitivity level (PER = 5%), carrier wave interferer power level increased until PER = 5%, AFC enabled |
| CALIBRATED IMAGE REJECTION Configuration 460 MHz/7.2 kbps | | 54 | | dB | Desired signal 3 dB above the input sensitivity level (PER = 5%), carrier wave interferer power level increased until PER = 5%, AFC enabled, image calibrated |
| ACP Configuration 460 MHz/7.2 kbps | | -49 | | dBc | Spectrum analyzer settings: resolution bandwidth = 100 Hz, video bandwidth = 300 Hz |
| OCCUPIED BANDWIDTH Configuration 460 MHz/7.2 kbps | | 7.7 | | kHz | Occupied bandwidth is the bandwidth containing 99% of the total integrated power; spectrum analyzer settings: resolution bandwidth = 100 Hz, video bandwidth = 300 Hz |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|-------|-----|------|---|
| SPURIOUS EMISSIONS (EXCLUDING HARMONICS) | | | | | Measured conductively at antenna port; RF frequency = 460 MHz PA2, output power = 17 dBm, transmitting continuous carrier wave |
| Receive | | | | | |
| <960 MHz | | -74 | | dBm | |
| 960 MHz to 12.7 GHz | | -51 | | dBm | |
| Transmit | | | | | |
| <960 MHz | | -46 | | dBc | |
| 960 MHz to 12.7 GHz | | -71 | | dBc | |
| HARMONIC EMISSIONS | | | | | Measured conductively at antenna port, transmitting continuous carrier wave; RF frequency = 460 MHz, output power = 17 dBm, PA2 |
| Second Harmonic | | -63 | | dBc | |
| All Other Harmonics | | < -90 | | dBc | |

863 MHz to 876 MHz

Unless otherwise noted, the configurations detailed in Table 12 are used to specify the performance of the ADF7030-1 in Table 13. All measurements are performed on the [EV-ADF70301-868BZ](#) evaluation board, unless otherwise noted. The [EV-ADF70301-868BZ](#) uses a separate transmit/receive match design and a 26 MHz TCXO reference.

Table 12. Configurations in the 863 MHz to 876 MHz Frequency Band

| Configuration Name | RF Frequency (MHz) | Data Rate (kbps) | Modulation | Frequency Deviation (kHz) | Channel Spacing (kHz) | IF Frequency (kHz) | Receiver Bandwidth (kHz) | Packet Setup for Packet Based Testing |
|--------------------|--------------------|------------------|------------|---------------------------|-----------------------|--------------------|--------------------------|---|
| 868 MHz/4.8 kbps | 868 | 4.8 | 2GFSK | 2.4 | 12.5 | 81.25 | 11.7 | Preamble = 0xAAAAAAAA, sync word = 0xF672, payload length = 23 bytes, CRC = 2 bytes |
| 868 MHz/100 kbps | 868 | 100 | 2FSK | 50 | 500 | 270.83 | 203.12 | Preamble = 0xAAAAAAAA, sync word = 0x543D54CD, payload length = 20 bytes, CRC = 2 bytes |

Table 13. Specifications in the 863 MHz to 876 MHz Frequency Band

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|--------|-----|------|--|
| SENSITIVITY, PER | | | | | |
| Configuration 868 MHz/4.8 kbps | | -118.4 | | dBm | At PER = 5%, AFC enabled, RF frequency error range = ± 3 ppm |
| Configuration 868 MHz/100 kbps | | -106.4 | | dBm | At PER = 5%, AFC enabled, RF frequency error range = ± 25 ppm, data rate error range = ± 100 ppm, frequency deviation error range = $\pm 25\%$ |
| CHANNEL SELECTIVITY AND BLOCKING— BER-BASED TEST METHOD | | | | | Desired signal 3 dB above the input sensitivity level (BER = 0.1%), carrier wave interferer power level increased until BER = 0.1%, image calibrated, AFC disabled |
| Configuration 868 MHz/4.8 kbps | | | | | |
| Adjacent Channel (± 12.5 kHz) | | 60 | | dB | |
| Alternate Channel (± 25 kHz) | | 60 | | dB | |
| ± 2 MHz | | 82 | | dB | |
| ± 10 MHz | | 90 | | dB | |
| ± 20 MHz | | 95 | | dB | |
| CHANNEL SELECTIVITY AND BLOCKING— PER-BASED TEST METHOD | | | | | Desired signal 3 dB above the input sensitivity level (PER = 5%), carrier wave interferer power level increased until PER = 5%, image calibrated, AFC enabled |
| Configuration 868 MHz/4.8 kbps | | | | | |
| Adjacent Channel (± 12.5 kHz) | | 43 | | dB | |
| Alternate Channel (± 25 kHz) | | 57 | | dB | |
| ± 2 MHz | | 79 | | dB | |
| ± 10 MHz | | 87 | | dB | |
| Configuration 868 MHz/100 kbps | | | | | |
| Adjacent Channel (500 kHz) | | 35 | | dB | |
| Adjacent Channel (-500 kHz) | | 53 | | dB | |
| Alternate Channel (± 1000 kHz) | | 60 | | dB | |
| ± 2 MHz | | 65 | | dB | |
| ± 10 MHz | | 74 | | dB | |
| COCHANNEL REJECTION | | | | | Desired signal 3 dB above the input sensitivity level (PER = 5%), carrier wave interferer power level increased until PER = 5%, AFC enabled |
| Configuration 868 MHz/4.8 kbps | | -11 | | dB | |
| Configuration 868 MHz/100 kbps | | -11 | | dB | |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|-------|-----|------|---|
| UNCALIBRATED IMAGE REJECTION | | | | | Desired signal 3 dB above the input sensitivity level (PER = 5%), carrier wave interferer power level increased until PER = 5%, AFC enabled |
| Configuration 868 MHz/4.8 kbps | | 37 | | dB | |
| Configuration 868 MHz/100 kbps | | 34 | | dB | |
| ACP | | | | | Spectrum analyzer settings: resolution bandwidth = 100 Hz, video bandwidth = 300 Hz |
| Configuration 868 MHz/4.8 kbps | | -66 | | dBc | |
| Configuration 868 MHz/100 kbps | | -39 | | dBc | |
| OCCUPIED BANDWIDTH | | | | | Occupied bandwidth is the bandwidth containing 99% of the total integrated power; spectrum analyzer settings: resolution bandwidth = 100 Hz, video bandwidth = 300 Hz |
| Configuration 868 MHz/4.8 kbps | | 7.8 | | kHz | |
| Configuration 868 MHz/100 kbps | | 225 | | kHz | |
| SPURIOUS EMISSIONS (EXCLUDING HARMONICS) | | | | | Measured conductively at antenna input; RF frequency = 868 MHz PA2, 17dBm output power, transmitting continuous carrier wave |
| Receive | | | | | |
| <1 GHz | | -77 | | dBm | |
| 1 GHz to 4 GHz | | -50 | | dBm | |
| Transmit | | | | | |
| <1 GHz | | -59 | | dBc | |
| 1 GHz to 4 GHz | | -66 | | dBc | |
| HARMONIC EMISSIONS | | | | | Measured conductively at antenna input, transmitting continuous carrier wave; RF frequency = 868 MHz PA1 PA2 |
| 13 dBm Output Power | | | | | |
| Second Harmonic | | -53 | | dBc | |
| Third Harmonic | | -78 | | dBc | |
| Seventh Harmonic | | -95 | | dBc | |
| 17 dBm Output Power | | | | | |
| Second Harmonic | | -51 | | dBc | |
| Third Harmonic | | -70 | | dBc | |
| All Other Harmonics | | <-100 | | dBc | |

902 MHz to 928 MHz

Unless otherwise noted, the configurations detailed in Table 14 are used to specify the performance of the ADF7030-1 in Table 15. All measurements are performed on the [EV-ADF70301-868BZ](#) evaluation board, unless otherwise noted. The [EV-ADF70301-868BZ](#) uses a separate transmit/receive match design and a 26 MHz TCXO reference.

Table 14. Configurations in the 902 MHz to 928 MHz Frequency Band

| Configuration Name | RF Frequency (MHz) | Data Rate (kbps) | Modulation | Frequency Deviation (kHz) | Channel Spacing (kHz) | IF Frequency (kHz) | Receiver Bandwidth (kHz) | Packet Setup for Packet Based Testing |
|----------------------|--------------------|------------------|------------|---------------------------|-----------------------|--------------------|--------------------------|---|
| 915 MHz/ 50 kbps | 915 | 50 | 2GFSK | 25 | 200 | 180.55 | 135.42 | Preamble = 0xAAAAAAA, sync word = 0x904E, payload length = 100 bytes, CRC = 2 bytes |
| 915 MHz/ 150 kbps | 915 | 150 | 2GFSK | 37.5 | 400 | 325.0 | 243.75 | Preamble = 0xAAAAAAAAAAAAAAAAAAAAA, sync word = 0xFF7D7F5D, payload length = 100 bytes, CRC = 2 bytes |
| 915 MHz/ 300 kbps | 915 | 300 | 2GFSK | 120 | 600 | 406.25 | 395 | Preamble = 0xAAAAAAA, sync word = 0xF672, payload length = 23 bytes, CRC = 2 bytes |

Table 15. 902 MHz to 928 MHz Specifications

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|--------|-----|------|--|
| 2GFSK SENSITIVITY, PER | | | | | |
| Configuration 915 MHz/50 kbps | | -109.2 | | dBm | At PER = 5%, FEC disabled, AFC enabled, RF frequency error range = ± 40 ppm |
| Configuration 915 MHz/150 kbps | | -100.7 | | dBm | At PER = 5%, FEC disabled, AFC enabled, RF frequency error range = ± 40 ppm |
| Configuration 915 MHz/300 kbps | | -98.8 | | dBm | At PER = 5%, AFC disabled, RF frequency error range = ± 11.5 ppm |
| CHANNEL SELECTIVITY AND BLOCKING— BER-BASED TEST METHOD | | | | | Desired signal 3 dB above the input sensitivity level (BER = 0.1%), carrier wave interferer power level increased until BER = 0.1%, AFC disabled |
| Configuration 915 MHz/150 kbps | | | | | |
| Adjacent Channel (± 400 kHz) | | 49 | | dB | |
| Alternate Channel (± 800 kHz) | | 56 | | dB | |
| ± 2 MHz | | 66 | | dB | |
| ± 10 MHz | | 75 | | dB | |
| ± 20 MHz | | 80 | | dB | |
| CHANNEL SELECTIVITY AND BLOCKING— PER-BASED TEST METHOD | | | | | Desired signal 3 dB above the input sensitivity level (PER = 5%), carrier wave interferer power level increased until PER = 5%, image calibrated |
| Configuration 915 MHz/50 kbps | | | | | FEC disabled, AFC enabled |
| Adjacent Channel (± 200 kHz) | | 44 | | dB | |
| Alternate Channel (-400 kHz) | | 36 | | dB | |
| Alternate Channel (400 kHz) | | 52 | | | |
| ± 2 MHz | | 68 | | dB | |
| ± 10 MHz | | 77 | | dB | |
| Configuration 915 MHz/150 kbps | | | | | FEC disabled, AFC enabled |
| Adjacent Channel (± 400 kHz) | | 43 | | dB | |
| Alternate Channel (-800 kHz) | | 48 | | dB | |
| Alternate Channel (800 kHz) | | 53 | | | |
| ± 2 MHz | | 59 | | dB | |
| ± 10 MHz | | 68 | | dB | |
| Configuration 915 MHz/300 kbps | | | | | AFC disabled |
| Adjacent Channel (± 600 kHz) | | 36 | | dB | |
| Alternate Channel (± 1200 kHz) | | 53 | | dB | |
| ± 2 MHz | | 57 | | dB | |
| ± 10 MHz | | 67 | | dB | |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|------|-----|------|--|
| COCHANNEL REJECTION | | | | | Desired signal 3 dB above the input sensitivity level (PER = 5%), carrier wave interferer power level increased until PER = 5% |
| Configuration 915 MHz/50 kbps | | -9 | | dB | |
| Configuration 915 MHz/150 kbps | | -8 | | dB | |
| Configuration 915 MHz/300 kbps | | -7 | | dB | |
| UNCALIBRATED IMAGE REJECTION | | | | | Desired signal 3 dB above the input sensitivity level (PER = 5%), carrier wave interferer power level increased until PER = 5% |
| Configuration 915 MHz/50 kbps | | 37 | | dB | |
| Configuration 915 MHz/150 kbps | | 36 | | dB | |
| Configuration 915 MHz/300 kbps | | 35 | | dB | |
| ACP | | | | | |
| Configuration 915 MHz/50 kbps | | | | | Spectrum analyzer settings: resolution bandwidth = 300 Hz, video bandwidth = 1 kHz |
| Adjacent Channel (± 200 kHz) | | -54 | | dBc | |
| Alternate Channel (± 400 kHz) | | -61 | | dBc | |
| Configuration 915 MHz/150 kbps | | | | | Spectrum analyzer settings: resolution bandwidth = 300 Hz, video bandwidth = 1 kHz |
| Adjacent Channel (± 400 kHz) | | -52 | | dBc | |
| Alternate Channel (± 800 kHz) | | -65 | | dBc | |
| Configuration 915 MHz/300 kbps | | | | | Spectrum analyzer settings: resolution bandwidth = 300 Hz, video bandwidth = 1 kHz |
| Adjacent Channel (± 600 kHz) | | -38 | | dBc | |
| Alternate Channel (± 1200 kHz) | | -65 | | dBc | |
| OCCUPIED BANDWIDTH | | | | | Occupied bandwidth is the bandwidth containing 99% of the total integrated power |
| Configuration 915 MHz/50 kbps | | 86 | | kHz | Spectrum analyzer settings: resolution bandwidth = 300 Hz, video bandwidth = 1 kHz |
| Configuration 915 MHz/150 kbps | | 165 | | kHz | Spectrum analyzer settings: resolution bandwidth = 300 Hz, video bandwidth = 1 kHz |
| Configuration 915 MHz/300 kbps | | 326 | | kHz | Spectrum analyzer settings: resolution bandwidth = 300 Hz, video bandwidth = 1 kHz |
| SPURIOUS EMISSIONS (EXCLUDING HARMONICS) | | | | | Measured conductively at antenna input; RF frequency = 915 MHz |
| Receive | | | | | |
| <960 MHz | | -78 | | dBm | |
| 960 MHz to 12.7 GHz | | -51 | | dBm | |
| Transmit | | | | | PA2, output power = 17 dBm, transmitting continuous carrier wave |
| <960 MHz | | -61 | | dBc | |
| 960 MHz to 12.7 GHz | | -63 | | dBc | |
| HARMONIC EMISSIONS | | | | | Measured conductively at antenna input, transmitting continuous carrier wave; RF frequency = 915 MHz |
| 13 dBm Output Power | | | | | PA1 |
| Second Harmonic | | -52 | | dBc | |
| Third Harmonic | | -85 | | dBc | |
| Seventh Harmonic | | -91 | | dBc | |
| 17 dBm Output Power | | | | | PA2 |
| Second Harmonic | | -51 | | dBc | |
| Third Harmonic | | -68 | | dBc | |
| All Other Harmonics | | <-90 | | dBc | |

EXTERNAL 26 MHZ OSCILLATOR

The ADF7030-1 requires a 26 MHz reference clock. This reference can be a 26 MHz crystal oscillator operating in parallel mode and connected between the HFXTALP and HFXTALN pins. Alternatively, a 26 MHz TCXO can be dc-coupled to the HFXTALN input. A TCXO is typically used in narrow-band applications where the transmit and receive RF frequency must meet accuracies not supported by a crystal oscillator.

Table 16.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------|-----|------|----------|--------------------------------|
| DC-COUPLED TCXO | | | | | HFXTALN pin, clipped sine wave |
| TCXO Frequency | | 26 | | MHz | |
| Peak-to-Peak Voltage Level | 0.8 | | 1.8 | V | |
| Voltage Level with Respect to Ground | -0.1 | | +1.9 | V | |
| Duty Cycle | 40 | | 60 | % | |
| CRYSTAL OSCILLATOR | | | | | Parallel resonant crystal |
| Crystal Frequency | | 26 | | MHz | |
| Maximum Crystal ESR | | | 50 | Ω | |
| Crystal Oscillator Load Capacitance | | 12 | | pF | |
| HFXTALN, HFXTALP Pin Capacitance in Parallel with Crystal Oscillator | | 5 | | pF | |

LOW FREQUENCY OSCILLATOR

Table 17.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|-------------------------------|-----|--------|-----|------|--|
| 26 kHz INTERNAL RC OSCILLATOR | | | | | After calibration After calibration at 25°C |
| Frequency | | 26 | | kHz | |
| Frequency Accuracy | | 0.2 | | % | |
| Frequency Drift | | | | | |
| Temperature Coefficient | | 0.3 | | %/°C | |
| Voltage Coefficient | | 0.5 | | %/V | |
| Calibration Time | | 30 | | ms | |
| 32 kHz EXTERNAL OSCILLATOR | | | | | |
| Frequency | | 32.768 | | kHz | |
| Start-Up Time | | 1.45 | | sec | |

TEMPERATURE SENSOR

Table 18.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--------------------|-----|-----|-----|------|---|
| TEMPERATURE SENSOR | | | | | |
| Range | -40 | | +85 | °C | |
| Accuracy | | ±5 | | °C | T _A = -40°C to +85°C; calibrated at 25°C |

DIGITAL INPUT/OUTPUT

Table 19.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----------|---------------------|-----|---------------------|------|--------------------------|
| LOGIC INPUTS | | | | | | |
| Input Voltage | | | | | | |
| High | V_{INH} | $0.7 \times V_{DD}$ | | | V | |
| Low | V_{INL} | | | $0.2 \times V_{DD}$ | V | |
| Input Capacitance | C_{IN} | | 3.6 | | pF | |
| LOGIC OUTPUTS | | | | | | |
| Output Voltage | | | | | | |
| High | V_{OH} | $V_{DD} - 0.4$ | | | V | $I_{OH} = 500 \mu A$ |
| Low | V_{OL} | | | 0.4 | V | $I_{OL} = 500 \mu A$ |
| Maximum GPIO Drive Strength for V_{OH} | | | 2 | | mA | |
| Maximum GPIO Drive Strength for V_{OL} | | | 2 | | mA | |

DIGITAL TIMING

Table 20. SPI Interface Timing

| Parameter | Description | Min | Typ | Max | Unit |
|-----------|--|----------------------------|-----|-----|---------|
| t_1 | Falling edge to MISO setup time | | | 15 | ns |
| t_2 | \overline{CS} low to SCLK setup time | 40 | | | ns |
| t_3 | SCLK high time | 40 | | | ns |
| t_4 | SCLK low time | 40 | | | ns |
| t_5 | SCLK period | 80 | | | ns |
| t_6 | SCLK falling edge to MISO delay | | | 10 | ns |
| t_7 | MOSI to SCLK rising edge setup time | 5 | | | ns |
| t_8 | MOSI to SCLK rising edge hold time | 5 | | | ns |
| t_9 | SCLK falling edge to \overline{CS} hold time | 40 | | | ns |
| t_{10} | \overline{CS} high time | 80 | | | ns |
| t_{11} | \overline{CS} low to MISO high wake-up time | | 92 | | μs |
| t_{12} | MISO high to SCLK setup time | SCLK low time ¹ | | | μs |
| t_{13} | \overline{RST} low time | 2 | | | μs |

¹ The minimum for t_{12} changes with the SCLK frequency.

Timing Diagrams

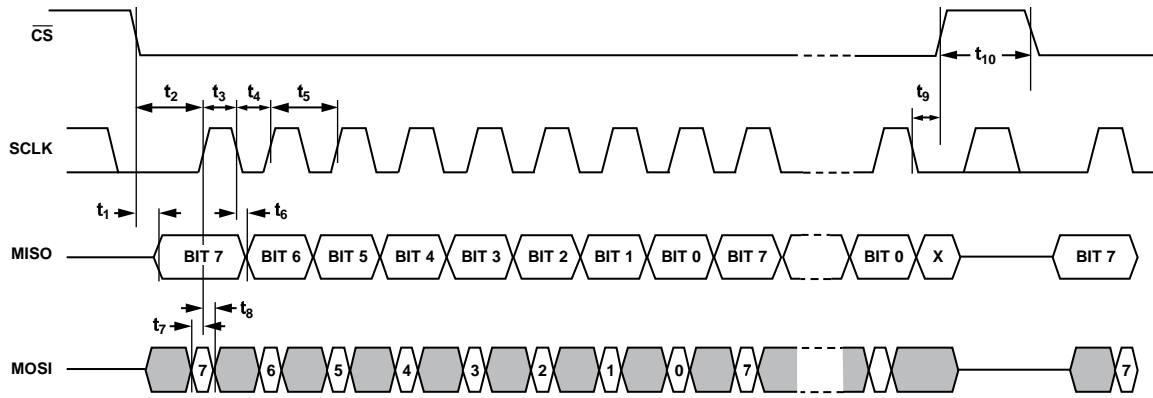


Figure 2. SPI Interface Timing

14373-002

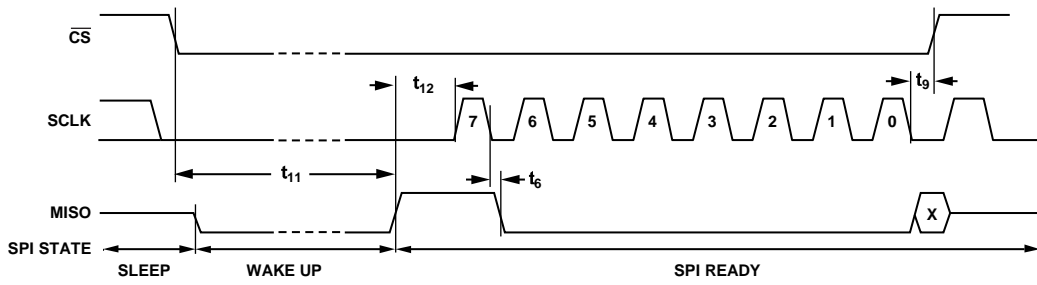


Figure 3. PHY_SLEEP to SPI Ready State Timing

14373-003

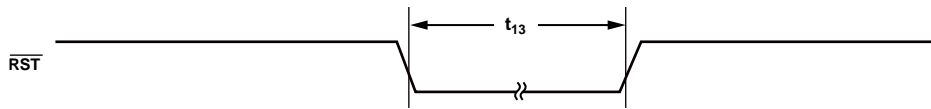


Figure 4. Reset Pin (\overline{RST}) Timing

14373-004

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted. All VBATx pins must be tied together. The LNAIN1 and LNAIN2 inputs must be ac-coupled.

Table 21.

| Parameter | Rating |
|--|-------------------|
| Supply Pins | |
| VBAT1, VBAT2, VBAT3, VBAT4, VBAT5, VBAT6 to Ground | -0.3 V to +3.9 V |
| LNAIN1, LNAIN2 | -0.3 V to +1.98 V |
| PAOUT1, PAOUT2 | -0.3 V to +3.9 V |
| HFXTALP, HFXTALN | -0.3 V to +1.98 V |
| CLF | -0.3 V to +1.98 V |
| CREG1, CREG2, CREG4, CREG5, CREG6, CREG7 | -0.3 V to +1.98 V |
| CREG3 | -0.3 V to +3.9 V |
| Digital Inputs/Outputs, GPIOx | -0.3 V to +3.9 V |
| MOSI, MISO, SCLK, $\overline{\text{CS}}$, $\overline{\text{RST}}$ | -0.3 V to +3.9 V |
| Industrial Operating Temperature Range | -40°C to +85°C |
| Storage Temperature Range | -65°C to +125°C |
| Maximum Junction Temperature | 150°C |
| θ_{JA} Thermal Impedance | 26°C/W |
| ESD Rating, Human Body Model (HBM) | |
| 40-Lead LFCSP Package | |
| LNAIN1, LNAIN2, PAOUT1, PAOUT2 | ±250 V |
| All Other Pins | ±2 kV |
| 48-Lead LQFP Package | |
| LNAIN1, LNAIN2, PAOUT1, PAOUT2 | ±250 V |
| All Other Pins | ±2 kV |
| ESD Rating, Field Induced Charged Device Model (FICDM) | |
| 40-Lead LFCSP Package | |
| LNAIN1, LNAIN2, PAOUT1, PAOUT2 | ±1250 V |
| All Other Pins | ±1250 V |
| 48-Lead LQFP Package | |
| LNAIN1, LNAIN2, PAOUT1, PAOUT2 | ±1250 V |
| All Other Pins | ±1250 V |
| Reflow Soldering | |
| Peak Temperature | 260°C |
| Time at Peak Temperature | 40 sec |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Connect the exposed pad of the 40-lead LFCSP device to ground.

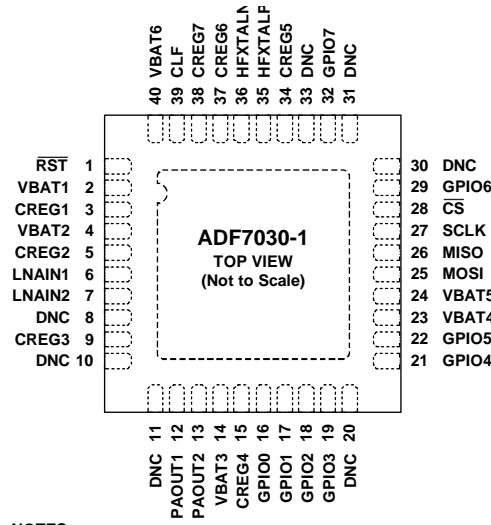
This device is a high performance, RF integrated circuit with an ESD rating as indicated in Table 21; it is ESD sensitive. Take proper precautions for handling and assembly.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



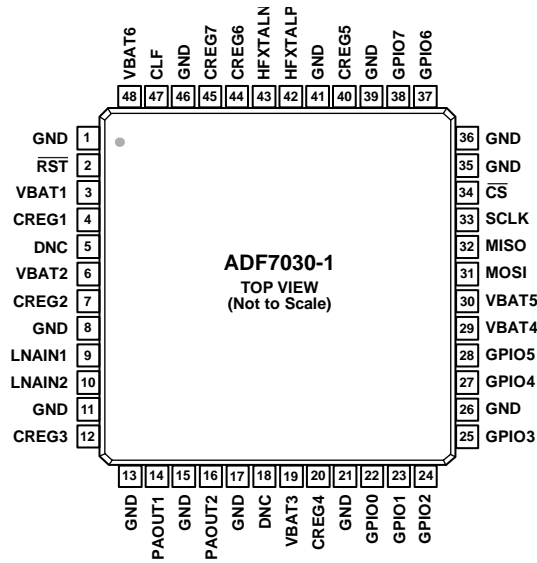
NOTES
 1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.
 2. CONNECT THE EXPOSED PAD TO GROUND.

Figure 5. 40-Lead LFCSP Pin Configuration

Table 22. 40-Lead LFCSP Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|----------|--|
| 1 | RST | External Reset, Active Low. |
| 2 | VBAT1 | Power Supply Pin 1 to the Internal Regulators. |
| 3 | CREG1 | Regulator Output 1. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. Also, place a 1.2 nF capacitor between this pin and the CLF pin. |
| 4 | VBAT2 | Power Supply Pin 2 to the Internal Regulators. |
| 5 | CREG2 | Regulator Output 2. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. |
| 6 | LNAIN1 | LNA Input 1. |
| 7 | LNAIN2 | LNA Input 2. |
| 8 | DNC | Do Not Connect. Do not connect to this pin. |
| 9 | CREG3 | Regulator Output 3. Connect this pin to the PA choke inductor to provide bias to the PA. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. |
| 10 | DNC | Do Not Connect. Do not connect to this pin. |
| 11 | DNC | Do Not Connect. Do not connect to this pin. |
| 12 | PAOUT1 | Single-Ended PA1 Output. |
| 13 | PAOUT2 | Single-Ended PA2 Output. |
| 14 | VBAT3 | Power Supply Pin 3 to the Internal Regulators. |
| 15 | CREG4 | Regulator Output 4. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. |
| 16 | GPIO0 | Digital GPIO Pin 0. |
| 17 | GPIO1 | Digital GPIO Pin 1. |
| 18 | GPIO2 | Digital GPIO Pin 2. |
| 19 | GPIO3 | Digital GPIO Pin 3. |
| 20 | DNC | Do Not Connect. Do not connect to this pin. |
| 21 | GPIO4 | Digital GPIO Pin 4. |
| 22 | GPIO5 | Digital GPIO Pin 5. |
| 23 | VBAT4 | Power Supply Pin 4 to the Internal Regulators. |
| 24 | VBAT5 | Power Supply Pin 5 to the Internal Regulators. |
| 25 | MOSI | Serial Port Master Output/Slave Input. |
| 26 | MISO | Serial Port Master Input/Slave Output. |
| 27 | SCLK | Serial Port Clock. |
| 28 | CS | Chip Select (Active Low). A pull-up resistor of 100 kΩ to V _{DD} is recommended to prevent the host processor from inadvertently waking the ADF7030-1 from sleep. |

| Pin No. | Mnemonic | Description |
|---------|----------|---|
| 29 | GPIO6 | Digital GPIO Pin 6. |
| 30 | DNC | Do Not Connect. Do not connect to this pin. |
| 31 | DNC | Do Not Connect. Do not connect to this pin. |
| 32 | GPIO7 | Digital GPIO Pin 7. |
| 33 | DNC | Do Not Connect. Do not connect to this pin. |
| 34 | CREG5 | Regulator Output 5. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. |
| 35 | HFX TALP | Positive Reference Input. If a 26 MHz TCXO is used as the external reference, do not connect this pin. If a 26 MHz XTAL is used as the reference, connect this pin to the XTAL. |
| 36 | HFX TALN | Negative Reference Input. If a 26 MHz TCXO is used as the external reference, connect this pin to the TCXO output. If a 26 MHz XTAL is used as the reference, connect this pin to the XTAL. |
| 37 | CREG6 | Regulator Output 6. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. |
| 38 | CREG7 | Regulator Output 7. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. |
| 39 | CLF | External Loop Filter Capacitor. Place a 1.2 nF capacitor between this pin and the CREG1 pin. |
| 40 | VBAT6 | Power Supply Pin 6 to the Internal Regulators. |
| | EPAD | Exposed Pad. Connect the exposed pad to ground. |



NOTES
 1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

14373-006

Figure 6. 48-Lead LQFP Pin Configuration

Table 23. 48-Lead LQFP Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|----------|--|
| 1 | GND | Connection to Ground. |
| 2 | RST | External Reset, Active Low. |
| 3 | VBAT1 | Power Supply Pin 1 to the Internal Regulators. |
| 4 | CREG1 | Regulator Output 1. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. Also, place a 1.2 nF capacitor between this pin and the CLF pin. |
| 5 | DNC | Do Not Connect. Do not connect to this pin. |
| 6 | VBAT2 | Power Supply Pin 2 to the Internal Regulators. |
| 7 | CREG2 | Regulator Output 2. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. |
| 8 | GND | Connection to Ground. |
| 9 | LNAIN1 | LNA Input 1. |
| 10 | LNAIN2 | LNA Input 2. |
| 11 | GND | Connection to Ground. |
| 12 | CREG3 | Regulator Output 3. Connect this pin to the PA choke inductor to provide bias to the PA. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. |
| 13 | GND | Connection to Ground. |
| 14 | PAOUT1 | Single-Ended PA1 Output. |
| 15 | GND | Connection to Ground. |
| 16 | PAOUT2 | Single-Ended PA2 Output. |
| 17 | GND | Connection to Ground. |
| 18 | DNC | Do Not Connect. Do not connect to this pin. |
| 19 | VBAT3 | Power Supply Pin 3 to the Internal Regulators. |
| 20 | CREG4 | Regulator Output 4. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. |
| 21 | GND | Connection to Ground. |
| 22 | GPIO0 | Digital GPIO Pin 0. |
| 23 | GPIO1 | Digital GPIO Pin 1. |
| 24 | GPIO2 | Digital GPIO Pin 2. |
| 25 | GPIO3 | Digital GPIO Pin 3. |
| 26 | GND | Connection to Ground. |
| 27 | GPIO4 | Digital GPIO Pin 4. |
| 28 | GPIO5 | Digital GPIO Pin 5. |
| 29 | VBAT4 | Power Supply Pin 4 to the Internal Regulators. |
| 30 | VBAT5 | Power Supply Pin 5 to the Internal Regulators. |
| 31 | MOSI | Master Out Slave In (MOSI). |
| 32 | MISO | Master In Slave Out (MISO). |
| 33 | SCLK | Serial Clock (SCLK). |
| 34 | CS | Chip Select (CS). |
| 35 | GND | Connection to Ground. |
| 36 | GND | Connection to Ground. |

| Pin No. | Mnemonic | Description |
|---------|------------------------|---|
| 30 | VBAT5 | Power Supply Pin 5 to the Internal Regulators. |
| 31 | MOSI | Serial Port Master Output/Slave Input. |
| 32 | MISO | Serial Port Master Input/Slave Output. |
| 33 | SCLK | Serial Port Clock. |
| 34 | $\overline{\text{CS}}$ | Chip Select (Active Low). A pull-up resistor of 100 k Ω to V _{DD} is recommended to prevent the host processor from inadvertently waking the ADF7030-1 from sleep. |
| 35 | GND | Connection to Ground. |
| 36 | GND | Connection to Ground. |
| 37 | GPIO6 | Digital GPIO Pin 6. |
| 38 | GPIO7 | Digital GPIO Pin 7. |
| 39 | GND | Connection to Ground. |
| 40 | CREG5 | Regulator Output 5. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. |
| 41 | GND | Connection to Ground. |
| 42 | HFX TALP | Positive Reference Input. If a 26 MHz TCXO is used as the external reference, do not connect this pin. If a 26 MHz XTAL is used as the reference, connect this pin to the XTAL. |
| 43 | HFX TALN | Negative Reference Input. If a 26 MHz TCXO is used as the external reference, connect this pin to the TCXO output. If a 26 MHz XTAL is used as the reference, connect this pin to the XTAL. |
| 44 | CREG6 | Regulator Output 6. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. |
| 45 | CREG7 | Regulator Output 7. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. |
| 46 | GND | Connection to Ground. |
| 47 | CLF | External Loop Filter Capacitor. Place a 1.2 nF capacitor between this pin and the CREG1 pin. |
| 48 | VBAT6 | Power Supply Pin 6 to the Internal Regulators. |

TYPICAL PERFORMANCE CHARACTERISTICS

169 MHz—RECEIVE

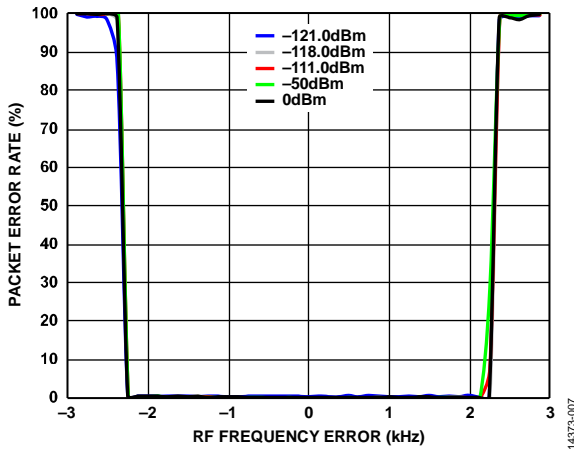


Figure 7. Packet Error Rate vs. RF Frequency Error and RF Input Power, Configuration 169.43125 MHz/2.4 kbps; AFC Enabled; $V_{DD} = 3.0\text{ V}$; $T_A = 25^\circ\text{C}$

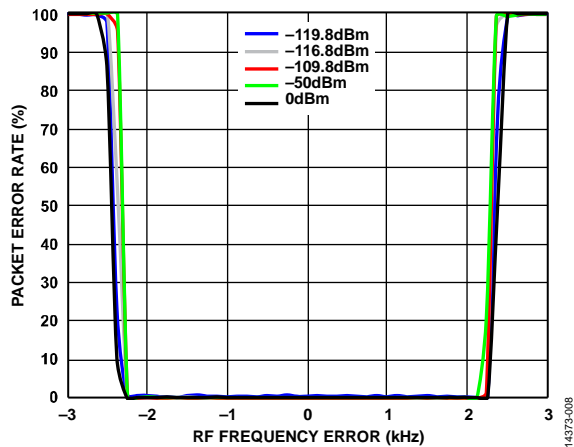


Figure 8. Packet Error Rate vs. RF Frequency Error and RF Input Power, Configuration 169.43125 MHz/4.8 kbps; AFC Enabled; $V_{DD} = 3.0\text{ V}$; $T_A = 25^\circ\text{C}$

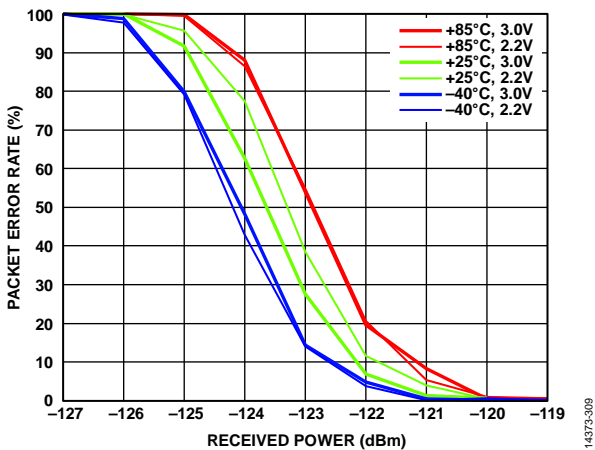


Figure 9. Packet Error Rate vs. RF Input Power, Temperature and VDD Configuration 169.43125 MHz/2.4 kbps

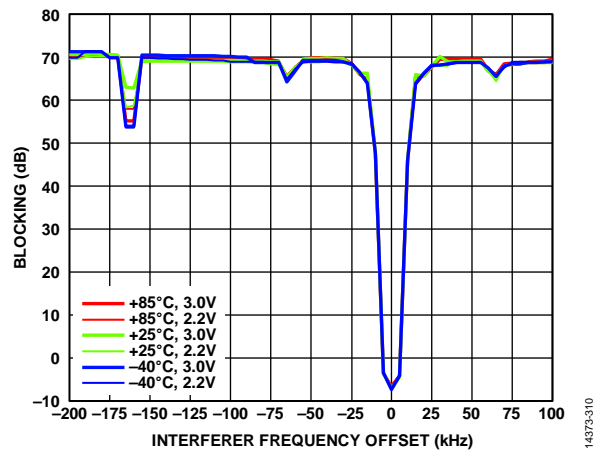


Figure 10. Receiver Close-In Blocking vs. Interferer Frequency Offset, Temperature, and V_{DD} ; Configuration 169.43125 MHz/2.4 kbps; Unmodulated Interferer; Desired Signal 3 dB Above the Sensitivity Level of PER = 5%; PER-Based Test

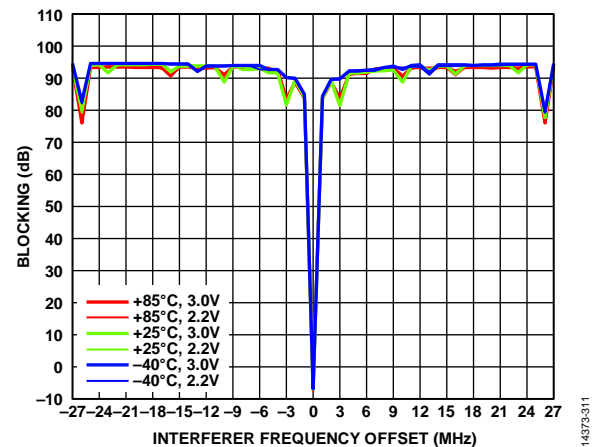


Figure 11. Receiver Wideband Blocking vs. Interferer Frequency Offset, Temperature, and V_{DD} ; Configuration 169.43125 MHz/2.4 kbps; Unmodulated Interferer; Desired Signal 3 dB Above the Sensitivity Level of PER = 5%; PER-Based Test

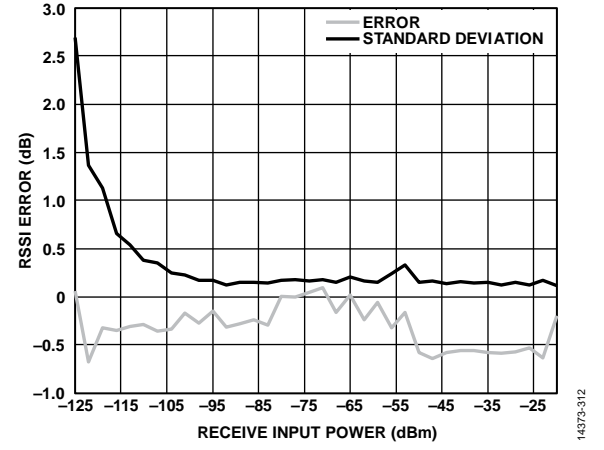
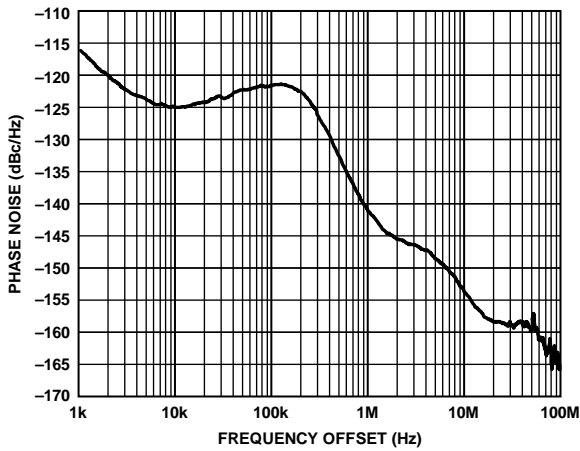


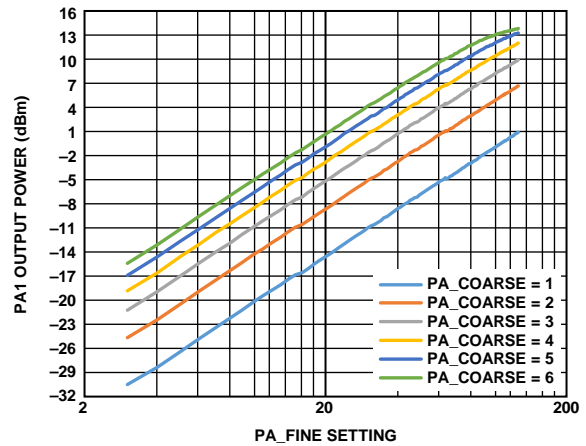
Figure 12. Packet RSSI Error vs. Rx Input Power with One-Point Calibration at -50 dBm , $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$, Configuration 169.43125 MHz/2.4 kbps (Error is Based on the Mean RSSI of 100 Packets)

169 MHz—TRANSMIT



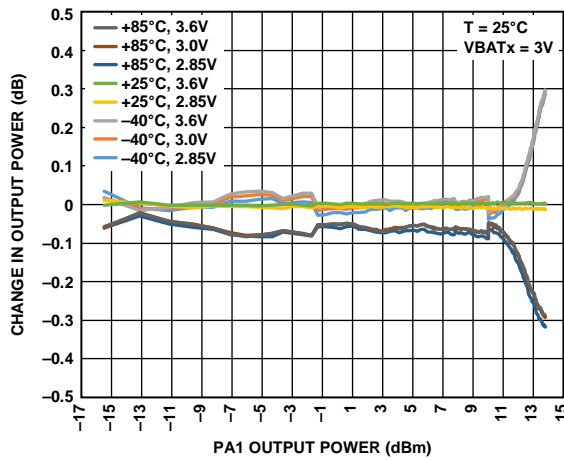
14373-014

Figure 13. Phase Noise vs. Frequency Offset, RF Frequency = 169.43125 MHz, PA2 Output Power = 17 dBm, V_{DD} = 3.0 V, T_A = 25°C



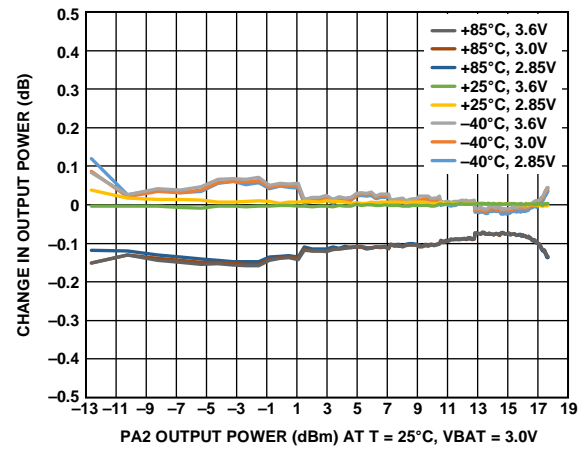
14373-017

Figure 16. PA1 Output Power vs. PA_FINE Setting and PA_COARSE Setting with PA_FINE on a Log Scale, RF Frequency = 169.43125 MHz, V_{DD} = 3.0 V, T_A = 25°C



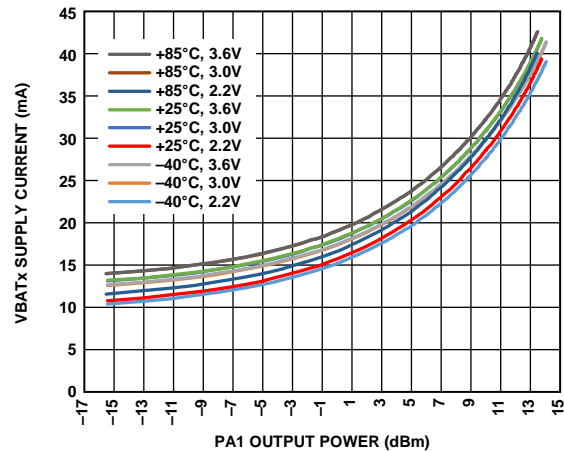
14373-015

Figure 14. Change in PA1 Output Power vs. Temperature, and V_{DD} with PA_COARSE = 6, RF Frequency = 169.43125 MHz; Variation Above 11 dBm Can Be Improved by Matching the PA for Higher Output Power



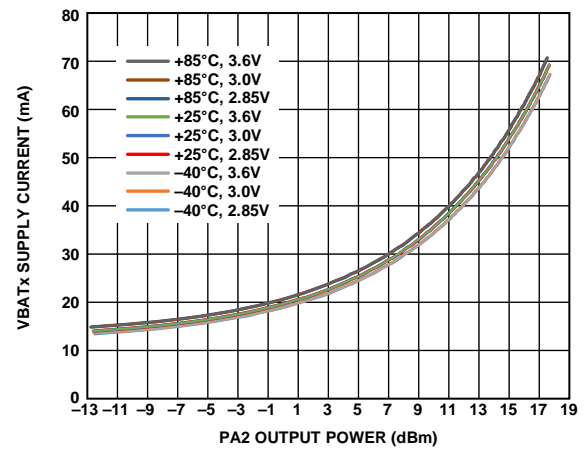
14373-018

Figure 17. Change in PA2 Output Power vs. Temperature, and V_{DD} with PA_COARSE = 10, PAOLDO_VOUT_CON = 15, RF Frequency = 169.43125 MHz



14373-016

Figure 15. VBATx Supply Current vs. PA1 Output Power, Temperature, and V_{DD} with PA_COARSE = 6, RF Frequency = 169.43125 MHz



14373-019

Figure 18. VBATx Supply Current vs. PA2 Output Power, Temperature, and V_{DD}, PA_COARSE = 10, PAOLDO_VOUT_CON = 15, RF Frequency = 169.43125 MHz

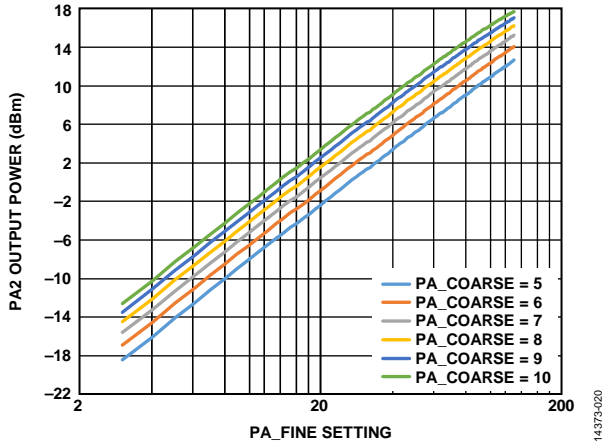


Figure 19. PA2 Output Power vs. PA_FINE Setting and PA_COARSE Setting with PA_FINE on a Logarithmic Scale, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$, RF Frequency = 169 MHz

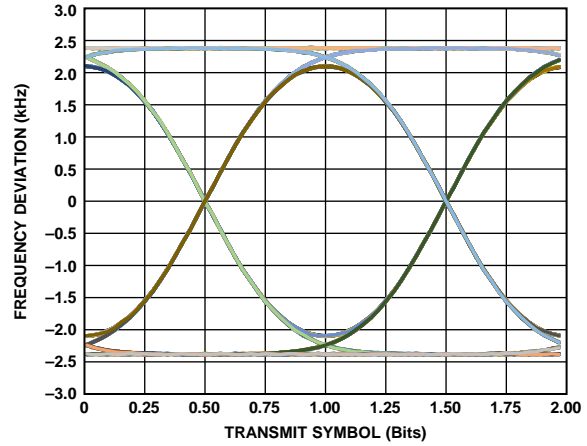


Figure 21. Transmit Eye Diagram, PA2 Output Power = 17 dBm, Configuration 169.43125 MHz/2.4 kbps, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

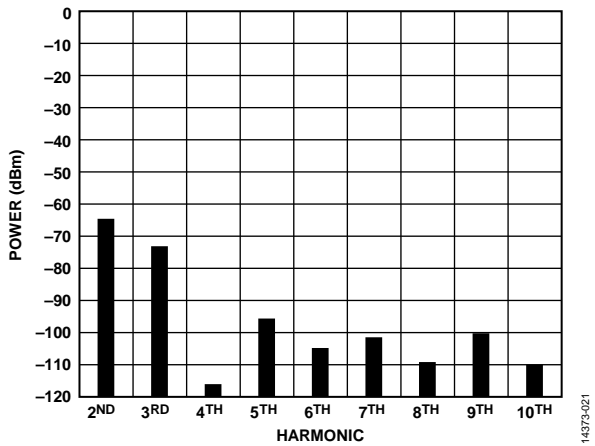


Figure 20. Conductive Harmonic Emission Level, PA2 Output Power = 17 dBm, Carrier Unmodulated, RF Frequency = 169.43125 MHz, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

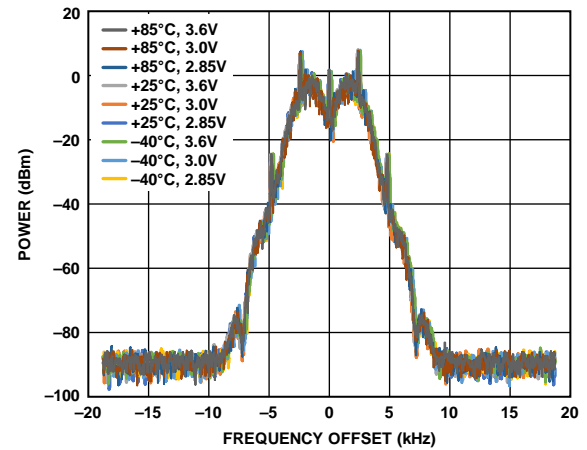


Figure 22. Transmit Spectrum, PA2 Output Power = 17 dBm, Configuration 169.43125 MHz/2.4 kbps, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

433 MHz—RECEIVE

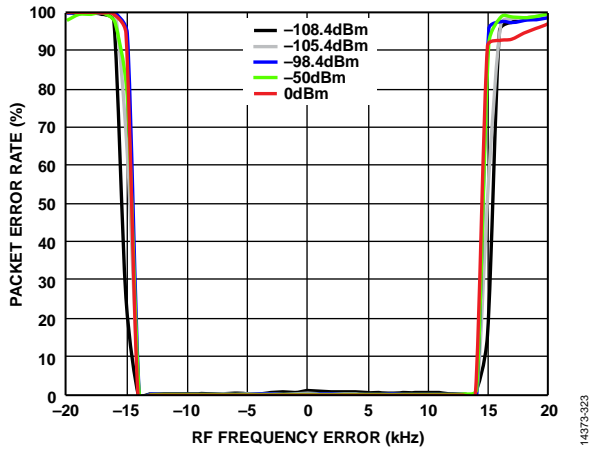


Figure 23. Packet Error Rate vs. RF Frequency Error and RF Input Power; Configuration 433 MHz/50 kbps, AFC Enabled; $V_{DD} = 3.0\text{ V}$; $T_A = 25^\circ\text{C}$

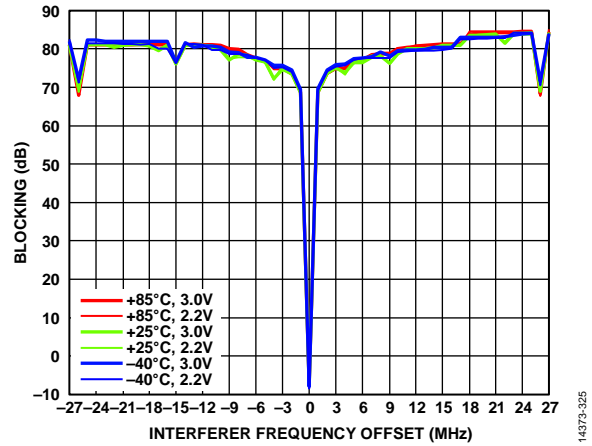


Figure 25. Receiver Wideband Blocking vs. Interferer Frequency Offset, Temperature, and V_{DD} ; Configuration 433 MHz/50 kbps; Unmodulated Interferer; Desired Signal 3 dB Above the Sensitivity Level of PER = 5%; PER-Based Test

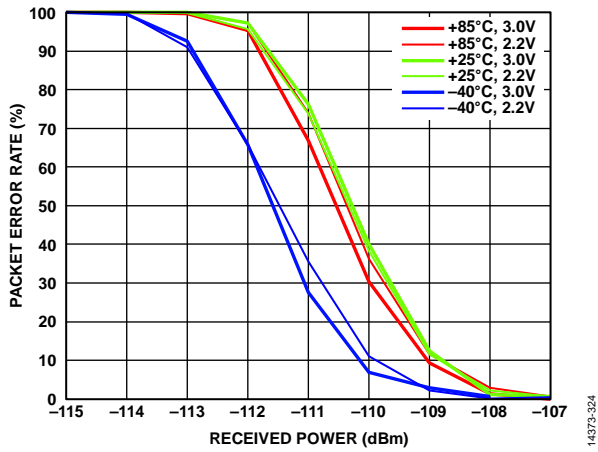


Figure 24. Packet Error Rate vs. RF Input Power, Temperature, and V_{DD} ; Configuration 433 MHz/50 kbps

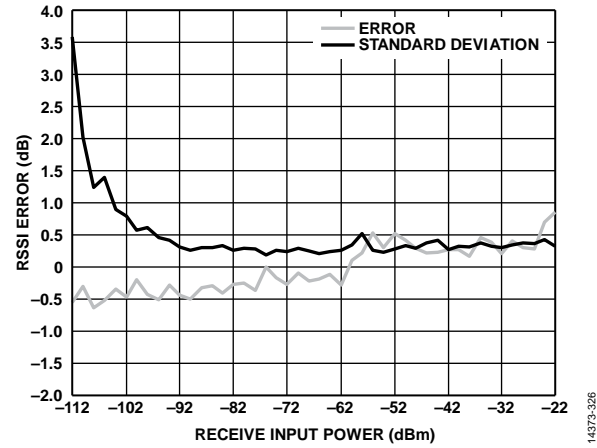


Figure 26. Packet RSSI Error vs. RX Input Power with One-Point Calibration at -77 dBm ; Configuration 433 MHz/50 kbps; $V_{DD} = 3.0\text{ V}$; $T_A = 25^\circ\text{C}$ (Error is Based on the Mean RSSI of 100 Packets)

433 MHZ—TRANSMIT

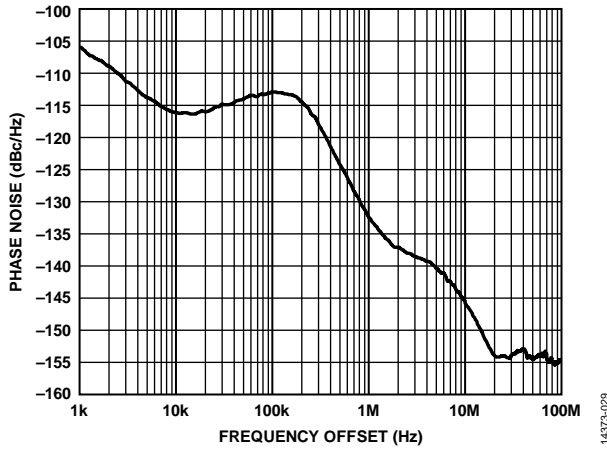


Figure 27. Phase Noise vs. Frequency Offset, RF Frequency = 433 MHz, PA1 Output Power = 10 dBm, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

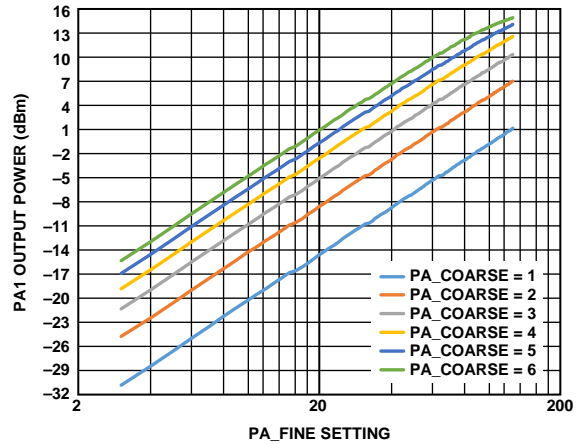


Figure 30. PA1 Output Power vs. PA_FINE Setting and PA_COARSE Setting with PA_FINE on a Logarithmic Scale, RF Frequency = 433 MHz, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

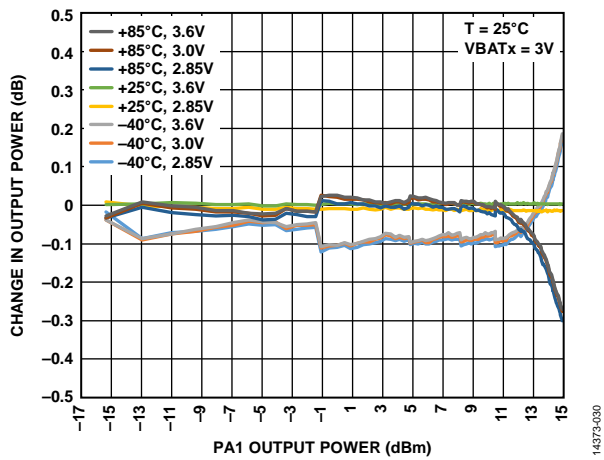


Figure 28. Change in PA1 Output Power vs. Temperature, and V_{DD} with PA_COARSE = 6, RF Frequency = 433 MHz

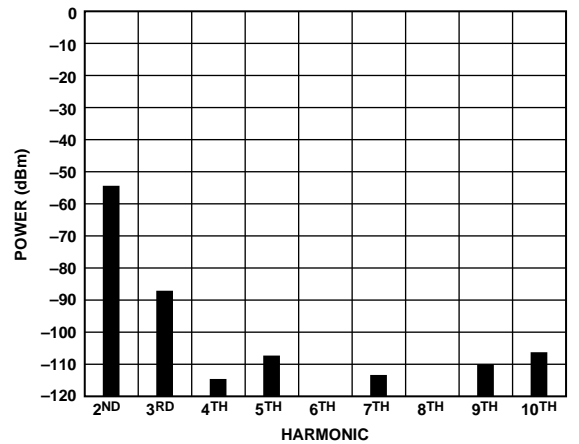


Figure 31. Conductive Harmonic Emission Level, PA1 Output Power = 10 dBm, RF Frequency = 433.92 MHz, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

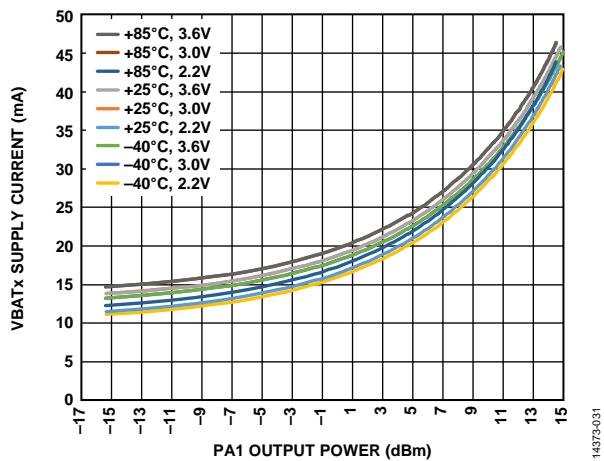


Figure 29. VBATx Supply Current vs. PA1 Output Power, Temperature, and V_{DD} with PA_COARSE = 6, RF Frequency = 433 MHz

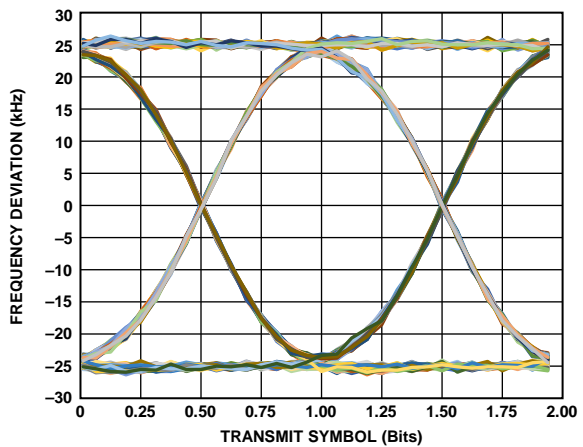


Figure 32. Transmit Eye Diagram, PA2 Output Power = 17 dBm, Configuration 433 MHz/50 kbps, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

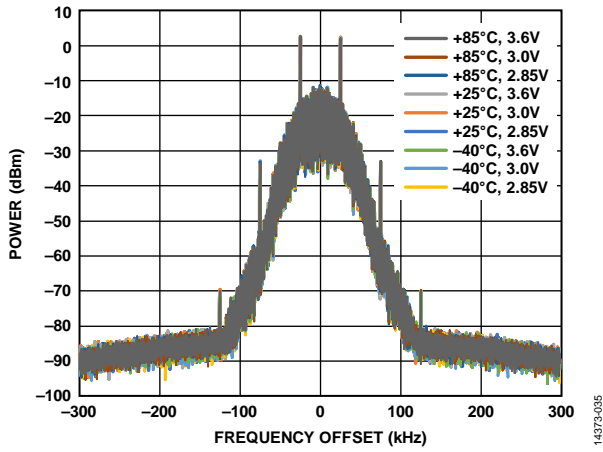


Figure 33. Transmit Spectrum, PA1 Output Power = 10 dBm, Configuration 433 MHz/50 kbps, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

460 MHz—RECEIVE

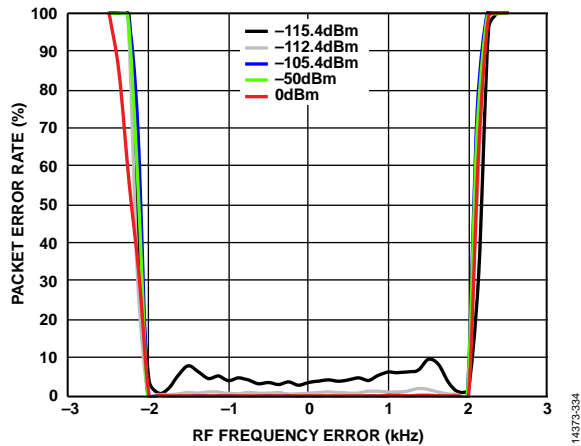


Figure 34. Packet Error Rate vs. RF Frequency Error and RF Input Power; Configuration 460 MHz/7.2 kbps; AFC Enabled; $V_{DD} = 3.0\text{ V}$; $T_A = 25^\circ\text{C}$

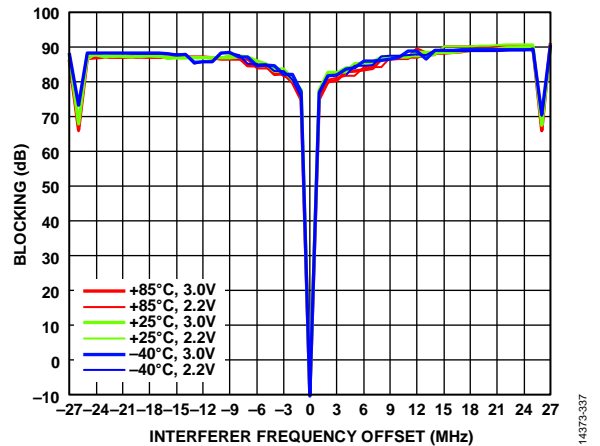


Figure 37. Receiver Wideband Blocking vs. Interferer Frequency Offset, Temperature, and V_{DD} ; Configuration 460 MHz/7.2 kbps; Unmodulated Interferer; Desired Signal 3 dB Above the Sensitivity Level of PER = 5%; PER-Based Test

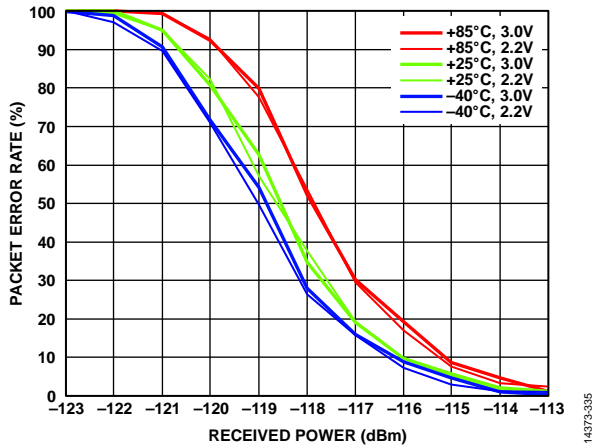


Figure 35. Packet Error Rate vs. RF Input Power, Temperature, and V_{DD} ; Configuration 460 MHz/7.2 kbps

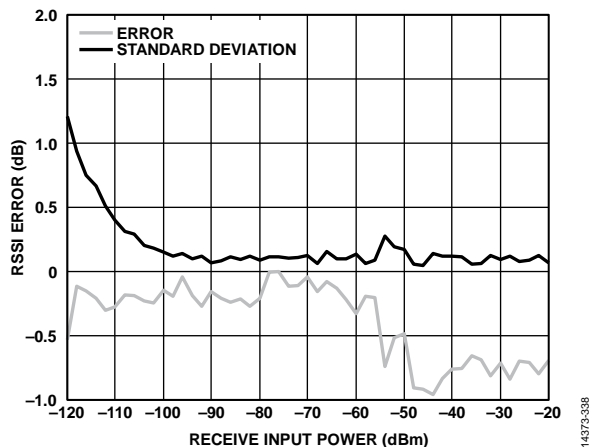


Figure 38. Packet RSSI Error vs. RF Input Power with One-Point Calibration at -77 dBm ; Configuration 460 MHz/7.2 kbps, 7.2 kbps; $V_{DD} = 3.0\text{ V}$; $T_A = 25^\circ\text{C}$ (Error is Based on the Mean RSSI of 100 Packets)

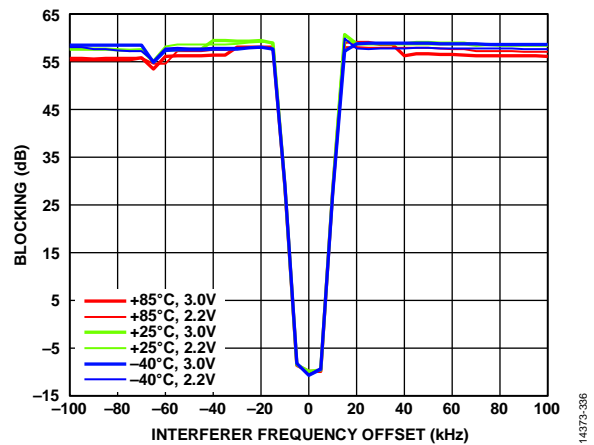


Figure 36. Receiver Close-In Blocking vs. Interferer Frequency Offset and Temperature and V_{DD} ; Configuration 460 MHz/7.2 kbps; Unmodulated Interferer; Desired Signal 3 dB Above the Sensitivity Level of PER = 5%; PER-Based Test

460 MHz—TRANSMIT

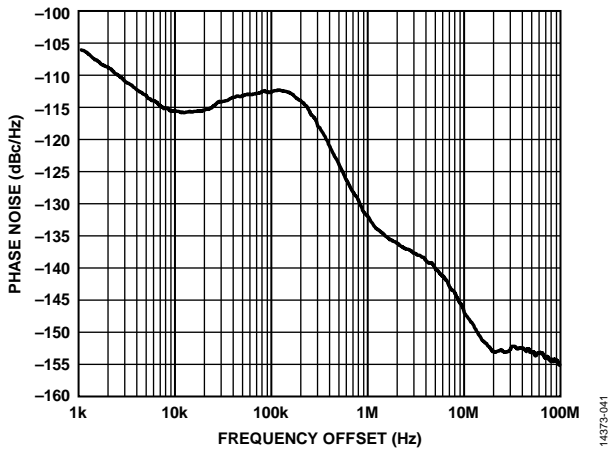


Figure 39. Phase Noise vs. Frequency Offset, RF Frequency = 460 MHz, PA2 Output Power = 17 dBm, $V_{DD} = 3.0 V$, $T_A = 25^\circ C$

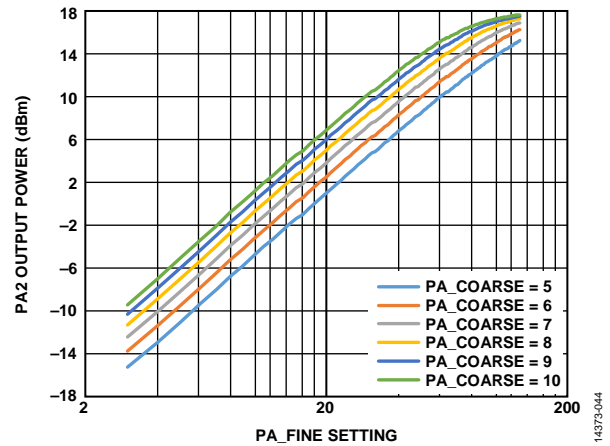


Figure 42. PA2 Output Power vs. PA_FINE Setting and PA_COARSE Setting with PA_FINE on a Logarithmic Scale, PAOLDO_VOUT_CON=15, RF Frequency = 460 MHz, $V_{DD} = 3.0 V$, $T_A = 25^\circ C$

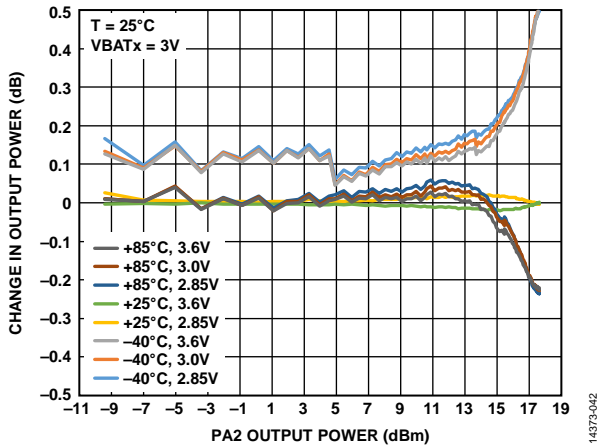


Figure 40. Change in PA2 Output Power vs. Temperature, and V_{DD} with PA_COARSE = 10, PAOLDO_VOUT_CON=15, RF Frequency = 460 MHz; Variation Above 15 dBm Can Be Improved by Matching the PA for Higher Output Power

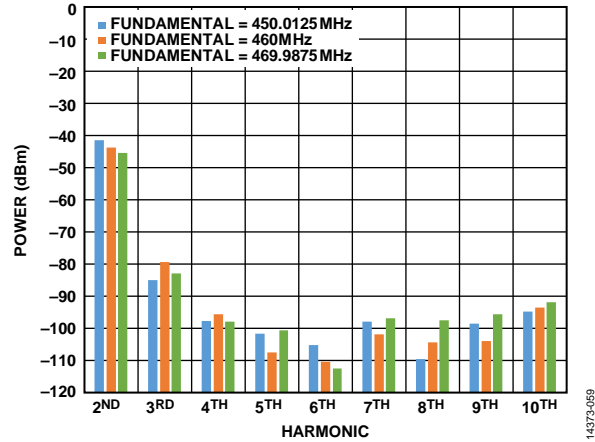


Figure 43. Conductive Harmonic Emission Level, PA2 Output Power = 17 dBm, RF Frequency = 460 MHz, $V_{DD} = 3.0 V$, $T_A = 25^\circ C$

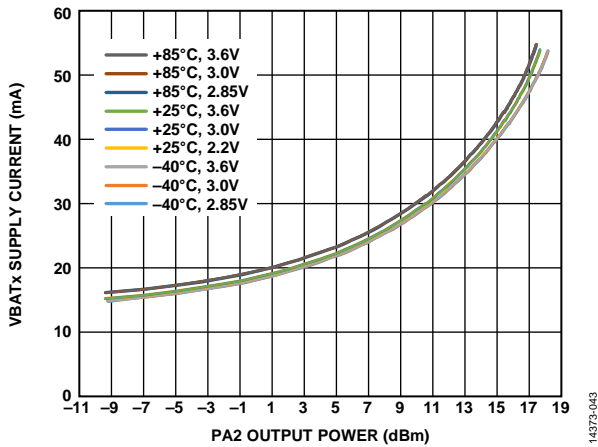


Figure 41. VBATx Supply Current vs. PA2 Output Power, Temperature, and V_{DD} with PA_COARSE = 10, PAOLDO_VOUT_CON = 15, RF Frequency = 460 MHz

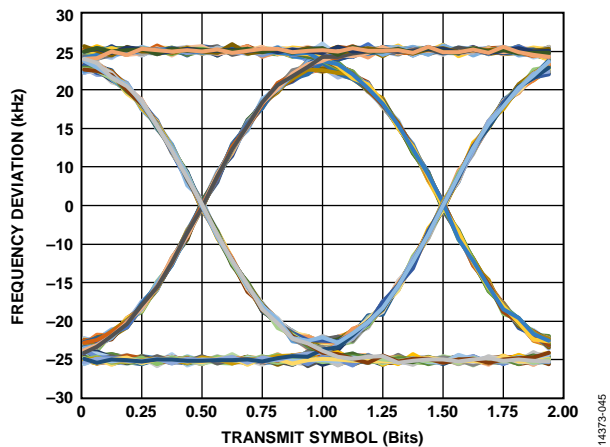


Figure 44. Transmit Eye Diagram; PA2 Output Power = 17 dBm; Configuration 460 MHz/7.2 kbps; BT = 0.5; $V_{DD} = 3.0 V$; $T_A = 25^\circ C$

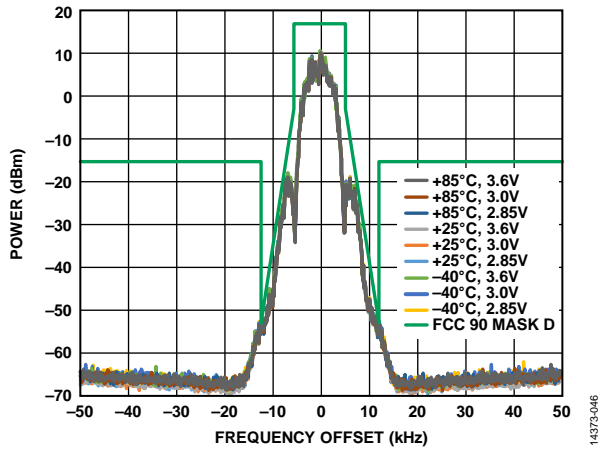


Figure 45. Transmit Spectrum, PA2 Output Power = 17 dBm, Configuration 460 MHz/7.2 kbps, BT = 0.5, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$; Margin to the Mask Can Be Improved by Reducing the BT or By Reducing the Data Rate

868 MHz—RECEIVE

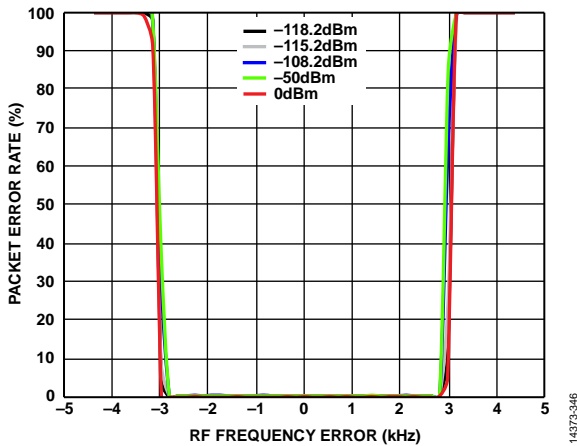


Figure 46. Packet Error Rate vs. RF Frequency Error and RF Input Power, Configuration 868 MHz/4.8 kbps, AFC Enabled, $V_{DD} = 3.0V$, $T_A = 25^\circ C$

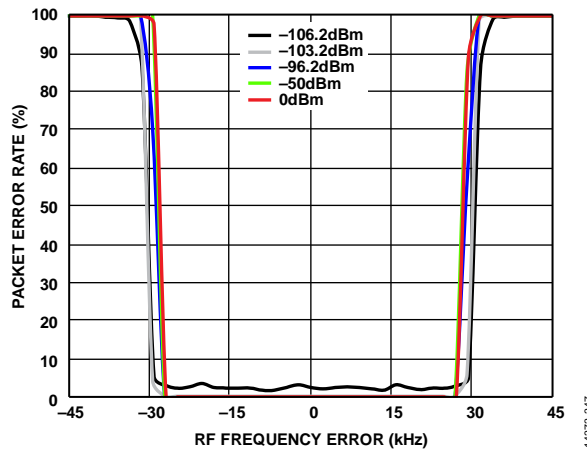


Figure 47. Packet Error Rate vs. RF Frequency Error and RF Input Power, Configuration 868 MHz/100 kbps, AFC Enabled, $V_{DD} = 3.0V$, $T_A = 25^\circ C$

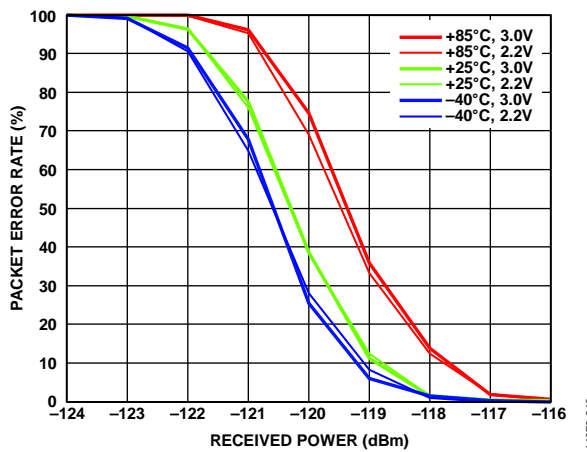


Figure 48. Packet Error Rate vs. RF Input Power, Temperature, and V_{DD} ; Configuration 868 MHz/4.8 kbps

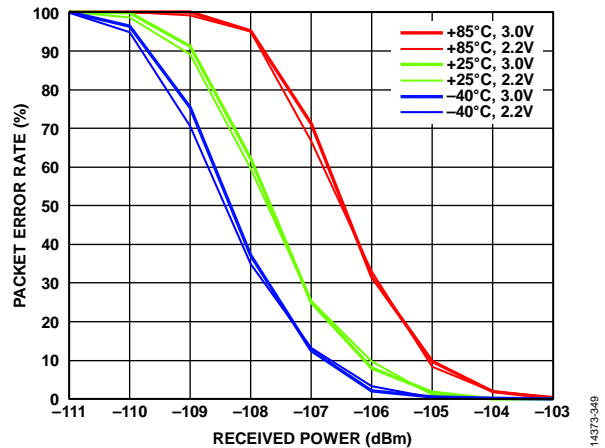


Figure 49. Packet Error Rate vs. Rx Input Power, Temperature, and V_{DD} ; Configuration 868 MHz/100 kbps

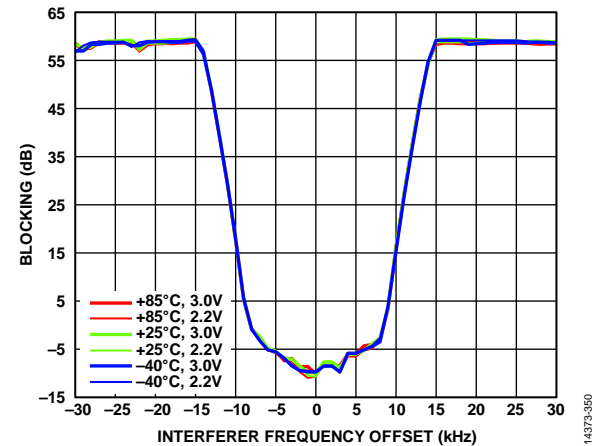


Figure 50. Receiver Close-In Blocking vs. Interferer Frequency Offset, Temperature, and V_{DD} ; Configuration 868 MHz/4.8 kbps, Unmodulated Interferer; Desired Signal 3 dB Above the Sensitivity Level of PER = 5% PER-Based Test

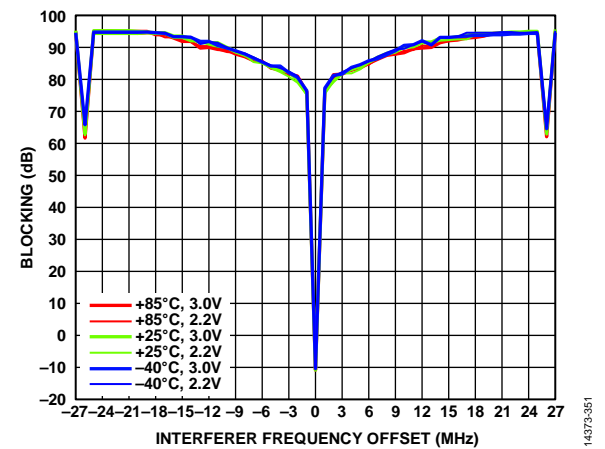


Figure 51. Receiver Wideband Blocking vs. Interferer Frequency Offset, Temperature, and V_{DD} ; Configuration 868 MHz/4.8 kbps, Unmodulated Interferer; Desired Signal 3 dB Above the Sensitivity Level of PER = 5%; PER-Based Test

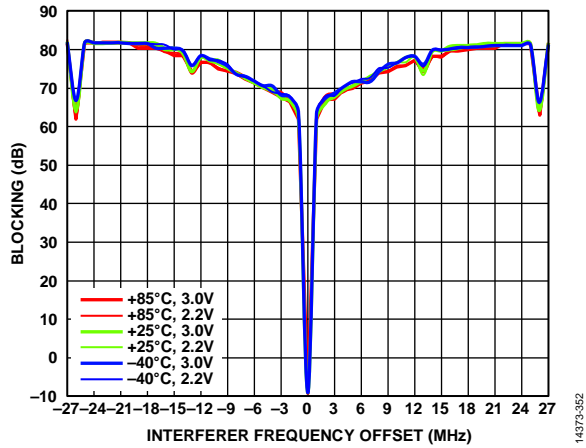


Figure 52. Receiver Wideband Blocking vs. Interferer Frequency Offset, Temperature, V_{DD} ; Configuration 868 MHz/100 kbps; Unmodulated Interferer; Desired Signal 3 dB Above the Sensitivity Level of PER = 5%; PER-Based Test

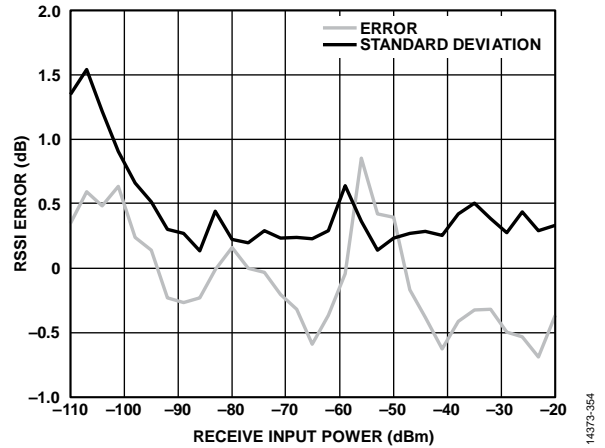


Figure 54. Packet RSSI Error vs. Rx Input Power with One-Point Calibration at -70 dBm; Configuration 868 MHz/100 kbps; $V_{DD} = 3.0$ V; $T_A = 25^\circ\text{C}$ (Error is Based on the Mean RSSI of 100 Packets)

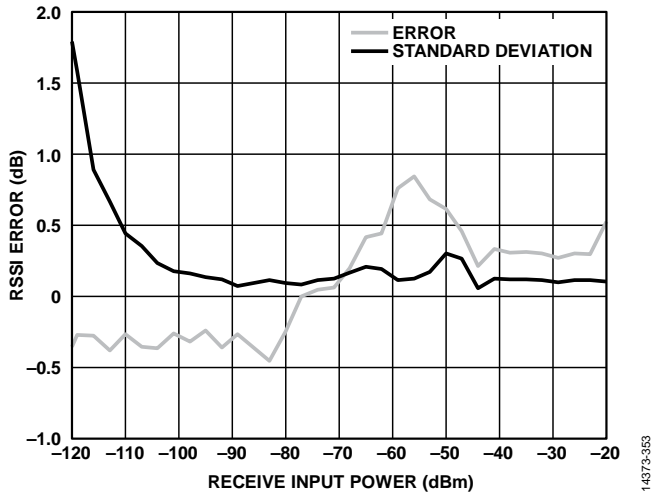


Figure 53. Packet RSSI Error vs. Rx Input Power with One-Point Calibration at -77 dBm; Configuration 868 MHz/4.8 kbps; $V_{DD} = 3.0$ V; $T_A = 25^\circ\text{C}$ (Error is Based on the Mean RSSI of 100 Packets)

868 MHz—TRANSMIT

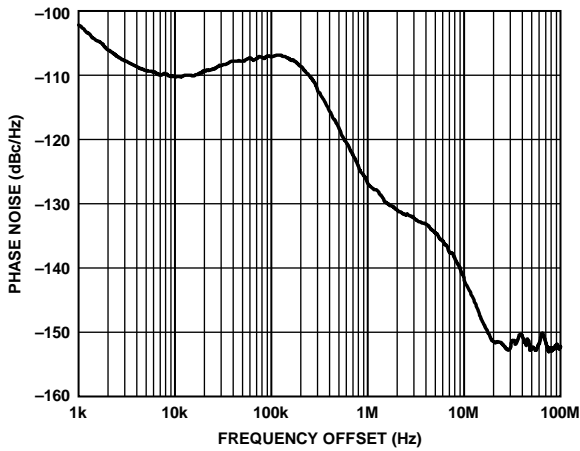


Figure 55. Phase Noise vs. Frequency Offset, RF Frequency = 868 MHz, PA2 Output Power = 17 dBm, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

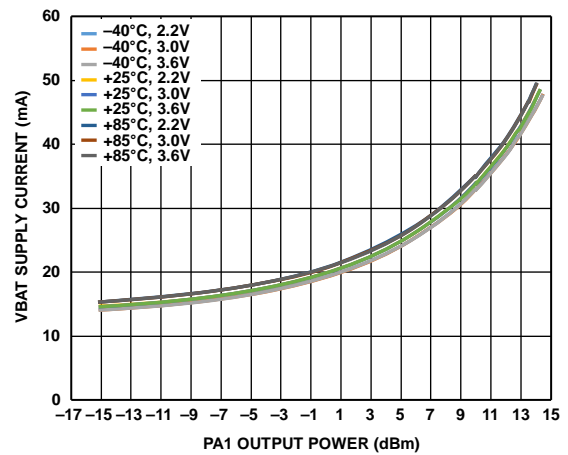


Figure 58. VBATx Supply Current vs. PA1 Output Power, Temperature, and V_{DD} with PA_COARSE = 6, RF Frequency = 868 MHz

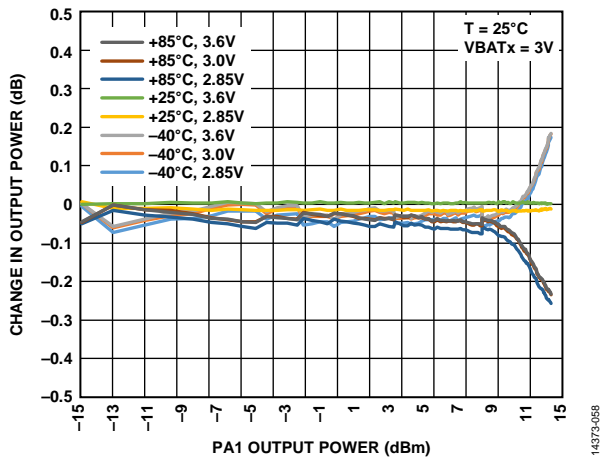


Figure 56. Change in PA1 Output Power vs. Temperature, and V_{DD} with PA_COARSE = 10, RF Frequency = 868 MHz

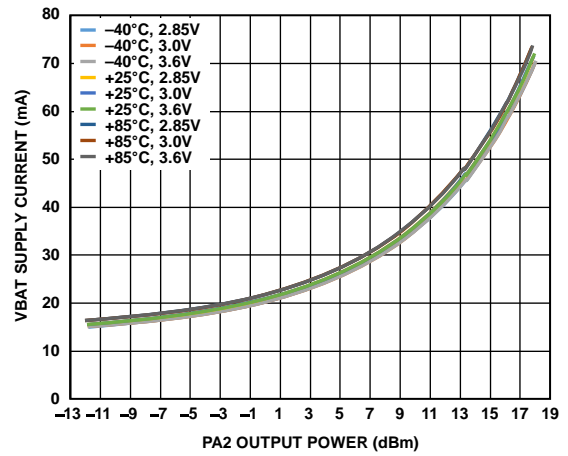


Figure 59. VBATx Supply Current vs. PA2 Output Power, Temperature, and V_{DD} with PA_COARSE = 10, RF Frequency = 868 MHz

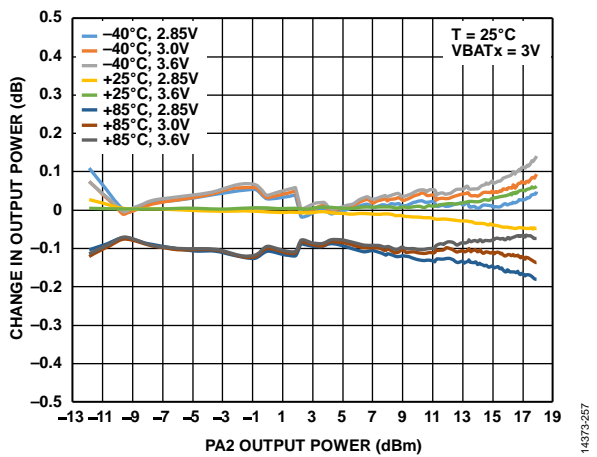


Figure 57. Change in PA2 Output Power vs. Temperature, and V_{DD} with PA_COARSE = 10, PAOLDO_VOUT_CON = 15, RF Frequency = 868 MHz

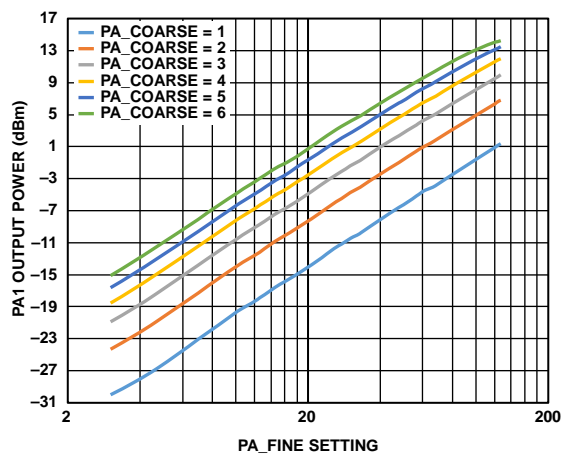


Figure 60. PA1 Output Power vs. PA_FINE Setting and PA_COARSE Setting with PA_FINE on a Logarithmic Scale, RF Frequency = 868 MHz, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

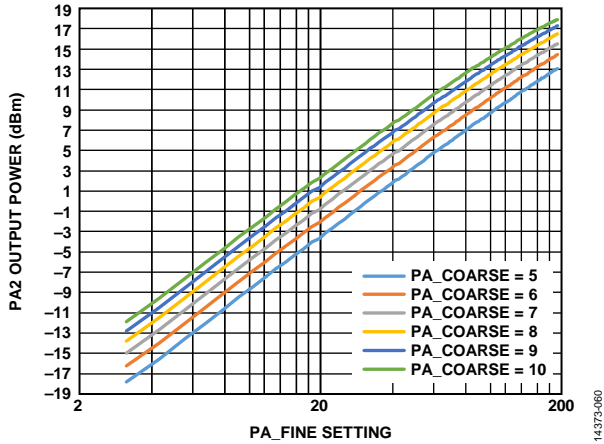


Figure 61. PA2 Output Power vs. PA_FINE Setting and PA_COARSE Setting with PA_FINE on a Logarithmic Scale, PAOLDO_VOUT_CON = 15, RF Frequency = 868 MHz, V_{DD} = 3.0 V, T_A = 25°C

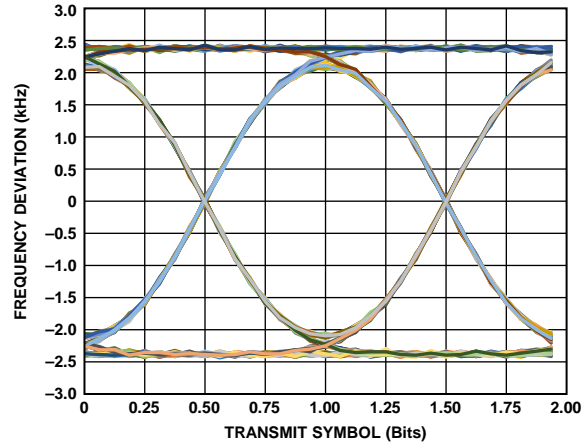


Figure 63. Transmit Eye Diagram, PA2 Output Power = 17 dBm, Configuration 868 MHz/4.8 kbps; V_{DD} = 3.0 V; T_A = 25°C

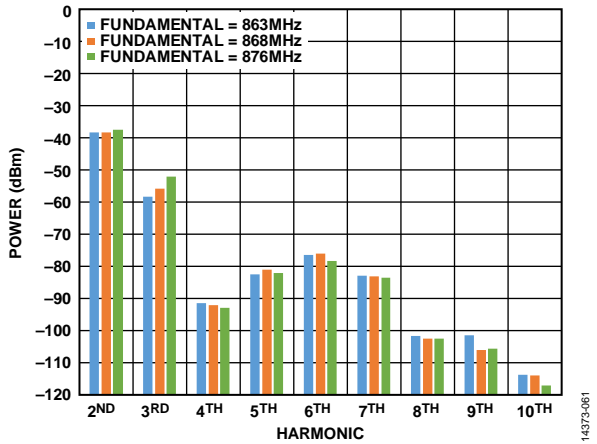


Figure 62. Conductive Harmonic Emission Level, PA2 Output Power = 17 dBm, RF Frequency = 868 MHz, V_{DD} = 3.0 V, T_A = 25°C

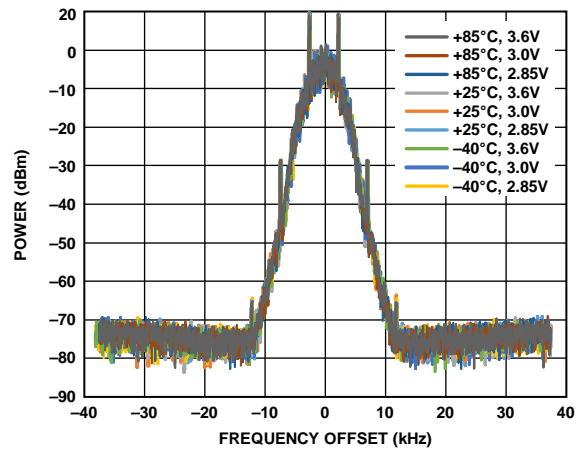


Figure 64. Transmit Spectrum vs. Temperature, and V_{DD} with PA2 Output Power = 17 dBm, Configuration 868 MHz/4.8 kbps, V_{DD} = 3.0 V; T_A = 25°C

915 MHz—RECEIVE

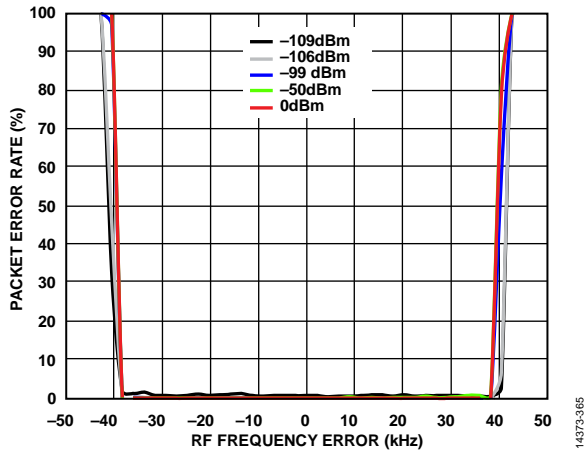


Figure 65. Packet Error Rate vs. RF Frequency Error and RF Input Power; Configuration 915 MHz/50 kbps; AFC Enabled; $V_{DD} = 3.0\text{ V}$; $T_A = 25^\circ\text{C}$

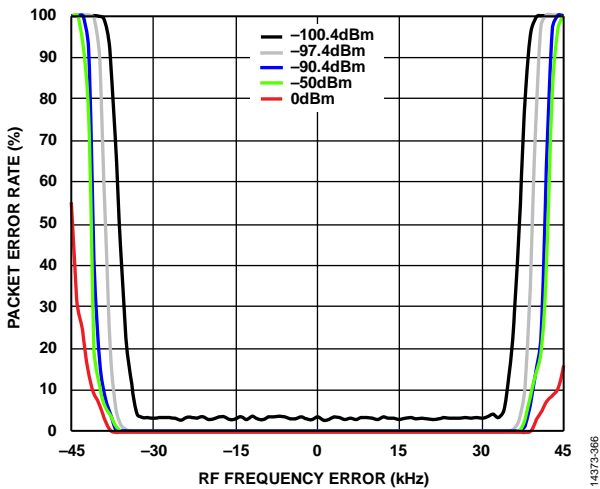


Figure 66. Packet Error Rate vs. RF Frequency Error and RF Input Power; Configuration 915 MHz/150 kbps; AFC Enabled; $V_{DD} = 3.0\text{ V}$; $T_A = 25^\circ\text{C}$

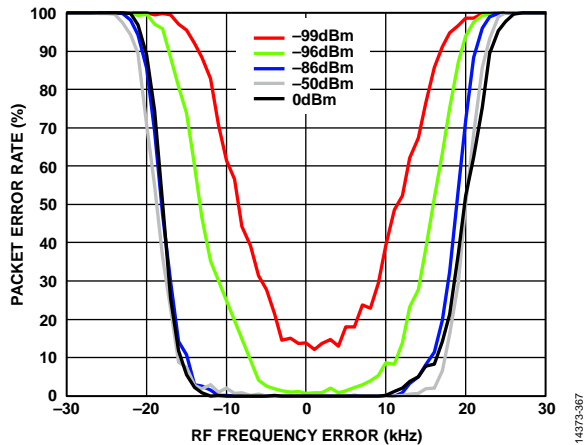


Figure 67. Packet Error Rate vs. RF Frequency Error and RF Input Power; Configuration 915 MHz/300 kbps; AFC Disabled; $V_{DD} = 3.0\text{ V}$; $T_A = 25^\circ\text{C}$

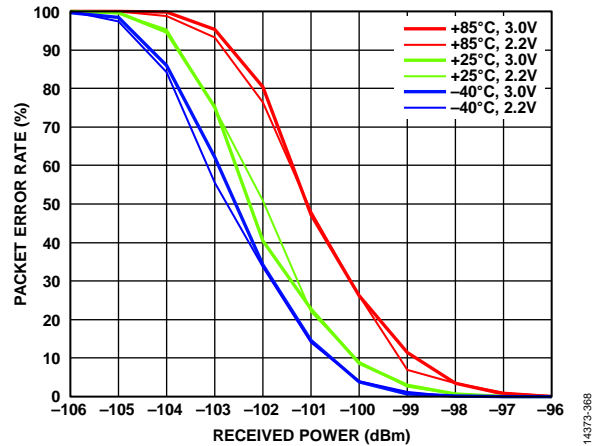


Figure 68. Packet Error Rate vs. Rx Input Power, Temperature, and V_{DD} ; Configuration 915 MHz/150 kbps; FEC Disabled; AFC Enabled

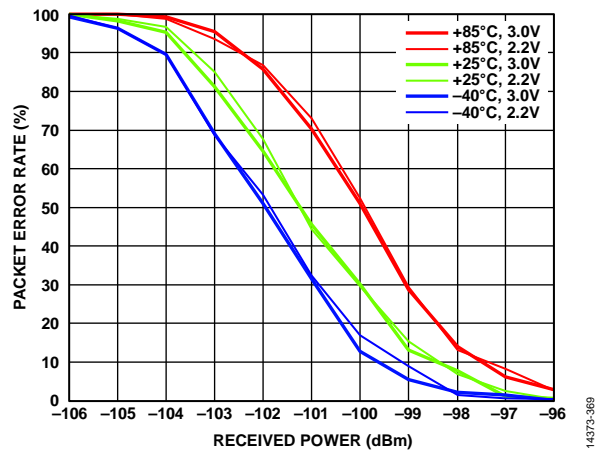


Figure 69. Packet Error Rate vs. Rx Power, Temperature, and V_{DD} ; Configuration 915 MHz/300 kbps; AFC Disabled

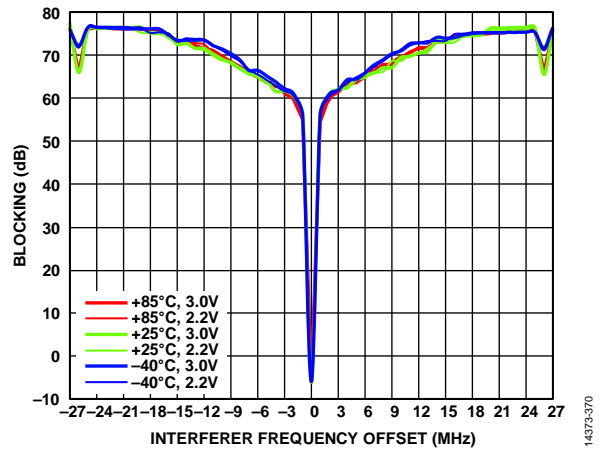


Figure 70. Receiver Wideband Blocking vs. Interferer Frequency Offset, Temperature, and V_{DD} ; Configuration 915 MHz/150 kbps; Unmodulated Interferer; Desired Signal 3 dB Above the Sensitivity Level of PER = 5%; PER-Based Test

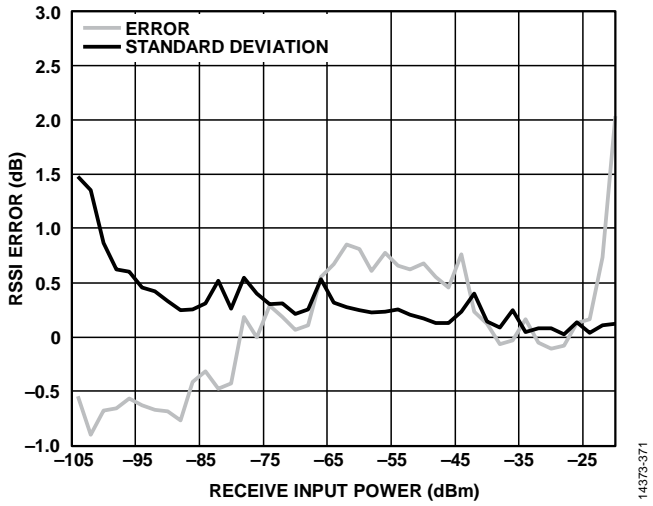


Figure 71. Packet RSSI Error vs. Rx Input Power with One-Point Calibration at -70 dBm; Configuration 915 MHz/150 kbps; $V_{DD} = 3.0\text{ V}$; $T_A = 25^\circ\text{C}$ (Error is Based on the Mean RSSI of 100 Packets)

915 MHz—TRANSMIT

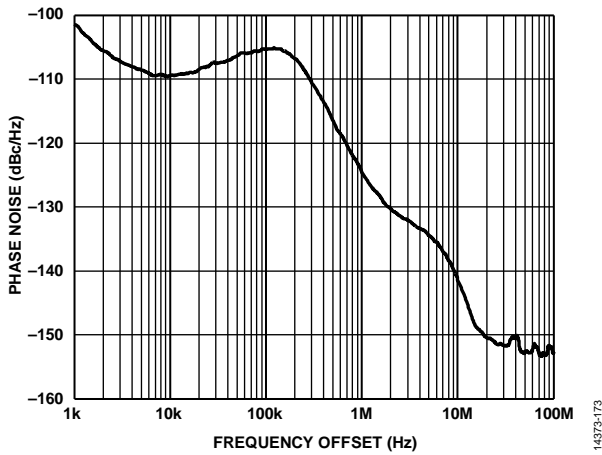


Figure 72. Phase Noise vs. Frequency Offset, RF Frequency = 915 MHz, PA2 Output Power = 17 dBm, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

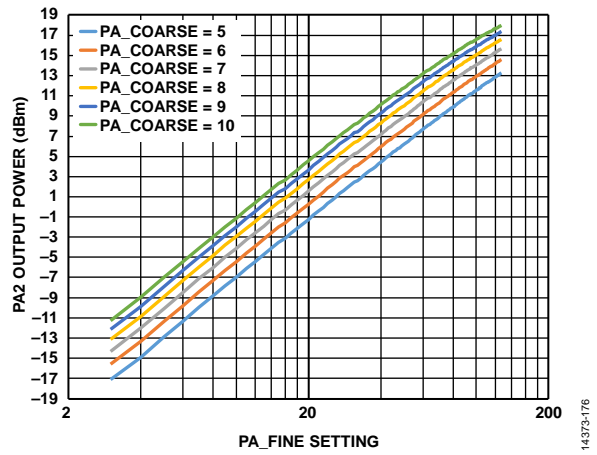


Figure 75. PA2 Output Power vs. PA_FINE Setting and PA_COARSE Setting with PA_FINE on a Logarithmic Scale, PAOLDO_VOUT_CON = 15, RF Frequency = 915 MHz, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

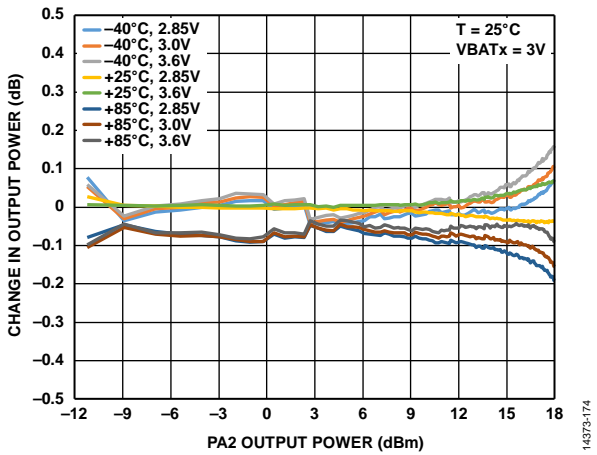


Figure 73. Change in PA2 Output Power vs. Temperature, and V_{DD} with PA_COARSE = 10, PAOLDO_VOUT_CON = 15, RF Frequency = 915 MHz

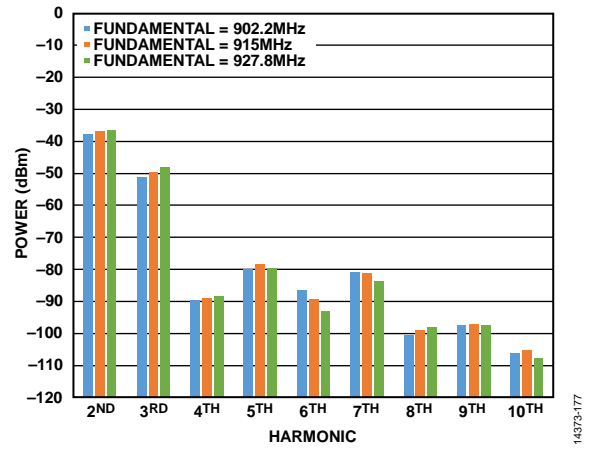


Figure 76. Conductive Harmonic Emission Level, PA2 Output Power = 17 dBm, RF Frequency = 915 MHz, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

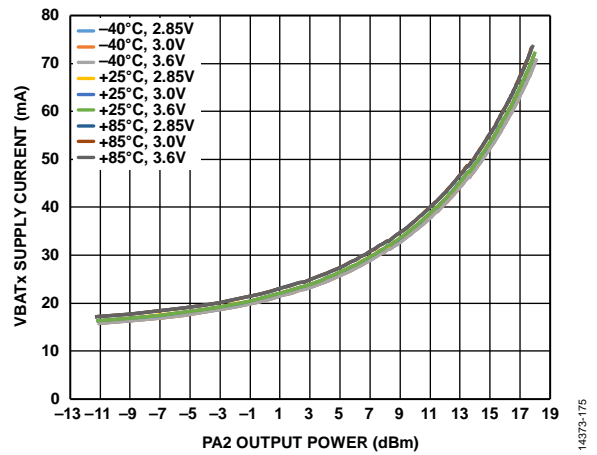


Figure 74. VBATx Supply Current vs. PA2 Output Power, Temperature, and V_{DD} with PA_COARSE = 10, PAOLDO_VOUT_CON = 15, RF Frequency = 915 MHz

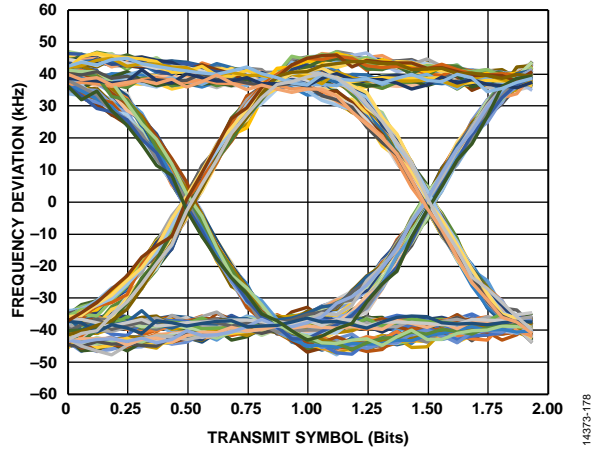


Figure 77. Transmit Eye Diagram, PA2 Output Power = 17 dBm, Configuration 915 MHz/150 kbps, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

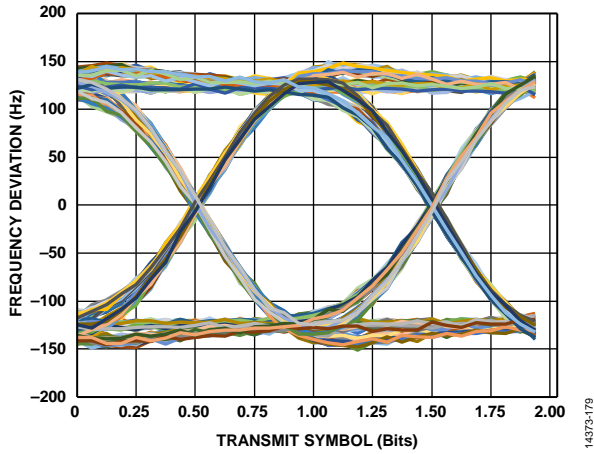


Figure 78. Transmit Eye Diagram, PA2 Output Power = 17 dBm, Configuration 915 MHz/300 kbps, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

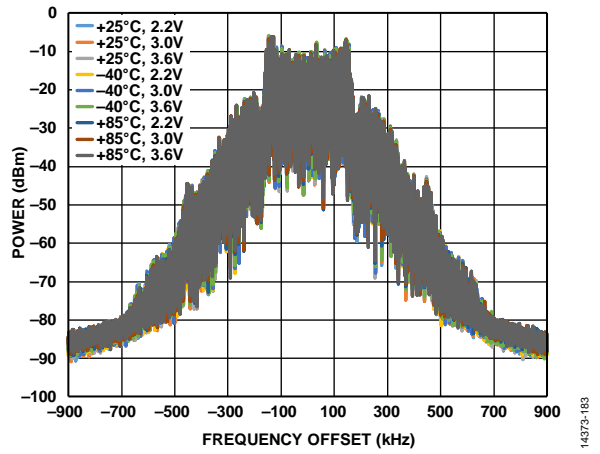


Figure 80. Transmit Spectrum vs. Temperature, and VDDPA2 Output Power = 17 dBm, Configuration 915 MHz/300 kbps; $V_{DD} = 3.0\text{ V}$; $T_A = 25^\circ\text{C}$

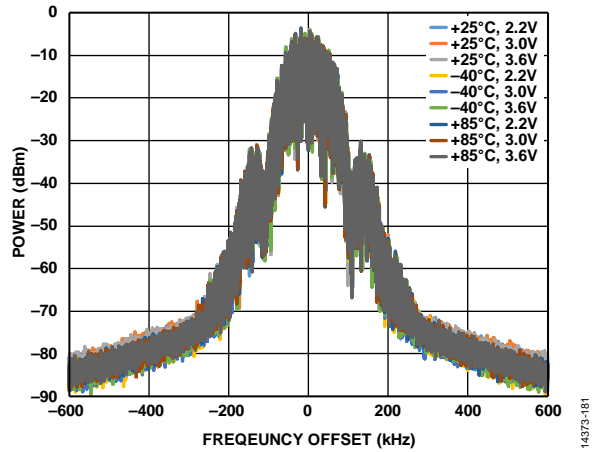


Figure 79. Transmit Spectrum, PA2 Output Power = 17 dBm, Configuration: 915 MHz/150 kbps, $V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

14373-179

14373-183

14373-181

THEORY OF OPERATION

STATE MACHINE

The ADF7030-1 operates as a simple state machine as illustrated in Figure 81. The host processor can transition the ADF7030-1 between states by issuing single-byte commands over the SPI interface.

The ADF7030-1 processor handles the sequencing of various radio circuits and critical timing functions, thereby simplifying radio operation and easing the burden on the host processor.

The ADF7030-1 states are described in Table 24.

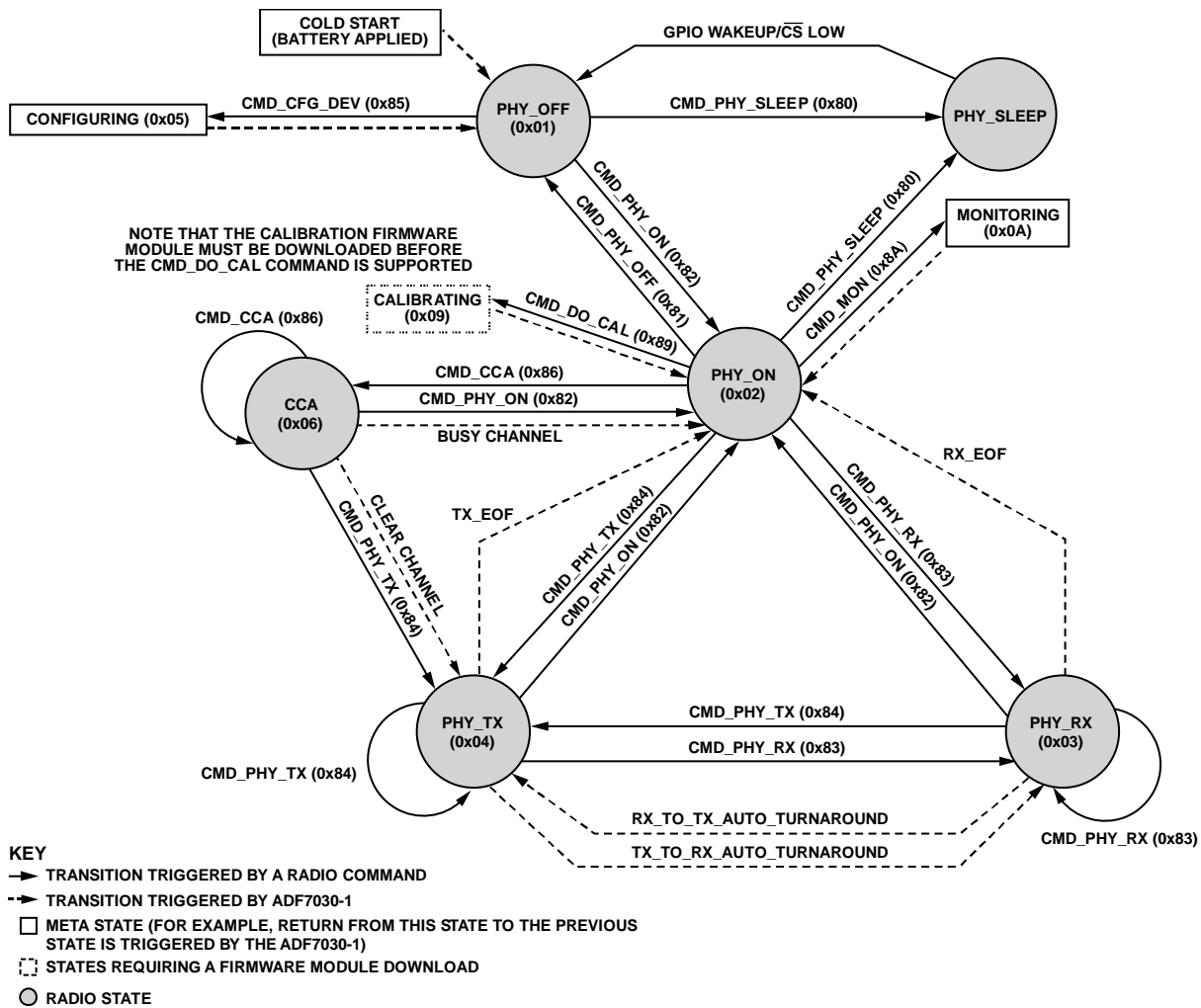


Figure 81. Radio State Machine Diagram

Table 24. Radio States

| State | Description | Typical Current |
|-----------|---|---|
| PHY_SLEEP | In this state, the ADF7030-1 is in sleep. Memory can be optionally retained. | 10 nA |
| PHY_OFF | In this state, the ADF7030-1 executes using its own internal oscillator clock. The host configures the radio from this state. | 3.7 mA |
| PHY_ON | In this state, the external reference clock source is enabled. After entering this state, the ADF7030-1 is ready for the transmission and reception of packets. | 3.7 mA |
| PHY_RX | In this state, the ADF7030-1 can receive and process an incoming packet. | 21 mA to 25.4 mA (RF frequency and data rate dependent) |
| PHY_TX | In this state, the ADF7030-1 transmits the programmed packet data. | 16 mA to 65 mA (RF frequency and Tx power dependent) |
| CCA | In this state, the ADF7030-1 performs clear channel assessment. | 21 mA to 25.4 mA (frequency and data rate dependent) |

RADIO TIMING

Table 25. Radio Timing Specifications

| Present State | Next State | Command/Bit | Command Initiated By | Transition Time (μs), Typical at Data Rate = 2.4 kbps | Transition Time (μs), Typical at Data Rate = 300 kbps | Condition |
|---------------|------------|--|----------------------|---|---|---|
| PHY_SLEEP | PHY_OFF | Wakeup from PHY_SLEEP (RTC timeout event) | Automatic | 101 | 101 | None |
| PHY_SLEEP | PHY_OFF | Wakeup from PHY_SLEEP (\overline{CS} low) | Host | 101 | 101 | From \overline{CS} low to PHY_OFF |
| PHY_OFF | PHY_SLEEP | CMD_PHY_SLEEP | Host | 95 | 95 | From \overline{CS} low to PHY_SLEEP, memory retention enabled |
| PHY_OFF | PHY_ON | CMD_PHY_ON | Host | 206, 188 | 206, 188 | First transition after cold start or wake from PHY_SLEEP, subsequent transitions; 26 MHz TCXO reference |
| PHY_OFF | PHY_ON | CMD_PHY_ON | Host | 490, 188 | 490, 188 | First transition after cold start or wake from PHY_SLEEP, subsequent transitions; 26 MHz XTAL reference |
| PHY_OFF | PHY_OFF | CMD_CFG_DEV | Host | 36 | 36 | RTC not enabled |
| PHY_ON | PHY_SLEEP | CMD_PHY_SLEEP | Host | 30 | 30 | None |
| PHY_ON | PHY_OFF | CMD_PHY_OFF | Host | 19 | 19 | None |
| PHY_ON | PHY_ON | CMD_LFRC_CAL | Host | 30000 | 30000 | None |
| PHY_ON | CCA | CMD_CCA | Host | 230 | 230 | To receiver enabled |
| PHY_ON | PHY_TX | CMD_PHY_TX | Host | 245 | 245 | To start of PA ramp |
| PHY_ON | PHY_RX | CMD_PHY_RX | Host | 223 | 225 | To receiver enabled |
| CCA | PHY_ON | CMD_PHY_ON | Host | 46 | 46 | None |
| CCA | PHY_ON | Channel busy | Automatic | 16 | 16 | From receiver disabled |
| CCA | PHY_TX | Clear channel | Automatic | 208 | 203 | From receiver disabled to start of PA ramp |
| CCA | PHY_TX | CMD_PHY_TX | Host | 239 | 239 | From receiver disabled to start of PA ramp |
| PHY_TX | PHY_ON | CMD_PHY_ON | Host | 36 | 36 | From PA ramp finished to PHY_ON |
| PHY_TX | PHY_ON | TX_EOF | Automatic | 26 | 26 | From PA ramp finished to PHY_ON |
| PHY_TX | PHY_TX | CMD_PHY_TX | Host | 258 | 231 | From start of PA ramp down (at fastest PA ramp rate) to start of PA ramp up on new channel |
| PHY_TX | PHY_RX | CMD_PHY_RX | Host | 204 | 208 | From PA ramp finished to receiver enabled |
| PHY_TX | PHY_RX | Autoturnaround | Automatic | 204 | 208 | From PA ramp finished to receiver enabled |
| PHY_RX | PHY_ON | CMD_PHY_ON | Host | 46 | 46 | None |
| PHY_RX | PHY_ON | RX_EOF | Automatic | 32 | 32 | From end of frame IRQ to PHY_ON |
| PHY_RX | PHY_RX | CMD_PHY_RX | Host | 216 | 220 | From \overline{CS} high to receiver enabled on new channel |
| PHY_RX | PHY_TX | Autoturnaround | Automatic | 220 | 220 | From end of frame IRQ to start of PA ramp |
| PHY_RX | PHY_TX | CMD_PHY_TX | Host | 203 | 203 | From \overline{CS} high to start of PA ramp |

HOST INTERFACE

Physical Interface

The ADF7030-1 provides a simple host interface (HIF) that consists of a 4-wire standard SPI, a hardware reset pin (RST) and GPIOs. The ADF7030-1 always acts as a slave to the host processor. The host uses the SPI to read and write ADF7030-1 memory and registers, to issue commands, to track the status of the state machine, and to wake up the ADF7030-1 from PHY_SLEEP.

Host Interface Protocol

The ADF7030-1 implements a very simple protocol over the SPI interface. Using this protocol, the host processor can perform a number of operations, as described in the Memory Access section, the Radio Commands section, and the Status Byte section.

Memory Access

The memory access commands allow the host processor to read from and write to the internal memory of the ADF7030-1. Typically, the host uses these commands to update the configuration of the ADF7030-1 and to write packets for transmission or to read received packets.

Radio Commands

A state machine command triggers a change of radio state as described in Table 26.

Table 26. State Machine Radio Commands

| Command | Description |
|---------------|--|
| CMD_PHY_SLEEP | Performs a transition of the device into the PHY_SLEEP state |
| CMD_PHY_OFF | Performs a transition of the device into the PHY_OFF state |
| CMD_PHY_ON | Performs a transition of the device into the PHY_ON state |
| CMD_PHY_RX | Performs a transition of the device into the PHY_RX state |
| CMD_PHY_TX | Performs a transition of the device into the PHY_TX state |
| CMD_CFG_DEV | Configures the ADF7030-1 based on the radio profile |
| CMD_CCA | Performs a transition of the device into the CCA state |
| CMD_DO_CAL | Executes selected calibration routines; requires the OffLineCalibrations.cfg firmware module |
| CMD_MON | Measures and reports the ADF7030-1 temperature |
| CMD_LFRC_CAL | Performs a frequency calibration of the internal 26kHz RC oscillator; requires the OffLineCalibrations.cfg firmware module |

Status Byte

The ADF7030-1 reports the status via a status byte. The ADF7030-1 returns this byte on the SPI MISO in response to a no operation command (NOP) (0xFF) on the SPI MOSI.

RECEIVER

The ADF7030-1 features a fully integrated, highly configurable receiver that enables exceptionally high performance reception of narrow-band and wideband 2FSK/2GFSK signals. The receiver is based on a low IF architecture. Figure 82 shows a simplified block diagram of the receiver.

RF Front End

The receive signal is amplified by a differential LNA. The LNA is followed by a quadrature downconversion mixer that converts the RF signal to the IF frequency. The automatic gain control (AGC) circuit automatically controls the gain of the RF front end. The fully integrated, fractional-N frequency synthesizer generates the LO for the mixer. When the ADF7030-1 enters the PHY_RX state, the bandwidth of the synthesizer is set automatically to ensure optimum interference rejection performance.

IF Processing

The quadrature IF signal is band-pass filtered using a high performance, configurable analog filter. The filter is followed by a programmable gain array (PGA) that is controlled by the AGC circuit.

The ADF7030-1 features a narrow-band and wideband IF processing path. In the narrow-band path, the IF signal is digitized by a high performance, high dynamic range analog-to-digital converter (ADC). RSSI, decimation, and offset correction are performed before the digitized IF is filtered using a configurable narrow-band digital channel filter.

In the wideband path, a limiter converts the IF signal to digital levels for the demodulator. The limiter also provides offset correction and RSSI, which is digitized using the ADC.

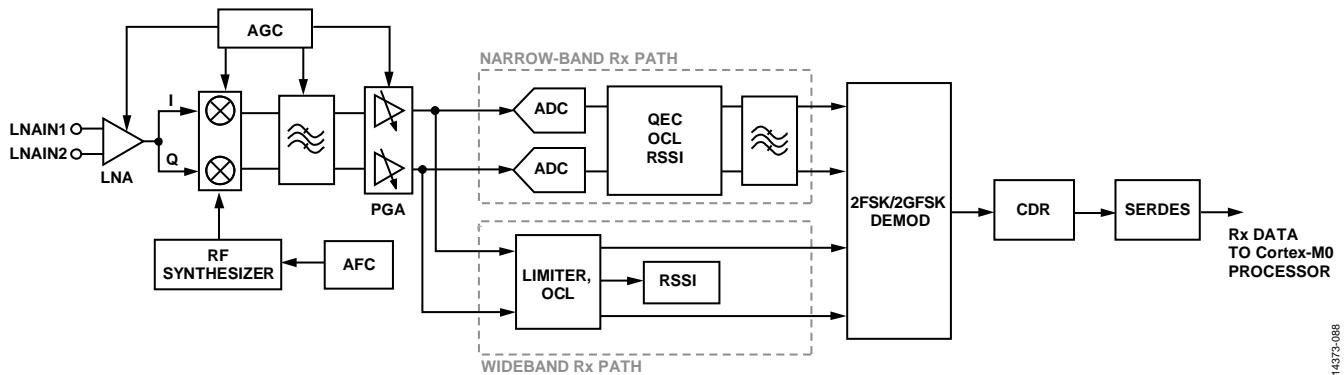


Figure 82. Receiver Block Diagram

Table 27 and Table 28 list the supported channel bandwidths and IF frequencies. The ADF7030-1 graphic user interface (GUI) automatically chooses the correct receive path, channel bandwidth, and IF frequency based on the data rate and modulation settings.

Table 27. Narrow-Band Rx Path Channel Bandwidths and IFs

| Channel Bandwidth (kHz) | IF (kHz) |
|-------------------------|----------|
| 2.6 | 81.25 |
| 3.0 | 81.25 |
| 3.2 | 81.25 |
| 3.4 | 81.25 |
| 3.7 | 81.25 |
| 3.9 | 81.25 |
| 4.2 | 81.25 |
| 4.4 | 81.25 |
| 4.7 | 81.25 |
| 5.1 | 81.25 |
| 5.4 | 81.25 |
| 5.8 | 81.25 |
| 6.2 | 81.25 |
| 6.6 | 81.25 |
| 7.0 | 81.25 |
| 7.5 | 81.25 |
| 8.1 | 81.25 |
| 8.5 | 81.25 |
| 8.7 | 81.25 |
| 9.1 | 81.25 |
| 9.7 | 81.25 |
| 10.4 | 81.25 |
| 10.6 | 81.25 |
| 11.1 | 81.25 |
| 11.7 | 81.25 |
| 11.9 | 81.25 |
| 12.7 | 81.25 |
| 13.5 | 81.25 |
| 14.4 | 81.25 |
| 15.4 | 81.25 |
| 16.4 | 81.25 |
| 17.6 | 81.25 |
| 18.7 | 81.25 |
| 20.0 | 81.25 |

Table 28. Wideband Rx Path Channel Bandwidths and IFs

| Channel Bandwidth (kHz) | IF (kHz) |
|-------------------------|----------|
| 77.38 | 103.17 |
| 82.63 | 110.17 |
| 101.57 | 135.42 |
| 121.88 | 162.50 |
| 135.42 | 180.55 |
| 147.73 | 196.97 |
| 162.50 | 216.67 |
| 180.56 | 240.74 |
| 203.12 | 270.83 |
| 221.59 | 295.45 |
| 243.75 | 325.00 |
| 270.83 | 361.11 |
| 353.00 | 361.11 |
| 395.00 | 406.25 |
| 406.25 | 433.33 |

AGC

AGC is enabled by default and keeps the receiver gain at the correct level by selecting the LNA, mixer, and filter gain settings based on the measured RSSI level.

AFC

The ADF7030-1 features an internal real-time automatic frequency control loop. In receive mode, the control loop automatically monitors the frequency error during the packet preamble sequence and adjusts the receiver synthesizer local oscillator. AFC is supported without the need for any additional preamble bits in the received packet.

Baseband Processing

The demodulator is based on a digital frequency correlator that performs filtering and frequency discrimination of the 2FSK/2GFSK spectrum. Following the demodulator is an oversampled digital clock and data recovery (CDR) phase-locked loop (PLL) that resynchronizes the received bit stream to a local clock in all modulation modes. A serializer/deserializer (SERDES) block processes the received bit stream, carries out pattern matching, and produces the byte sized data for the ARM Cortex-M0 processor.

14373-088

The ARM Cortex-M0 processor performs all of the byte level packet processing and packet management.

Received Signal Strength Indicator (RSSI)

The ADF7030-1 supports accurate measurement of the received signal strength. To achieve the calibrated absolute accuracy specification, a one-point factory calibration is required (see the Radio System Calibration section). The ADF7030-1 measures the RSSI during packet reception and the value is stored in a register for access by the host processor. The RSSI measurement is also used during CCA, where the RSSI measurement is evaluated against a user set threshold. The RSSI is reported in dBm.

TRANSMITTER

The ADF7030-1 transmitter supports 2FSK/2GFSK, 4FSK/4GFSK, and OOK modulation. It comprises a high performance PLL synthesizer and power efficient dual PAs. A block diagram of the ADF7030-1 transmitter architecture is shown in Figure 83. All blocks are fully integrated.

Synthesizer and VCO

An integrated, low noise PLL synthesizer and VCO generate both the transmit signal and the receiver LO signal.

The synthesizer loop filter has a programmable bandwidth. Upon entering the PHY_RX state, the ADF7030-1 sets a narrow bandwidth to ensure optimum receiver rejection. In the PHY_TX state, the bandwidth is chosen to ensure optimum modulation quality.

A high speed, fully automatic calibration scheme ensures that the VCO performance is maintained over temperature, supply voltage, and process variations. The calibration is automatically performed when the CMD_PHY_RX or CMD_PHY_TX command is issued.

Power Amplifiers

The ADF7030-1 has two integrated power amplifiers. PA1 and PA2 are designed for optimum power consumption performance at 13 dBm and 17 dBm, respectively. The PAs cannot be operated simultaneously. The user selects the appropriate PA for their specific system. The power amplifiers are implemented as Class F type amplifiers.

For systems where very fine power control is required, a PA microsetting can be used to achieve 0.1 dB of resolution across the power range. To reduce spectral splatter when the PA is turning on and off, a programmable PA ramp is provided.

Transmit Modulation Schemes

The ADF7030-1 supports 2FSK/2GFSK and 4FSK/4GFSK modulation in transmit mode. In 2FSK/2GFSK mode, a binary zero value generates a frequency deviation tone, $-f_{DEV}$. A binary one generates a $+f_{DEV}$ tone. In 4FSK/4GFSK, the symbol mapping is configurable.

OOK modulation is also supported in transmit mode at a data rate of 16.384 kbps.

Transmit Filtering

The ADF7030-1 supports Gaussian filtering in both 2FSK and 4FSK mode. Gaussian filtering reduces the occupied bandwidth of the signal by digitally prefiltering the transmit data. The BT factors are configurable with the following options: 0.5, 0.4, 0.35, or 0.3. Reducing BT increases the roll-off factor of the filter resulting in a narrower signal bandwidth. As BT is reduced, intersymbol interference is introduced, which affects the receiver sensitivity performance.

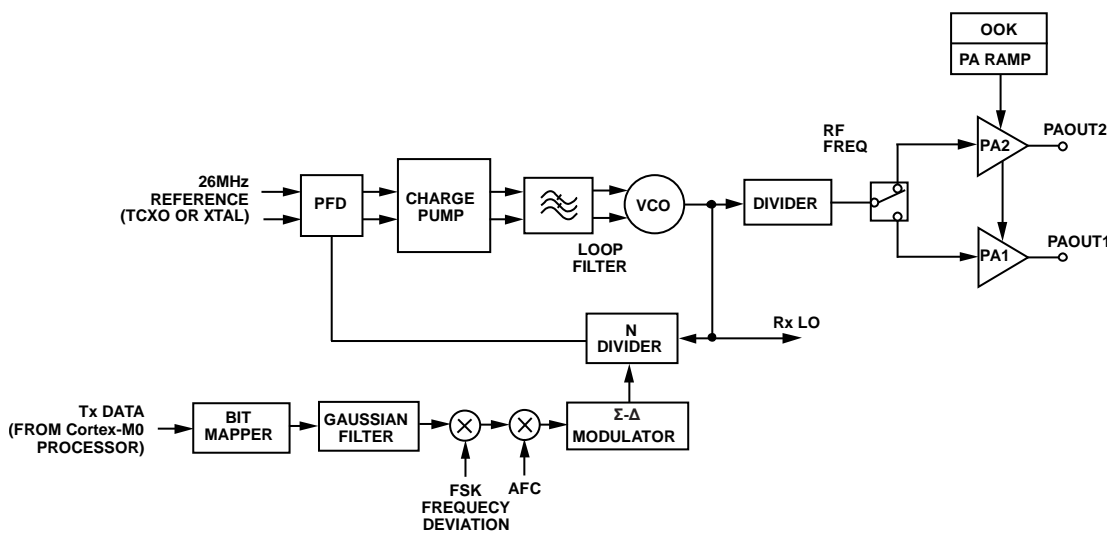


Figure 83. Transmitter Block Diagram

CALIBRATION

Table 29 provides an overview of the calibrations associated with the [ADF7030-1](#) and when to run calibrations.

Radio System Calibration

To ensure that the [ADF7030-1](#) radio performance meets the data sheet specifications, it is necessary to perform a one-time radio system calibration at $25^{\circ}\text{C} \pm 10^{\circ}\text{C}$.

The radio system calibration routine is provided as a firmware module, `OffLineCalibrations.cfg`, that the host processor must download to the [ADF7030-1](#) memory. The firmware module is available as part of the [ADF7030-1](#) design package. The calibration is fully autonomous when initiated by the `CMD_DO_CAL` command.

The radio system calibration firmware module can be downloaded to the [ADF7030-1](#) and run as part of a factory calibration procedure and the calibration data stored on the host processor as part of the configuration settings for the [ADF7030-1](#). Calibration data is maintained in `PHY_SLEEP` if memory retention is enabled. If the memory is not retained, the host processor must replay the calibration data to the [ADF7030-1](#). Refer to the [ADF7030-1 Software Reference Manual](#) for further details on downloading and using firmware modules with the [ADF7030-1](#).

In the Field Radio System Calibration

The only receiver performance metric that benefits appreciably from a recalibration over temperature, is the image rejection. In applications where image rejection performance is critical over temperature, it may be necessary to perform a recalibration as the temperature changes.

If the application requires the calibration to be performed in the field (in addition to the one-time factory calibration), it is important to consider interferer signals during calibration, because

the calibration uses internally generated RF signals to perform certain aspects of the receiver calibration. If an interferer signal is present on the RF input of the [ADF7030-1](#) during calibration, this signal can degrade the calibration performance. The consequence of a degraded calibration is a reduction in the image rejection performance of the receiver.

If the application uses an external switch, the switch can be used to provide extra isolation between the antenna and the RF input of the [ADF7030-1](#) during calibration.

26 kHz RC Oscillator Calibration

To ensure that the 26 kHz RC oscillator meets the calibrated frequency accuracy specification, it is necessary to perform a calibration. During calibration, the `OffLineCalibrations.cfg` firmware module must be downloaded to the [ADF7030-1](#). The calibration is fully autonomous when initiated by the `CMD_LFRC_CAL` command. Refer to the [ADF7030-1 Software Reference Manual](#) for further details.

RSSI Offset Calibration

To ensure that the [ADF7030-1](#) RSSI performance meets the calibrated RSSI data sheet specifications, it is necessary to perform a measurement of the [ADF7030-1](#) RSSI measurement offset.

The offset can be measured as part of a factory calibration procedure where an RF signal source applies a signal to the receiver input while the [ADF7030-1](#) is in the continuous CCA state. The offset between the applied signal power and the [ADF7030-1](#) RSSI result is stored on the host processor as part of the configuration settings for the [ADF7030-1](#). The [ADF7030-1](#) has allocated registers for the RSSI offset, and the [ADF7030-1](#) automatically applies these offsets to the RSSI measurement result returned over the SPI. Refer to the [ADF7030-1 Software Reference Manual](#) for further details on the RSSI offset calibration procedure and the RSSI offset registers.

Table 29. ADF7030-1 Calibrations

| Calibration | Description | When to Run this Calibration | Firmware Module Required | Radio Command | Typical Calibration Time (ms) |
|----------------------|--|--|--|---------------------------|-------------------------------|
| Radio System | Calibration of the radio system | A one-time calibration is required to meet the data sheet specifications. This calibration can be performed as part of a factory calibration of the end product. | The <code>OffLineCalibrations.cfg</code> firmware module must be downloaded to the ADF7030-1 . | <code>CMD_DO_CAL</code> | 660 |
| 26 kHz RC Oscillator | Frequency calibration of the internal 26 kHz RC oscillator | A frequency calibration of the 26 kHz RC oscillator is required to meet the typical frequency accuracy specification. Depending on the frequency accuracy requirements of the application, it may also be necessary to calibrate as the temperature changes. Refer to Table 17 for specifications. | The <code>OffLineCalibrations.cfg</code> firmware module must be downloaded to the ADF7030-1 . | <code>CMD_LFRC_CAL</code> | 30 |
| RSSI Offset | A single point, one-time, offset calibration of the RSSI | A single-point, one-time, RSSI offset calibration is required to meet the RSSI accuracy specification of Table 3. This calibration can be performed as part of a factory calibration of the end product. | None required. | Not applicable | Not applicable |

PACKET HANDLING

The ADF7030-1 includes comprehensive transmit and receive packet management capabilities and can be configured for use with a wide variety of packet-based radio protocols.

IEEE 802.15.4g Packet Mode

The ADF7030-1 supports the multirate frequency shift keying (MR-FSK) PHY 802.15.4g specified packet format in the IEEE 802.15.4g-2012 standard with FEC, whitening, and interleaving at data rates of up to 150 kbps.

Generic Packet Mode

The ADF7030-1 supports a wide variety of packet formats via its fully flexible generic packet format. In generic packet transmit mode, the ADF7030-1 can be configured to add the preamble, sync word, and cyclic redundancy check (CRC) to the payload data stored in the packet memory. The number of preamble bits and sync bits is programmable, and an optional length field can be added to allow packet length decoding at the receiver. The CRC polynomial and length are fully programmable in generic packet mode.

Transmitting and Receiving packets

The ADF7030-1 can be programmed to transmit and receive variable and fixed length payloads. The packet data to be transmitted must be written by the host into the ADF7030-1 internal memory. 511 bytes of dedicated RAM are available to store, transmit, and receive packets. For payload lengths greater than 511 bytes, the ADF7030-1 provides a rolling buffer mode.

To transmit or receive a packet, the host processor must first configure the ADF7030-1. Then, the host processor issues the commands to place the ADF7030-1 into the PHY_RX state or the PHY_TX state. After either state is entered, the ADF7030-1 automatically starts transmitting or receiving a packet.

In transmit mode, a preamble, sync word, and CRC can be added by the ADF7030-1 to the payload data stored in the RAM. In receive mode, the ADF7030-1 can qualify received packets based on preamble detection, sync word detection, or CRC validation. When the ADF7030-1 receives a valid packet, the received payload data is loaded to packet memory.

The host can track the progress of the transmission or reception of a packet by monitoring the interrupt signals coming from the ADF7030-1. There are two independent logical interrupts from the ADF7030-1, and events can be configured to trigger one or both of these logical interrupts.

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

A typical application circuit is shown in Figure 84. Refer to the [ADF7030-1 Hardware Reference Manual](#) for a comprehensive

guide on application circuits, external hardware requirements, and RF matching for the [ADF7030-1](#).

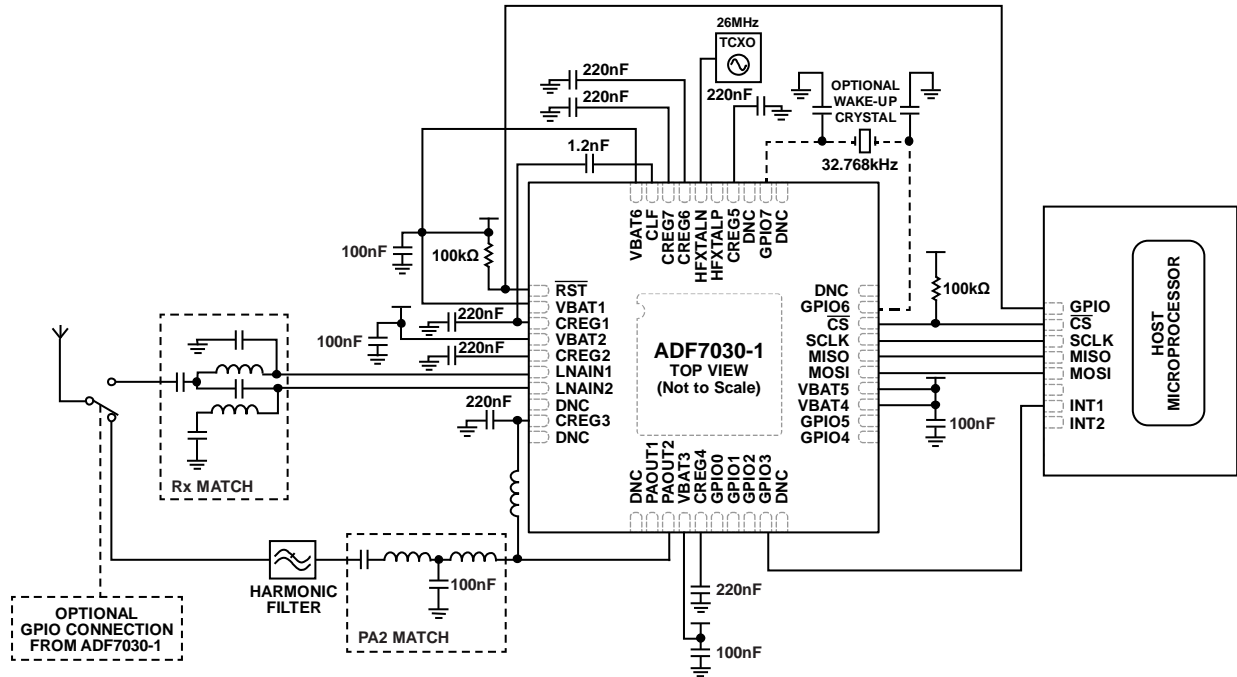


Figure 84. Typical Application Circuit with External Switch and TCXO Reference

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SILICON ANOMALY

This anomaly list describes the known bugs, anomalies, and workarounds for the [ADF7030-1](#).

Analog Devices, Inc., is committed, through future silicon revisions and/or firmware module revisions, to continuously improve functionality. Analog Devices tries to ensure that these future revisions of the [ADF7030-1](#) silicon or firmware modules remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

The silicon revision information can be electronically determined by reading the PART_ID and ROM_ID fields from the [ADF7030-1](#) memory locations described in Table 30.

Table 30. Silicon Revision ID

| IF Field | Length (Bytes) | Memory Address |
|----------|----------------|----------------|
| PART_ID | 2 | 0x00007FF6 |
| ROM_ID | 1 | 0x00007FF9 |

ADF7030-1 FUNCTIONALITY ISSUES

| Silicon Revision ID | Chip Marking | Silicon Status | No. of Reported Anomalies |
|---------------------------------|----------------------------------|----------------|---------------------------|
| PART_ID = 0x0602, ROM_ID = 0x02 | ADF7030-1BCPZN or ADF7030-1BSTZN | Release | 2 |

FUNCTIONALITY ISSUES

Table 31. Short Transmit Pulse Preceding Packet preamble on OOK Transmit [er001]

| | |
|-----------------------|--|
| Background | In OOK transmit, a preamble sequence with the length controlled by PREAMBLE_LEN in the GENERIC_PKT_FRAME_CFG0 register is transmitted at the start of a packet. |
| Issue | The first OOK transmit packet after a reset event or cold start has the correct preamble sequence. Subsequent OOK transmit packets prepend a short transmit pulse with a duration of less than one bit, before the preamble sequence. The output power of the pulse is at the configured output power. |
| Workaround | None. |
| Related Issues | None. |

Table 32. CCA After Aborting PHY_TX During Packet Transmission for Data Rates < 3.064 kbps [er002]

| | |
|-----------------------|--|
| Background | The host processor can abort a transmission by issuing any radio command while the ADF7030-1 is in the PHY_TX state. |
| Issue | For data rates < 3.064 kbps, the first CCA operation is inoperative after aborting a transmission. |
| Workaround | After aborting a transmission, enter the CCA state twice. On the first CCA entry, CCA is inoperative. On the second and subsequent entries to the CCA state, CCA is fully operational. |
| Related Issues | None. |

Section 1. [ADF7030-1](#) Functionality Issues

| Reference Number | Description | Status |
|------------------|--|--------|
| er001 | Short transmit pulse preceding packet preamble on OOK transmit | Open |
| er002 | CCA after aborting PHY_TX during packet transmission for data rates < 3.064 kbps | Open |

This completes the Silicon Anomaly section.

DEVELOPMENT SUPPORT

DESIGN PACKAGE

The [ADF7030-1](#) design resource package is a complete documentation and resource package for the [ADF7030-1](#). It is recommended to download this package as a starting point for evaluation and development from the [ADF7030-1](#) product page. It contains manuals, application notes, hardware information, and firmware modules.

REFERENCE MANUALS

[ADF7030-1 Software Reference Manual \(UG-1002\)](#)

The [ADF7030-1 Software Reference Manual](#) is the detailed programming guide for the device. The [ADF7030-1](#) hardware reference manual provides a description of the [ADF7030-1](#) hardware features and application circuit requirements.

[ADF7030-1 Hardware Reference Manual \(UG-957\)](#)

The [ADF7030-1 Hardware Reference Manual](#) provides a description of the [ADF7030-1](#) radio functionality, hardware features, and application circuit requirements. It is intended as a resource for a hardware engineer designing a printed circuit board (PCB) that includes the [ADF7030-1](#).

EVALUATION KITS

Evaluation and development kits are available that include the [ADF7030-1](#) radio daughter boards. The [ADF7030-1 EZ-KIT](#)[®] is an evaluation and development system for the [ADF7030-1](#) high performance, sub GHz, RF transceiver, and includes four models. These kits are listed in Table 33.

Table 33. ADF7030-1 EZ-KIT Models

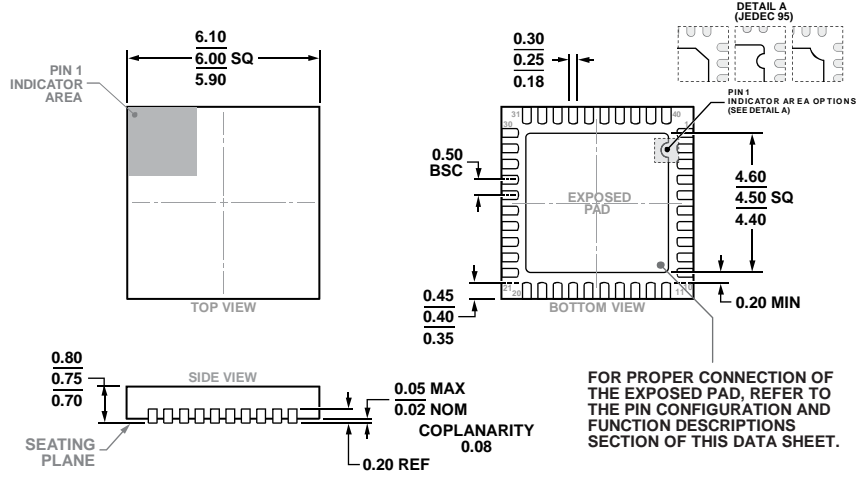
| Model | Frequency (MHz) |
|-----------------------------------|-----------------|
| ADF70301-915EZKIT | 902 to 928 |
| ADF70301-868EZKIT | 863 to 876 |
| ADF70301-433EZKIT | 433 to 434 |
| ADF70301-169EZKIT | 169 |

A selection of individual daughter boards is also available covering various frequency bands and matching topologies.

EVALUATION SOFTWARE

The [ADF7030-1](#) design center is a graphical user interface (GUI) that can be used for configuring the [ADF7030-1](#), evaluating transmit and receive operation, and transmitting and receiving packets. This [ADF7030-1](#) design center allows the user to rapidly prototype different configurations with the [ADF7030-1](#) and simplifies the migration to host code development.

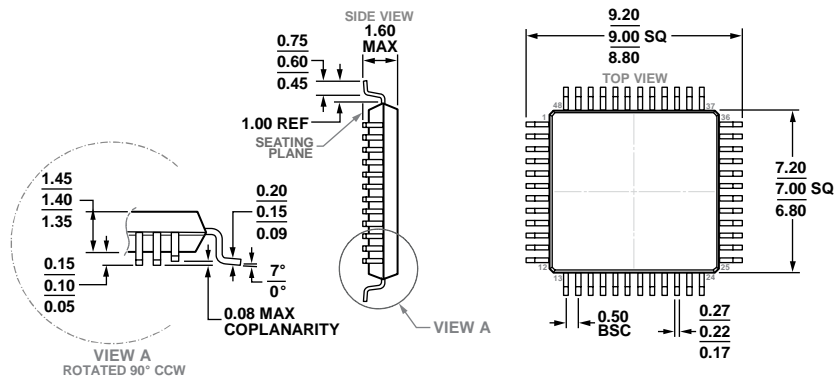
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD-5

Figure 85. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.75 mm Package Height
(CP-40-17)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 86. 48-Lead Low Profile Quad Flat Package [LQFP]
7 mm × 7 mm Body
(ST-48)

Dimensions shown in millimeters