

FEATURES

- 1.5 Ω on resistance
- 0.3 Ω on-resistance flatness
- 0.1 Ω on-resistance match between channels
- Continuous current per channel
 - LFCSP: 250 mA
 - TSSOP: 190 mA
- Fully specified at +12 V, ± 15 V, and ± 5 V
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 16-lead TSSOP and 16-lead, 4 mm \times 4 mm LFCSP
- AEC-Q100 qualified for automotive applications

APPLICATIONS

- Automated test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Video signal routing
- Communications systems
- Relay replacement

GENERAL DESCRIPTION

The [ADG1411/ADG1412/ADG1413](#) are monolithic complementary metal-oxide semiconductor (CMOS) devices containing four independently selectable switches designed on an iCMOS[®] process. iCMOS (industrial CMOS) is a modular manufacturing process combining high voltage CMOS and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage devices has been able to achieve. Unlike analog ICs using conventional CMOS processes, iCMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The on-resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching signals.

iCMOS construction ensures ultralow power dissipation, making the devices ideally suited for portable and battery-powered instruments.

The [ADG1411/ADG1412/ADG1413](#) contain four independent single-pole/single-throw (SPST) switches. The [ADG1411](#) and

FUNCTIONAL BLOCK DIAGRAM

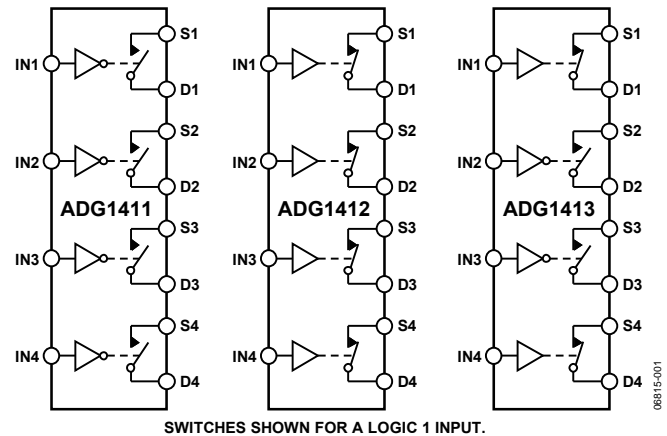


Figure 1.

[ADG1412](#) differ only in that the digital control logic is inverted. The [ADG1411](#) switches are turned on with Logic 0 on the appropriate control input, whereas the [ADG1412](#) switches are turned on with Logic 1. The [ADG1413](#) has two switches with digital control logic similar to that of the [ADG1411](#); the logic is inverted on the other two switches. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

The [ADG1413](#) exhibits break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection, which results in minimum transients when the digital inputs are switched.

PRODUCT HIGHLIGHTS

1. 2.6 Ω maximum on resistance over temperature.
2. Minimum distortion.
3. Ultralow power dissipation: <0.03 μ W.
4. 16-lead TSSOP and 16-lead, 4 mm \times 4 mm LFCSP.

Rev. D

Document Feedback

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REVISION HISTORY

1/2020—Rev. C to Rev. D

Change to Features Section	1
Changes to Leakage Currents Parameter, Table 1	3
Changes to Leakage Currents Parameter, Table 2	4
Changes to Leakage Currents Parameter, Table 3	5
Updated Outline Dimensions	15

3/2016—Rev. B to Rev. C

Changed CP-16-13 to CP-16-26	Throughout
Changes to Figure 2, Figure 3, and Table 5	7
Updated Outline Dimensions	15
Changes to Ordering Guide	16

3/2011—Rev. A to Rev. B

Changes to Features Section	1
Changes to Table 5, Added Exposed Pad Notation	3
Updated Outline Dimensions.....	15
Changes to Ordering Guide	40
Added Automotive Products Section	40

3/2009—Rev. 0 to Rev. A

Changes to Power Requirements, IDD, Digital Inputs = 5 V Parameter, Table 1	3
Changes to Power Requirements, IDD, Digital Inputs = 5 V Parameter Table 2	4

5/2008—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	1.5			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 23
	1.8	2.3	2.6	Ω max	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	0.18	0.19	0.21	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.3			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	0.36	0.4	0.45	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.03			nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
	± 0.55	± 2	± 12.5	nA max	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 24
ADG1411WBCPZ-REEL Only	± 3		± 40	nA max	
Drain Off Leakage, I_D (Off)	± 0.03			nA typ	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 24
	± 0.55	± 2	± 12.5	nA max	
ADG1411WBCPZ-REEL Only	± 3		± 40	nA max	
Channel On Leakage, I_D , I_S (On)	± 0.15			nA typ	$V_S = V_D = \pm 10\text{ V}$; see Figure 25
	± 2	± 4	± 30	nA max	
ADG1411WBCPZ-REEL Only	± 3		± 40	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS¹					
t_{ON}	100			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	150	170	190	ns max	$V_S = 10\text{ V}$; see Figure 30
t_{OFF}	90			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	120	140	160	ns max	$V_S = 10\text{ V}$; see Figure 30
Break-Before-Make Time Delay, t_D (ADG1413 Only)	25			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			10	ns min	$V_{S1} = V_{S2} = 10\text{ V}$; see Figure 31
Charge Injection, Q_{INJ}	-20			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32
Off Isolation	-80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 26
Channel-to-Channel Crosstalk	-100			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 27
Total Harmonic Distortion + Noise	0.014			% typ	$R_L = 110\ \Omega$, 15 V p-p , $f = 20\text{ Hz}$ to 20 kHz ; see Figure 29
-3 dB Bandwidth	170			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 28
Insertion Loss	-0.35			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28
C_S (Off)	23			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)	23			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D , C_S (On)	116			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001			μA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
			1	μA max	Digital inputs = 0 V or V_{DD}
I_{DD}	220			μA typ	Digital inputs = 5 V
			380	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			$\pm 4.5/\pm 16.5$	V min/V max	$GND = 0\text{ V}$

¹ Guaranteed by design; not subject to production test.

+12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	2.8 3.5	4.3	4.8	Ω typ Ω max	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 23 $V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.13			Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	0.21 0.6	0.23	0.25	Ω max Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$
	1.1	1.2	1.3	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.02 ± 0.55	± 2	± 12.5	nA typ nA max	$V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/0\text{ V}$; see Figure 24
ADG1411WBCPZ-REEL Only	± 3		± 40	nA max	
Drain Off Leakage, I_D (Off)	± 0.02 ± 0.55	± 2	± 12.5	nA typ nA max	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/0\text{ V}$; see Figure 24
ADG1411WBCPZ-REEL Only	± 3		± 40	nA max	
Channel On Leakage, I_D , I_S (On)	± 0.15 ± 1.5	± 4	± 30	nA typ nA max	$V_S = V_D = 1\text{ V}/10\text{ V}$; see Figure 25
ADG1411WBCPZ-REEL Only	± 3		± 40	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001		± 0.1	μA typ μA max	$V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS¹					
t_{ON}	170 250	295	330	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; see Figure 30
t_{OFF}	75 135	165	190	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; see Figure 30
Break-Before-Make Time Delay, t_D (ADG1413 Only)	100		40	ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
Charge Injection, Q_{INJ}	30			ns min pC typ	$V_{S1} = V_{S2} = 8\text{ V}$; see Figure 31 $V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32
Off Isolation	-80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 26
Channel-to-Channel Crosstalk	-100			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 27
-3 dB Bandwidth	130			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 28
Insertion Loss	-0.5			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28
C_S (Off)	38			pF typ	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)	40			pF typ	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$
C_D , C_S (On)	104			pF typ	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001 220		1 380	μA typ μA max μA max	$V_{DD} = 13.2\text{ V}$ Digital inputs = 0 V or V_{DD} Digital inputs = 5 V
V_{DD}			5/16.5	V min/V max	$GND = 0\text{ V}$, $V_{SS} = 0\text{ V}$

¹ Guaranteed by design; not subject to production test.

±5 V DUAL SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	3.3 4	4.9	5.4	Ω typ Ω max	$V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$; see Figure 23 $V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.13			Ω typ	$V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	0.22 0.9	0.23	0.25	Ω max Ω typ	$V_S = \pm 4.5\text{ V}$; $I_S = -10\text{ mA}$
	1.1	1.24	1.31	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.03 ± 0.55	± 2	± 12.5	nA typ nA max	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ $V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 24
ADG1411WBCPZ-REEL Only	± 3		± 40	nA max	
Drain Off Leakage, I_D (Off)	± 0.03 ± 0.55	± 2	± 12.5	nA typ nA max	$V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 24
ADG1411WBCPZ-REEL Only	± 3		± 40	nA max	
Channel On Leakage, I_D , I_S (On)	± 0.05 ± 1.0	± 4	± 30	nA typ nA max	$V_S = V_D = \pm 4.5\text{ V}$; see Figure 25
ADG1411WBCPZ-REEL Only1	± 3		± 40	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001		± 0.1	μA typ μA max	$V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS¹					
t_{ON}	275 400	465	510	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$; see Figure 30
t_{OFF}	175 290	320	380	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$; see Figure 30
Break-Before-Make Time Delay, t_D (ADG1413 Only)	100		50	ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
Charge Injection, Q_{INJ}	30			ns min pC typ	$V_{S1} = V_{S2} = 3\text{ V}$; see Figure 31 $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32
Off Isolation	-80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 26
Channel-to-Channel Crosstalk	-100			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 27
Total Harmonic Distortion + Noise	0.03			% typ	$R_L = 110\ \Omega$, 5 V p-p , $f = 20\text{ Hz to } 20\text{ kHz}$; see Figure 29
-3 dB Bandwidth	130			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 28
Insertion Loss	-0.5			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28
C_S (Off)	32			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)	33			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D , C_S (On)	116			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001		1.0	μA typ μA max	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ Digital inputs = 0 V or V_{DD}
I_{SS}	0.001		1.0	μA typ μA max	Digital inputs = 0 V or V_{DD}
V_{DD}/V_{SS}			$\pm 4.5/\pm 16.5$	V min/V max	$GND = 0\text{ V}$

¹ Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	-0.3 V to +25 V
V_{SS} to GND	+0.3 V to -25 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ¹	GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins	500 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current per Channel at 25°C	
16-Lead TSSOP	190 mA
16-Lead LFCSP	250 mA
Continuous Current per Channel at 125°C	
16-Lead TSSOP	90 mA
16-Lead LFCSP	100 mA
Operating Temperature Range	
Automotive (Y Version)	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
16-Lead TSSOP (4-Layer Board)	112°C/W
16-Lead LFCSP	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/-5)°C

¹ Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

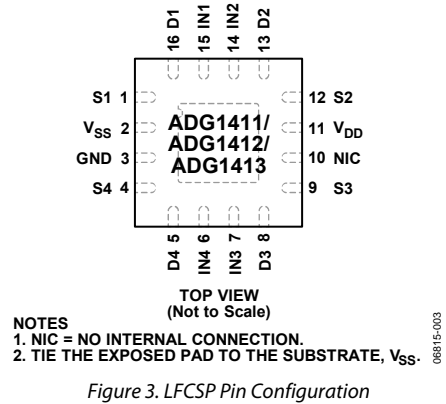
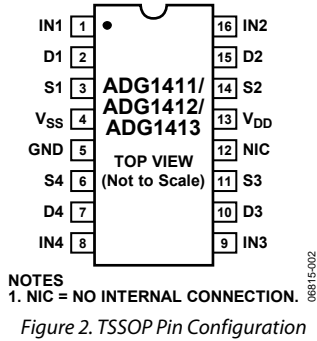


Table 5. Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	15	IN1	Logic Control Input.
2	16	D1	Drain Terminal. This pin can be an input or output.
3	1	S1	Source Terminal. This pin can be an input or output.
4	2	VSS	Most Negative Power Supply Potential.
5	3	GND	Ground (0 V) Reference.
6	4	S4	Source Terminal. This pin can be an input or output.
7	5	D4	Drain Terminal. This pin can be an input or output.
8	6	IN4	Logic Control Input.
9	7	IN3	Logic Control Input.
10	8	D3	Drain Terminal. This pin can be an input or output.
11	9	S3	Source Terminal. This pin can be an input or output.
12	10	NIC	No Internal Connection.
13	11	VDD	Most Positive Power Supply Potential.
14	12	S2	Source Terminal. This pin can be an input or output.
15	13	D2	Drain Terminal. This pin can be an input or output.
16	14	IN2	Logic Control Input.
N/A ¹	0	EPAD	Exposed Pad. Tie the exposed pad to the substrate, VSS.

¹ N/A means not applicable.

Table 6. ADG1411/ADG1412 Truth Table

ADG1411 INx	ADG1412 INx	Switch Condition
0	1	On
1	0	Off

Table 7. ADG1413 Truth Table

ADG1413 INx	S1, S4	S2, S3
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

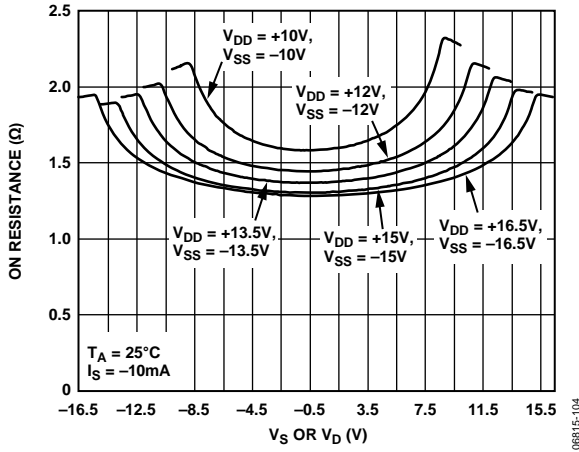


Figure 4. On Resistance vs. V_D or V_S, Dual Supply

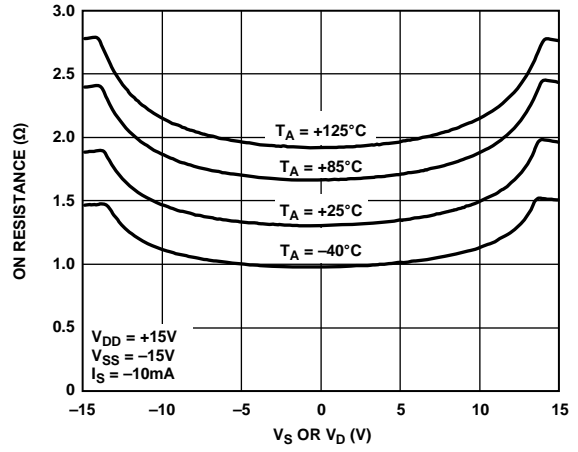


Figure 7. On Resistance vs. V_D or V_S for Different Temperatures, ±15 V Dual Supply

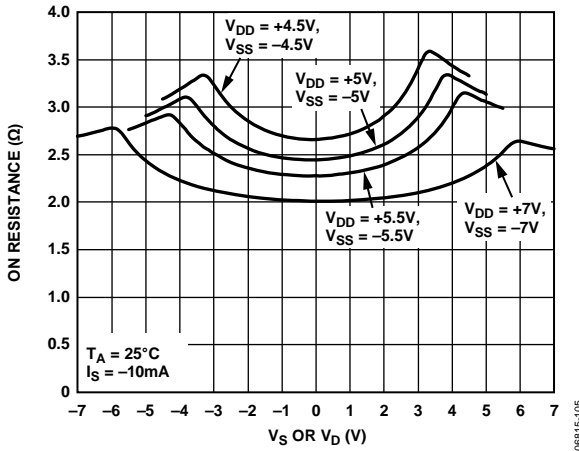


Figure 5. On Resistance vs. V_D or V_S, Dual Supply

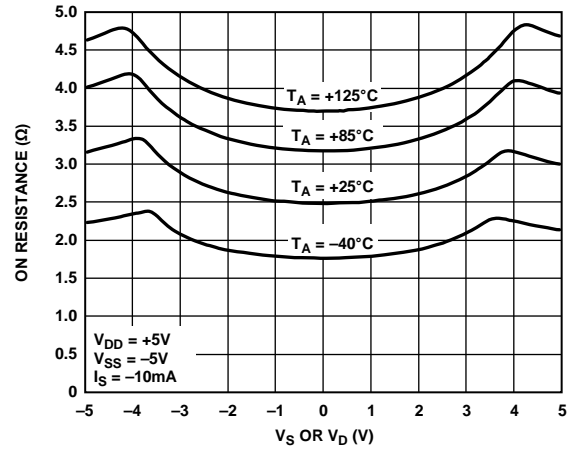


Figure 8. On Resistance vs. V_D or V_S for Different Temperatures, ±5 V Dual Supply

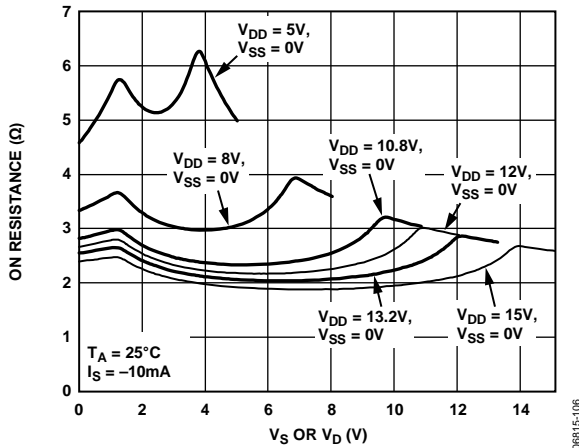


Figure 6. On Resistance vs. V_D or V_S, Single Supply

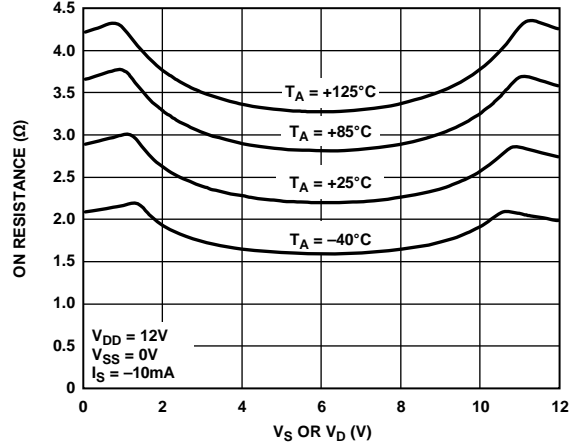


Figure 9. On Resistance vs. V_D or V_S for Different Temperatures, +12 V Single Supply

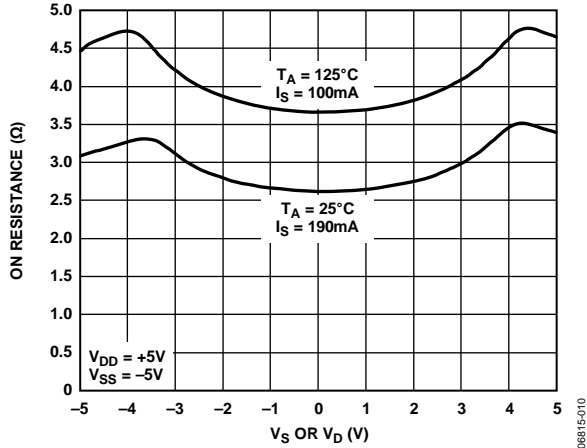


Figure 10. On Resistance vs. V_D or V_S for Different Current Levels, ± 5 V Dual Supply

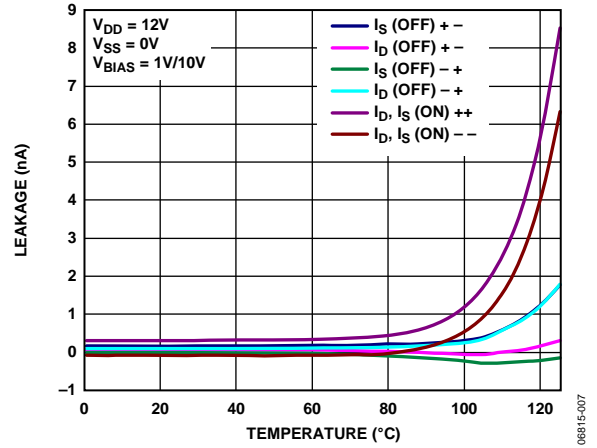


Figure 13. Leakage Currents vs. Temperature, +12V Single Supply

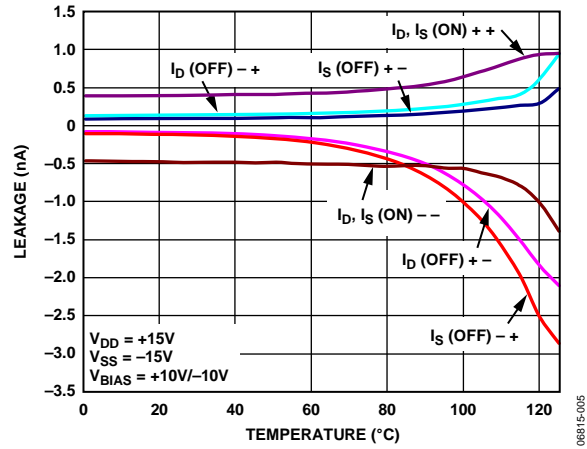


Figure 11. Leakage Currents vs. Temperature, ± 15 V Dual Supply

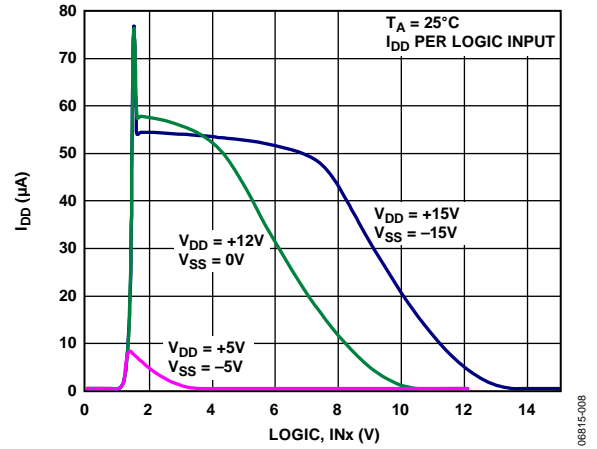


Figure 14. I_{DD} vs. Logic Level

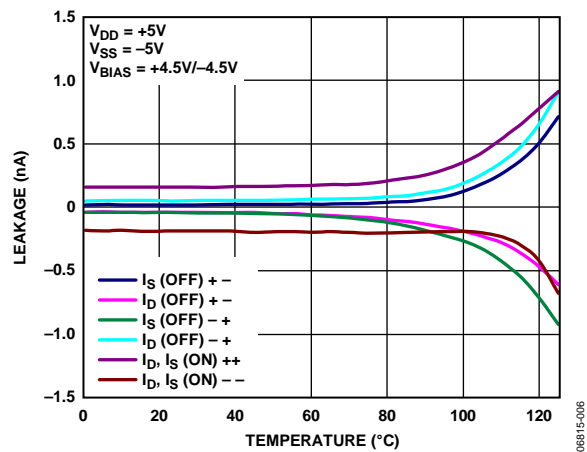


Figure 12. Leakage Currents vs. Temperature, ± 5 V Dual Supply

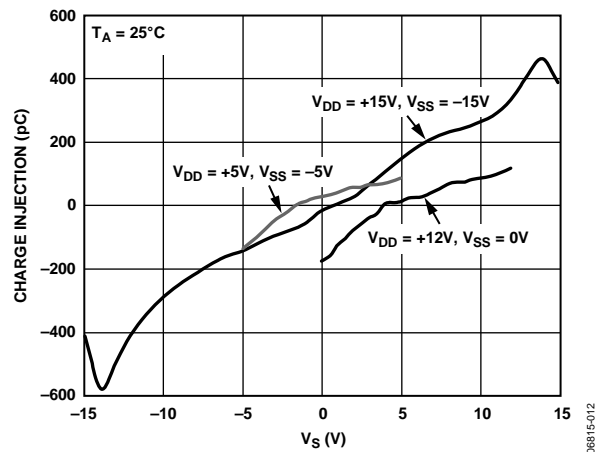


Figure 15. Charge Injection vs. Source Voltage

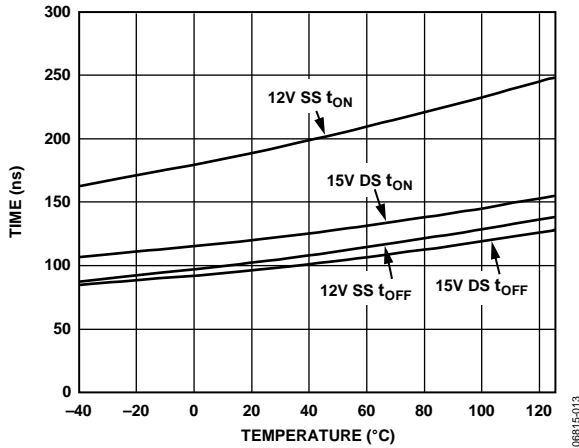


Figure 16. t_{ON}/t_{OFF} Times vs. Temperature for Single Supply (SS) and Dual Supply (DS)

06815-013

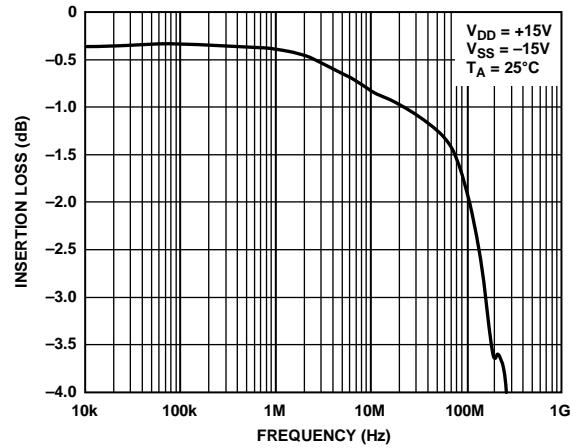


Figure 19. On Response vs. Frequency, ± 15 V Dual Supply

06815-016

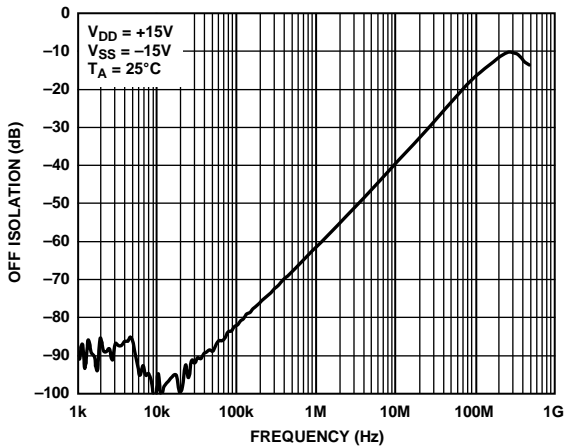


Figure 17. Off Isolation vs. Frequency, ± 15 V Dual Supply

06815-014

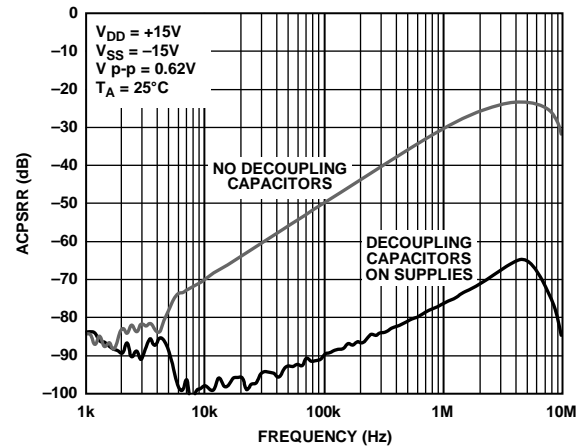


Figure 20. ACPSRR vs. Frequency, ± 15 V Dual Supply

06815-017

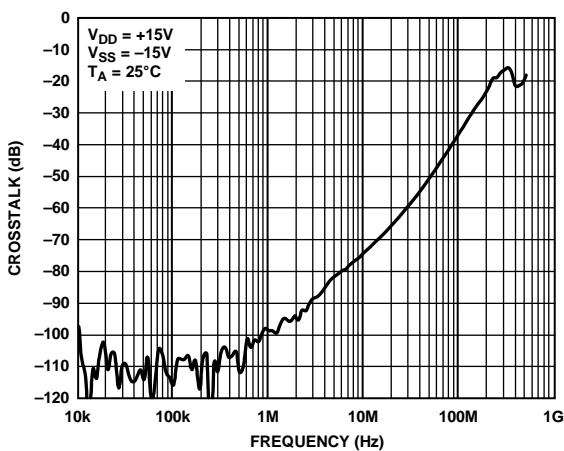


Figure 18. Crosstalk vs. Frequency, ± 15 V Dual Supply

06815-015

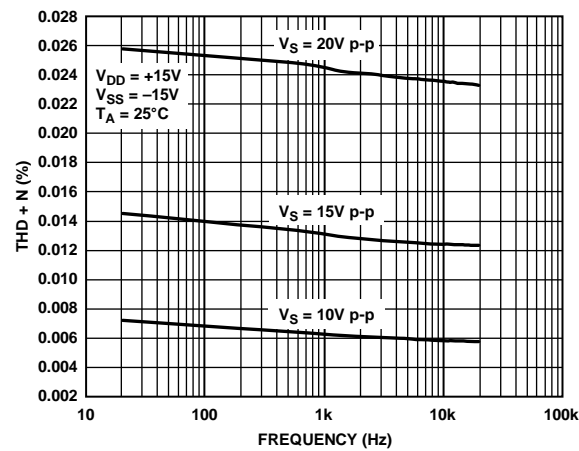


Figure 21. THD + N vs. Frequency, ± 15 V Dual Supply

06815-117

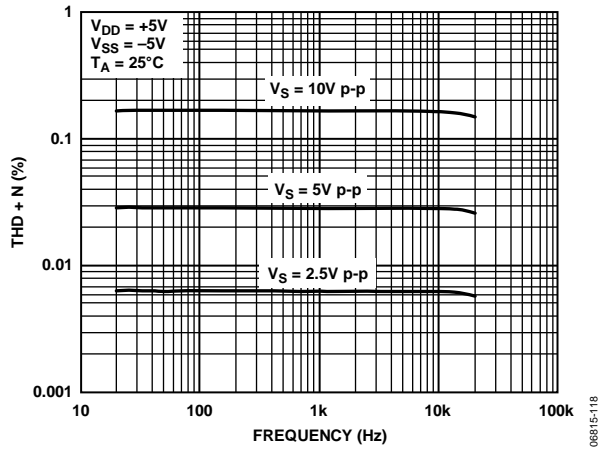


Figure 22. THD + N vs. Frequency, $\pm 5V$ Dual Supply

08815-118

TERMINOLOGY

I_{DD}

The positive supply current.

I_{SS}

The negative supply current.

V_D, V_S

The analog voltage on Terminal D and Terminal S.

R_{ON}

The ohmic resistance between Terminal D and Terminal S.

$R_{FLAT(ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)

The source leakage current with the switch off.

I_D (Off)

The drain leakage current with the switch off.

I_D, I_S (On)

The channel leakage current with the switch on.

V_{INL}

The maximum input voltage for Logic 0.

V_{INH}

The minimum input voltage for Logic 1.

I_{INL}, I_{INH}

The input current of the digital input when high or when low.

C_S (Off)

The off switch source capacitance, which is measured with reference to ground.

C_D (Off)

The off switch drain capacitance, which is measured with reference to ground.

C_D, C_S (On)

The on switch capacitance, which is measured with reference to ground.

C_{IN}

The digital input capacitance.

t_{ON}

The delay between applying the digital control input and the output switching on. See Figure 30.

t_{OFF}

The delay between applying the digital control input and the output switching off.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)

A measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of the signal on the output to the amplitude of the modulation is the ACPSRR.

TEST CIRCUITS

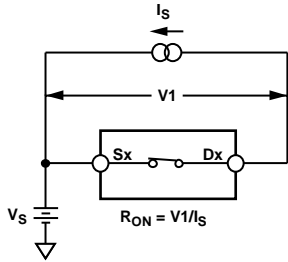


Figure 23. On Resistance

06815-020

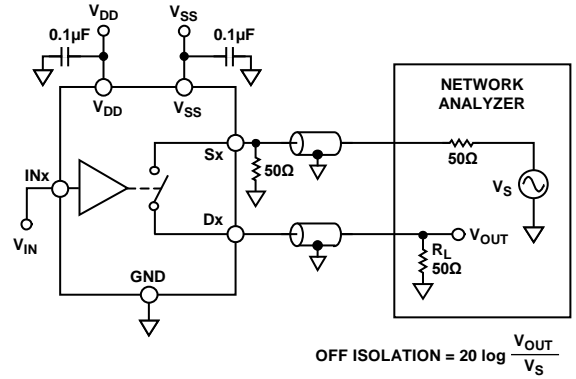


Figure 26. Off Isolation

06815-026

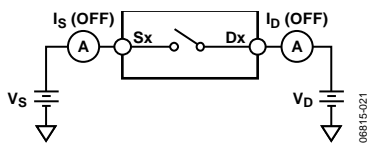


Figure 24. Off Leakage

06815-021

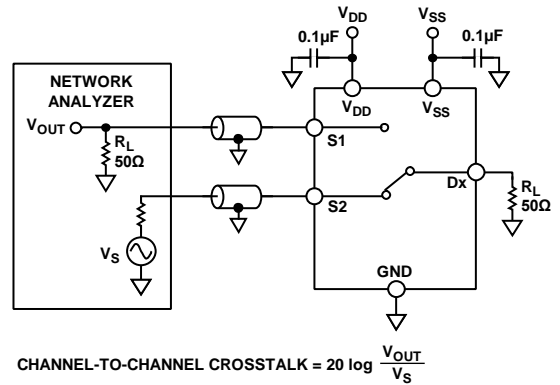


Figure 27. Channel-to-Channel Crosstalk

06815-027

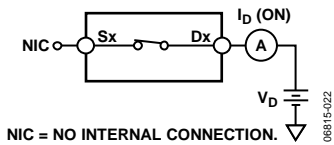


Figure 25. On Leakage

06815-022

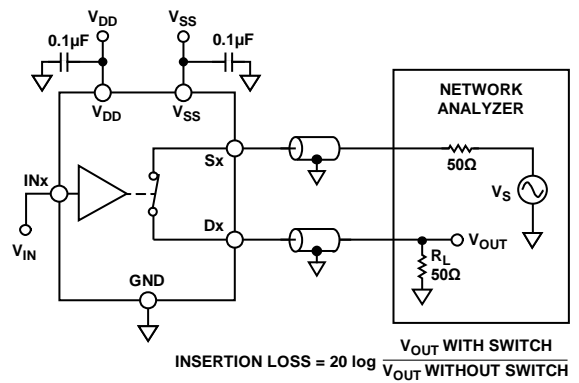


Figure 28. Bandwidth

06815-028

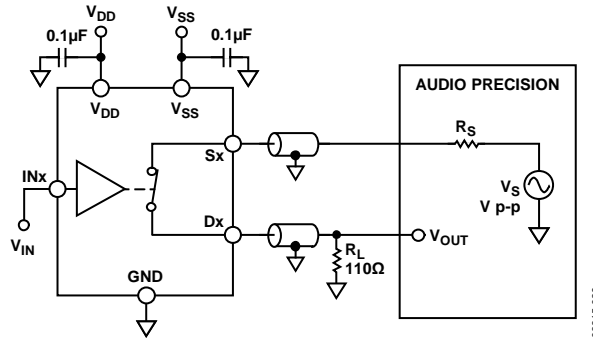


Figure 29. THD + Noise

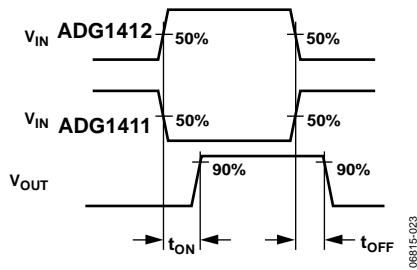
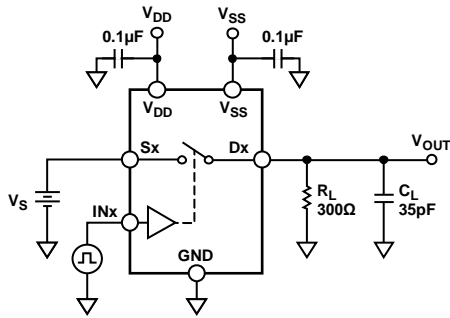


Figure 30. Switching Times

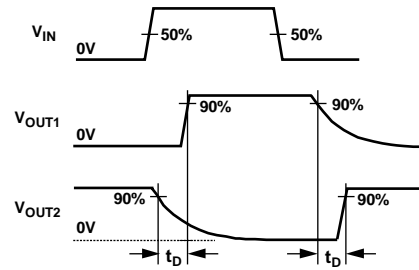
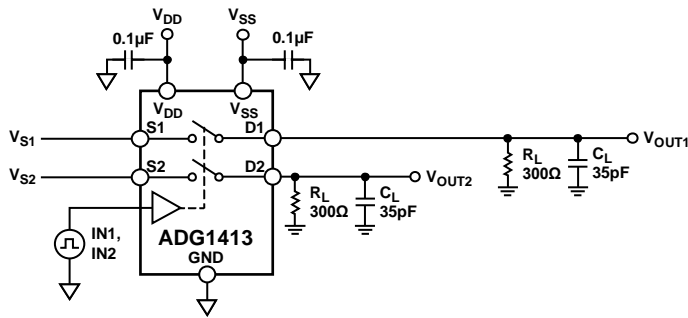


Figure 31. Break-Before-Make Time Delay

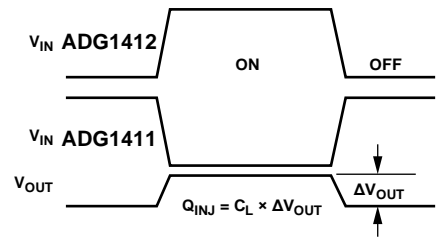
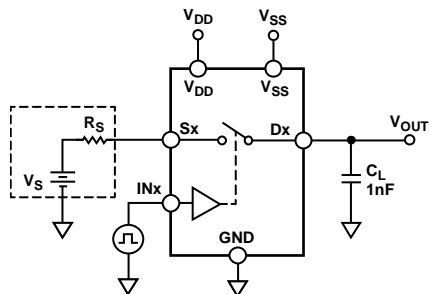
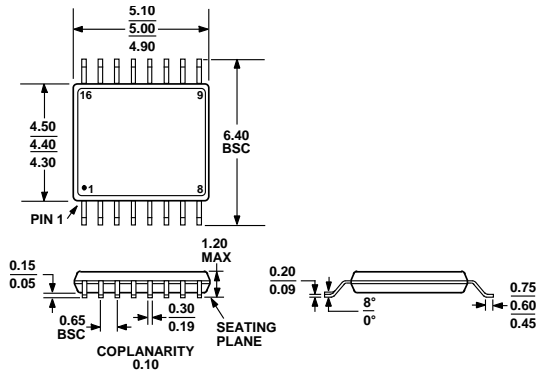


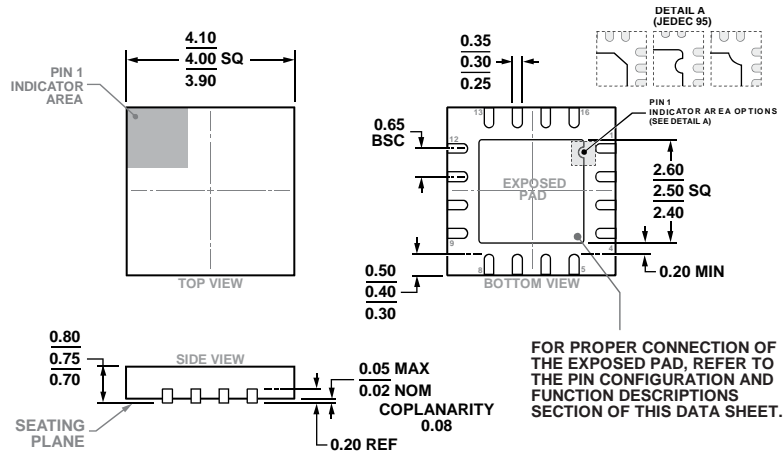
Figure 32. Charge Injection

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 33. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC-3

Figure 34. 16-Lead Lead Frame Chip Scale Package [LFCS] (CP-16-26)
4 mm x 4 mm Body and 0.75 mm Package Height
Dimensions shown in millimeters