



FEATURES

- 1.5 Ω on resistance
- 0.3 Ω on-resistance flatness
- 0.1 Ω on-resistance match between channels
- Continuous current per channel
 - LFCSP package: up to 400 mA
 - TSSOP package: up to 260 mA
- Fully specified at +12 V, ±15 V, and ±5 V
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 16-lead TSSOP and 4 mm × 4 mm, 16-lead LFCSP packages

APPLICATIONS

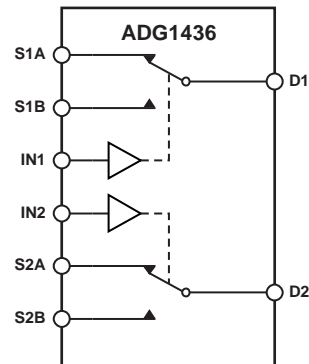
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Communication systems
- Relay replacement

GENERAL DESCRIPTION

The ADG1436 is a monolithic CMOS device containing two independently selectable SPDT switches. An EN input on the LFCSP package enables or disable the device. When disabled, all channels are switched off. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. Both switches exhibit break-before-make switching action for use in multiplexer applications.

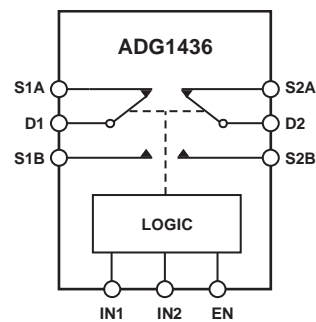
The ADG1436 is designed on an iCMOS® process. iCMOS (industrial-CMOS) is a modular manufacturing process combining high voltage CMOS (complementary metal-oxide semiconductor) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A ONE-INPUT LOGIC. 08817-001

Figure 1. TSSOP Package



SWITCHES SHOWN FOR A ONE-INPUT LOGIC. 08817-002

Figure 2. LFCSP Package

CMOS processes, iCMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The on-resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals. iCMOS construction ensures ultralow power dissipation, making the part ideally suited for portable and battery-powered instruments.

PRODUCT HIGHLIGHTS

1. 2.6 Ω maximum on resistance over temperature.
2. Minimum distortion.
3. Ultralow power dissipation: <0.03 μW.
4. 16-lead TSSOP and 16-lead 4 mm × 4 mm LFCSP packages.

Rev. B

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REVISION HISTORY

9/2016—Rev. A to Rev. B

Changes to Figure 4.....	8
Updated Outline Dimensions.....	16
Changes to Ordering Guide	16

3/2009—Rev. 0 to Rev. A

Change to I_{DD} Parameter, Table 1	3
Change to I_{DD} Parameter, Table 2	4

7/2008—Revision 0: Initial Version

SPECIFICATIONS

15 V DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	1.5			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 23
	1.8	2.3	2.6	Ω max	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
On-Resistance Match Between Channels (ΔR_{ON})	0.1			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	0.18	0.19	0.21	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.28			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	0.36	0.4	0.45	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.04			nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
	± 0.55	± 2	± 12.5	nA max	$V_S = \pm 10\text{ V}$, $V_D = \pm 10\text{ V}$; see Figure 24
Drain Off Leakage, I_D (Off)	± 0.04			nA typ	
	± 0.55	± 2	± 12.5	nA max	$V_S = \pm 10\text{ V}$, $V_D = \pm 10\text{ V}$; see Figure 24
Channel On Leakage, I_D , I_S (On)	± 0.1			nA typ	$V_S = V_D = \pm 10\text{ V}$; see Figure 25
	± 2	± 4	± 35	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	125			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	170	215	245	ns max	$V_S = +10\text{ V}$; see Figure 30
t_{ON} (EN)	95			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	120	140	155	ns max	$V_S = 10\text{ V}$; see Figure 30
t_{OFF} (EN)	105			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	130	150	170	ns max	$V_S = 10\text{ V}$; see Figure 30
Break-Before-Make Time Delay, t_{BBM}	20			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			10	ns min	$V_{S1} = V_{S2} = +10\text{ V}$; see Figure 31
Charge Injection	-20			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 33
Off Isolation	-80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 26
Channel-to-Channel Crosstalk	-80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 27
Total Harmonic Distortion + Noise	0.011			% typ	$R_L = 110\ \Omega$, 15 V p-p , $f = 20\text{ Hz to } 20\text{ kHz}$; see Figure 29
-3 dB Bandwidth	110			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 28
Insertion Loss	-0.18			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28
C_S (Off)	23			pF typ	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$
C_D (Off)	50			pF typ	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$
C_D , C_S (On)	120			pF typ	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$
POWER REQUIREMENTS					
I_{DD}	0.001			μA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
			1	μA max	Digital Inputs = 0 V or V_{DD}
I_{DD}	170			μA typ	Digital Input = 5 V
			285	μA max	
I_{SS}	0.001			μA typ	Digital Inputs = 0 V, 5 V, or V_{DD}
			1.0	μA max	
V_{DD}/V_{SS}			$\pm 4.5/\pm 16.5$	V min/max	GND = 0 V

¹ Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	2.8 3.5	4.3	4.8	Ω typ Ω max	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 23 $V_{DD} = +10.8\text{ V}$, $V_{SS} = 0\text{ V}$
On-Resistance Match Between Channels (ΔR_{ON})	0.13			Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.21 0.6	0.23	0.25	Ω max Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$
	1.1	1.2	1.3	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.04 ± 0.55	± 2	± 12.5	nA typ nA max	$V_{DD} = 13.2\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 24
Drain Off Leakage, I_D (Off)	± 0.04 ± 0.55	± 2	± 12.5	nA typ nA max	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 24
Channel On Leakage, I_D , I_S (On)	± 0.1 ± 1	± 4	± 35	nA typ nA max	$V_S = V_D = 1\text{ V or }10\text{ V}$; see Figure 25
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001		± 0.1	μA typ μA max	$V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	200 270	320	350	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; see Figure 30
t_{ON} (EN)	175 235	280	310	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; see Figure 30
t_{OFF} (EN)	105 145	175	195	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; see Figure 30
Break-Before-Make Time Delay, t_{BBM}	70		10	ns typ ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 8\text{ V}$; see Figure 31
Charge Injection	30			pC typ	$V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 33
Off Isolation	−80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 26;
Channel-to-Channel Crosstalk	−80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 27
−3 dB Bandwidth	78			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 28
Insertion Loss	−0.3			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28
C_S (Off)	40			pF typ	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$
C_D (Off)	80			pF typ	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$
C_D , C_S (On)	140			pF typ	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$
POWER REQUIREMENTS					
I_{DD}	0.001		1.0	μA typ μA max	$V_{DD} = 13.2\text{ V}$ Digital inputs = 0 V or V_{DD}
I_{DD}	170		285	μA typ μA max	Digital inputs = 5 V
V_{DD}			5/16.5	V min/max	$GND = 0\text{ V}$, $V_{SS} = 0\text{ V}$

¹ Guaranteed by design, not subject to production test.

5 V DUAL SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	3.3 4	4.9	5.4	Ω typ Ω max	$V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$; see Figure 23 $V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$
On-Resistance Match Between Channels (ΔR_{ON})	0.13			Ω typ	$V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.22	0.23	0.25	Ω max	$V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$
	0.9			Ω typ	
	1.1	1.24	1.31	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.03			nA typ	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ $V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 24
	± 0.2	± 1	± 12.5	nA max	
Drain Off Leakage, I_D (Off)	± 0.03			nA typ	$V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 24
	± 0.2	± 1	± 12.5	nA max	
Channel On Leakage, I_D , I_S (On)	± 0.05 ± 0.25	± 1 ± 1.5	± 12.5 ± 35	nA typ nA max	$V_S = V_D = \pm 4.5\text{ V}$; see Figure 25
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	$V_{IN} = V_{GND}$ or V_{DD}
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			μA typ μA max	
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	310 445	510	565	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$; see Figure 30
t_{ON} (EN)	255 355	415	460	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$; see Figure 30
t_{OFF} (EN)	215 305	355	400	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$; see Figure 30
Break-Before-Make Time Delay, t_{BBM}	80		10	ns typ ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 3\text{ V}$; see Figure 31
Charge Injection	30			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 33
Off Isolation	-80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 26
Channel-to-Channel Crosstalk	-80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 27
Total Harmonic Distortion + Noise	0.03			% typ	$R_L = 110\ \Omega$, 2.5 V pp , $f = 20\text{ Hz}$ to 20 kHz ; see Figure 29
-3 dB Bandwidth	85			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 28
Insertion Loss	-0.28			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28
C_S (Off)	33			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)	65			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D , C_S (On)	145			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001			μA typ	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ Digital inputs = 0 V or V_{DD}
			1.0	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
V_{DD}/V_{SS}			$\pm 4.5/\pm 16.5$	V min/max	$GND = 0\text{ V}$

¹ Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL

Table 4.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT PER CHANNEL ¹					
15 V Dual Supply					$V_{DD} = +13.5\text{ V}, V_{SS} = -13.5\text{ V}$
ADG1436 TSSOP	260	170	100	mA max	
ADG1436 LFCSP	400	250	120	mA max	
12 V Single Supply					$V_{DD} = 10.8\text{ V}, V_{SS} = 0\text{ V}$
ADG1436 TSSOP	240	160	100	mA max	
ADG1436 LFCSP	350	240	120	mA max	
5 V Dual Supply					$V_{DD} = +4.5\text{ V}, V_{SS} = -4.5\text{ V}$
ADG1436 TSSOP	240	160	100	mA max	
ADG1436 LFCSP	300	240	120	mA max	

¹ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 5.

Parameter	Ratings
V_{DD} to V_{SS}	35 V
V_{DD} to GND	-0.3 V to +25 V
V_{SS} to GND	+0.3 V to -25 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ¹	GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D	600 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current per Channel, S or D ²	Data + 15%
Operating Temperature Range Automotive (Y Version)	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θ_{JA} Thermal Impedance (4-Layer Board)	112°C/W
16-Lead LFCSP, θ_{JA} Thermal Impedance	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/-5)°C

¹ Over voltages at IN, S, and D are clamped by internal diodes. Current must be limited to the maximum ratings given.

² See data given in Table 4.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

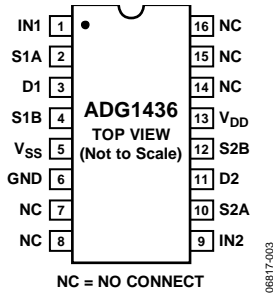
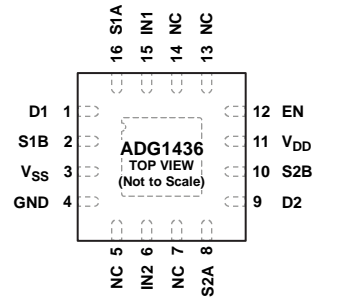


Figure 3. TSSOP Pin Configuration



NOTES
 1. EXPOSED PAD TIED TO SUBSTRATE, V_{SS}.
 2. NC = NO CONNECT.

Figure 4. LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.		Mnemonic	Function
TSSOP	LFCSP		
1	15	IN1	Logic Control Input.
2	16	S1A	Source Terminal. Can be an input or output.
3	1	D1	Drain Terminal. Can be an input or output.
4	2	S1B	Source Terminal. Can be an input or output.
5	3	V _{SS}	Most Negative Power Supply Potential.
6	4	GND	Ground (0 V) Reference.
7, 8, 14 to 16	5, 7, 13, 14	NC	No Connect.
9	6	IN2	Logic Control Input.
10	8	S2A	Source Terminal. Can be an input or output.
11	9	D2	Drain Terminal. Can be an input or output.
12	10	S2B	Source Terminal. Can be an input or output.
13	11	V _{DD}	Most Positive Power Supply Potential.
N/A	12	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, IN _x logic inputs determine the on switches.

TRUTH TABLE FOR SWITCHES

Table 7. ADG1436 TSSOP Truth Table

IN _x	S _x A	S _x B
0	Off	On
1	On	Off

Table 8. ADG1436 LFCSP Truth Table

EN	IN _x	S _x A	S _x B
0	X	Off	Off
1	0	Off	On
1	1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

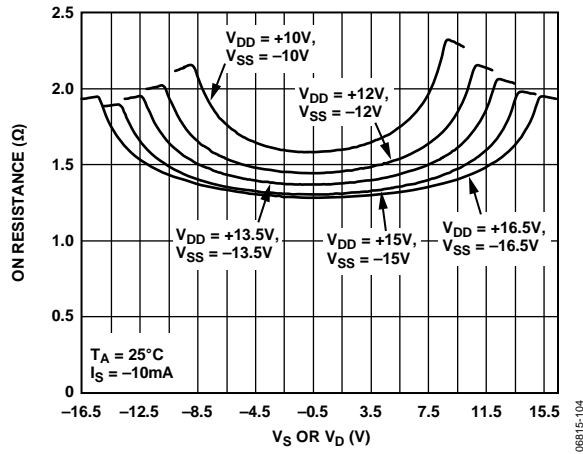


Figure 5. On Resistance vs. V_D or V_S , Dual Supply

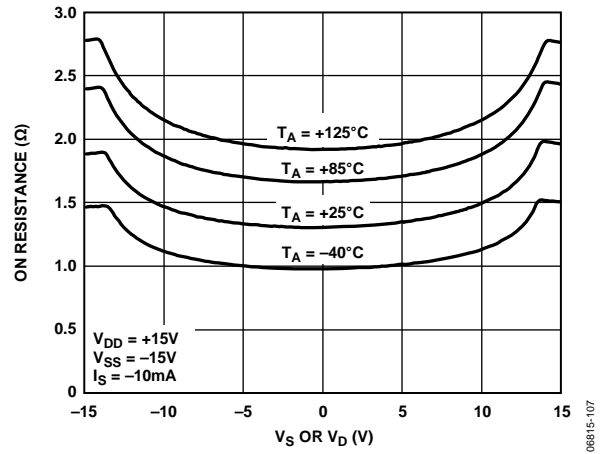


Figure 8. On Resistance vs. V_D or V_S for Different Temperatures, 15 V Dual Supply

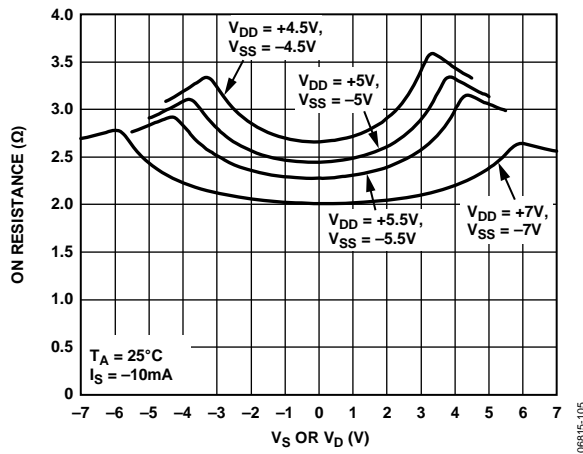


Figure 6. On Resistance vs. V_D or V_S , Dual Supply

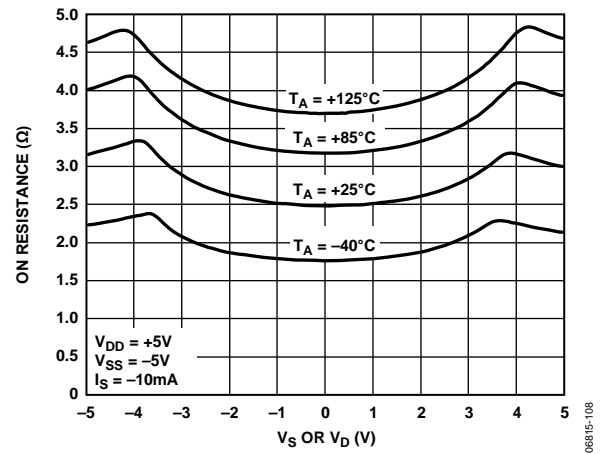


Figure 9. On Resistance vs. V_D or V_S for Different Temperatures, 5 V Dual Supply

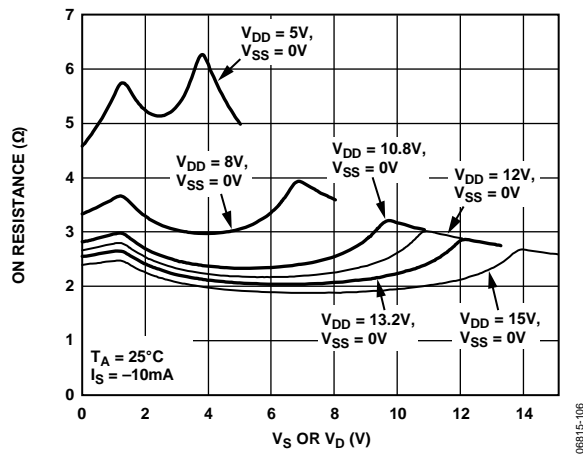


Figure 7. On Resistance vs. V_D or V_S , Single Supply

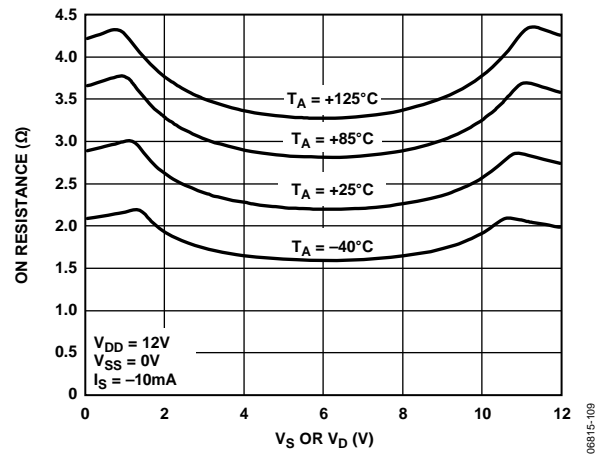


Figure 10. On Resistance vs. V_D or V_S for Different Temperatures, Single Supply

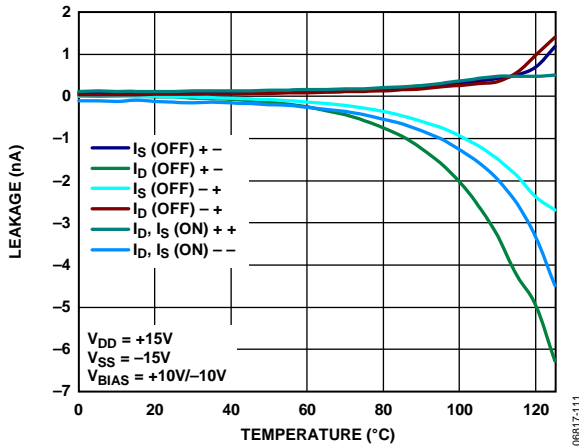


Figure 11. Leakage Currents vs. Temperature, 15 V Dual Supply

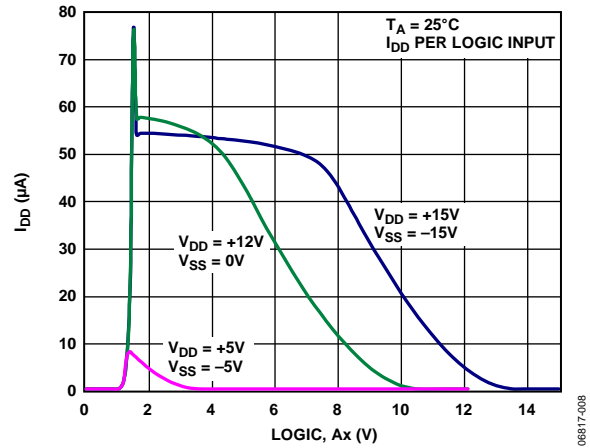


Figure 14. I_{DD} vs. Logic Level

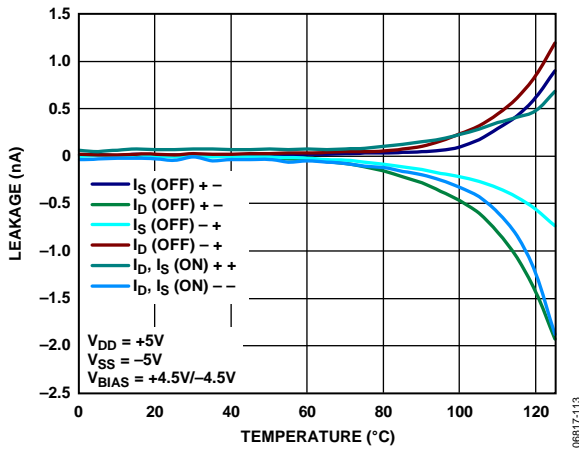


Figure 12. Leakage Currents vs. Temperature, 5 V Dual Supply

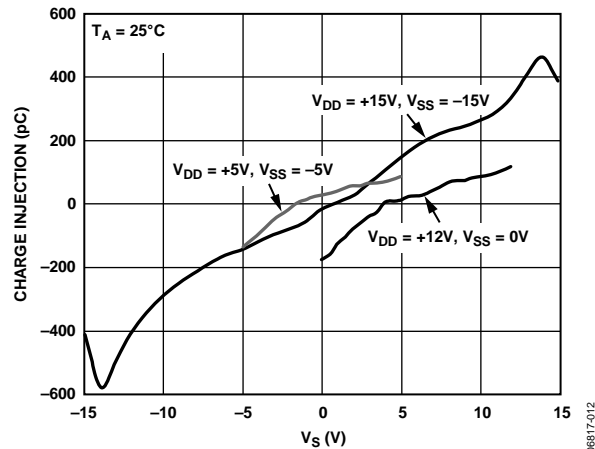


Figure 15. Charge Injection vs. Source Voltage

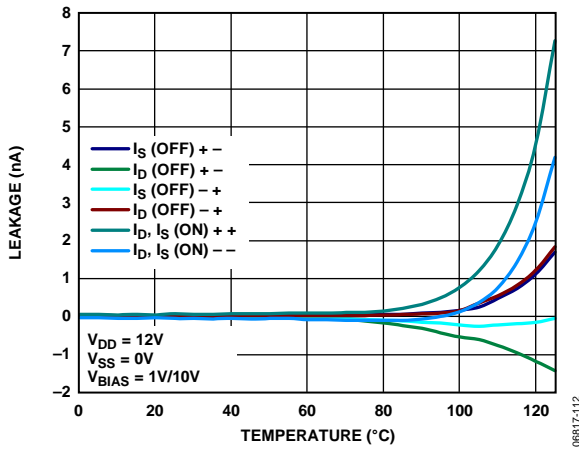


Figure 13. Leakage Currents vs. Temperature, 12 V Single Supply

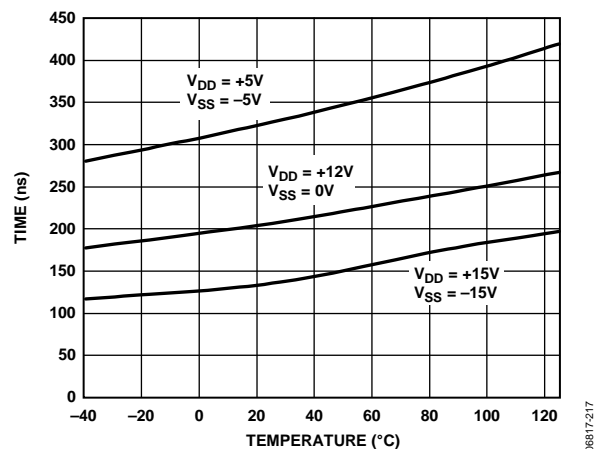


Figure 16. $t_{TRANSITION}$ Time vs. Temperature

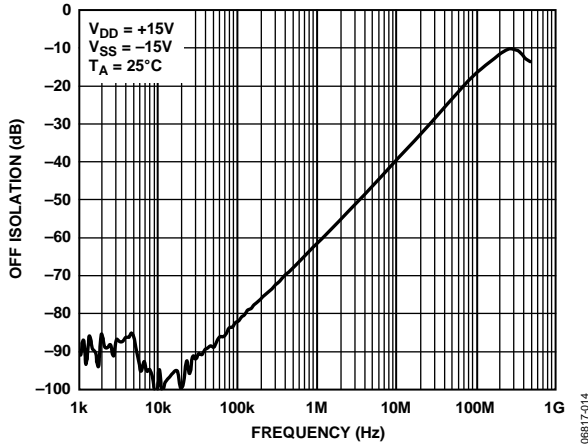


Figure 17. Off Isolation vs. Frequency

06817-014

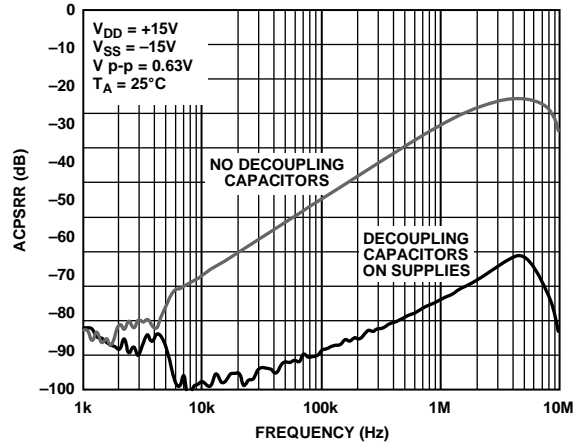


Figure 20. ACPSRR vs. Frequency

06817-017

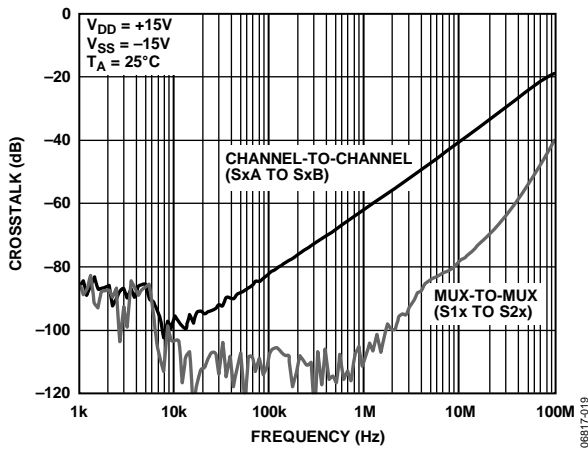


Figure 18. Crosstalk vs. Frequency

06817-019

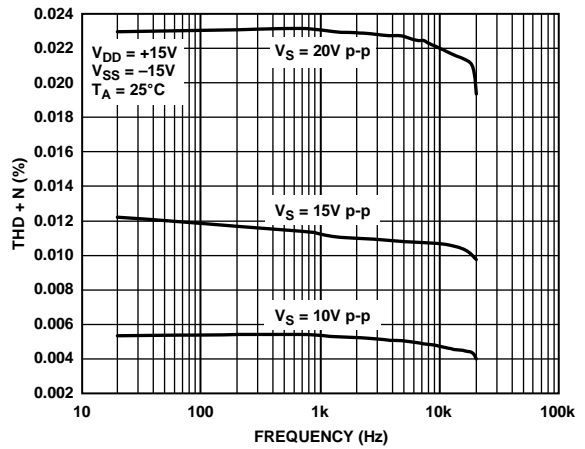


Figure 21. THD + N vs. Frequency, 15 V Dual Supply

06817-117

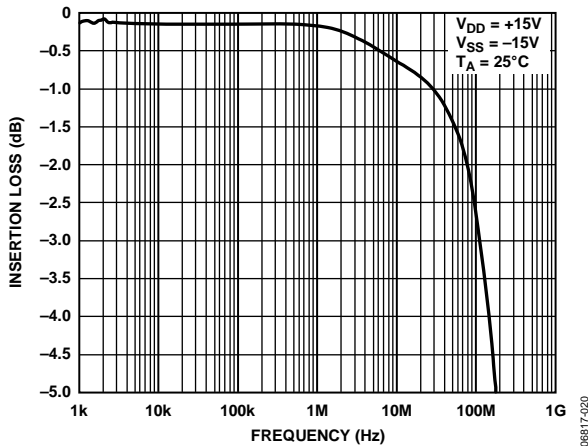


Figure 19. On Response vs. Frequency

06817-020

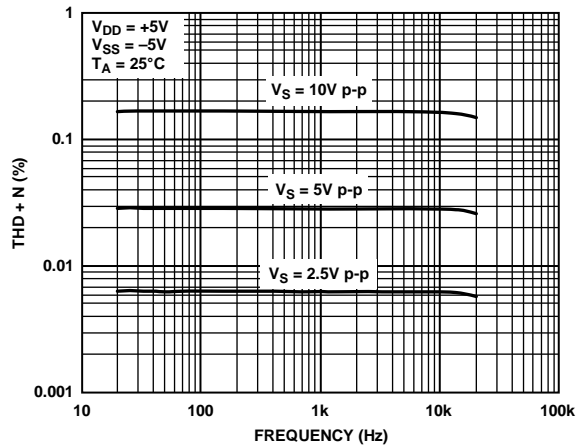


Figure 22. THD + N vs. Frequency, 5 V Dual Supply

06817-118

TERMINOLOGY

I_{DD}

The positive supply current.

I_{SS}

The negative supply current.

V_D, V_S

The analog voltage on Terminal D and Terminal S.

R_{ON}

The ohmic resistance between Terminal D and Terminal S.

R_{FLAT(ON)}

Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)

The source leakage current with the switch off.

I_D (Off)

The drain leakage current with the switch off.

I_D, I_S (On)

The channel leakage current with the switch on.

V_{INL}

The maximum input voltage for Logic 0.

V_{INH}

The minimum input voltage for Logic 1.

I_{INL}, I_{INH}

The input current of the digital input.

C_S (Off)

The off-switch source capacitance, which is measured with reference to ground.

C_D (Off)

The off-switch drain capacitance, which is measured with reference to ground.

C_D, C_S (On)

The on-switch capacitance, which is measured with reference to ground.

C_{IN}

The digital input capacitance.

t_{TRANSITION}

The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address state to another.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

THD + N

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

TEST CIRCUITS

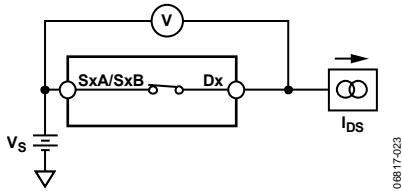


Figure 23. On Resistance

06817-023

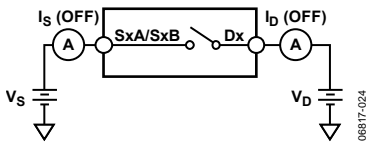


Figure 24. Off Leakage

06817-024

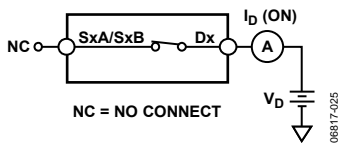
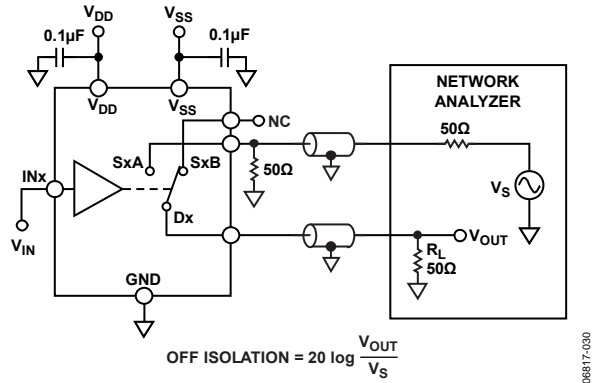


Figure 25. On Leakage

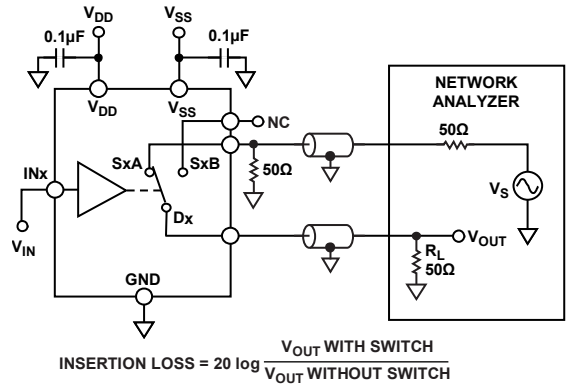
06817-025



$$\text{OFF ISOLATION} = 20 \log \frac{V_{\text{OUT}}}{V_s}$$

Figure 26. Off Isolation

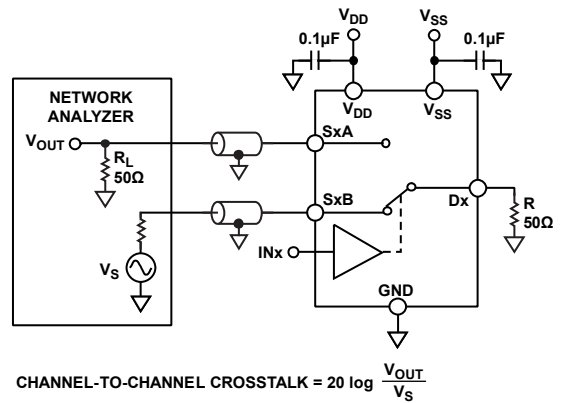
06817-030



$$\text{INSERTION LOSS} = 20 \log \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

Figure 27. Channel-to-Channel Crosstalk

06817-031



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{\text{OUT}}}{V_s}$$

Figure 28. Bandwidth

06817-032

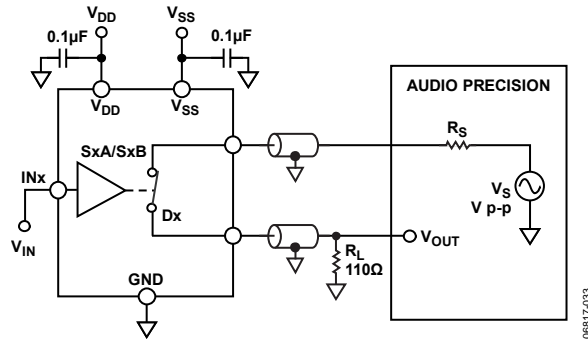


Figure 29. THD + Noise

06817-033

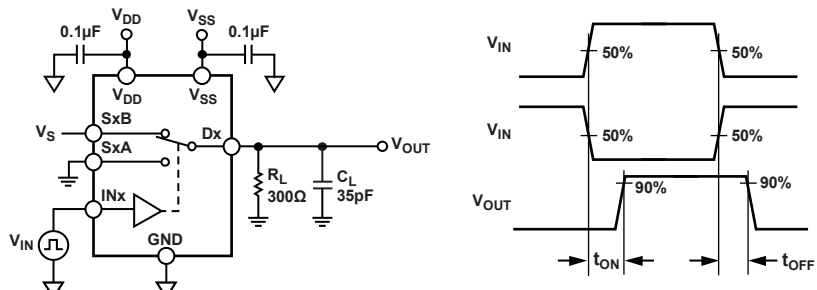


Figure 30. Switching Times

06817-026

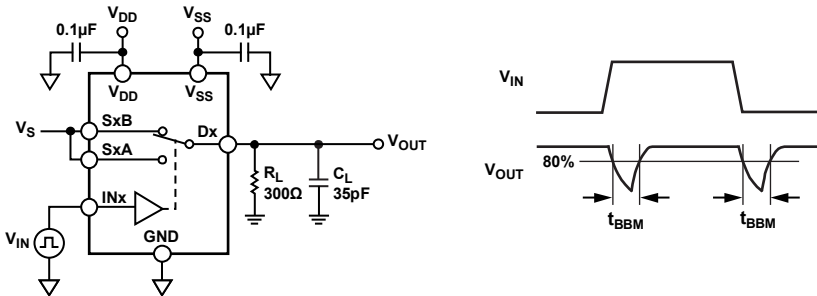


Figure 31. Break-Before-Make Time Delay

06817-027

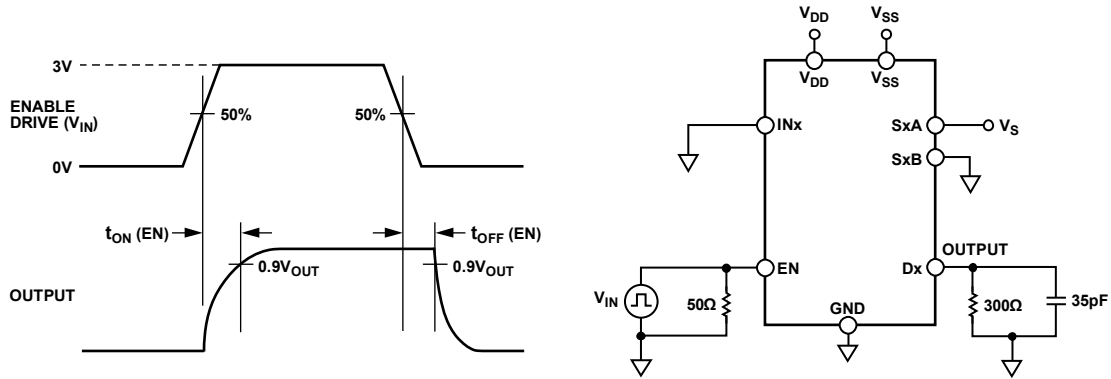


Figure 32. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$

06817-028

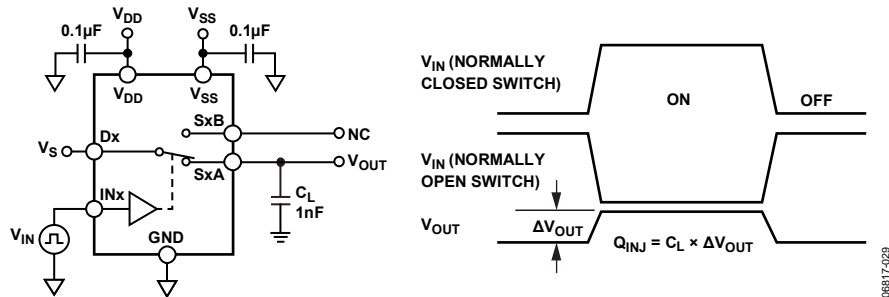


Figure 33. Charge Injection

06817-029