

ADG201A/ADG202A

FEATURES

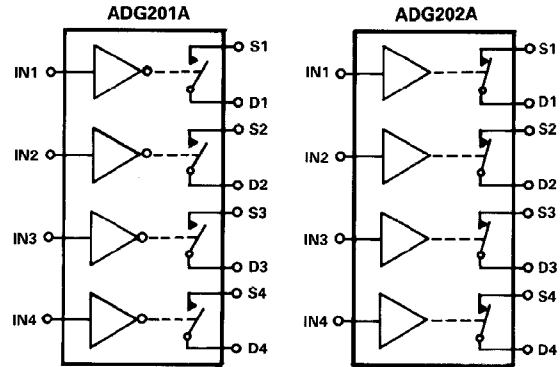
- 44V Supply Maximum Rating
- ±15V Analog Signal Range
- Low R_{ON} (60Ω)
- Low Leakage (0.5nA)
- Break Before Make Switching
- Extended Plastic Temperature Range
(-40°C to +85°C)
- Low Power Dissipation (33mW)
- Available in 16-Lead DIP/SOIC and
20-Lead PLCC/LCCC Packages
- Superior Second Source:
ADG201A Replaces DG201A, HI-201
ADG202A Replaces DG202

GENERAL DESCRIPTION

The ADG201A and ADG202A are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process which gives an increased signal handling capability of ±15V. These switches also feature high switching speeds and low R_{ON}.

The ADG201A and ADG202A consist of four SPST switches. They differ only in that the digital control logic is inverted. All devices exhibit break before make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

PRODUCT HIGHLIGHTS

1. **Extended Signal Range:**
These switches are fabricated on an enhanced LC²MOS process, resulting in high breakdown and an increased analog signal range of ±15V.
2. **Single Supply Operation:**
For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.
3. **Low Leakage:**
Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

| ADG201A IN | ADG202A IN | SWITCH CONDITION |
|---------------|---------------|---------------------|
| 0 | 1 | ON |
| 1 | 0 | OFF |

Table I. Truth Table

REV. A

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ADG201A/ADG202A—SPECIFICATIONS ($V_{DD} = +15V, V_{SS} = -15V$, unless otherwise specified)

| Parameter | K Version -40°C to | | B Version -40°C to | | T Version -55°C to | | Units | Test Conditions |
|--|-----------------------|-------|-----------------------|-------|-----------------------|--------|----------|--|
| | 25°C | +85°C | 25°C | +85°C | 25°C | +125°C | | |
| ANALOG SWITCH | | | | | | | | |
| Analog Signal Range | ±15 | ±15 | ±15 | ±15 | ±15 | ±15 | Volts | -10V ≤ V _S ≤ +10V I _{DS} = 1.0mA Test Circuit 1 |
| R _{ON} | 60 | | 60 | | 60 | | Ω typ | |
| | 90 | 145 | 90 | 145 | 90 | 145 | Ω max | |
| R _{ON} vs. V _D (V _S) | 20 | | 20 | | 20 | | % typ | V _S = 0V, I _{DS} = 1mA |
| R _{ON} Drift | 0.5 | | 0.5 | | 0.5 | | %/°C typ | |
| R _{ON} Match | 5 | | 5 | | 5 | | % typ | |
| I _S (OFF) | 0.5 | | 0.5 | | 0.5 | | nA typ | V _D = ±14V; V _S = ±14V; Test Circuit 2 |
| OFF Input Leakage | 2 | 100 | 2 | 100 | 1 | 100 | nA max | |
| I _D (OFF) | 0.5 | | 0.5 | | 0.5 | | nA typ | V _D = ±14V; V _S = ±14V; Test Circuit 2 |
| OFF Output Leakage | 2 | 100 | 2 | 100 | 1 | 100 | nA max | |
| I _D (ON) | 0.5 | | 0.5 | | 0.5 | | nA typ | V _D = ±14V; Test Circuit 3 |
| ON Channel Leakage | 2 | 200 | 2 | 200 | 1 | 200 | nA max | |
| DIGITAL CONTROL | | | | | | | | |
| V _{INH} , Input High Voltage | | 2.4 | | 2.4 | | 2.4 | V min | |
| V _{INL} , Input Low Voltage | | 0.8 | | 0.8 | | 0.8 | V max | |
| I _{INL} or I _{INH} | | 1 | | 1 | | 1 | μA max | |
| DYNAMIC CHARACTERISTICS | | | | | | | | |
| t _{OPEN} | 30 | | 30 | | 30 | | ns typ | Test Circuit 4 Test Circuit 4 V _S = 10V(p-p); f = 100kHz R _L = 75Ω; Test Circuit 6 Test Circuit 7 R _S = 0Ω; C _L = 1000pF; V _S = 0V Test Circuit 5 |
| t _{ON} ¹ | 300 | | 300 | | 300 | | ns max | |
| t _{OFF} ¹ | 250 | | 250 | | 250 | | ns max | |
| OFF Isolation | 80 | | 80 | | 80 | | dB typ | |
| Channel-to-Channel Crosstalk | 80 | | 80 | | 80 | | dB typ | |
| C _S (OFF) | 5 | | 5 | | 5 | | pF typ | |
| C _D (OFF) | 5 | | 5 | | 5 | | pF typ | |
| C _D , C _S (ON) | 16 | | 16 | | 16 | | pF typ | |
| C _{IN} Digital Input Capacitance | 5 | | 5 | | 5 | | pF typ | |
| Q _{INJ} Charge Injection | 20 | | 20 | | 20 | | pC typ | |
| POWER SUPPLY | | | | | | | | |
| I _{DD} | 0.6 | | 0.6 | | 0.6 | | mA typ | Digital Inputs = V _{INL} or V _{INH} |
| I _{DD} | | 2 | | 2 | | 2 | mA max | |
| I _{SS} | 0.1 | | 0.1 | | 0.1 | | mA typ | |
| I _{SS} | | 0.2 | | 0.2 | | 0.2 | mA max | |
| Power Dissipation | | 33 | | 33 | | 33 | mW max | |

NOTES

¹Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

| | |
|------------------------------------|--|
| V _{DD} to V _{SS} | 44V |
| V _{DD} to GND | 25V |
| V _{SS} to GND | -25V |
| Analog Inputs¹ | |
| Voltage at S, D | V _{SS} - 0.3V to V _{DD} + 0.3V |
| Continuous Current, S or D | 30mA |
| Pulsed Current S or D | |
| 1ms Duration, 10% Duty Cycle | 70mA |
| Digital Inputs¹ | |
| Voltage at IN | V _{SS} - 2V to V _{DD} + 2V or 20mA, Whichever Occurs First |

Power Dissipation (Any Package)

Up to +75°C 470mW
Derates above +75°C by 6mW/°C

Operating Temperature

Commercial (K Version) -40°C to +85°C
Industrial (B Version) -40°C to +85°C
Extended (T Version) -55°C to +125°C
Storage Temperature Range -65°C to +150°C
Lead Temperature (Soldering 10sec) +300°C

NOTE

¹Overtoltage at IN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE

| Model ¹ | Temperature Range | Package Option ² |
|--------------------|-------------------|-----------------------------|
| ADG201AKN | -40°C to +85°C | N-16 |
| ADG201AKR | -40°C to +85°C | R-16A |
| ADG201AKP | -40°C to +85°C | P-20A |
| ADG201ABQ | -40°C to +85°C | Q-16 |
| ADG201ATQ | -55°C to +125°C | Q-16 |
| ADG201ATE | -55°C to +125°C | E-20A |
| ADG202AKN | -40°C to +85°C | N-16 |
| ADG202AKR | -40°C to +85°C | R-16A |
| ADG202AKP | -40°C to +85°C | P-20A |
| ADG202ABQ | -40°C to +85°C | Q-16 |
| ADG202ATQ | -55°C to +125°C | Q-16 |
| ADG202ATE | -55°C to +125°C | E-20A |

NOTES

¹To order MIL-STD-883, Class B processed parts, add/883B to T grade part numbers. See Analog Devices Military Products Databook (1990) for military data sheet.

²E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip.

PIN CONFIGURATIONS

DIP, SOIC



LCCC



PLCC



ADG201A/ADG202A FUNCTIONAL DIAGRAM



Figure 1. Typical Digital Input Cell

ADG201A/ADG202A—Typical Performance Characteristics

The switches are guaranteed functional with reduced single or dual supplies down to 4.5V.



R_{ON} as a Function of V_D (V_S): Dual Supply Voltage



R_{ON} as a Function of V_D (V_S): Single Supply Voltage



Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)



Trigger Level vs. Power Supply Voltage: Dual or Single Supply Voltage



Switching Time vs. Supply Voltage (Dual Supply)



Switching Time vs. Supply Voltage (Single Supply)

Test Circuits—ADG201A/ADG202A



Test Circuit 1



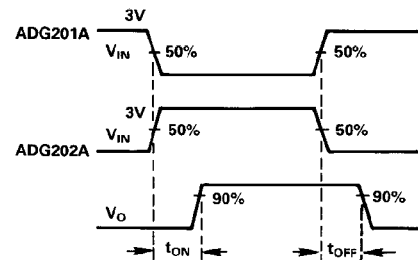
Test Circuit 2



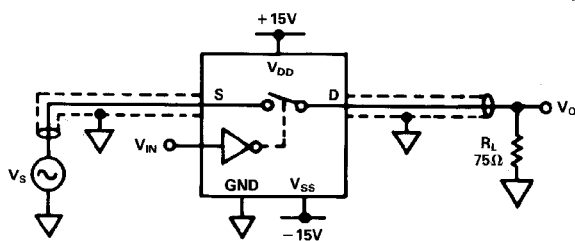
Test Circuit 3



Test Circuit 4



Test Circuit 5. Charge Injection



ADG201A $V_{IN} = 5V$
ADG202A $V_{IN} = 0V$

OFF ISOLATION =
 $20 \times \text{LOG} |V_s/V_O|$

Test Circuit 6. Off Isolation



ADG201A $V_{IN} = 0V$
ADG202A $V_{IN} = 5V$

CHANNEL-TO-CHANNEL CROSSTALK =
 $20 \times \text{LOG} |V_s/V_O|$

Test Circuit 7. Channel-to-Channel Crosstalk