

## FEATURES

### SPI interface with error detection

Includes CRC, invalid read/write address, and SCLK count error detection

Supports burst and daisy-chain mode

Industry-standard SPI Mode 0 and Mode 3 interface-compatible

Guaranteed break-before-make switching, allowing external wiring of switches to deliver multiplexer configurations

### $V_{SS}$ to $V_{DD}$ analog signal range

Fully specified at  $\pm 15$  V,  $\pm 20$  V, +12 V, and +36 V

9 V to 40 V single-supply operation ( $V_{DD}$ )

$\pm 9$  V to  $\pm 22$  V dual-supply operation ( $V_{DD}/V_{SS}$ )

8 kV HBM ESD rating

Low on resistance

1.8 V logic compatibility with  $2.7$  V  $\leq V_L \leq 3.3$  V

## APPLICATIONS

Relay replacement

Automatic test equipment

Data acquisition

Instrumentation

Avionics

Audio and video switching

Communication systems

## GENERAL DESCRIPTION

The ADGS5414 contains eight independent single-pole/single-throw (SPST) switches. An SPI interface controls the switches and has robust error detection features, including cyclic redundancy check (CRC) error detection, invalid read/write address error detection, and SCLK count error detection.

It is possible to daisy-chain multiple ADGS5414 devices together. This enables the configuration of multiple devices with a minimal amount of digital lines. The ADGS5414 can also operate in burst mode to decrease the time between SPI commands.

Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

The on-resistance profile is flat over the full analog input range, ensuring ideal linearity and low distortion when switching audio signals. The ADGS5414 exhibits break-before-make switching action, allowing the use of the device in multiplexer applications with external wiring.

## FUNCTIONAL BLOCK DIAGRAM

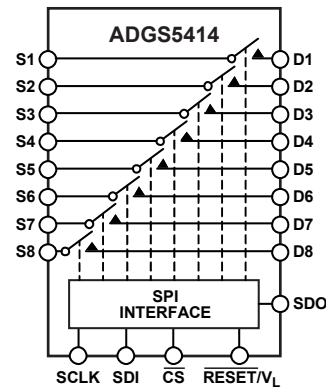


Figure 1.

1592-001

## PRODUCT HIGHLIGHTS

1. The SPI interface removes the need for parallel conversion, logic traces, and reduces the general-purpose input/output (GPIO) channel count.
2. Daisy-chain mode removes the need for additional logic traces when using multiple devices.
3. CRC error detection, invalid read/write address error detection, and SCLK count error detection ensures a robust digital interface.
4. CRC and error detection capabilities allow the use of the ADGS5414 in safety critical systems.
5. Break-before-make switching allows external wiring of the switches to deliver multiplexer configurations.
6. The trench isolation analog switch section guards against latch-up. A dielectric trench separates the positive and negative channel transistors, preventing latch-up even under severe overvoltage conditions.

### Rev. 0

### Document Feedback

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## REVISION HISTORY

10/2017—Revision 0: Initial Version

## SPECIFICATIONS

### ±15 V DUAL SUPPLY

Digital logic voltage ( $V_{DD}$ ) = +15 V ± 10%, negative supply voltage ( $V_{SS}$ ) = -15 V ± 10%, positive supply voltage ( $V_L$ ) = 2.7 V to 5.5 V, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance, $R_{ON}$	13.5			Ω typ	Source voltage ( $V_S$ ) = ±10 V, $I_S$ = -10 mA; see Figure 29
On-Resistance Match Between Channels, $\Delta R_{ON}$	15	18	22	Ω max	$V_{DD}$ = +13.5 V, $V_{SS}$ = -13.5 V
On-Resistance Flatness, $R_{FLAT(ON)}$	0.3			Ω typ	$V_S$ = ±10 V, source current ( $I_S$ ) = -10 mA
	0.8	1.3	1.4	Ω max	
	1.8			Ω typ	$V_S$ = ±10 V, $I_S$ = -10 mA
	2.2	2.6	3	Ω max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	±0.1			nA typ	$V_{DD}$ = +16.5 V, $V_{SS}$ = -16.5 V
Drain Off Leakage, $I_D$ (Off)	±0.25	±1	±7	nA max	$V_S$ = ±10 V, $V_D$ = ±10 V; see Figure 32
	±0.1			nA typ	$V_S$ = ±10 V, $V_D$ = ±10 V; see Figure 32
Channel On Leakage, $I_D$ (On), $I_S$ (On)	±0.25	±1	±7	nA max	
	±0.15			nA typ	$V_S = V_D = \pm 10$ V; see Figure 28
	±0.4	±2	±14	nA max	
<b>DIGITAL OUTPUT</b>					
Output Voltage Low, $V_{OL}$			0.4	V max	Sink current ( $I_{SINK}$ ) = 5 mA
Output Current, Low ( $I_{OL}$ ) or High ( $I_{OH}$ )	0.001		0.2	V max	$I_{SINK}$ = 1 mA
			±0.1	μA typ	Output voltage ( $V_{OUT}$ ) = ground voltage ( $V_{GND}$ ) or $V_L$
Digital Output Capacitance, $C_{OUT}$	4			μA max	
				pF typ	
<b>DIGITAL INPUTS</b>					
Input Voltage High, $V_{INH}$			2	V min	3.3 V < $V_L$ ≤ 5.5 V
Input Voltage Low, $V_{INL}$			1.35	V min	2.7 V ≤ $V_L$ ≤ 3.3 V
Input Current, Low ( $I_{INL}$ ) or High ( $I_{INH}$ )	0.001		0.8	V max	3.3 V < $V_L$ ≤ 5.5 V
			0.8	V max	2.7 V ≤ $V_L$ ≤ 3.3 V
			±0.1	μA typ	$V_{IN} = V_{GND}$ or $V_L$
Digital Input Capacitance, $C_{IN}$	4			μA max	
				pF typ	
<b>DYNAMIC CHARACTERISTICS</b>					
$t_{ON}$	410			ns typ	Load resistance ( $R_L$ ) = 300 Ω, load capacitance ( $C_L$ ) = 35 pF
$t_{OFF}$	420	515	515	ns max	$V_S = 10$ V; see Figure 37
	135			ns typ	$R_L = 300$ Ω, $C_L = 35$ pF
Break-Before-Make Time Delay, $t_D$	140	185	195	ns max	$V_S = 10$ V; see Figure 37
	260			ns typ	$R_L = 300$ Ω, $C_L = 35$ pF
Charge Injection, $Q_{INJ}$	250		210	ns min	$V_{S1} = V_{S2} = 10$ V; see Figure 36
	125			pC typ	$V_S = 0$ V, $R_S = 0$ Ω, $C_L = 1$ nF; see Figure 38

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
Off Isolation	-60			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , frequency (f) = 1 MHz; see Figure 32
Channel to Channel Crosstalk	-75			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , f = 1 MHz; see Figure 30
Total Harmonic Distortion + Noise (THD + N)	0.01			% typ	$R_L = 1 \text{ k}\Omega$ , 15 V p-p, f = 20 Hz to 20 kHz; see Figure 33
-3 dB Bandwidth	200			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; see Figure 34
Insertion Loss	-0.9			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , f = 1 MHz; see Figure 34
Source Capacitance ( $C_S$ ) (Off)	11			pF typ	$V_S = 0 \text{ V}$ , f = 1 MHz
Drain Capacitance ( $C_D$ ) (Off)	11			pF typ	$V_S = 0 \text{ V}$ , f = 1 MHz
$C_D$ (On), $C_S$ (On)	30			pF typ	$V_S = 0 \text{ V}$ , f = 1 MHz
<b>POWER REQUIREMENTS</b>					
Positive Supply Current ( $I_{DD}$ )	45		70	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = +16.5 \text{ V}$ , $V_{SS} = -16.5 \text{ V}$ All switches open All switches open
$I_L$	45		70	$\mu\text{A}$ typ $\mu\text{A}$ max	All switches closed, $V_L = 5.5 \text{ V}$ All switches closed, $V_L = 5.5 \text{ V}$
	310		430	$\mu\text{A}$ typ $\mu\text{A}$ max	All switches closed, $V_L = 2.7 \text{ V}$ All switches closed, $V_L = 2.7 \text{ V}$
Inactive	6.3		8.0	$\mu\text{A}$ typ $\mu\text{A}$ max	Digital inputs = 0 V or $V_L$
SCLK = 1 MHz	14			$\mu\text{A}$ typ	$\overline{\text{CS}}$ and SDI = 0 V or $V_L$ , $V_L = 5 \text{ V}$
	7			$\mu\text{A}$ typ	$\overline{\text{CS}}$ and SDI = 0 V or $V_L$ , $V_L = 3 \text{ V}$
SCLK = 50 MHz	390			$\mu\text{A}$ typ	$\overline{\text{CS}} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 5 \text{ V}$
	210			$\mu\text{A}$ typ	$\overline{\text{CS}} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 3 \text{ V}$
SDI = 1 MHz	15			$\mu\text{A}$ typ	$\overline{\text{CS}}$ and SCLK = 0 V or $V_L$ , $V_L = 5 \text{ V}$
	7.5			$\mu\text{A}$ typ	$\overline{\text{CS}}$ and SCLK = 0 V or $V_L$ , $V_L = 3 \text{ V}$
SDI = 25 MHz	230			$\mu\text{A}$ typ	$\overline{\text{CS}}$ and SCLK = 0 V or $V_L$ , $V_L = 5 \text{ V}$
	120			$\mu\text{A}$ typ	$\overline{\text{CS}}$ and SCLK = 0 V or $V_L$ , $V_L = 3 \text{ V}$
Active at 50 MHz	1.8			mA typ	Digital inputs toggle between 0 V and $V_L$ , $V_L = 5.5 \text{ V}$
	0.7	2	2.1	mA max mA typ	Digital inputs toggle between 0 V and $V_L$ , $V_L = 2.7 \text{ V}$
Negative Supply Current ( $I_{SS}$ )	0.05		1.0	mA max	Digital inputs = 0 V or $V_L$
			1.0	$\mu\text{A}$ max	
Dual-Supply Operation ( $V_{DD}/V_{SS}$ )			$\pm 9$	V min	GND = 0 V
			$\pm 22$	V max	GND = 0 V

**±20 V DUAL SUPPLY**

$V_{DD} = +20\text{ V} \pm 10\%$ ,  $V_{SS} = -20\text{ V} \pm 10\%$ ,  $V_L = 2.7\text{ V to } 5.5\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 2.**

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance, $R_{ON}$	12.5			$\Omega$ typ	$V_S = \pm 15\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 29
On-Resistance Match Between Channels, $\Delta R_{ON}$	14	17	21	$\Omega$ max	$V_{DD} = +18\text{ V}$ , $V_{SS} = -18\text{ V}$ $V_S = \pm 15\text{ V}$ , $I_S = -10\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	0.3			$\Omega$ typ	
	0.8	1.3	1.4	$\Omega$ max	
	2.3			$\Omega$ typ	$V_S = \pm 15\text{ V}$ , $I_S = -10\text{ mA}$
	2.7	3.1	3.5	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = +22\text{ V}$ , $V_{SS} = -22\text{ V}$ $V_S = \pm 15\text{ V}$ , $V_D = \pm 15\text{ V}$ ; see Figure 32
Drain Off Leakage, $I_D$ (Off)	$\pm 0.25$ $\pm 0.1$	$\pm 1$	$\pm 7$	nA max nA typ	$V_S = \pm 15\text{ V}$ , $V_D = \pm 15\text{ V}$ ; see Figure 32
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.25$ $\pm 0.15$ $\pm 0.4$	$\pm 1$ $\pm 2$	$\pm 7$ $\pm 14$	nA max nA typ nA max	$V_S = V_D = \pm 15\text{ V}$ ; see Figure 28
<b>DIGITAL OUTPUT</b>					
Output Voltage Low, $V_{OL}$			0.4	V max	$I_{SINK} = 5\text{ mA}$
Output Current, $I_{OL}$ or $I_{OH}$	0.001		0.2	V max $\mu\text{A}$ typ	$I_{SINK} = 1\text{ mA}$ $V_{OUT} = V_{GND}$ or $V_L$
Digital Output Capacitance, $C_{OUT}$	4		$\pm 0.1$	$\mu\text{A}$ max pF typ	
<b>DIGITAL INPUTS</b>					
Input Voltage High, $V_{INH}$			2	V min	$3.3\text{ V} < V_L \leq 5.5\text{ V}$
Input Voltage Low, $V_{INL}$			1.35	V min	$2.7\text{ V} \leq V_L \leq 3.3\text{ V}$
Input Current, $I_{INL}$ or $I_{INH}$	0.001		0.8	V max	$3.3\text{ V} < V_L \leq 5.5\text{ V}$
			0.8	V max	$2.7\text{ V} \leq V_L \leq 3.3\text{ V}$
			$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{GND}$ or $V_L$
Digital Input Capacitance, $C_{IN}$	4			pF typ	
<b>DYNAMIC CHARACTERISTICS</b>					
$t_{ON}$	410			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	418	485	495	ns max	$V_S = 10\text{ V}$ ; see Figure 37
$t_{OFF}$	135			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	144	185	195	ns max	$V_S = 10\text{ V}$ ; see Figure 37
Break-Before-Make Time Delay, $t_D$	255			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
Charge Injection, $Q_{INJ}$	245		205	ns min	$V_{S1} = V_{S2} = 10\text{ V}$ ; see Figure 36
Off Isolation	160			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 38
Channel to Channel Crosstalk	-60			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 34
(THD + N)	-75			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 30
	0.012			% typ	$R_L = 1\text{ k}\Omega$ , $20\text{ V p-p}$ , $f = 20\text{ Hz to } 20\text{ kHz}$ ; see Figure 33

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
-3 dB Bandwidth	200			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; see Figure 34
Insertion Loss	-0.8			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ ; see Figure 34
$C_S$ (Off)	11			pF typ	$V_S = 0 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (Off)	11			pF typ	$V_S = 0 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (On), $C_S$ (On)	30			pF typ	$V_S = 0 \text{ V}$ , $f = 1 \text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	50			$\mu\text{A}$ typ	$V_{DD} = +22 \text{ V}$ , $V_{SS} = -22 \text{ V}$ All switches open
			110	$\mu\text{A}$ max	All switches open
	50			$\mu\text{A}$ typ	All switches closed, $V_L = 5.5 \text{ V}$
			110	$\mu\text{A}$ max	All switches closed, $V_L = 5.5 \text{ V}$
	320			$\mu\text{A}$ typ	All switches closed, $V_L = 2.7 \text{ V}$
			450	$\mu\text{A}$ max	All switches closed, $V_L = 2.7 \text{ V}$
$I_L$	Inactive	6.3		$\mu\text{A}$ typ	Digital inputs = 0 V or $V_L$
			8.0	$\mu\text{A}$ max	
	SCLK = 1 MHz	14		$\mu\text{A}$ typ	$\overline{CS}$ and SDI = 0 V or $V_L$ , $V_L = 5 \text{ V}$
			7	$\mu\text{A}$ typ	$\overline{CS}$ and SDI = 0 V or $V_L$ , $V_L = 3 \text{ V}$
	SCLK = 50 MHz	390		$\mu\text{A}$ typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 5 \text{ V}$
			210	$\mu\text{A}$ typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 3 \text{ V}$
	SDI = 1 MHz	15		$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 5 \text{ V}$
			7.5	$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 3 \text{ V}$
	SDI = 25 MHz	230		$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 5 \text{ V}$
			120	$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 3 \text{ V}$
Active at 50 MHz	1.8		mA typ	Digital inputs toggle between 0 V and $V_L$ , $V_L = 5.5 \text{ V}$	
		2	mA max		
		0.7	mA typ	Digital inputs toggle between 0 V and $V_L$ , $V_L = 2.7 \text{ V}$	
$I_{SS}$	0.05		mA max		
		1.0	$\mu\text{A}$ typ	Digital inputs = 0 V or $V_L$	
		1.0	$\mu\text{A}$ max		
Dual-Supply Operation ( $V_{DD}/V_{SS}$ )		$\pm 9$	V min	GND = 0 V	
		$\pm 22$	V max	GND = 0 V	

**12 V SINGLE SUPPLY**

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $V_L = 2.7\text{ V}$  to  $5.5\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 3.**

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance, $R_{ON}$	26			$\Omega$ typ	$V_S = 0\text{ V}$ to $10\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 29
On-Resistance Match Between Channels, $\Delta R_{ON}$	30 0.3	36	42	$\Omega$ max $\Omega$ typ	$V_{DD} = 10.8\text{ V}$ , $V_{SS} = 0\text{ V}$ $V_S = 0\text{ V}$ to $10\text{ V}$ , $I_S = -10\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	1 5.5 6.5	1.5 8	1.6 12	$\Omega$ max $\Omega$ typ $\Omega$ max	$V_S = 0\text{ V}$ to $10\text{ V}$ , $I_S = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = 13.2\text{ V}$ , $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 32
Drain Off Leakage, $I_D$ (Off)	$\pm 0.25$ $\pm 0.1$	$\pm 1$	$\pm 7$	nA max nA typ	$V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 32
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.25$ $\pm 0.15$	$\pm 1$	$\pm 7$	nA max nA typ	$V_S = V_D = 1\text{ V}/10\text{ V}$ ; see Figure 28
	$\pm 0.4$	$\pm 2$	$\pm 14$	nA max	
<b>DIGITAL OUTPUT</b>					
Output Voltage Low, $V_{OL}$			0.4 0.2	V max V max	$I_{SINK} = 5\text{ mA}$ $I_{SINK} = 1\text{ mA}$
Output Current, $I_{OL}$ or $I_{OH}$	0.001		$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{OUT} = V_{GND}$ or $V_L$
Digital Output Capacitance, $C_{OUT}$	4			pF typ	
<b>DIGITAL INPUTS</b>					
Input Voltage High, $V_{INH}$			2 1.35	V min V min	$3.3\text{ V} < V_L \leq 5.5\text{ V}$ $2.7\text{ V} \leq V_L \leq 3.3\text{ V}$
Low, $V_{INL}$			0.8 0.8	V max V max	$3.3\text{ V} < V_L \leq 5.5\text{ V}$ $2.7\text{ V} \leq V_L \leq 3.3\text{ V}$
Input Current, $I_{INL}$ or $I_{INH}$	0.001		$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{GND}$ or $V_L$
Digital Input Capacitance, $C_{IN}$	4			pF typ	
<b>DYNAMIC CHARACTERISTICS</b>					
$t_{ON}$	450			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	455	555	575	ns max	$V_S = 8\text{ V}$ ; see Figure 37
$t_{OFF}$	135			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	141	195	205	ns max	$V_S = 8\text{ V}$ ; see Figure 37
Break-Before-Make Time Delay, $t_D$	285			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
Charge Injection, $Q_{INJ}$	275		225	ns min	$V_{S1} = V_{S2} = 8\text{ V}$ ; see Figure 36
Off Isolation	55			pC typ	$V_S = 6\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 38
Channel to Channel Crosstalk	-60			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 31
	-75			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 30

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
THD +N	0.1			% typ	$R_L = 1\text{ k}\Omega$ , 6 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 33
-3 dB Bandwidth	220			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 34
Insertion Loss	-1.55			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 34
$C_S$ (Off)	12			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	12			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (On), $C_S$ (On)	30			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	40			$\mu\text{A}$ typ	$V_{DD} = 13.2\text{ V}$ All switches open
			65	$\mu\text{A}$ max	All switches open
	40			$\mu\text{A}$ typ	All switches closed, $V_L = 5.5\text{ V}$
			65	$\mu\text{A}$ max	All switches closed, $V_L = 5.5\text{ V}$
	300			$\mu\text{A}$ typ	All switches closed, $V_L = 2.7\text{ V}$
$I_L$			420	$\mu\text{A}$ max	All switches closed, $V_L = 2.7\text{ V}$
	Inactive	6.3		$\mu\text{A}$ typ	Digital inputs = 0 V or $V_L$
				8.0	$\mu\text{A}$ max
	SCLK = 1 MHz	14		$\mu\text{A}$ typ	$\overline{CS}$ and SDI = 0 V or $V_L$ , $V_L = 5\text{ V}$
		7		$\mu\text{A}$ typ	$\overline{CS}$ and SDI = 0 V or $V_L$ , $V_L = 3\text{ V}$
SCLK = 50 MHz	390		$\mu\text{A}$ typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 5\text{ V}$	
	210		$\mu\text{A}$ typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 3\text{ V}$	
SDI = 1 MHz	15		$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 5\text{ V}$	
	7.5		$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 3\text{ V}$	
SDI = 25 MHz	230		$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 5\text{ V}$	
	120		$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 3\text{ V}$	
Active at 50 MHz	1.8			mA typ	Digital inputs toggle between 0 V and $V_L$ , $V_L = 5.5\text{ V}$
	0.7	2	2.1	mA max	Digital inputs toggle between 0 V and $V_L$ , $V_L = 2.7\text{ V}$
Single-Supply Operation ( $V_{DD}$ )			1.0	mA max	
			9	V min	$GND = 0\text{ V}$ , $V_{SS} = 0\text{ V}$
			40	V max	$GND = 0\text{ V}$ , $V_{SS} = 0\text{ V}$



**36 V SINGLE SUPPLY**

$V_{DD} = 36\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $V_L = 2.7\text{ V}$  to  $5.5\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 4.**

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance, $R_{ON}$	14.5			$\Omega$ typ	$V_S = 0\text{ V}$ to $30\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 29
On-Resistance Match Between Channels, $\Delta R_{ON}$	16 0.3	19	23	$\Omega$ max $\Omega$ typ	$V_{DD} = 32.4\text{ V}$ , $V_{SS} = 0\text{ V}$ $V_S = 0\text{ V}$ to $30\text{ V}$ , $I_S = -10\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	0.8 3.5 4.3	1.3	1.4 6.5	$\Omega$ max $\Omega$ typ $\Omega$ max	$V_S = 0\text{ V}$ to $30\text{ V}$ , $I_S = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = 39.6\text{ V}$ , $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V}/30\text{ V}$ , $V_D = 30\text{ V}/1\text{ V}$ ; see Figure 32
Drain Off Leakage, $I_D$ (Off)	$\pm 0.25$ $\pm 0.1$	$\pm 1$	$\pm 7$	nA max nA typ	$V_S = 1\text{ V}/30\text{ V}$ , $V_D = 30\text{ V}/1\text{ V}$ ; see Figure 32
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.25$ $\pm 0.15$	$\pm 1$	$\pm 7$	nA max nA typ	$V_S = V_D = 1\text{ V}/30\text{ V}$ ; see Figure 28
	$\pm 0.4$	$\pm 2$	$\pm 14$	nA max	
<b>DIGITAL OUTPUT</b>					
Output Voltage Low, $V_{OL}$			0.4 0.2	V max V max	$I_{SINK} = 5\text{ mA}$ $I_{SINK} = 1\text{ mA}$
Output Current, $I_{OL}$ or $I_{OH}$	0.001		$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{OUT} = V_{GND}$ or $V_L$
Digital Output Capacitance, $C_{OUT}$	4			pF typ	
<b>DIGITAL INPUTS</b>					
Input Voltage High, $V_{INH}$			2	V min	$3.3\text{ V} < V_L \leq 5.5\text{ V}$
Low, $V_{INL}$			1.35 0.8 0.8	V min V max V max	$2.7\text{ V} \leq V_L \leq 3.3\text{ V}$ $3.3\text{ V} < V_L \leq 5.5\text{ V}$ $2.7\text{ V} \leq V_L \leq 3.3\text{ V}$
Input Current, $I_{INL}$ or $I_{INH}$	0.001		$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{GND}$ or $V_L$
Digital Input Capacitance, $C_{IN}$	4			pF typ	
<b>DYNAMIC CHARACTERISTICS</b>					
$t_{ON}$	425			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	435	515	515	ns max	$V_S = 18\text{ V}$ ; see Figure 37
$t_{OFF}$	145			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	151	195	195	ns max	$V_S = 18\text{ V}$ ; see Figure 37
Break-Before-Make Time Delay, $t_D$	260			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	245		205	ns min	$V_{S1} = V_{S2} = 18\text{ V}$ ; see Figure 36
Charge Injection, $Q_{INJ}$	145			pC typ	$V_S = 18\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 38
Off Isolation	-60			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 31
Channel to Channel Crosstalk	-75			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Figure 30

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments	
THD + N	0.04			% typ	$R_L = 1\text{ k}\Omega$ , 18 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 33	
-3 dB Bandwidth	200			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 34	
Insertion Loss	-0.85			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 34	
$C_S$ (Off)	11			pF typ	$V_S = 18\text{ V}$ , $f = 1\text{ MHz}$	
$C_D$ (Off)	11			pF typ	$V_S = 18\text{ V}$ , $f = 1\text{ MHz}$	
$C_D$ (On), $C_S$ (On)	26			pF typ	$V_S = 18\text{ V}$ , $f = 1\text{ MHz}$	
<b>POWER REQUIREMENTS</b>						
$I_{DD}$	80			$\mu\text{A typ}$	$V_{DD} = 39.6\text{ V}$ All switches open	
			130	$\mu\text{A max}$	All switches open	
	80			$\mu\text{A typ}$	All switches closed, $V_L = 5.5\text{ V}$	
			130	$\mu\text{A max}$	All switches closed, $V_L = 5.5\text{ V}$	
$I_L$	330			$\mu\text{A typ}$	All switches closed, $V_L = 2.7\text{ V}$	
			490	$\mu\text{A max}$	All switches closed, $V_L = 2.7\text{ V}$	
	Inactive	6.3			$\mu\text{A typ}$	Digital inputs = 0 V or $V_L$
				8.0	$\mu\text{A max}$	
SCLK = 1 MHz	14			$\mu\text{A typ}$	$\overline{CS}$ and SDI = 0 V or $V_L$ , $V_L = 5\text{ V}$	
	7			$\mu\text{A typ}$	$\overline{CS}$ and SDI = 0 V or $V_L$ , $V_L = 3\text{ V}$	
SCLK = 50 MHz	390			$\mu\text{A typ}$	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 5\text{ V}$	
	210			$\mu\text{A typ}$	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 3\text{ V}$	
SDI = 1 MHz	15			$\mu\text{A typ}$	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 5\text{ V}$	
	7.5			$\mu\text{A typ}$	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 3\text{ V}$	
SDI = 25 MHz	230			$\mu\text{A typ}$	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 5\text{ V}$	
	120			$\mu\text{A typ}$	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 3\text{ V}$	
Active at 50 MHz	1.8			mA typ	Digital inputs toggle between 0 V and $V_L$ , $V_L = 5.5\text{ V}$	
		2	2.1	mA max		
	0.7			mA typ	Digital inputs toggle between 0 V and $V_L$ , $V_L = 2.7\text{ V}$	
Single-Supply Operation ( $V_{DD}$ )			1.0	mA max		
			9	V min	$GND = 0\text{ V}$ , $V_{SS} = 0\text{ V}$	
			40	V max	$GND = 0\text{ V}$ , $V_{SS} = 0\text{ V}$	

**CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx Pins****Table 5. Eight Channels On**

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx PINS				
$V_{DD} = +15\text{ V}, V_{SS} = -15\text{ V} (\theta_{JA} = 50^\circ\text{C/W})$	82	61	38	mA maximum
$V_{DD} = +20\text{ V}, V_{SS} = -20\text{ V} (\theta_{JA} = 50^\circ\text{C/W})$	86	63	41	mA maximum
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V} (\theta_{JA} = 50^\circ\text{C/W})$	63	47	29	mA maximum
$V_{DD} = 36\text{ V}, V_{SS} = 0\text{ V} (\theta_{JA} = 50^\circ\text{C/W})$	85	62	40	mA maximum

**Table 6. One Channel On**

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx PINS				
$V_{DD} = +15\text{ V}, V_{SS} = -15\text{ V} (\theta_{JA} = 50^\circ\text{C/W})$	199	124	75	mA maximum
$V_{DD} = +20\text{ V}, V_{SS} = -20\text{ V} (\theta_{JA} = 50^\circ\text{C/W})$	210	129	77	mA maximum
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V} (\theta_{JA} = 50^\circ\text{C/W})$	157	104	68	mA maximum
$V_{DD} = 36\text{ V}, V_{SS} = 0\text{ V} (\theta_{JA} = 50^\circ\text{C/W})$	206	127	76	mA maximum

**TIMING SPECIFICATIONS**

$V_L = 2.7\text{ V}$  to  $5.5\text{ V}$ ;  $GND = 0\text{ V}$ ; all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

**Table 7.**

Parameter	Limit	Unit	Test Conditions/Comments
TIMING CHARACTERISTICS			
$t_1$	20	ns min	SCLK period
$t_2$	8	ns min	SCLK high pulse width
$t_3$	8	ns min	SCLK low pulse width
$t_4$	10	ns min	$\overline{CS}$ falling edge to SCLK active edge
$t_5$	6	ns min	Data setup time
$t_6$	8	ns min	Data hold time
$t_7$	10	ns min	SCLK active edge to $\overline{CS}$ rising edge
$t_8$	20	ns max	$\overline{CS}$ falling edge to SDO data available
$t_9^1$	20	ns max	SCLK falling edge to SDO data available
$t_{10}$	20	ns max	$\overline{CS}$ rising edge to SDO returns to high impedance
$t_{11}$	20	ns min	$\overline{CS}$ high time between SPI commands
$t_{12}$	8	ns min	$\overline{CS}$ falling edge to SCLK becomes stable
$t_{13}$	8	ns min	$\overline{CS}$ rising edge to SCLK becomes stable

<sup>1</sup> Measured with the 1 k $\Omega$  pull-up resistor to  $V_L$  and a 20 pF load.  $t_9$  determines the maximum SCLK frequency when using SDO.

Timing Diagrams

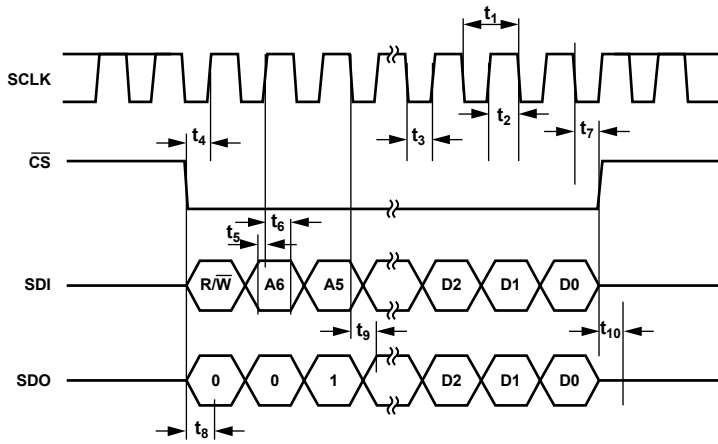


Figure 2. Addressable Mode Timing Diagram

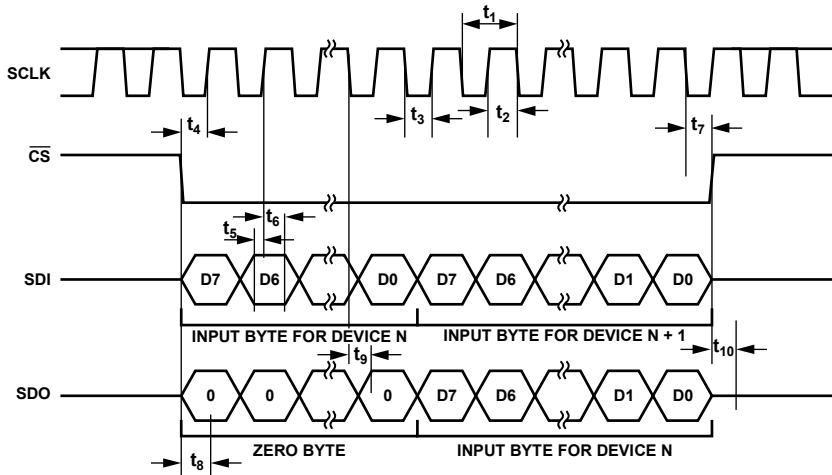


Figure 3. Daisy Chain Timing Diagram

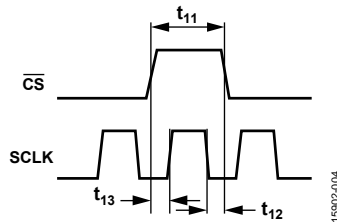


Figure 4. SCLK/CS Timing Diagram

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 8.**

Parameter	Rating
$V_{DD}$ to $V_{SS}$	48 V
$V_{DD}$ to GND	-0.3 V to +48 V
$V_{SS}$ to GND	+0.3 V to -48 V
$V_L$ to GND	-0.3 V to +5.75 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	-0.3 V to +5.75 V
Peak Current, Sx or Dx Pins	422 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx Pins <sup>2</sup>	Data (see Table 5 and Table 6) + 15%
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb Free	260(+0 or -5)°C
Human Body Model (HBM) Electrostatic Discharge (ESD)	8 kV

<sup>1</sup> Overvoltages at the Sx and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.

<sup>2</sup> See Table 5 and Table 6.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

### THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

$\theta_{JA}$  is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.  $\theta_{JC}$  is the junction to case thermal resistance.

**Table 9. Thermal Resistance**

Package Type	$\theta_{JA}$	$\theta_{JC}^2$	Unit
CP-24-17 <sup>1</sup>	50	3.28	°C/W

<sup>1</sup> Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD51.

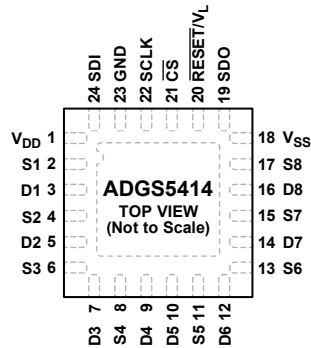
<sup>2</sup>  $\theta_{JCB}$  is the junction to the bottom of the case value.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



## NOTES

1. EXPOSED PAD. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE EXPOSED PAD BE SOLDERED TO THE SUBSTRATE,  $V_{SS}$ .

16902-005

Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{DD}$	Most Positive Power Supply Potential.
2	S1	Source Terminal 1. This pin can be an input or output.
3	D1	Drain Terminal 1. This pin can be an input or output.
4	S2	Source Terminal 2. This pin can be an input or output.
5	D2	Drain Terminal 2. This pin can be an input or output.
6	S3	Source Terminal 3. This pin can be an input or output.
7	D3	Drain Terminal 3. This pin can be an input or output.
8	S4	Source Terminal 4. This pin can be an input or output.
9	D4	Drain Terminal 4. This pin can be an input or output.
10	D5	Drain Terminal 5. This pin can be an input or output.
11	S5	Source Terminal 5. This pin can be an input or output.
12	D6	Drain Terminal 6. This pin can be an input or output.
13	S6	Source Terminal 6. This pin can be an input or output.
14	D7	Drain Terminal 7. This pin can be an input or output.
15	S7	Source Terminal 7. This pin can be an input or output.
16	D8	Drain Terminal 8. This pin can be an input or output.
17	S8	Source Terminal 8. This pin can be an input or output.
18	$V_{SS}$	Most Negative Power Supply Potential. In single-supply applications, tie this pin to ground.
19	SDO	Serial Data Output. This pin can daisy-chain a numeral ADGS5414 devices together or for reading back the data stored in a register for diagnostic purposes. The serial data is propagated on the falling edge of SCLK. Pull this open-drain output to $V_L$ with an external resistor.
20	$\overline{\text{RESET}}/V_L$	$\overline{\text{RESET}}$ /Logic Power Supply Input ( $V_L$ ). Under normal operation, drive the $\overline{\text{RESET}}/V_L$ pin with a 2.7 V to 5.5 V supply. Pull the pin low to complete a hardware reset. All switches are opened, and the appropriate registers are set to their default.
21	$\overline{\text{CS}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{CS}}$ goes low, it powers on the SCLK buffers and enables the input shift register. Data is transferred in on the falling edges of the following clocks. Taking $\overline{\text{CS}}$ high updates the switch condition.
22	SCLK	Serial Clock Input. Data is captured on the positive edge of SCLK. Data can be transferred at rates of up to 50 MHz.
23	GND	Ground (0 V) Reference.
24	SDI Exposed Pad	Serial Data Input. Data is captured on the positive edge of the serial clock input. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, $V_{SS}$ .

# TYPICAL PERFORMANCE CHARACTERISTICS

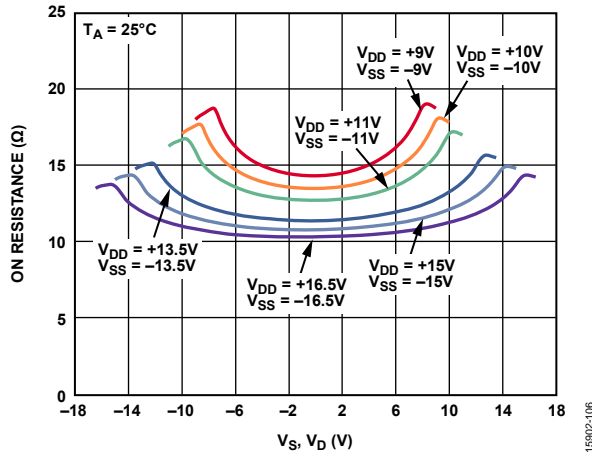


Figure 6.  $R_{ON}$  as a Function of  $V_S$  and  $V_D$  (Dual Supply)

15902-106

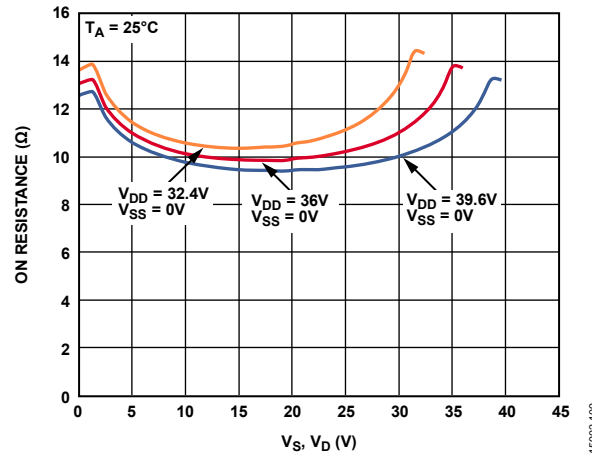


Figure 9.  $R_{ON}$  as a Function of  $V_S$  and  $V_D$  (Single Supply)

15902-109

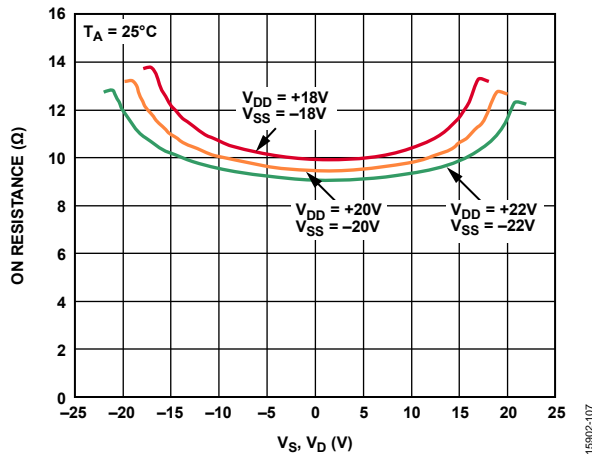


Figure 7.  $R_{ON}$  as a Function of  $V_S$  and  $V_D$  (Dual Supply)

15902-107

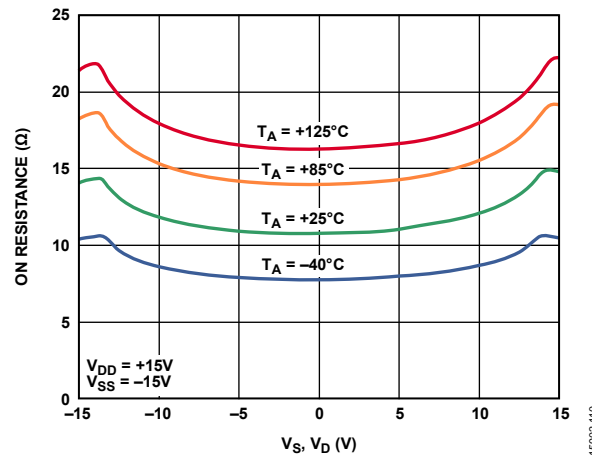


Figure 10.  $R_{ON}$  as a Function of  $V_S$  and  $V_D$  for Different Temperatures,  $\pm 15$  V Dual Supply

15902-110

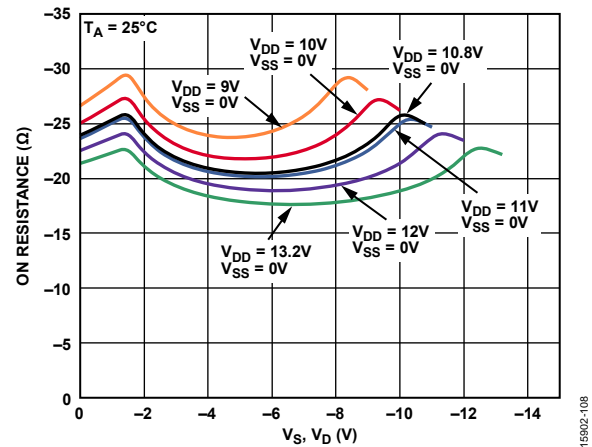


Figure 8.  $R_{ON}$  as a Function of  $V_S$  and  $V_D$  (Single Supply)

15902-108

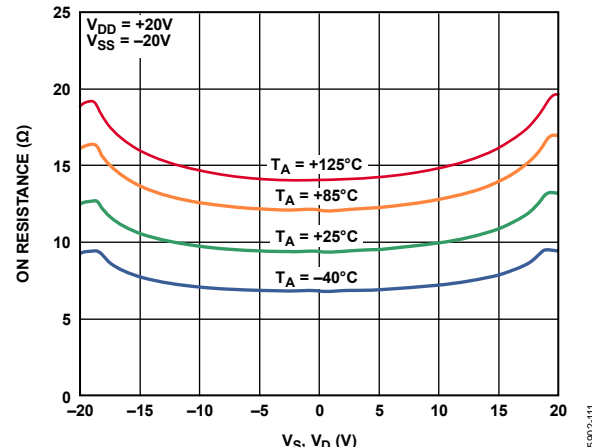


Figure 11.  $R_{ON}$  as a Function of  $V_S$  and  $V_D$  for Different Temperatures,  $\pm 20$  V Dual Supply

15902-111

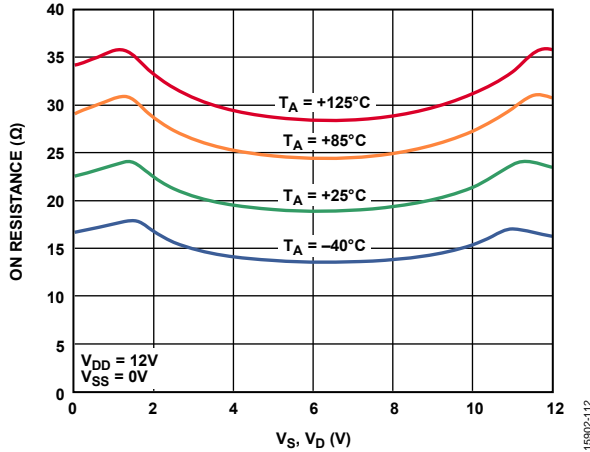


Figure 12.  $R_{ON}$  as a Function of  $V_S$  and  $V_D$  for Different Temperatures, 12 V Single Supply

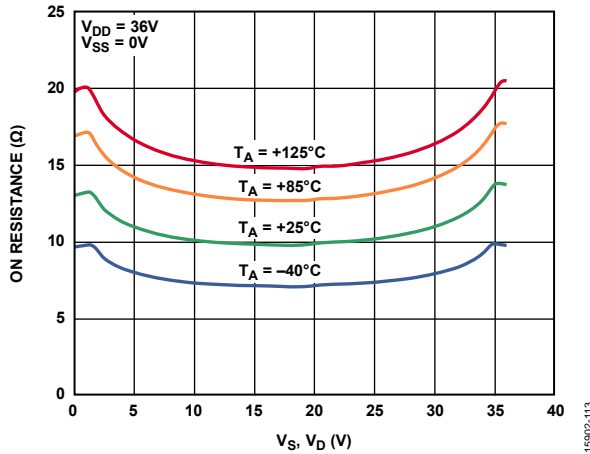


Figure 13.  $R_{ON}$  as a Function of  $V_S$  and  $V_D$  for Different Temperatures, 36 V Single Supply

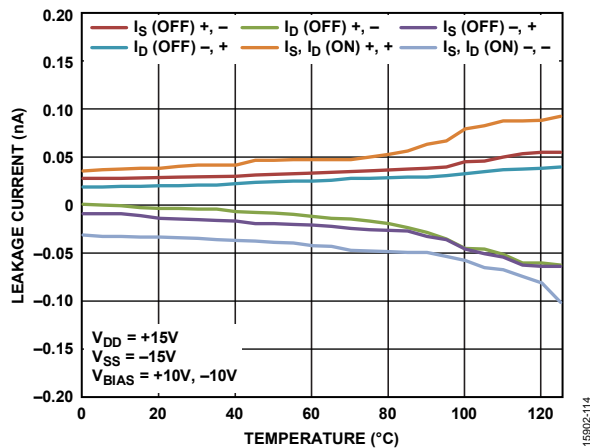


Figure 14. Leakage Currents vs. Temperature,  $\pm 15\text{V}$  Dual Supply

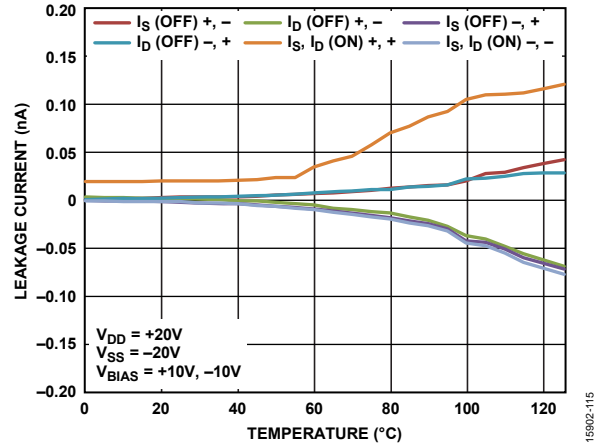


Figure 15. Leakage Currents vs. Temperature,  $\pm 20\text{V}$  Dual Supply

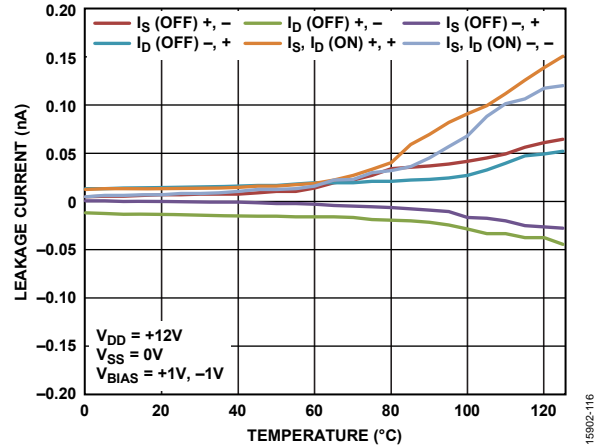


Figure 16. Leakage Currents vs. Temperature, 12 V Single Supply

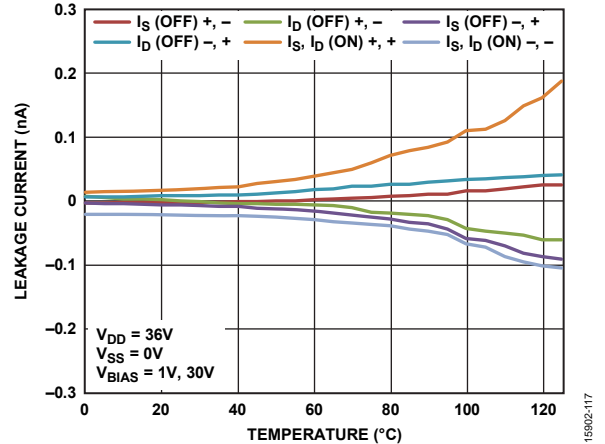


Figure 17. Leakage Currents vs. Temperature, 36 V Single Supply



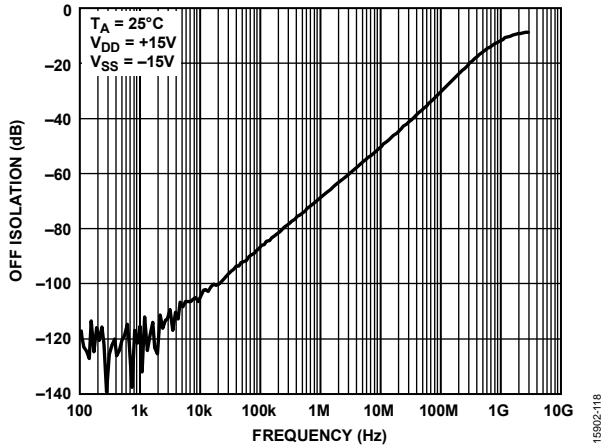


Figure 18. Off Isolation vs. Frequency, ±15 V Dual Supply

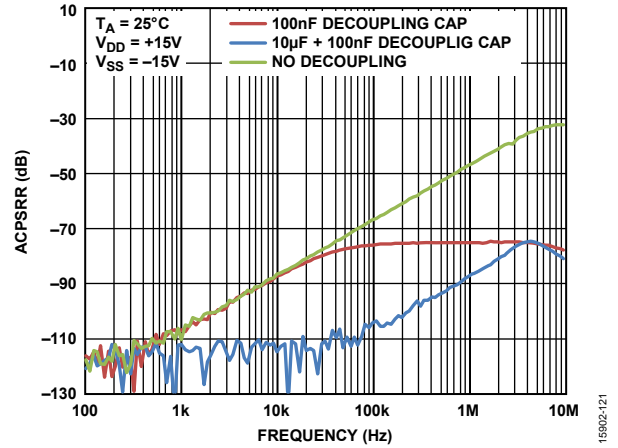


Figure 21. ACPSRR vs. Frequency, ±15 V Dual Supply

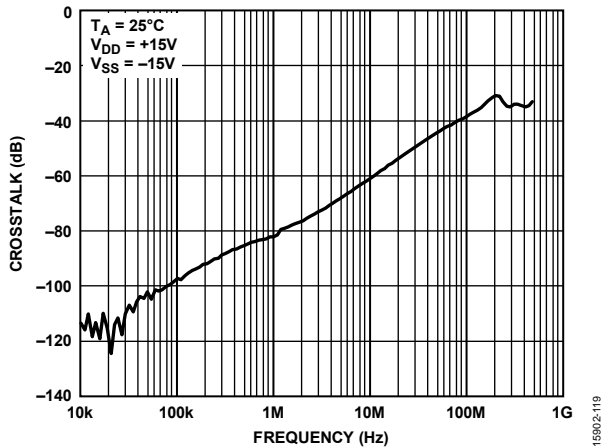


Figure 19. Crosstalk vs. Frequency, ±15 V Dual Supply

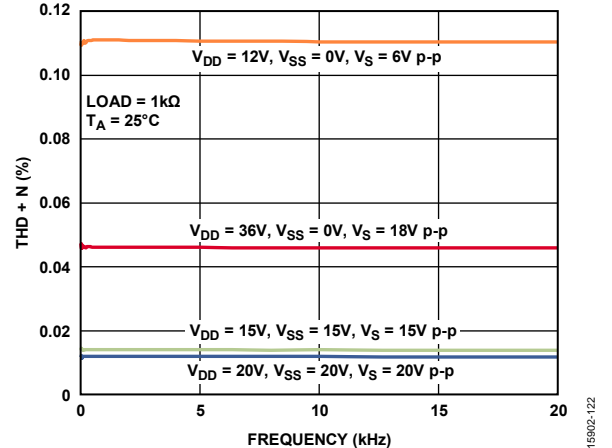


Figure 22. THD + N vs. Frequency, Dual Supply

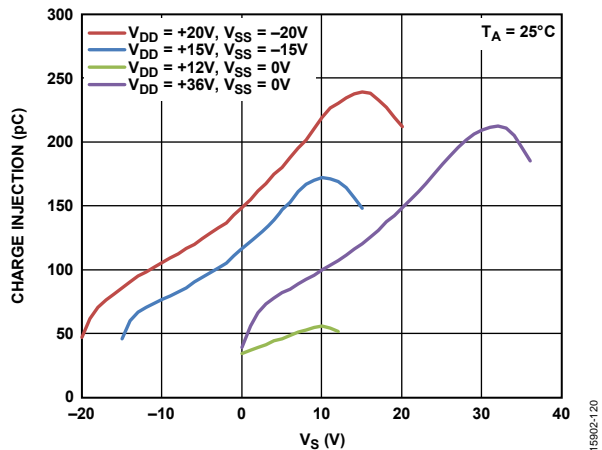


Figure 20. Charge Injection vs. Vs

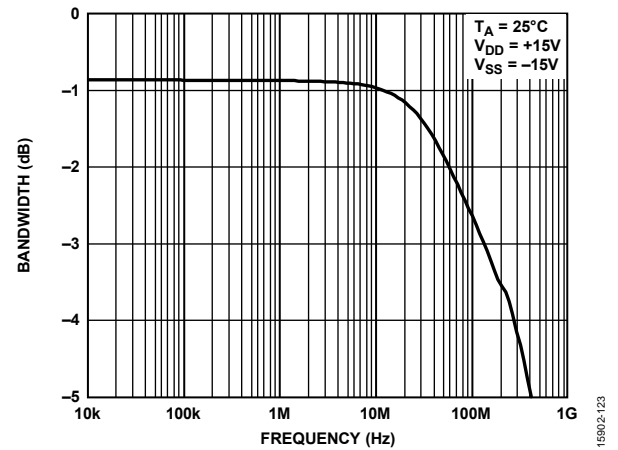


Figure 23. Bandwidth vs. Frequency

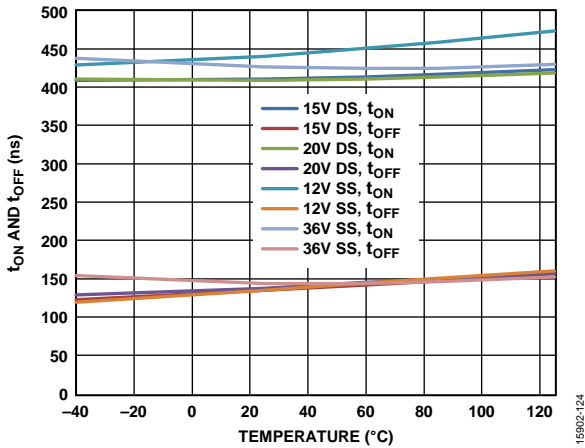


Figure 24.  $t_{ON}$  and  $t_{OFF}$  Times vs. Temperature

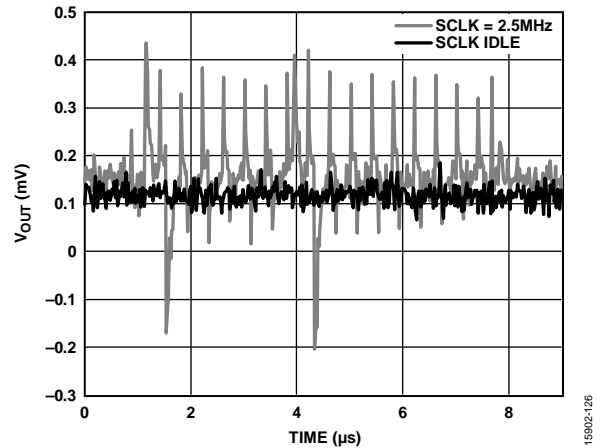


Figure 26. Digital Feedthrough

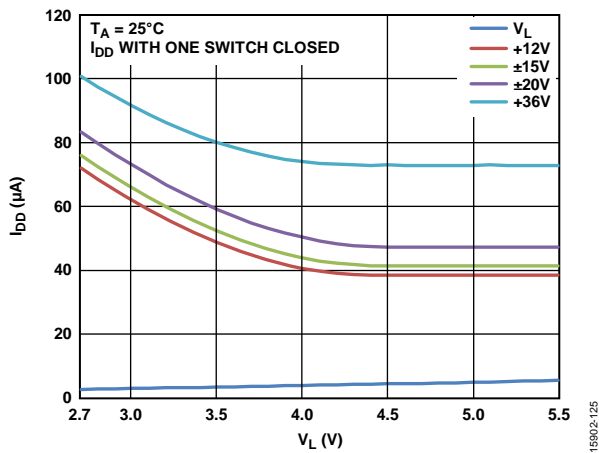


Figure 25.  $I_{DD}$  vs.  $V_L$

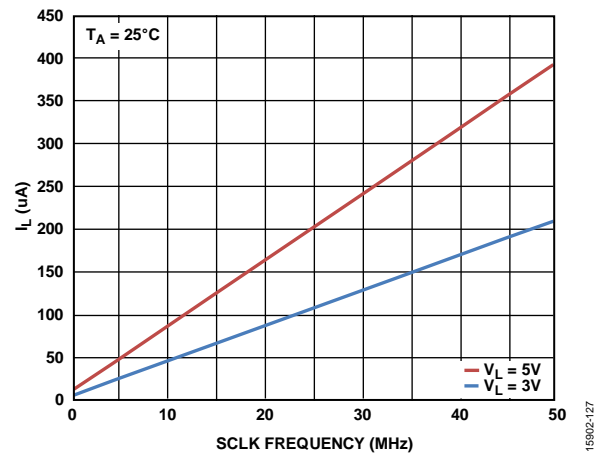


Figure 27.  $I_L$  vs. SCLK Frequency when  $\overline{CS}$  is High

TEST CIRCUITS

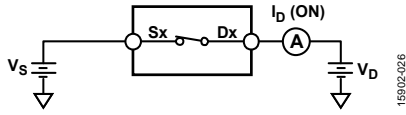


Figure 28. On Leakage

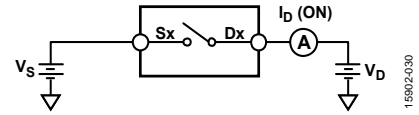


Figure 32. Off Leakage

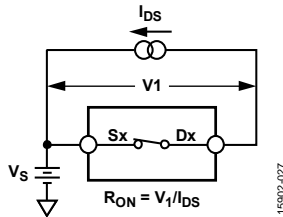


Figure 29. On Resistance

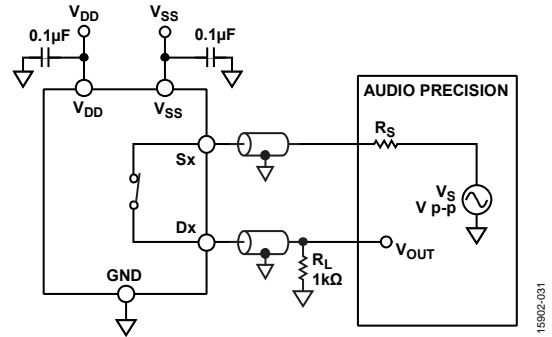
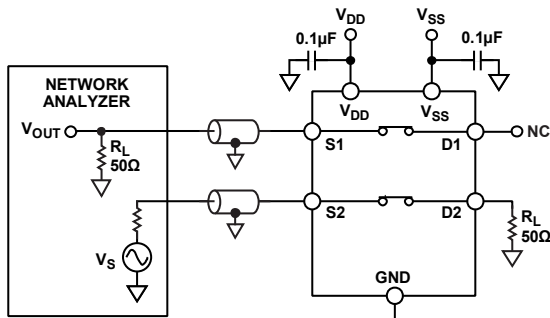
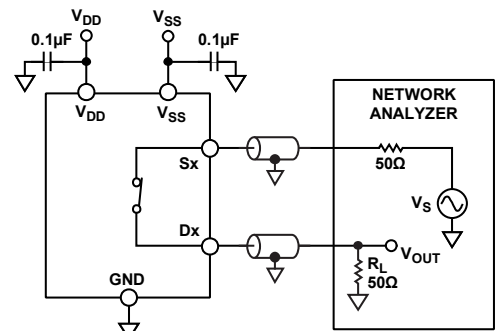


Figure 33. THD + Noise



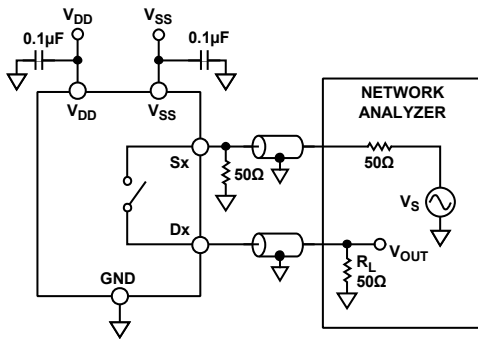
$$\text{CHANNEL TO CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{V_S}$$

Figure 30. Channel to Channel Crosstalk



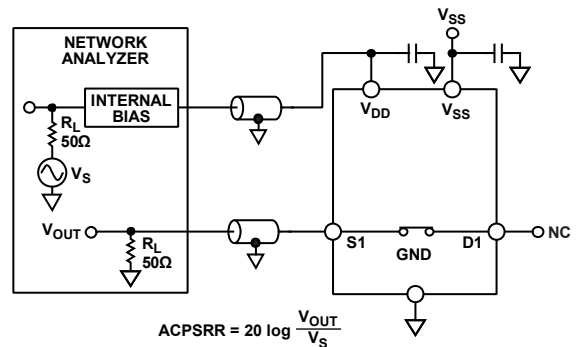
$$\text{INSERTION LOSS} = 20 \log \frac{V_{OUT \text{ WITH SWITCH}}}{V_S \text{ WITHOUT SWITCH}}$$

Figure 34. Bandwidth



$$\text{OFF ISOLATION} = 20 \log \frac{V_{OUT}}{V_S}$$

Figure 31. Off Isolation



$$\text{ACPSRR} = 20 \log \frac{V_{OUT}}{V_S}$$

Figure 35. ACPSRR

NOTES  
1. BOARD AND COMPONENT EFFECTS ARE NOT DE-EMBEDDED FROM THE ACPSRR MEASUREMENT.

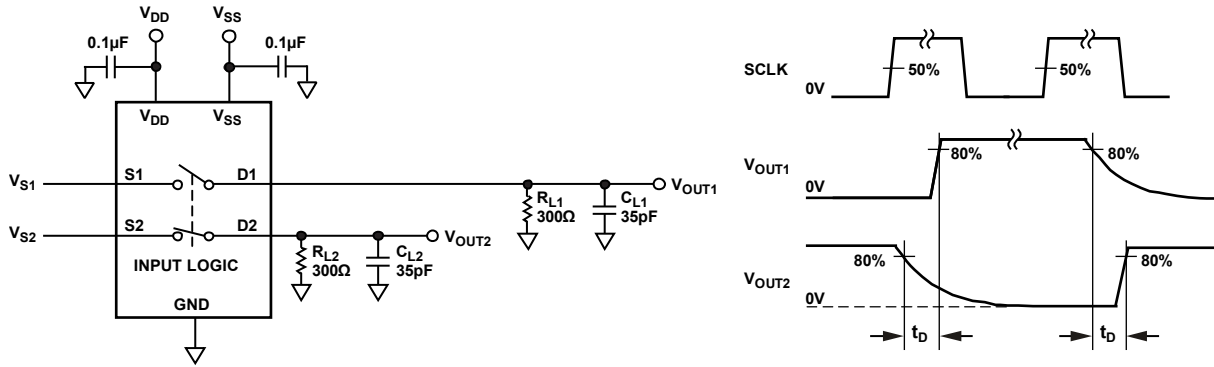


Figure 36. Break-Before-Make Time Delay,  $t_D$

15902-034

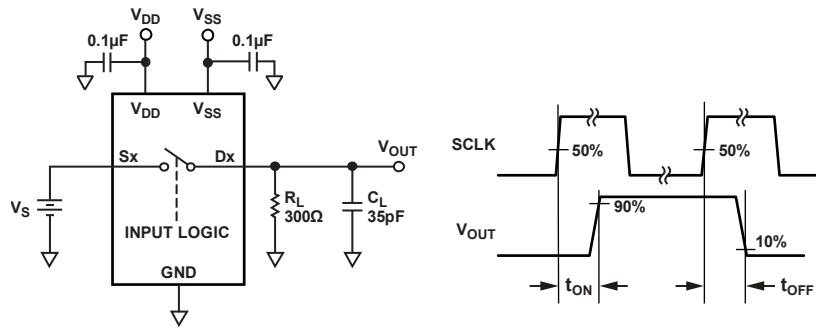


Figure 37. Switching Times

15902-035

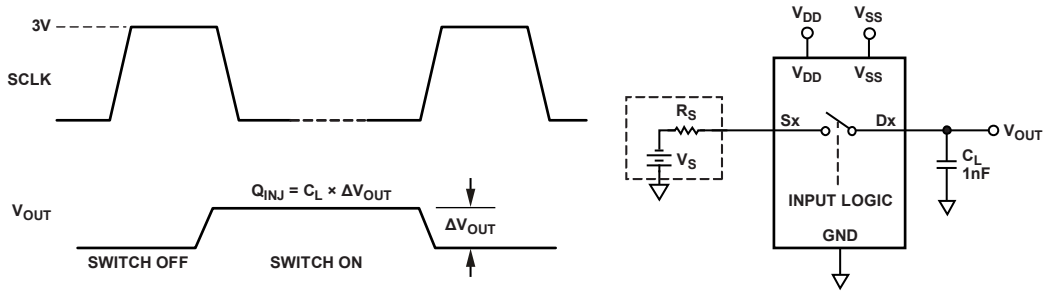


Figure 38. Charge Injection

15902-036

## TERMINOLOGY

### $I_{DD}$

$I_{DD}$  is the positive supply current.

### $I_{SS}$

$I_{SS}$  is the negative supply current.

### $V_D, V_S$

$V_D$  and  $V_S$  are the analog voltages on Terminal D and Terminal S, respectively.

### $R_{ON}$

$R_{ON}$  represents the ohmic resistance between Terminal D and Terminal S.

### $\Delta R_{ON}$

$\Delta R_{ON}$  is the difference between the  $R_{ON}$  of any two channels.

### $R_{FLAT(ON)}$

$R_{FLAT(ON)}$  is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

### $I_S$ (Off)

$I_S$  (Off) is the source leakage current with the switch off.

### $I_D$ (Off)

$I_D$  (Off) is the drain leakage current with the switch off.

### $I_D$ (On), $I_S$ (On)

$I_D$  (On) and  $I_S$  (On) are the channel leakage currents with the switch on.

### $V_{INL}$

$V_{INL}$  is the maximum input voltage for Logic 0.

### $V_{INH}$

$V_{INH}$  is the minimum input voltage for Logic 1.

### $I_{INL}, I_{INH}$

$I_{INL}$  and  $I_{INH}$  are the low and high input currents of the digital inputs.

### $C_D$ (Off)

$C_D$  (Off) is the off switch drain capacitance, which is measured with reference to GND.

### $C_S$ (Off)

$C_S$  (Off) is the off switch source capacitance, which is measured with reference to GND.

### $C_D$ (On), $C_S$ (On)

$C_D$  (On) and  $C_S$  (On) are the on switch capacitances, which are measured with reference to GND.

### $C_{IN}$

$C_{IN}$  is the digital input capacitance.

### $t_{ON}$

$t_{ON}$  is the delay between applying the digital control input and the output switching on.

### $t_{OFF}$

$t_{OFF}$  is the delay between applying the digital control input and the output switching off.

### $t_D$

$t_D$  is the off time measured between the 80% point of both switches when switching from one address state to another.

### Off Isolation

Off isolation is a measure of unwanted signal coupling through an off switch.

### Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

### Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

### Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB.

### On Response

On response is the frequency response of the on switch.

### Insertion Loss

Insertion loss is the loss due to the on resistance of the switch.

### Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

### AC Power Supply Rejection Ratio (ACPSRR)

ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. ACPSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

## THEORY OF OPERATION

The ADGS5414 is a set of SPI controlled, octal SPST switches with error detection features. SPI Mode 0 and Mode 3 can be used with the device, and it operates with SCLK frequencies up to 50 MHz. The default mode for the ADGS5414 is address mode in which the registers of the device are accessed by a 16-bit SPI command that is bounded by  $\overline{CS}$ . The SPI command becomes 24 bits long if the user enables CRC error detection. Other error detection features include SCLK count error detection and invalid read/write error detection. If any of these SPI interface errors occur, they are detectable by reading the error flags register. The ADGS5414 can also operate in two other modes: burst mode and daisy-chain mode.

The interface pins of the ADGS5414 are  $\overline{CS}$ , SCLK, SDI, and SDO. Hold  $\overline{CS}$  low when using the SPI interface. Data is captured on SDI on the rising edge of SCLK, and data is propagated out on SDO on the falling edge of SCLK. SDO has an open-drain output; thus, connect a pull-up to this output. When not pulled low by the ADGS5414, SDO is in a high impedance state.

### ADDRESS MODE

Address mode is the default mode for the ADGS5414 upon power-up. A single SPI frame in address mode is bounded by a  $\overline{CS}$  falling edge and the succeeding  $\overline{CS}$  rising edge. The SPI frame is comprised of 16 SCLK cycles. The timing diagram for address mode is shown in Figure 39. The first SDI bit indicates if the SPI command is a read or write command. When the first bit is set to 0, a write command is issued, and if the first bit is set to 1, a read command is issued. The next seven bits determine the target register address. The remaining eight bits provide the data to the addressed register. The last eight bits are ignored during a read command, because, during these clock cycles, SDO propagates out the data contained in the addressed register.

The target register address of an SPI command is determined on the eighth SCLK rising edge. Data from this register propagates out on SDO from the ninth to the 16<sup>th</sup> SCLK falling edge during SPI reads.

A register write occurs on the 16<sup>th</sup> SCLK rising edge during SPI writes.

During any SPI command, SDO sends out eight alignment bits on the first eight SCLK falling edges. The alignment bits observed at SDO are 0x25.

### ERROR DETECTION FEATURES

Protocol and communication errors on the SPI interface are detectable. There are three detectable errors: incorrect SCLK error detection, invalid read and write address error detection, and CRC error detection. Each of these errors has a corresponding enable bit in the error configuration register. In addition, there is an error flag bit for each of these errors in the error flags register.

#### CRC Error Detection

The CRC error detection feature extends a valid SPI frame by eight SCLK cycles. These eight extra cycles send the CRC byte for that SPI frame. The CRC byte is calculated by the SPI block using the 16-bit payload: the R/W bit, a selected register address, Bits[6:0], and selected Register Data Bits[7:0]. The CRC polynomial used in the SPI block is  $x^8 + x^2 + x^1 + 1$  with a seed value of 0. For a timing diagram with CRC enabled, see Figure 40. Register writes occur at the 24<sup>th</sup> SCLK rising edge with CRC error checking enabled.

During an SPI write, the microcontroller or computer processing unit (CPU) provides the CRC byte through SDI. The SPI block checks the CRC byte just before the 24<sup>th</sup> SCLK rising edge. On this same edge, the register write is prevented if an incorrect CRC byte is received by the SPI interface. The CRC error flag is asserted in the error flags register in the case of the incorrect CRC byte being detected.

During an SPI read, the CRC byte is provided to the microcontroller through SDO.

The CRC error detection feature is disabled by default and can be configured by the user through the error configuration register.

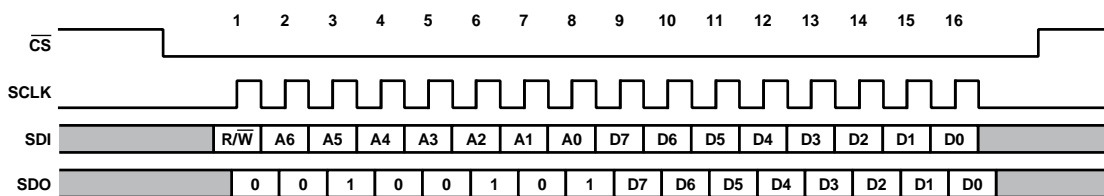


Figure 39. Address Mode Timing Diagram

15902-037

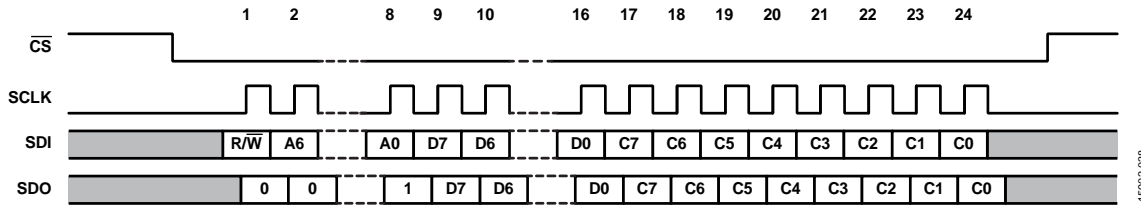


Figure 40. Timing Diagram with CRC Enabled

**SCLK Count Error Detection**

SCLK count error detection allows the user to detect if an incorrect number of SCLK cycles are sent by the microcontroller or CPU. When in address mode, with CRC disabled, 16 SCLK cycles are expected. If 16 SCLK cycles are not detected, the SCLK count error flag asserts in the error flags register. When less than 16 SCLK cycles are received by the device, a write to the register map does not occur. When the ADGS5414 receives more than 16 SCLK cycles, a write to the memory map still occurs at the 16<sup>th</sup> SCLK rising edge, and the flag asserts in the error flags register. With CRC enabled, the expected number of SCLK cycles becomes 24. SCLK count error detection is enabled by default and can be configured by the user through the error configuration register.

**Invalid Read/Write Address Error**

An invalid read/write address error detects when a nonexistent register address is a target for a read or write. In addition, this error asserts when a write to a read only register is attempted. The invalid read/write address error flag asserts in the error flags register when an invalid read/write address error occurs. The invalid read/write address error is detected on the ninth SCLK rising edge, which means a write to the register does not occur when an invalid address is targeted. Invalid read/write address error detection is enabled by default and can be disabled by the user through the error configuration register.

**CLEARING THE ERROR FLAGS REGISTER**

To clear the error flags register, write the 16-bit SPI frame (not included in the register map), 0x6CA9, to the device. This SPI command does not trigger the invalid R/W address error. When CRC is enabled, the user must send the correct CRC byte for a successful error clear command. At the 16<sup>th</sup> or 24<sup>th</sup> SCLK rising edge, the error flags register resets to zero.

**BURST MODE**

The SPI interface can accept consecutive SPI commands without the need to deassert the CS line, which is called burst mode. Burst mode is enabled through the burst enable register (Address 0x05). This mode uses the same 16-bit command to communicate with the device. In addition, the response of the device at SDO is still aligned with the corresponding SPI command. Figure 41 shows an example of SDI and SDO during burst mode.

The invalid read/write address and CRC error checking functions operate similarly during burst mode as they do during address mode. However, SCLK count error detection operates in a slightly different manner. The total number of SCLK cycles within a given CS frame is counted, and if the total is not a multiple of 16, or a multiple of 24 when CRC is enabled, the SCLK count error flag asserts.

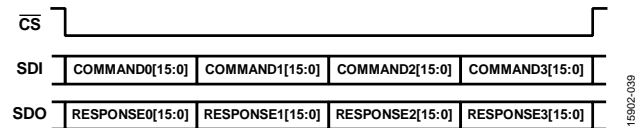


Figure 41. Burst Mode Frame

**SOFTWARE RESET**

When in address mode, the user can initiate a software reset. To do so, write two consecutive SPI commands, namely 0xA3 followed by 0x05, to Register 0x0B. After a software reset, all register values are set to default.

**DAISY-CHAIN MODE**

The connection of several ADGS5414 devices in a daisy-chain configuration is possible, and Figure 42 shows this setup. All devices share the same CS and SCLK line, whereas the SDO of a device forms a connection to the SDI of the next device, creating a shift register. In daisy-chain mode, SDO is an eight cycle delayed version of SDI. When in daisy-chain mode, all commands target the switch data register (SW\_DATA). Therefore, it is not possible to make configuration changes while in daisy-chain mode.

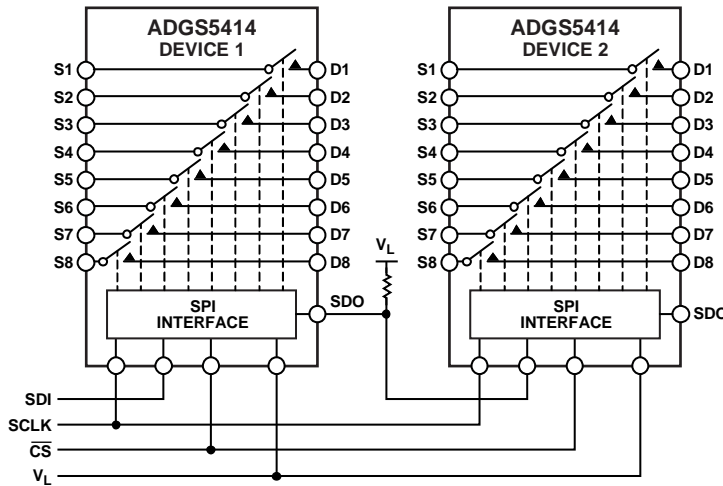


Figure 42. Two SPI Controlled Switches Connected in a Daisy-Chain Configuration

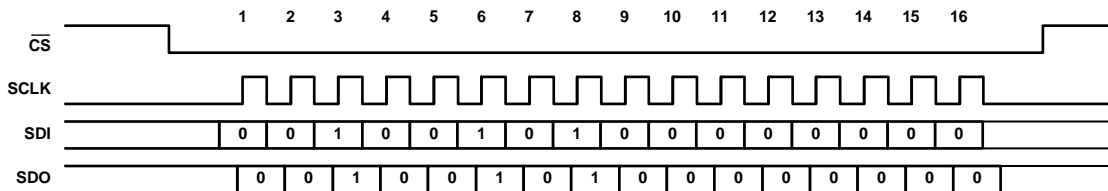
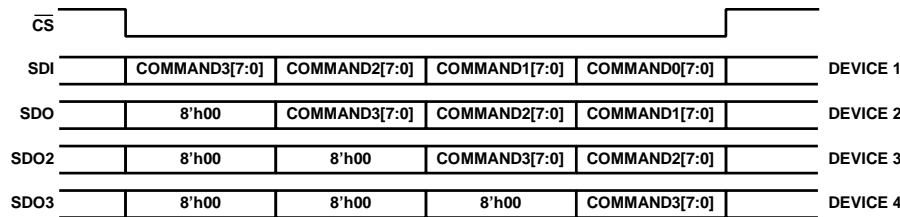


Figure 43. SPI Command to Enter Daisy-Chain Mode



NOTES  
1. SDO2 AND SDO3 ARE THE OUTPUT COMMANDS FROM DEVICE 2 AND DEVICE 3, RESPECTIVELY.

Figure 44. Example of an SPI Frame when Four ADGS5414 Devices are Connected in Daisy-Chain Mode

The ADGS5414 can only enter daisy-chain mode when in address mode by sending the 16-bit SPI command, 0x2500 (see Figure 43). When the ADGS5414 receives this command, the SDO of the device sends out the same command because the alignment bits at SDO are 0x25, which allows multiple daisy-connected devices to enter daisy-chain mode in a single SPI frame. A hardware reset is required to exit daisy-chain mode.

For the timing diagram of a typical daisy-chain SPI frame, see Figure 44. For example, when CS goes high, Device 1 writes Command 0, SW\_DATA, Bits[7:0] to its switch data register, Device 2 writes Command 1, SW\_DATA, Bits[7:0] to its switches. The SPI block uses the last eight bits it receives through SDI to update the switches. After entering daisy-chain mode, the first eight bits sent out by SDO on each device in the chain are 0x00. When CS goes high, the internal shift register value does not reset back to zero.

An SCLK rising edge reads in data on SDI while data is propagated out on SDO on an SCLK falling edge. The expected number of SCLK cycles must be a multiple of eight before CS goes high. If this is not the case, the SPI interface sends the last eight bits received to the switch data register.

### POWER-ON RESET

The digital section of the ADGS5414 goes through an initialization phase during V<sub>L</sub> power-up. This initialization also occurs after a hardware or software reset. After V<sub>L</sub> power-up or a reset, ensure a minimum of 120 μs from the time of power-up or reset before any SPI command is issued. Ensure V<sub>L</sub> does not drop out during the 120 μs initialization phase because it can result in the incorrect operation of the ADGS5414.



**BREAK-BEFORE-MAKE SWITCHING**

The ADGS5414 exhibits break-before-make switching action, which allows the use of the device in multiplexer applications. A multiplexer function can be achieved by externally hardwiring the device in the required mux configuration, as shown in Figure 45.

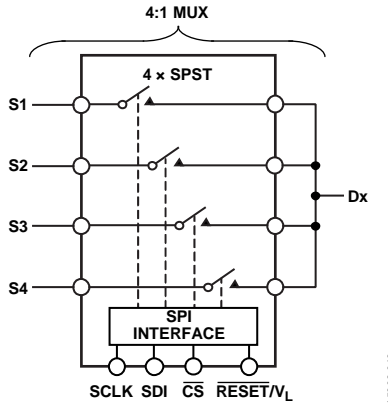


Figure 45. An SPI Controlled Switch Configured in a 4:1 Mux

**TRENCH ISOLATION**

In the analog switch section of the ADGS5414, an insulating oxide layer (trench) is placed between the N-type metal-oxide semiconductor (NMOS) and the P-type metal-oxide semiconductor (PMOS) transistors of each complementary metal-oxide semiconductor CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the P-well and N-well of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) circuit is formed by the two transistors, causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

The Analog Devices, Inc., high voltage latch-up proof family of switches and multiplexers provides a robust solution for instrumentation, industrial, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off. The ADGS5414 high voltage switches allow single-supply operation from 9 V to 40 V and dual-supply operation from ±9 V to ±22 V.

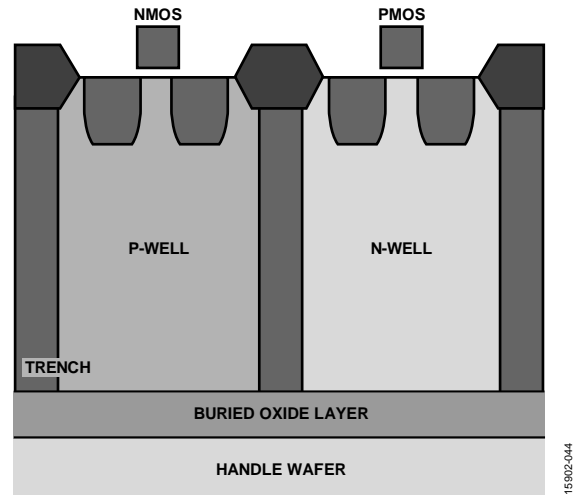


Figure 46. Trench Isolation

## APPLICATIONS INFORMATION

### POWER SUPPLY RAILS

To guarantee correct operation of the ADGS5414, 0.1  $\mu\text{F}$  decoupling capacitors are required.

The ADGS5414 can operate with bipolar supplies between  $\pm 9\text{ V}$  and  $\pm 22\text{ V}$ . The supplies on  $V_{\text{DD}}$  and  $V_{\text{SS}}$  do not need to be symmetrical; however, the  $V_{\text{DD}}$  to  $V_{\text{SS}}$  range must not exceed 44 V. The ADGS5414 can also operate with single supplies between 9 V and 40 V with  $V_{\text{SS}}$  connected to GND.

The voltage range that can be supplied to  $V_{\text{I}}$  is from 2.7 V to 5.5 V.

The device is fully specified at  $\pm 15\text{ V}$ ,  $\pm 20\text{ V}$ ,  $+12\text{ V}$ , and  $+36\text{ V}$ , analog supply voltage ranges.

### POWER SUPPLY RECOMMENDATIONS

Analog Devices has a wide range of power management products that meet the requirements of most high performance signal chains.

An example of a bipolar power solution is shown in Figure 47. The ADP5070 dual switching regulator generates a positive and negative supply rail for the ADGS5414, an amplifier, and/or a precision converter in a typical signal chain.

Figure 47 also shows two optional low dropout regulators (LDOs), ADP7118 and ADP7182, positive and negative LDOs respectively, that can reduce the output ripple of the ADP5070 in ultralow noise sensitive applications.

The ADM7160 can be used to generate the  $V_{\text{L}}$  voltage that is required to power the digital circuitry within the ADGS5414.

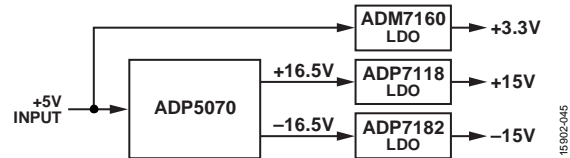


Figure 47. Bipolar Power Solution

Table 10. Recommended Power Management Devices

Product	Description
ADP5070	1 A/0.6 A, dc-to-dc switching regulator with independent positive and negative outputs
ADM7160	5.5 V, 200 mA, ultralow noise, linear regulator
ADP7118	20 V, 200 mA, low noise, CMOS LDO linear regulator
ADP7182	-28 V, -200 mA, low noise, LDO linear regulator

## REGISTER SUMMARY

Table 11. Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	RW
0x01	SW_DATA	SW8_EN	SW7_EN	SW6_EN	SW5_EN	SW4_EN	SW3_EN	SW2_EN	SW1_EN	0x00	R/W
0x02	ERR_CONFIG	Reserved					RW_ERR_EN	SCLK_ERR_EN	CRC_ERR_EN	0x06	R/W
0x03	ERR_FLAGS	Reserved					RW_ERR_FLAG	SCLK_ERR_FLAG	CRC_ERR_FLAG	0x00	R
0x05	BURST_EN	Reserved							BURST_MODE_EN	0x00	R/W
0x0B	SOFT_RESETB	SOFT_RESETB								0x00	R/W

## REGISTER DETAILS

### SWITCH DATA REGISTER

SW\_DATA, Address 0x01, Reset: 0x00

The switch data register controls the status of the eight switches of the ADGS5414.

Table 12. Bit Descriptions for SW\_DATA

Bit	Bit Name	Setting	Description	Default	Access
7	SW8_EN		Enable bit for Switch 8.	0x0	R/W
		0	Switch 8 open.		
		1	Switch 8 closed.		
		6	SW7_EN		Enable bit for Switch 7.
0	Switch 7 open.				
		1	Switch 7 closed.		
		5	SW6_EN		Enable bit for Switch 6.
0	Switch 6 open.				
		1	Switch 6 closed.		
		4	SW5_EN		Enable bit for Switch 5.
0	Switch 5 open.				
		1	Switch 5 closed.		
		3	SW4_EN		Enable bit for Switch 4.
0	Switch 4 open.				
		1	Switch 4 closed.		
		2	SW3_EN		Enable bit for Switch 3.
0	Switch 3 open.				
		1	Switch 3 closed.		
		1	SW2_EN		Enable bit for Switch 2.
0	Switch 2 open.				
		1	Switch 2 closed.		
		0	SW1_EN		Enable bit for Switch 1.
0	Switch 1 open.				
		1	Switch 1 closed.		

### ERROR CONFIGURATION REGISTER

ERR\_CONFIG, Address 0x02, Reset: 0x06

The error configuration register allows the user to enable or disable the relevant error features as required.

Table 13. Bit Descriptions for ERR\_CONFIG

Bit	Bit Name	Setting	Description	Default	Access
[7:3]	Reserved		These bits are reserved; set these bits to 0.	0x0	R
2	RW_ERR_EN		Enable bit for detecting an invalid read/write address.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
		1	SCLK_ERR_EN		Enable bit for detecting the correct number of SCLK cycles in an SPI frame. 16 SCLK cycles are expected when CRC is disabled and burst mode is disabled. 24 SCLK cycles are expected when CRC is enabled and burst mode is disabled. A multiple of 16 SCLK cycles is expected when CRC is disabled and burst mode is enabled. A multiple of 24 SCLK cycles is expected when CRC is enabled and burst mode is enabled.
0	Disabled.				
		1	Enabled.		
		0	CRC_ERR_EN		Enable bit for CRC error detection. SPI frames must be 24 bits wide when enabled.
0	Disabled.				
		1	Enabled.		

**ERROR FLAGS REGISTER****ERR\_FLAGS, Address 0x03, Reset: 0x00,**

The error flags register allows the user to determine if an error occurs. To clear the error flags register, write the special 16-bit SPI command, 0x6CA9, to the device. This SPI command does not trigger the invalid R/W address error. When CRC is enabled, the user must include the correct CRC byte during the SPI write for the clear Error Flags Register command to be successful.

**Table 14. Bit Descriptions for ERR\_FLAGS**

Bit	Bit Name	Setting	Description	Default	Access
[7:3]	RESERVED		These bits are reserved and are set to 0.	0x0	R
2	RW_ERR_FLAG	0 1	Error flag for invalid read/write address. The error flag asserts during an SPI read if the target address does not exist. The error flag also asserts when the target address of a SPI write is does not exist or is read only. No Error. Error.	0x0	R
1	SCLK_ERR_FLAG	0 1	Error flag for the detection of the correct number of SCLK cycles in an SPI frame. No Error. Error.	0x0	R
0	CRC_ERR_FLAG	0 1	Error Flag that determines if a CRC error occurs during a register write. No Error. Error.	0x0	R

**BURST ENABLE REGISTER****BURST\_EN, Address 0x05, Reset: 0x00**

The burst enable register allows the user to enable/disable the burst mode. When enabled, the user can send multiple consecutive SPI commands without deasserting CS.

**Table 15. Bit Descriptions for BURST\_EN**

Bits	Bit Name	Settings	Description	Default	Access
[7:1]	Reserved		These bits are reserved; set these bits to 0.	0x0	R
0	BURST_MODE_EN	0 1	Burst mode enable bit. Disabled. Enabled.	0x0	R/W

**SOFTWARE RESET REGISTER****SOFT\_RESETB, Address 0x0B, Reset: 0x00**

This register performs a software reset. Consecutively, write 0xA3 and 0x05 to this register and to reset the device registers to their default state.

**Table 15. Bit Descriptions for SOFT\_RESETB**

Bits	Bit Name	Settings	Description	Default	Access
[7:0]	SOFT_RESETB		To Perform a Software Reset, consecutively write 0xA3 followed by 0x05 to this register.	0x0	R