35 dB Gain, 500 MHz to 5200 MHz Transmit VGA

FEATURES

- Single-channel, high-linearity transmit VGA for RF DACs, transceivers, and SoCs to power amplifier interface
- Single 5 V supply
- Multiple versions covering frequencies of 500 MHz to 5200 MHz
- Power gain: 37.4 dB (ADL6337-A), 35.5 dB (ADL6337-B), 34 dB (ADL6337-C), 35.5 dB (ADL6337-D)
- OIP3: 42.0 dBm (ADL6337-A), 42.5 dBm (ADL6337-B), 38 dBm (ADL6337-C), 40 dBm (ADL6337-D)
- OIP2: 50 dBm (ADL6337-A), 55 dBm (ADL6337-B), 68 dBm (ADL6337-C), 74 dBm (ADL6337-D)
- Noise figure: 3.7 dB (ADL6337-A), 4.5 dB (ADL6337-B), 5.2 dB (ADL6337-C), 4.5 dB (ADL6337-D)
- OP1dB: 26.1 dBm (ADL6337-A), 26.0 dBm (ADL6337-B), 25.5 dBm (ADL6337-C), 23.5 dBm (ADL6337-D)
- RF DSA attenuation range: 31.5 dB with 0.5 dB resolution
- 50 Ω/100 Ω differential inputs and 50 Ω single-ended output
- Fully programmable via a 3-/4-wire SPI
- 32-lead, 5 mm × 5 mm LFCSP

APPLICATIONS

- 2G/3G/4G/long-term evolution (LTE) in FDD/TDD broadband
- Communication systems

GENERAL DESCRIPTION

The ADL6337 belongs to a family of transmit variable gain amplifiers (VGAs). It provides an interface from RF digital-to-analog converters (DACs), transceivers, and systems on a chip (SoC) to power amplifiers. It also includes an integrated RF balun and can be configured as a differential input, single-ended output to allow high-performance RF capability in the 500 MHz to 5200 MHz frequency range.

To optimize performance vs. power level, the ADL6337 includes high linearity amplifiers and a glitch free digital step attenuator (DSA). All of the ADL6337 components are programmable via a 3- or 4-wire serial port interface (SPI).

The ADL6337 is manufactured on an advanced silicon germanium (SiGe), bipolar complementary metal-oxide semiconductor (BiCMOS) process.

Table 1. ADL6337 Frequency Ranges

ADL6337 Variant	Frequency Range (MHz)
A	500 to 1000
B	1350 to 2800
C	3100 to 4400
D	4400 to 5200

FUNCTIONAL BLOCK DIAGRAM

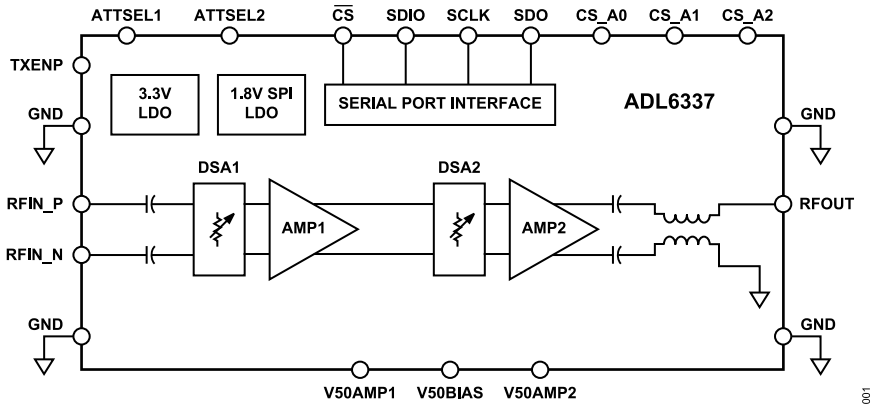

Figure 1. Functional Block Diagram

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REVISION HISTORY

11/2023—Rev. C to Rev. D

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SPECIFICATIONS

V50AMP1 voltage (V_{50AMP1}) = V50AMP2 voltage (V_{50AMP2}) = V50BIAS voltage (V_{50BIAS}) = 5.0 V, T_A = 25°C, input power (P_{IN}) = −25 dBm (–25 dBm per tone for two tones), DSA attenuation = 0 dB, source resistance (R_S) = load resistance (R_L) = 50 Ω, unless otherwise noted.

Table 2. Electrical Characteristics

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE (ADL6337-A)		500		1000	MHz
Noise/Linearity Performance					
Power Gain			37.4		dB
Output 1 dB Compression Point (OP1dB)	DSA = 0 dB		26.1		dBm
	DSA = 16 dB		23.0		dBm
	DSA = 31.5 dB		23.0		dBm
Output Second-Order Intercept (OIP2)			50		dBm
Output Third-Order Intercept (OIP3)	DSA = 0 dB		42.0		dBm
	DSA = 16 dB		35.5		dBm
	DSA = 31.5 dB		35.5		dBm
Noise Figure	DSA = 0 dB		3.7		dB
	DSA = 16 dB		5.3		dB
FREQUENCY RANGE (ADL6337-B)		1350		2800	MHz
Noise/Linearity Performance					
Power Gain			35.5		dB
OP1dB	DSA = 0 dB		26.0		dBm
	DSA = 16 dB		22.0		dBm
	DSA = 31.5 dB		22.0		dBm
OIP2			55		dBm
OIP3	DSA = 0 dB,		42.5		dBm
	DSA = 16 dB,		33.5		dBm
	DSA = 31.5 dB		33.5		dBm
Noise Figure	DSA = 0 dB		4.5		dB
	DSA = 16 dB		5.9		dB
FREQUENCY RANGE (ADL6337-C)		3100		4400	MHz
Noise/Linearity Performance					
Power Gain			34.0		dB
OP1dB	DSA = 0 dB		25.5		dBm
	DSA = 16 dB		18.8		dBm
	DSA = 31.5 dB		18.8		dBm
OIP2			68.0		dBm
OIP3	DSA = 0 dB		38.0		dBm
	DSA = 16 dB		32.0		dBm
	DSA = 31.5 dB		32.0		dBm
Noise Figure	DSA = 0 dB		5.2		dB
	DSA = 16 dB		8.3		dB
FREQUENCY RANGE (ADL6337-D)		4400		5200	MHz
Noise/Linearity Performance					
Power Gain			35.5		dB
OP1dB	DSA = 0 dB		23.5		dBm
	DSA = 16 dB		17.5		dBm
	DSA = 31.5 dB		17.5		dBm
OIP2			74		dBm
OIP3	DSA = 0 dB		40		dBm
	DSA = 16 dB		30.5		dBm
	DSA = 31.5 dB		30.5		dBm

SPECIFICATIONS

Table 2. Electrical Characteristics (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Noise Figure	DSA = 0 dB		4.5		dB
	DSA = 16 dB		9.0		dB
RF INPUT/OUTPUT CHARACTERISTICS					
Input					
Impedance	Differential		50		Ω
Return Loss	Inband, see the RF Input and Output section	10	15		dB
Output					
Impedance	Single-ended		50		Ω
Return Loss	Inband	10	18		dB
Gain Flatness, fc > 1.5 GHz	Over ±100 MHz bandwidth		±0.1		dB
	Over ±250 MHz bandwidth		±0.2		dB
	Over ±500 MHz bandwidth		±0.9		dB
Gain Flatness, 0.5 GHz < f_C < 1.5 GHz	Over ±40 MHz bandwidth		±0.1		dB
	Over ±100 MHz bandwidth		±0.2		dB
	Over ±200 MHz bandwidth		±0.5		dB
Settling Time for Disable to Enable				1	µs
Settling Time for Enable to Disable				1	µs
DSA Attenuation					
Range		31.5			dB
Step Size		0.4	0.5	0.6	dB
Gain Settling Time	Minimum attenuation to maximum attenuation		387		ns
	Maximum attenuation to minimum attenuation		1700		ns
POWER SUPPLY					
Voltage		4.75	5.0	5.25	V
Supply Current	High performance mode		460		mA
	Low power mode		380	400	mA
Power-Down Current			14		mA
DIGITAL LOGIC					
Input Voltage	SCLK, SDIO, $\overline{CS}$, CS_A2, CS_A1, CS_A0, TXENP				
High (V_{IH})		1.07			V
Low (V_{IL})				0.68	V
Input Current					
High (I_{IH})				−100	µA
Low (I_{IL})				100	µA
Output Voltage	SDO				
At 1.8 V	Register 0x121, Bit 4 = 0x0				
High (V_{OH})	Output high current (I_{OH}) = −100 µA or −1 mA static load	1.5			V
Low (V_{OL})	Output low current (I_{OL}) = 100 µA or 1 mA static load			0.2	V
At 3.3 V	Register 0x121, Bit 4 = 0x1				
High (V_{OH})	I_{OH} = −100 µA or −1 mA static load	2.7			V
Low (V_{OL})	I_{OL} = 100 µA or 1 mA static load			0.2	V

DIGITAL LOGIC TIMING

Table 3. SPI AC Timing

Parameter	Description	Min	Typ	Max	Unit
f_{SCLK}	Maximum serial clock rate, 1/t_{SCLK}			25	MHz
t_{PWH}	Minimum period that SCLK is in logic-high state	10			ns
t_{PWL}	Minimum period that SCLK is in logic-low state	10			ns

SPECIFICATIONS

Table 3. SPI AC Timing (Continued)

Parameter	Description	Min	Typ	Max	Unit
t_{DS}	Setup time between data and rising edge of SCLK	5			ns
t_{DH}	Hold time between data and rising edge of SCLK	5			ns
t_{DCS}	Setup time between falling edge of $\overline{CS}$ and rising edge of SCLK	10			ns
t_H	Hold time between rising edge of $\overline{CS}$ and the last falling edge of SCLK, minimum 10 ns	10			ns
t_{DV}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		5	14	ns
t_Z	Maximum time delay between $\overline{CS}$ deactivation and SDIO bus return to high impedance			12	ns

Timing Diagrams

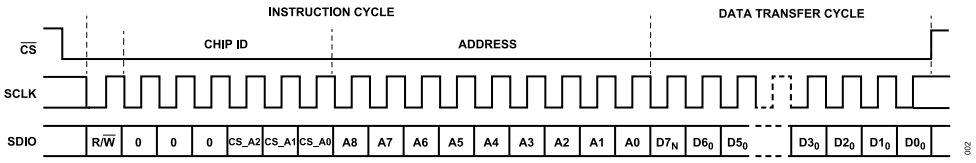

Figure 2. SPI Register Timing, MSB First

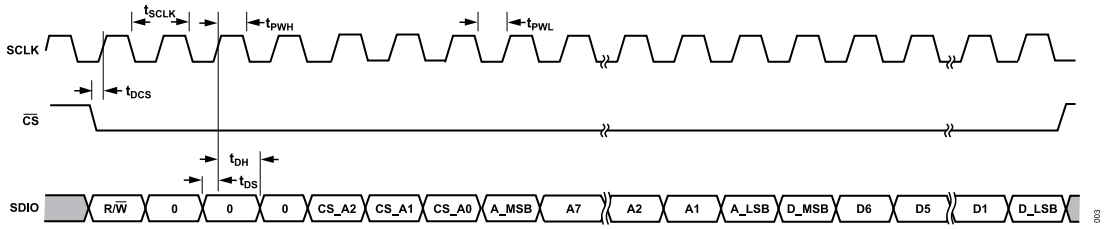

Figure 3. Timing Diagram for the SPI Register Write (3- and 4-Wire SPI Mode)

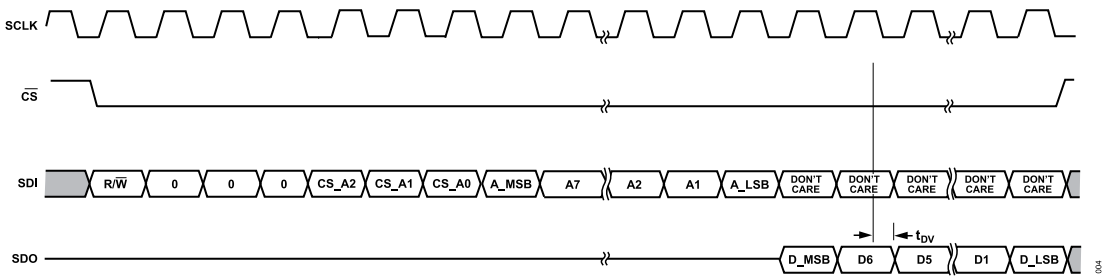

Figure 4. Timing Diagram for SPI Register Read (4-Wire SPI Mode)

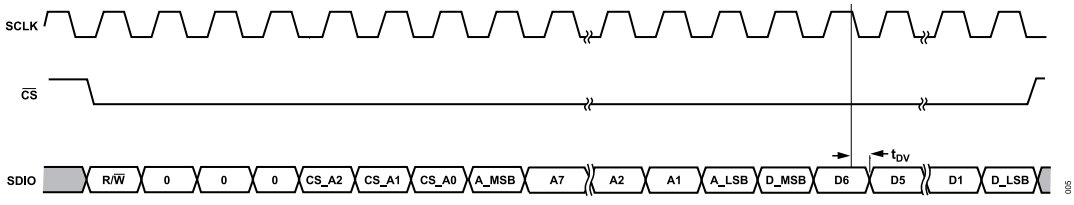

Figure 5. Timing Diagram for SPI Register Read (3-Wire SPI Mode, SDIO Pin is Bidirectional Mode)

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
V_{50AMP1}, V_{50AMP2}, V_{50BIAS}	−0.3 V to +5.6 V
SCLK, SDI, SDIO, $\overline{CS}$, CS_A2, CS_A1, CS_A0, TXENP	−0.3 V to +3.6 V
RF Input Power (IN_N, IN_P) at 50 Ω	10 dBm
Temperature	−40°C to +105°C
Operating Range (Measured at Exposed Pad)	
Junction Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the conduction thermal resistance from junction to case where the case temperature is measured at the bottom of the package.

The thermal resistance value specified in Table 5 is simulated based on JEDEC specifications (unless specified otherwise) and must be used in compliance with JESD51-12.

Table 5. Thermal Resistance

Package Type	θ_{JC}	Unit
CR-32-3	7.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

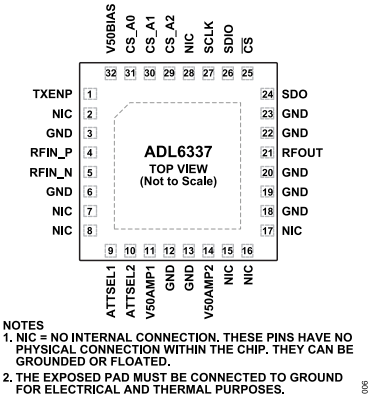

Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	TXENP	Input	Amplifier Enable.
2, 7, 8, 15, 16, 17, 28	NIC		No Internal Connection. These pins have no physical connection within the chip. They can be grounded or floated.
3, 6, 12, 13, 18, 19, 20, 22, 23	GND	Input/Output	Ground.
4	RFIN_P	Input	Positive RF Input.
5	RFIN_N	Input	Negative RF Input.
9	ATTSEL1	Input	Fast Attenuation Selection.
10	ATTSEL2	Input	Fast Attenuation Selection.
11	V50AMP1	Input	Amplifier 1 Analog Power Supply (5.0 V).
14	V50AMP2	Input	Amplifier 2 Analog Power Supply (5.0 V).
21	RFOUT	Output	Single-Ended RF Output.
24	SDO	Output	Serial Port Data Output in 4-Wire SPI Mode. Analog Devices, Inc., recommends to leave this pin floating when 3-wire SPI mode is used.
25	$\overline{CS}$	Input	Serial Port Latch Enable Input.
26	SDIO	Input/Output	Serial Port Bidirectional Data Input/Output.
27	SCLK	Input	Serial Port Clock Input.
29	CS_A2	Input	Chip Select. Refer to the Configuring Multiple Chips to Share the SPI Bus section for information about the connections in a multiple chip operation. Ground these pins if unused.
30	CS_A1	Input	Chip Select. Refer to the Configuring Multiple Chips to Share the SPI Bus section for information about the connections in a multiple chip operation. Ground these pins if unused.
31	CS_A0	Input	Chip Select. Refer to the Configuring Multiple Chips to Share the SPI Bus section for information about the connections in a multiple chip operation. Ground these pins if unused.
32	V50BIAS	Input	Bias Circuitry Power Supply (5.0 V)
	EPAD	Input/Output	Exposed Pad 1. The exposed pad must be connected to ground for electrical and thermal purposes.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{50AMP1} = V_{50AMP2} = 5 V, T_A = 25°C.

ADL6337-A: for the TRM_AMPx_IPx and TRM_AMPx_IREF_x bit settings, see the ADL6337-A section.

ADL6337-B: for the TRM_AMPx_IPx and TRM_AMPx_IREF_x bit settings, see the ADL6337-B section.

ADL6337-C: for the TRM_AMPx_IPx and TRM_AMPx_IREF_x bit settings, see the ADL6337-C section.

ADL6337-D: for the TRM_AMPx_IPx and TRM_AMPx_IREF_x bit settings, see the ADL6337-D section.

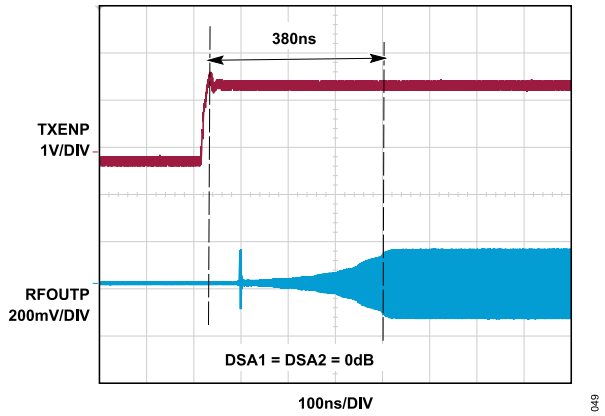

Figure 7. TXENP Enable Response at Minimum DSA Attenuation

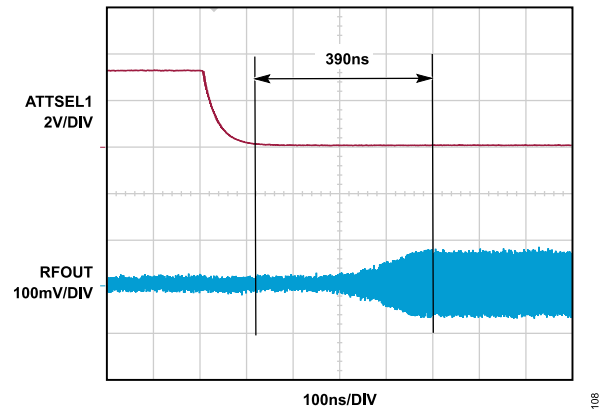

Figure 8. Gain Settling Time at DSA2 = 15.75 dB (Maximum), DSA1 from 15.75 dB to 0.00 dB

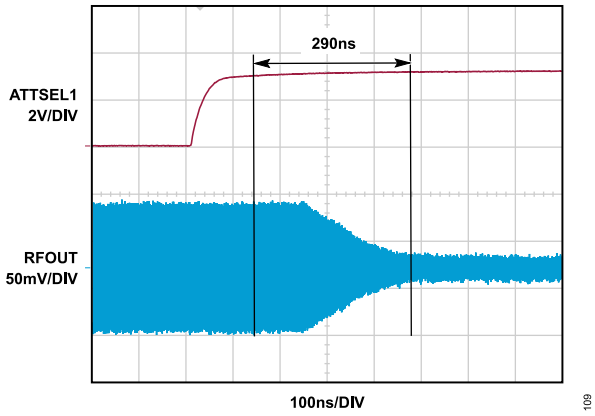

Figure 9. Gain Settling Time at DSA2 = 15.75 dB (Maximum), DSA1 from 0.00 dB to 15.75 dB

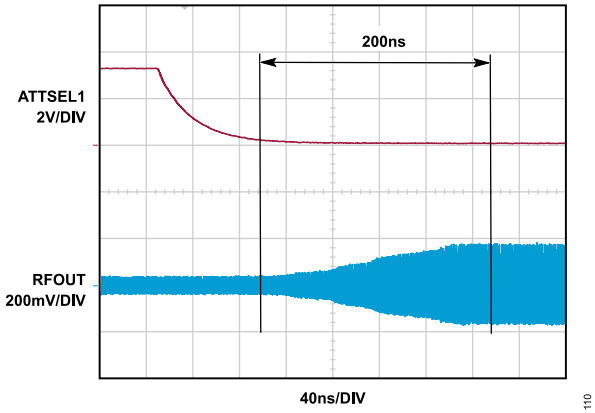

Figure 10. Gain Settling Time at DSA1 = 0.00 dB (Minimum), DSA2 from 15.75 dB to 0.00 dB

TYPICAL PERFORMANCE CHARACTERISTICS

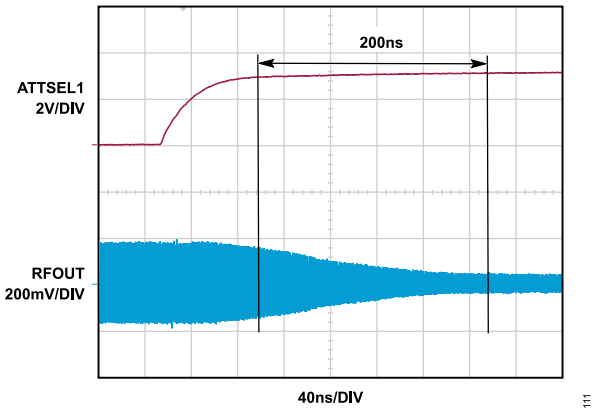

Figure 11. Gain Settling Time at DSA1 = 0.00 dB (Minimum), DSA2 from 0.00 dB to 15.75 dB

TYPICAL PERFORMANCE CHARACTERISTICS

ADL6337-A

V_{50AMP1} = V_{50AMP2} = 5 V, T_A = 25°C, input power = −25 dBm (−25 dBm per tone for two tones), DSA attenuation= 0 dB, R_S = R_L = 50 Ω, TRM_AMP1_IP3_0 = 2, TRM_AMP2_IP3_ = 3, TRM_AMP1_IREF_0_0 = TRM_AMP1_IREF_1 = TRM_AMP1_IREF_2 = TRM_AMP1_IREF_3 = 13, TRM_AMP2_IREF_0_0 = TRM_AMP2_IREF_1 = TRM_AMP2_IREF_2 = TRM_AMP2_IREF_3 = 11, unless otherwise noted.

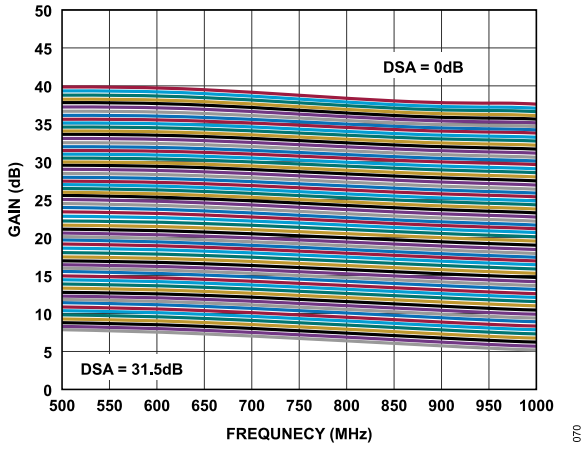

Figure 12. Gain vs. Frequency; 0.5 dB DSA Steps

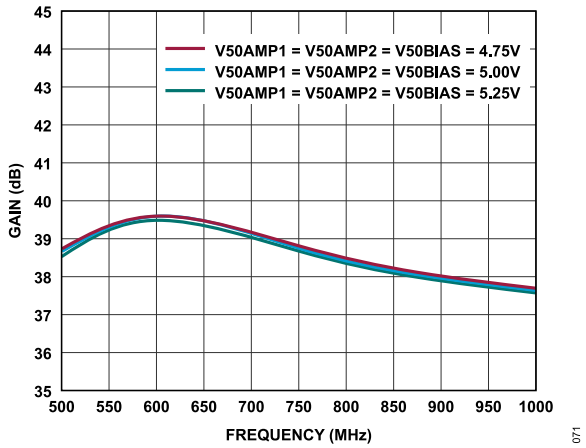

Figure 13. Gain vs. Frequency for Various Supplies

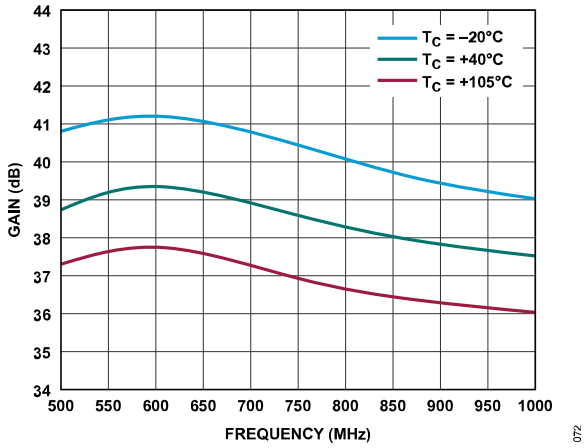

Figure 14. Gain vs. Frequency for Various Temperatures

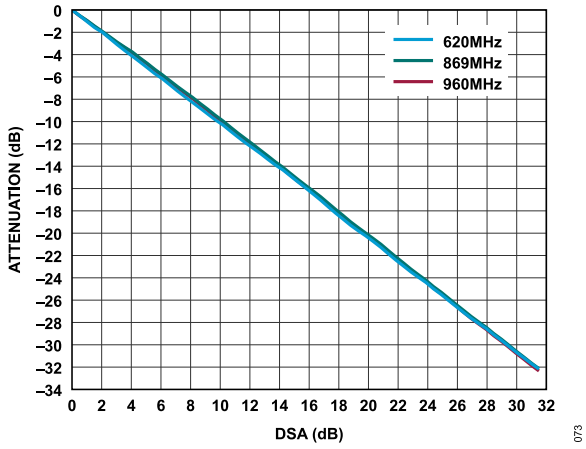

Figure 15. Attenuation vs. DSA at 620 MHz, 869 MHz, and 960 MHz

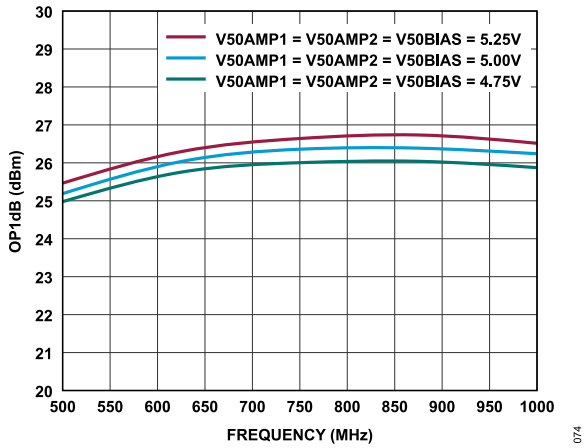

Figure 16. OP1dB vs. Frequency for Various Supplies

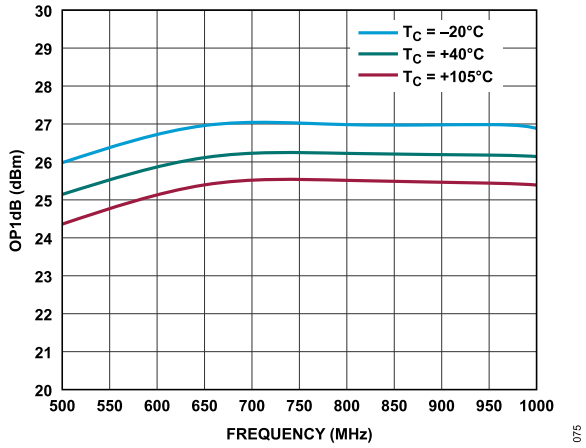

Figure 17. OP1dB vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

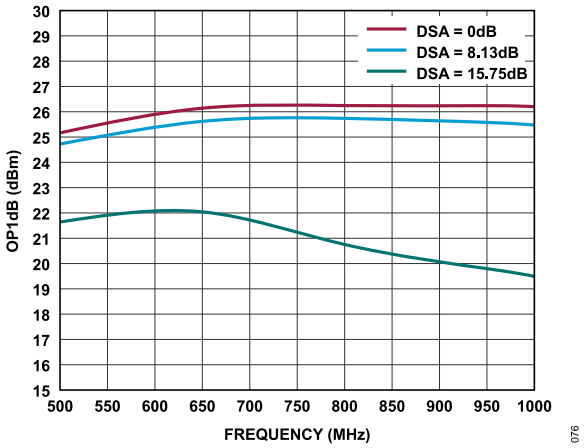

Figure 18. OP1dB vs. Frequency at Various DSA Values

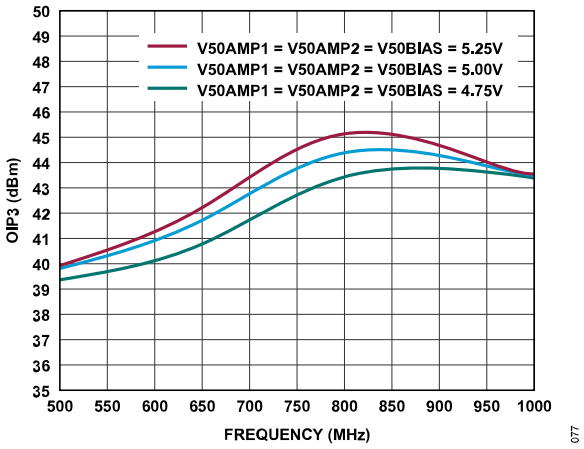

Figure 19. OIP3 vs. Frequency for Various Supplies

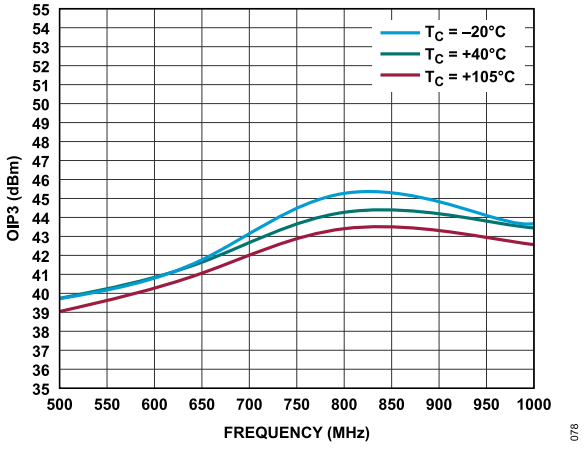

Figure 20. OIP3 vs. Frequency for Various Temperatures

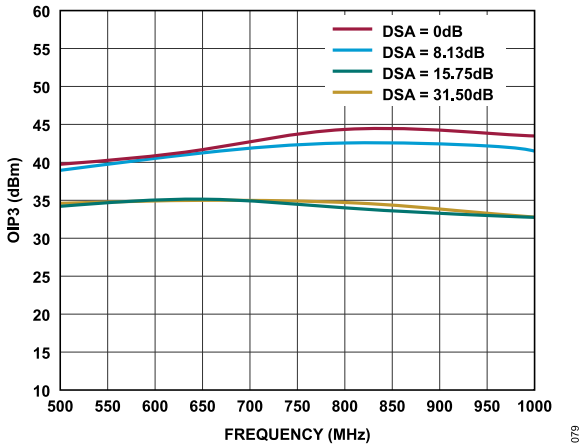

Figure 21. OIP3 vs. Frequency at Various DSA Values

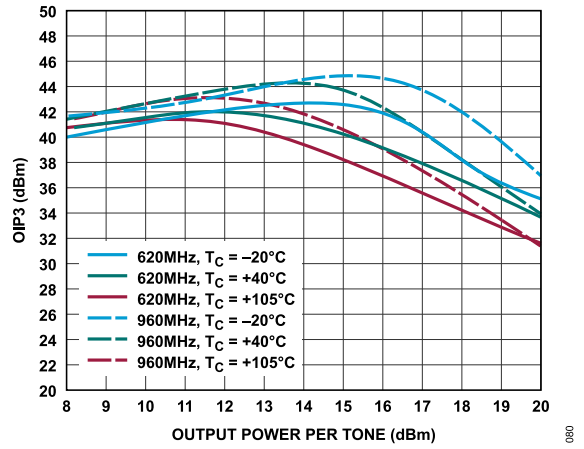

Figure 22. OIP3 vs. Output Power Per Tone for Various Temperatures at 620 MHz and 960 MHz

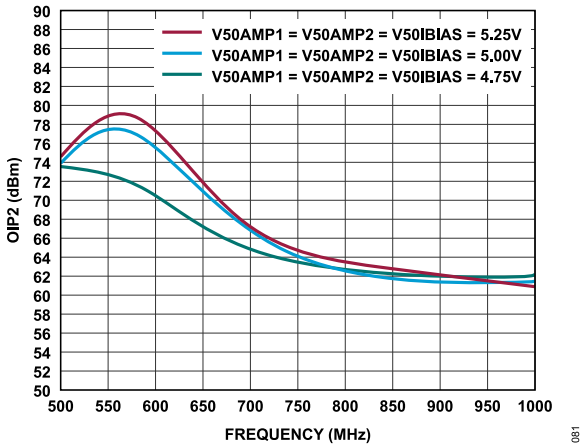

Figure 23. OIP2 vs. Frequency for Various Supplies

TYPICAL PERFORMANCE CHARACTERISTICS

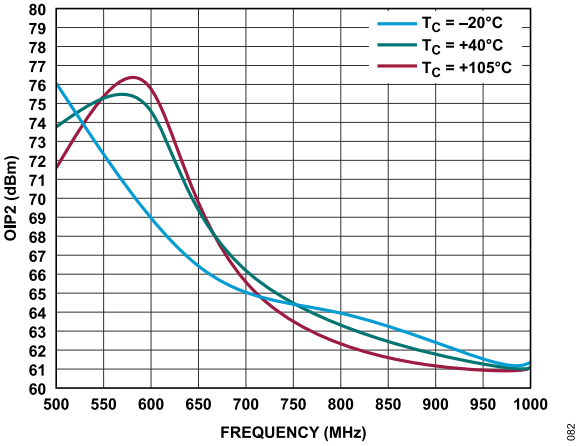

Figure 24. OIP2 vs. Frequency for Various Temperatures

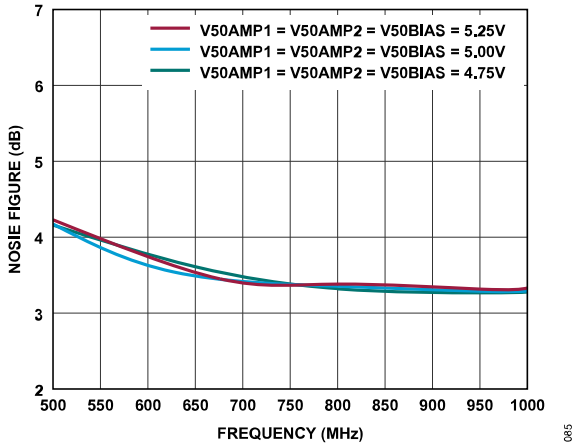

Figure 27. Noise Figure vs. Frequency for Various Supplies

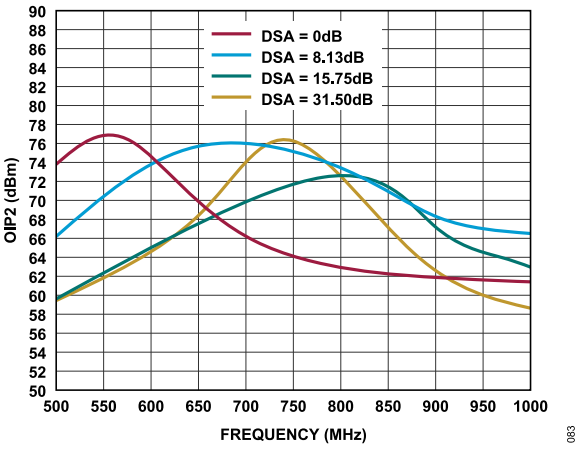

Figure 25. OIP2 vs. Frequency at Various DSA Values

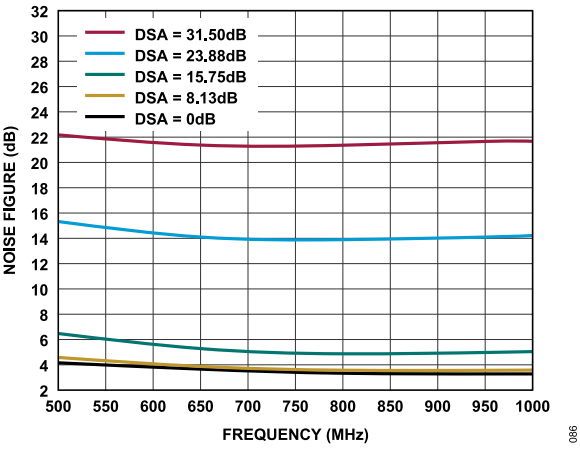

Figure 28. Noise Figure vs. Frequency at Various DSA Values

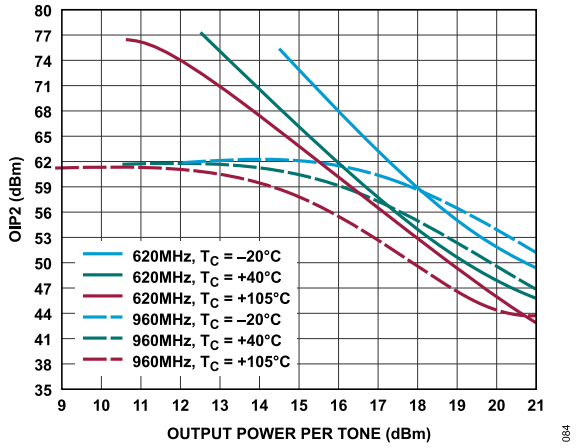

Figure 26. OIP2 vs. Output Power per Tone for Various Temperatures at 620 MHz and 960 MHz

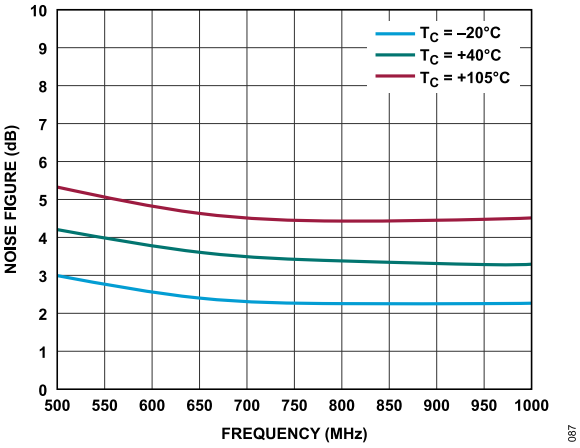

Figure 29. Noise Figure vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

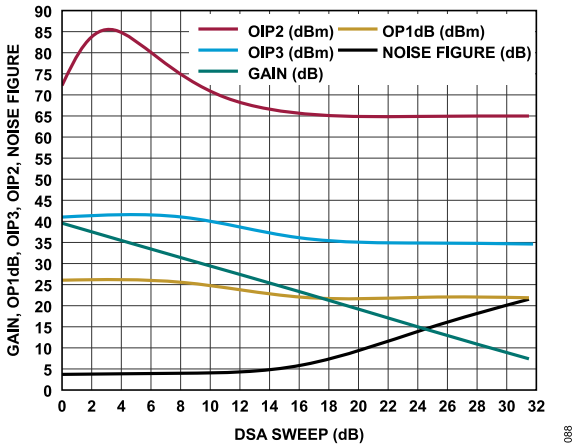

Figure 30. Gain, OP1dB, OIP3, OIP2, Noise Figure vs. DSA Sweep, Frequency = 620 MHz

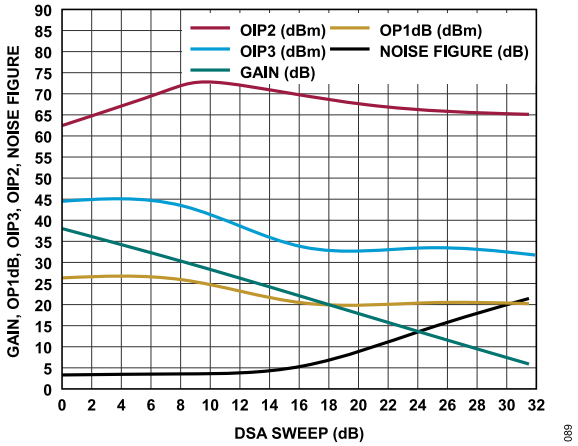

Figure 31. Gain, OP1dB, OIP3, OIP2, Noise Figure vs. DSA Sweep, Frequency = 869 MHz

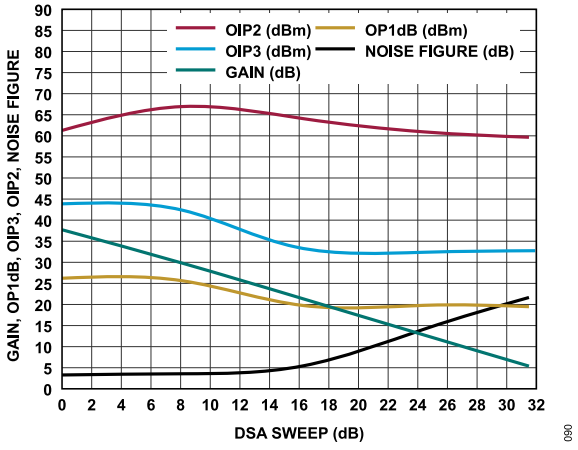

Figure 32. Gain, OP1dB, OIP3, OIP2, Noise Figure vs. DSA Sweep, Frequency = 960 MHz

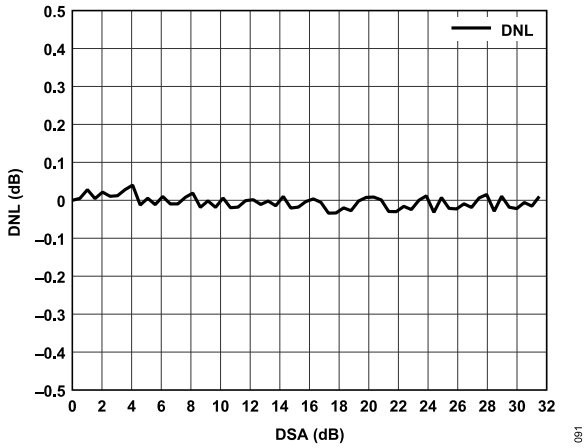

Figure 33. DSA Gain Step Error; Frequency = 869 MHz

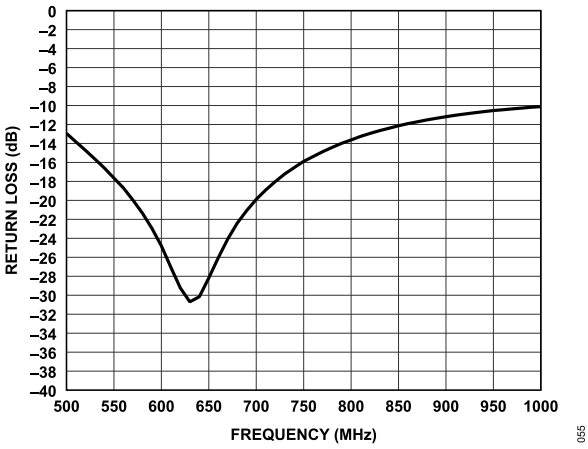

Figure 34. Return Loss of Differential RF Input S11 at 50 Ω Match

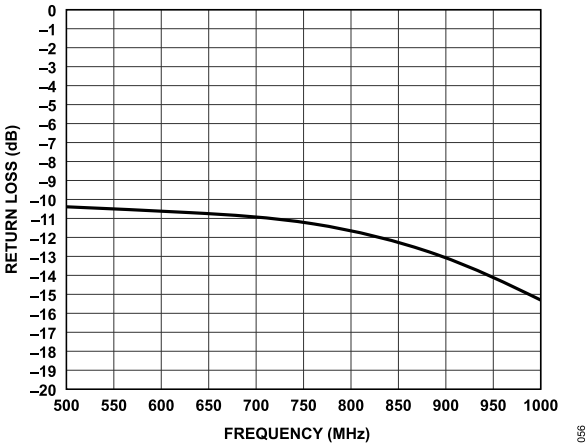

Figure 35. Return Loss of Single-Ended RF Output S22 at 50 Ω Match

TYPICAL PERFORMANCE CHARACTERISTICS

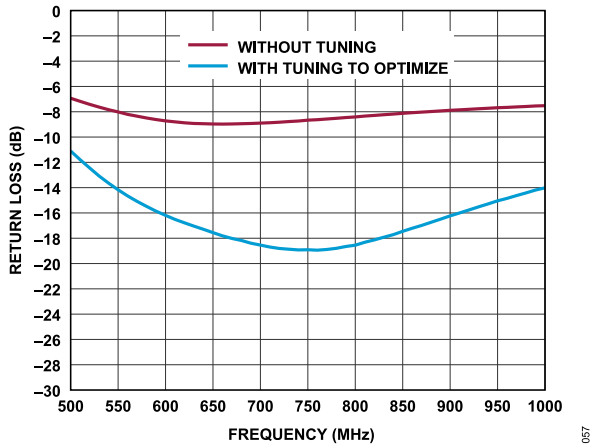

Figure 36. Return Loss of Differential RF Input S11 at 100 Ω Match; 14 nH in Shunt and 30 pF Series on Each Input

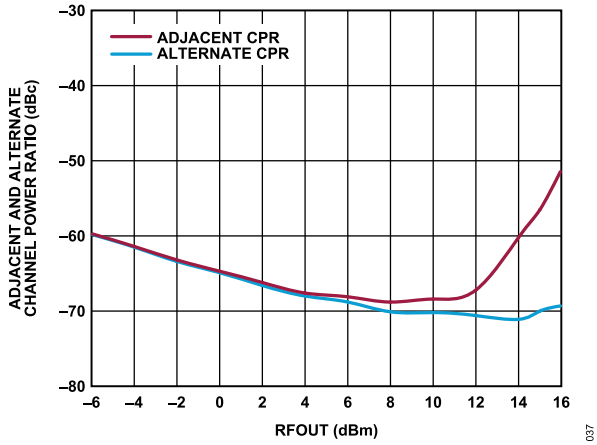

Figure 37. Adjacent and Alternate Channel Power Ratio vs. Output Power (RFOUT) by P_{IN} at 869 MHz, LTE Test Model 1.1 (TM1.1) 5 MHz, DSA = 0 dB

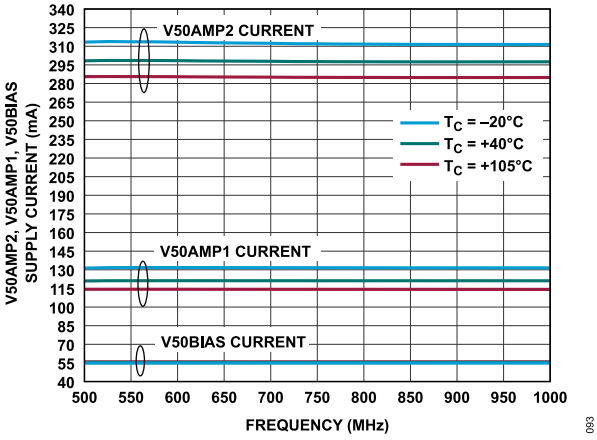

Figure 38. V50AMP1, V50AMP2, and V50BIAS Current vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

ADL6337-B

V_{50AMP1} = V_{50AMP2} = 5 V, T_A = 25°C, input power = −25 dBm (−25 dBm per tone for two tones), DSA attenuation= 0 dB, RS = RL = 50 Ω, TRM_AMP1_IP3_0 = TRM_AMP2_IP3_ = 5, TRM_AMP1_IREF_0_0 = TRM_AMP1_IREF_1 = TRM_AMP1_IREF_2 = TRM_AMP1_IREF_3 = 12, TRM_AMP2_IREF_0_0 = TRM_AMP2_IREF_1 = TRM_AMP2_IREF_2 = TRM_AMP2_IREF_3 = 11, unless otherwise noted.

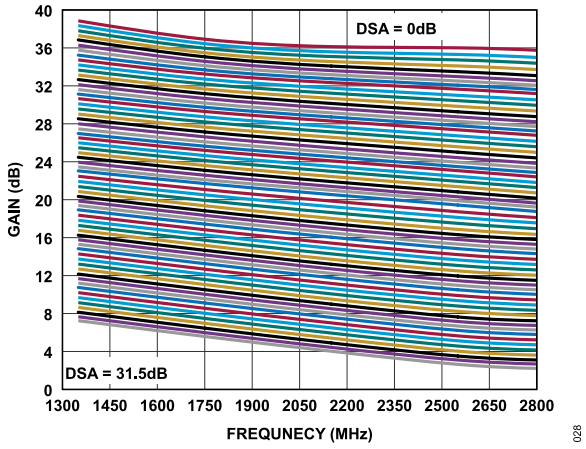

Figure 39. Gain vs. Frequency; 0.5 dB DSA Steps

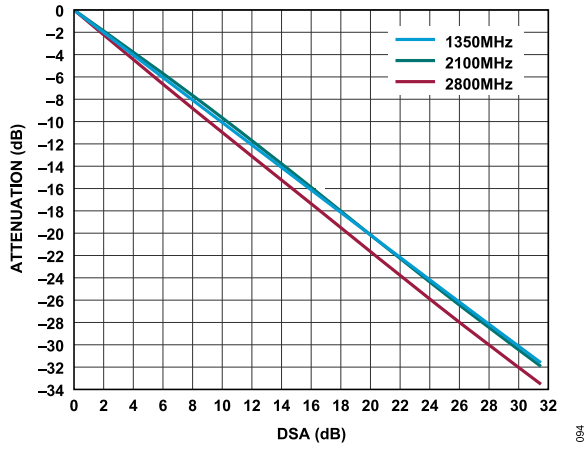

Figure 42. Attenuation vs. DSA at 1800 MHz, 2100 MHz, and 2700 MHz

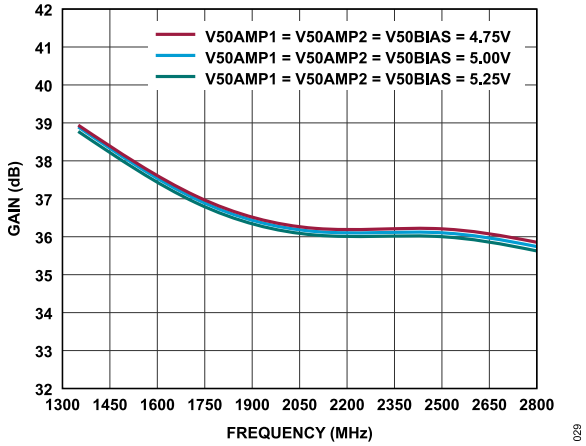

Figure 40. Gain vs. Frequency for Various Supplies

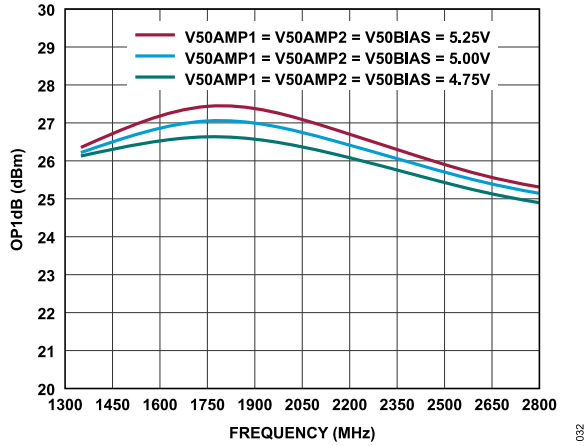

Figure 43. OP1dB vs. Frequency for Various Supplies

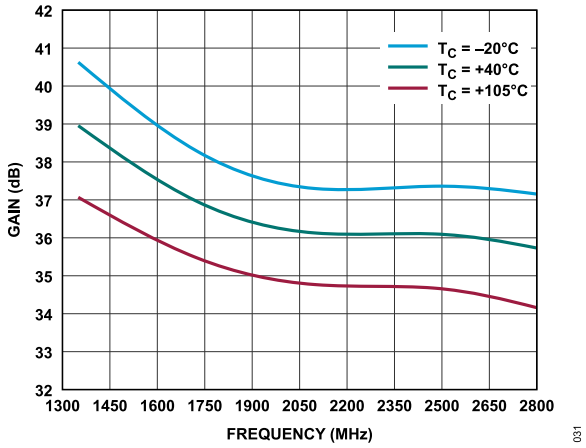

Figure 41. Gain vs. Frequency for Various Temperatures

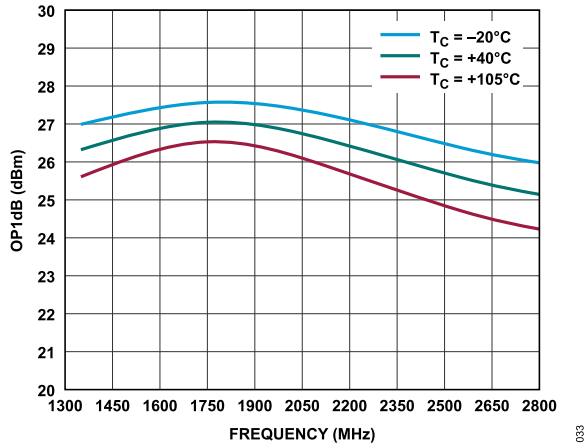

Figure 44. OP1dB vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

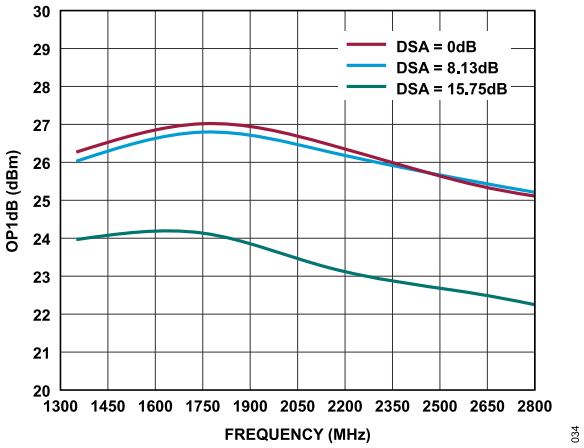

Figure 45. OP1dB vs. Frequency at Various DSA Values

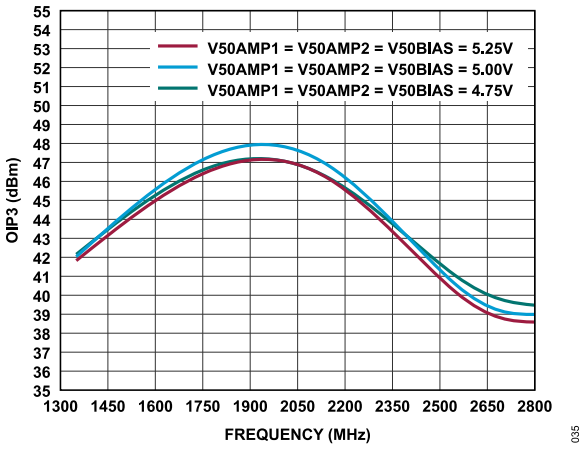

Figure 46. OIP3 vs. Frequency for Various Supplies

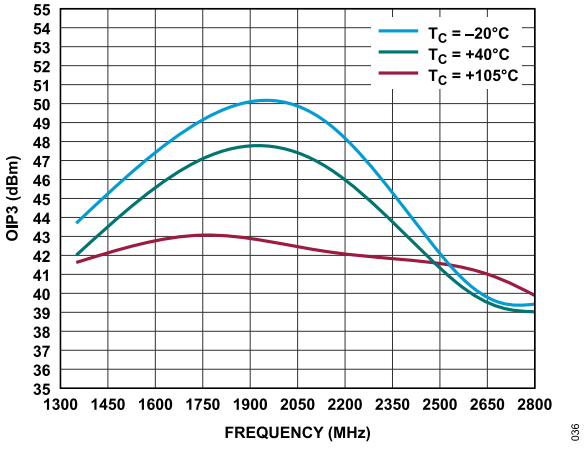

Figure 47. OIP3 vs. Frequency for Various Temperatures

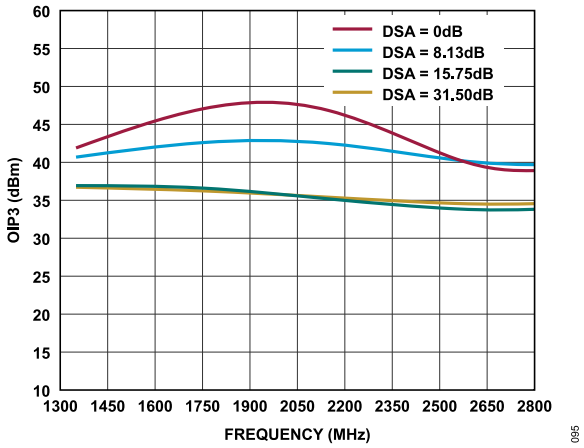

Figure 48. OIP3 vs. Frequency at Various DSA Values

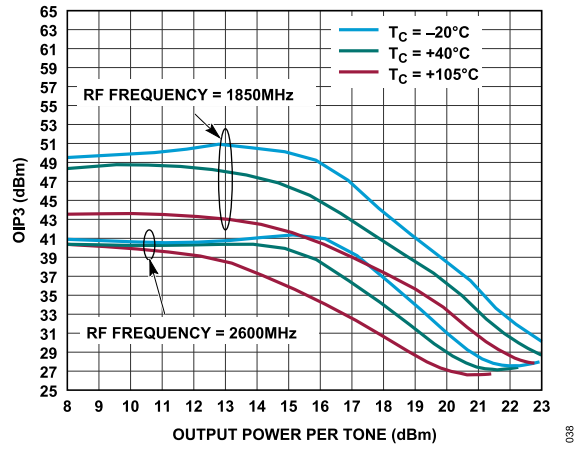

Figure 49. OIP3 vs. Output Power Per Tone for Various Temperatures at 1850 MHz and 2600 MHz

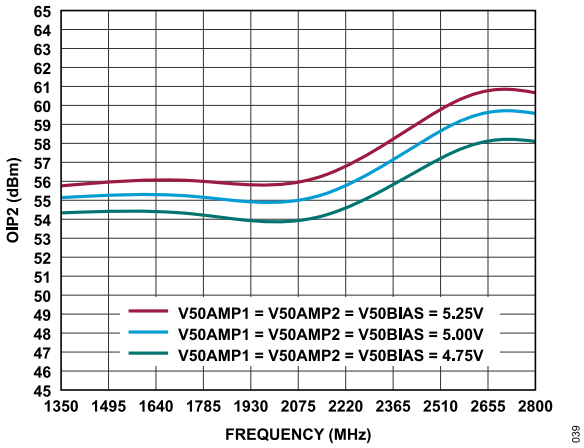

Figure 50. OIP2 vs. Frequency for Various Supplies

TYPICAL PERFORMANCE CHARACTERISTICS

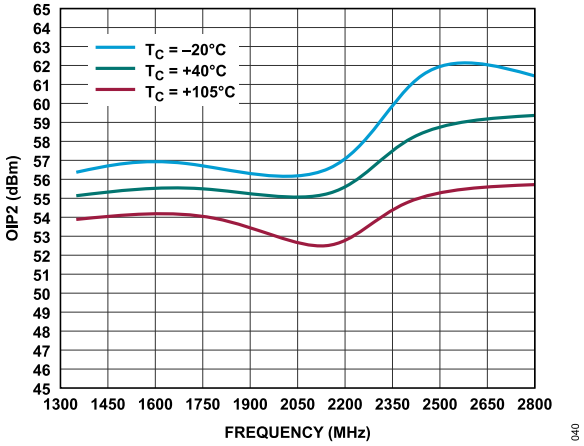

Figure 51. OIP2 vs. Frequency for Various Temperatures

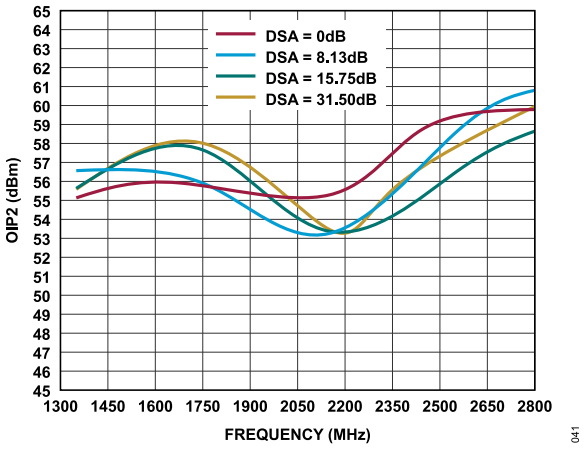

Figure 52. OIP2 vs. Frequency at Various DSA Values

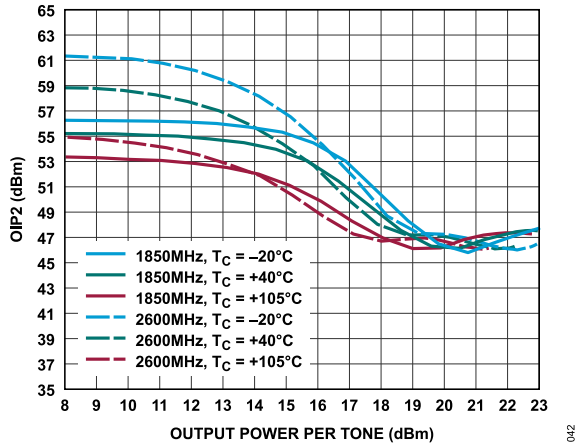

Figure 53. OIP2 vs. Output Power per Tone for Various Temperatures at 1850 MHz and 2600 MHz

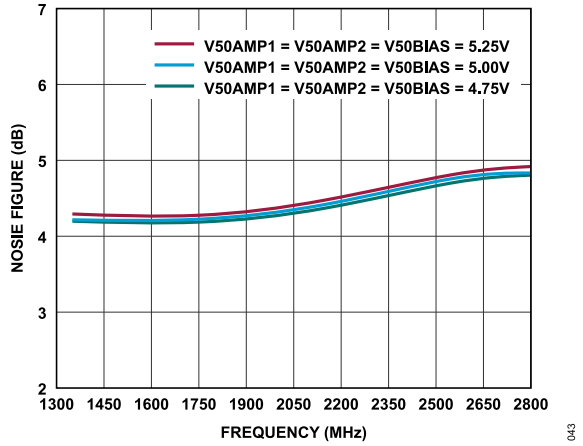

Figure 54. Noise Figure vs. Frequency for Various Supplies

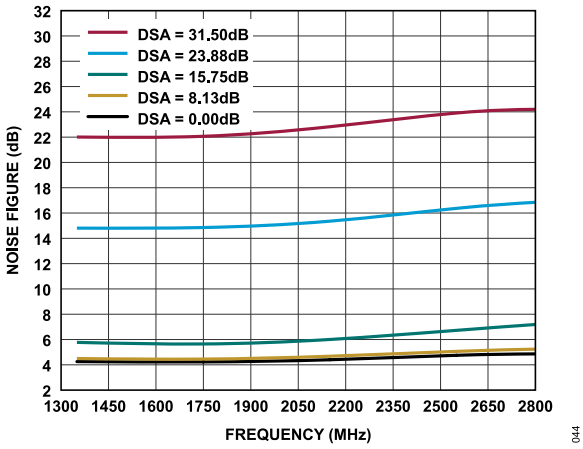

Figure 55. Noise Figure vs. Frequency at Various DSA Values

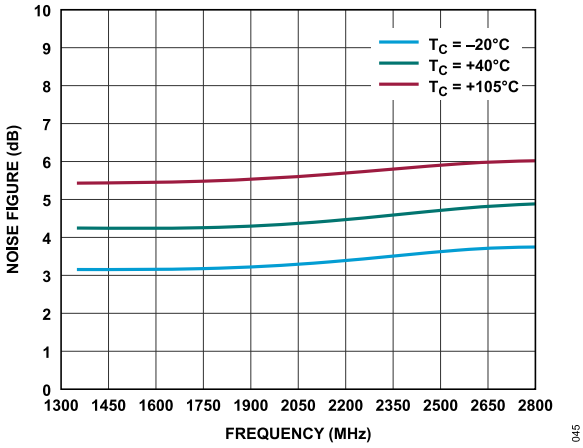

Figure 56. Noise Figure vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

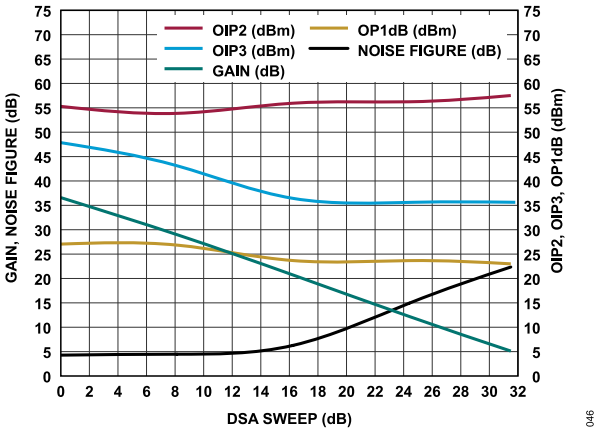

Figure 57. Gain, Noise Figure, OIP2, OIP3, OP1dB vs. DSA Sweep, Frequency = 1850 MHz

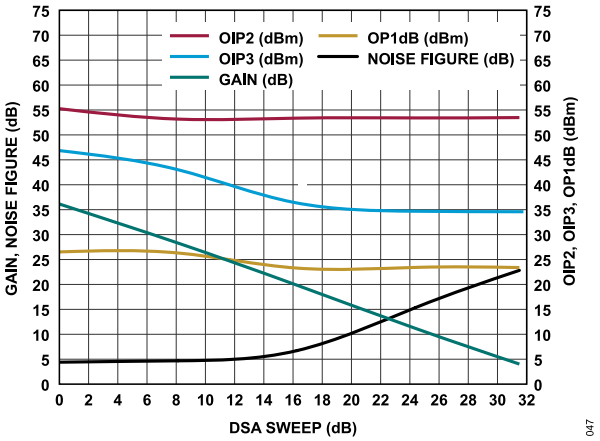

Figure 58. Gain, Noise Figure, OIP2, OIP3, OP1dB vs. DSA Sweep, Frequency = 2150 MHz

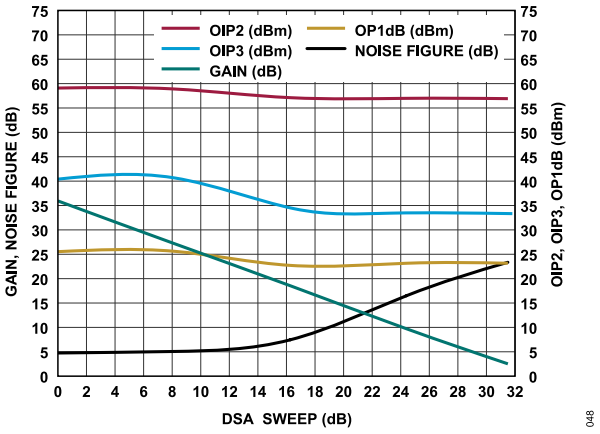

Figure 59. Gain, Noise Figure, OIP2, OIP3, OP1dB vs. DSA Sweep, Frequency = 2600 MHz

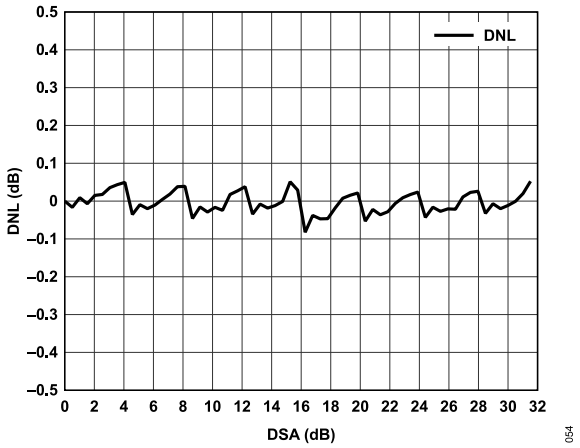

Figure 60. DSA Gain Step Error; Frequency = 2100 MHz

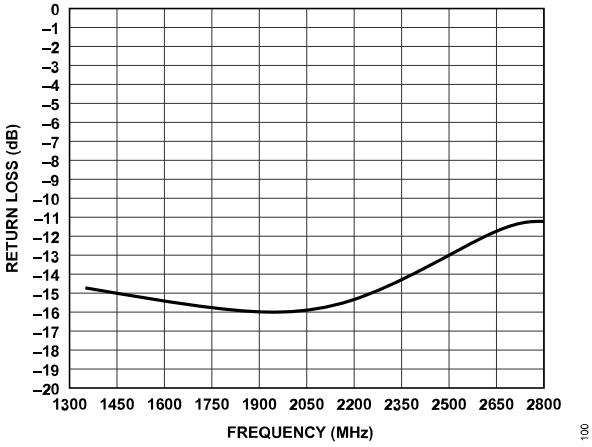

Figure 61. Return Loss of Differential RF Input S11 at 50 Ω Match

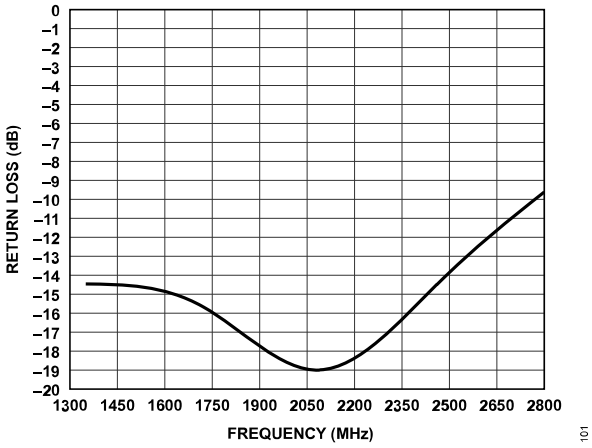

Figure 62. Return Loss of Single-Ended RF Output S22 at 50 Ω Match

TYPICAL PERFORMANCE CHARACTERISTICS

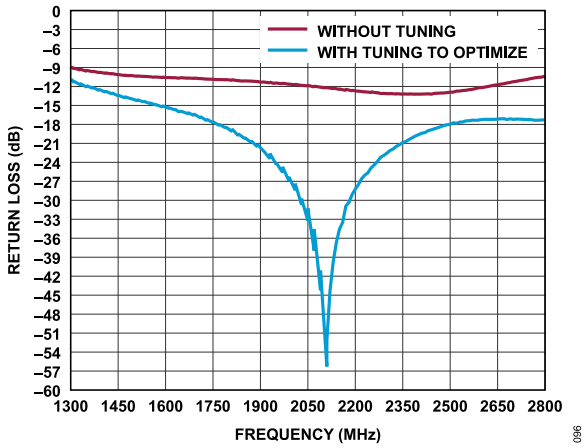

Figure 63. Return Loss of Differential RF Input S11 at 100 Ω Match; 1.1 pF in Shunt and 2.3 nH Series on Each Input

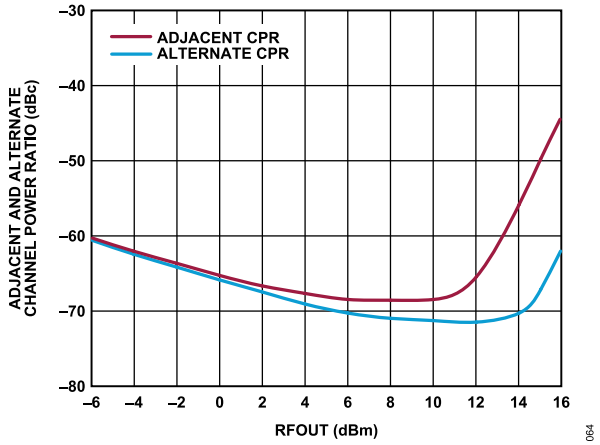

Figure 64. Adjacent and Alternate Channel Power Ratio vs. Output Power (RFOUT) by P_{IN} at 2400 MHz, LTE Test Model 1.1 (TM1.1) 5 MHz, DSA = 0 dB

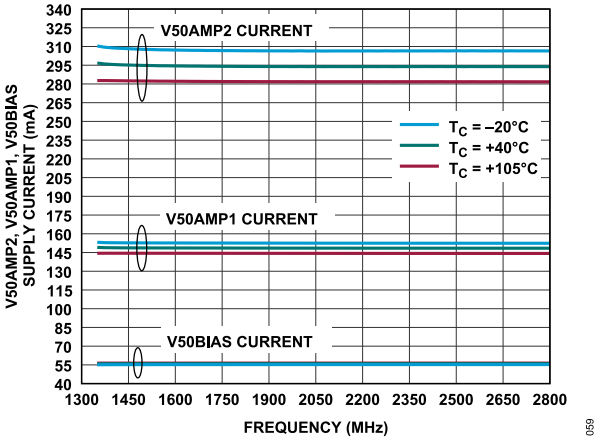

Figure 65. V50AMP1, V50AMP2, and V50BIAS Current vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

ADL6337-C

V_{50AMP1} = V_{50AMP2} = 5 V, T_A = 25°C, input power = −25 dBm (−25 dBm per tone for two tones), DSA attenuation= 0 dB, RS = RL = 50 Ω, TRM_AMP1_IP3_0 = TRM_AMP2_IP3_ = 6, TRM_AMP1_IREF_0_0 = TRM_AMP1_IREF_1 = TRM_AMP1_IREF_2 = TRM_AMP1_IREF_3 = 11, TRM_AMP2_IREF_0_0 = TRM_AMP2_IREF_1 = TRM_AMP2_IREF_2 = TRM_AMP2_IREF_3 = 11, unless otherwise noted.

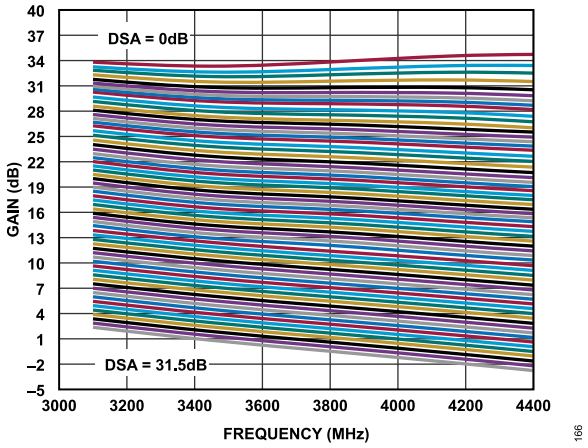

Figure 66. Gain vs. Frequency; 0.5 dB DSA Steps

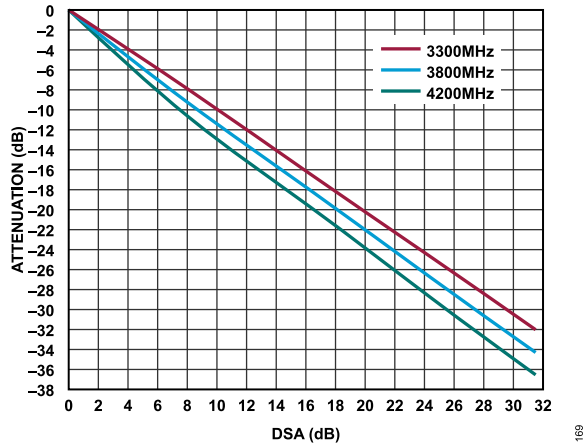

Figure 69. Attenuation vs. DSA at 3300 MHz, 3600 MHz, and 3800 MHz

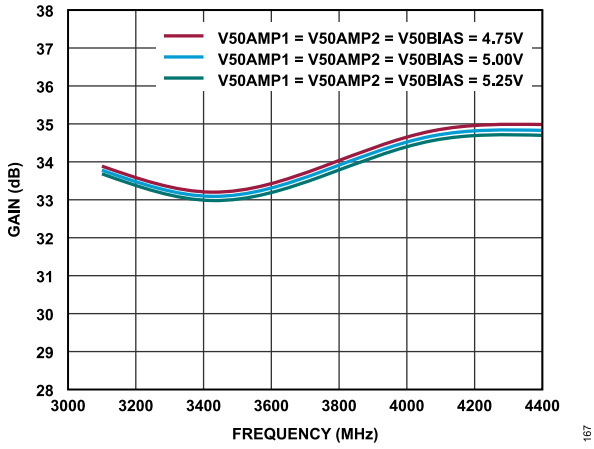

Figure 67. Gain vs. Frequency for Various Supplies

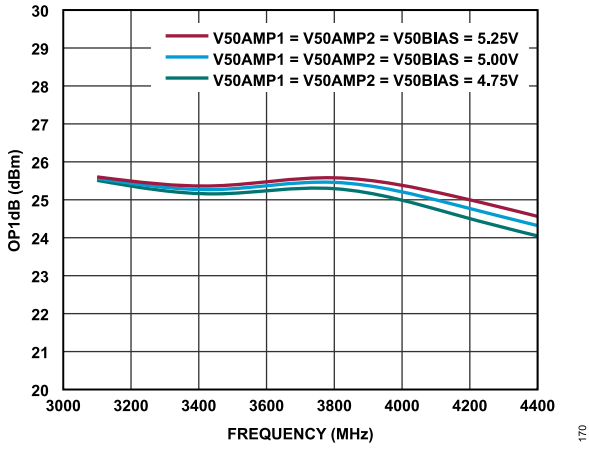

Figure 70. OP1dB vs. Frequency for Various Supplies

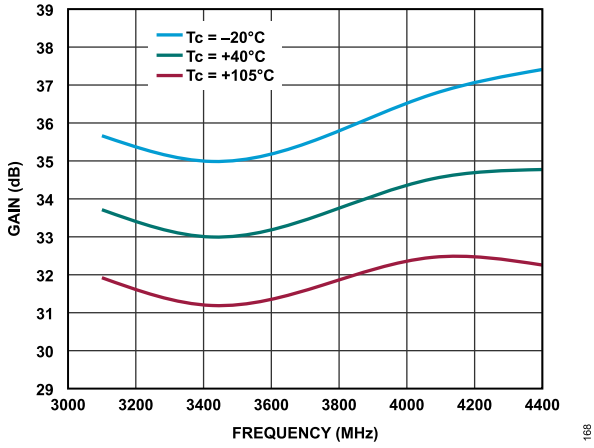

Figure 68. Gain vs. Frequency for Various Temperatures

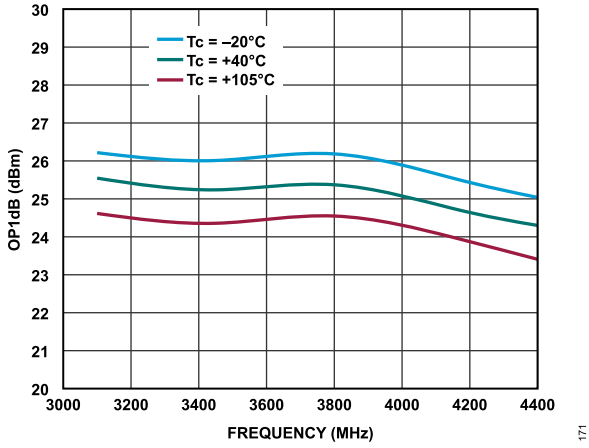

Figure 71. OP1dB vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

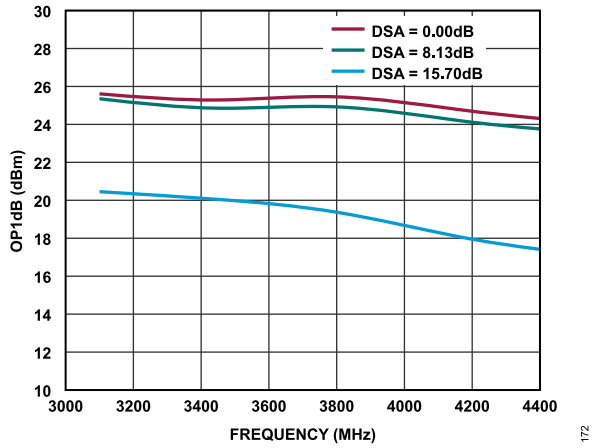

Figure 72. OP1dB vs. Frequency at Various DSA Values

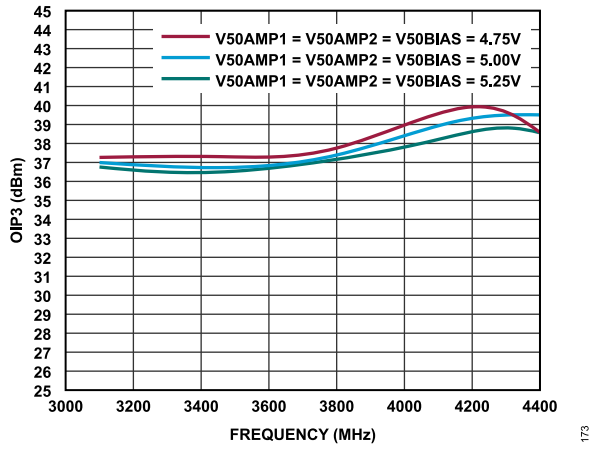

Figure 73. OIP3 vs. Frequency for Various Supplies

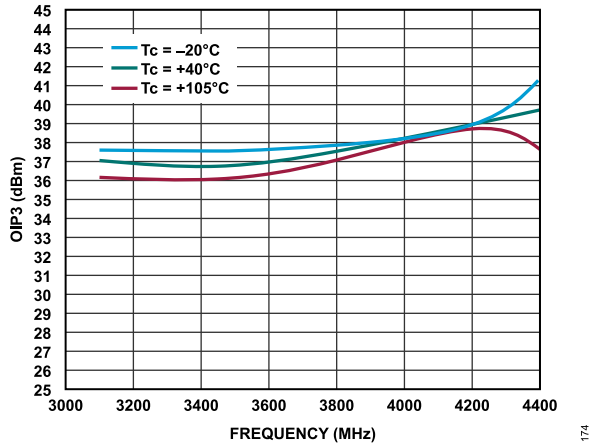

Figure 74. OIP3 vs. Frequency for Various Temperatures

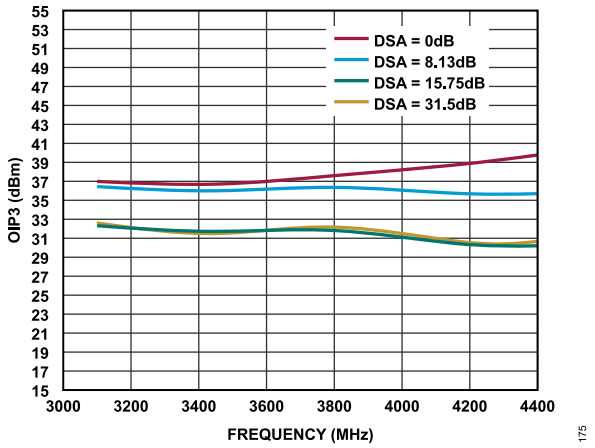

Figure 75. OIP3 vs. Frequency at Various DSA Values

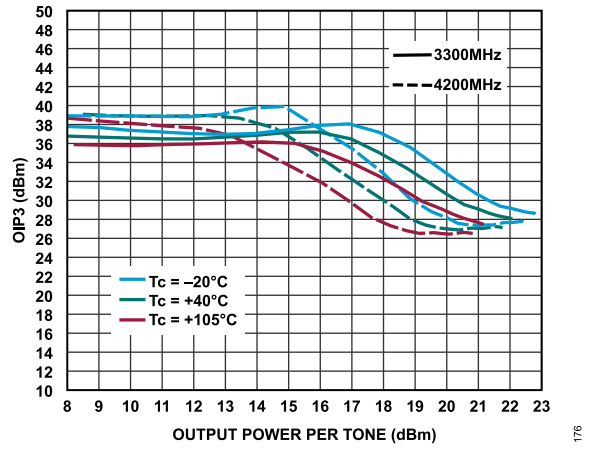

Figure 76. OIP3 vs. Output Power Per Tone for Various Temperatures at 3300 MHz and 4200 MHz

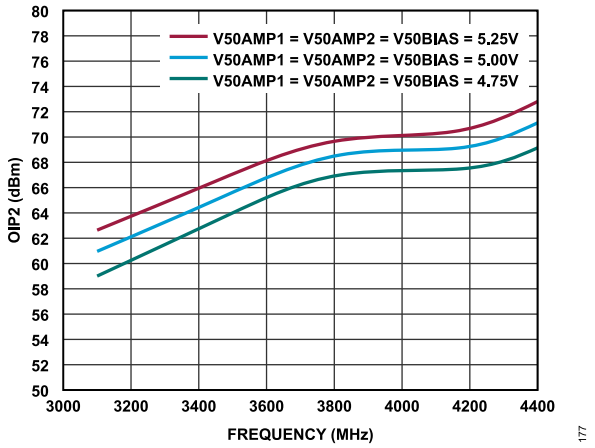

Figure 77. OIP2 vs. Frequency for Various Supplies

TYPICAL PERFORMANCE CHARACTERISTICS

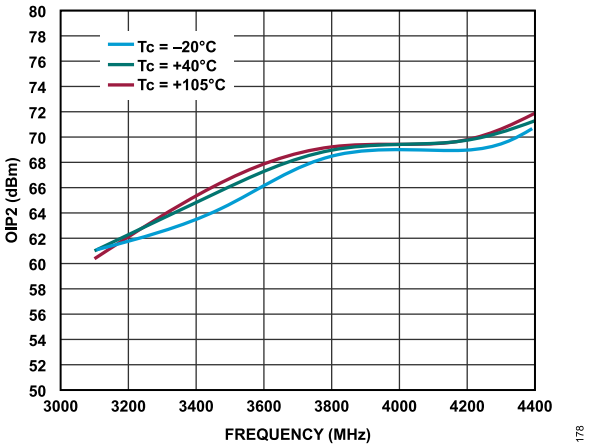

Figure 78. OIP2 vs. Frequency for Various Temperatures

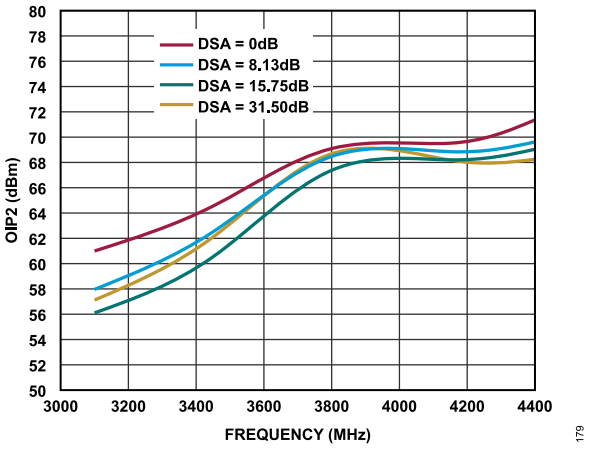

Figure 79. OIP2 vs. Frequency at Various DSA Values

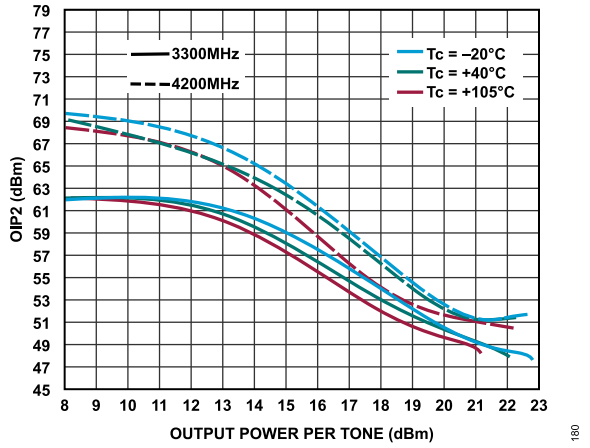

Figure 80. OIP2 vs. Output Power per Tone for Various Temperatures at 3300 MHz and 4200 MHz

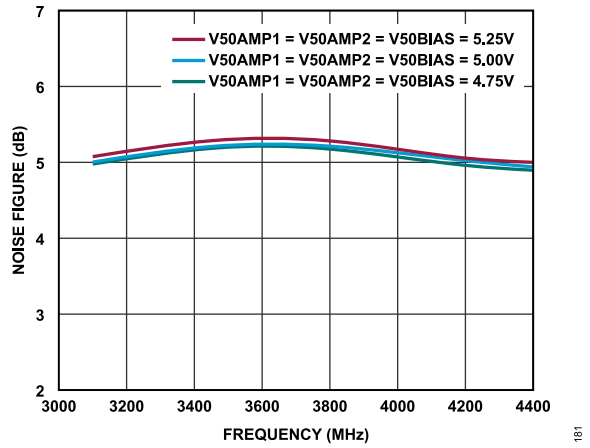

Figure 81. Noise Figure vs. Frequency for Various Supplies

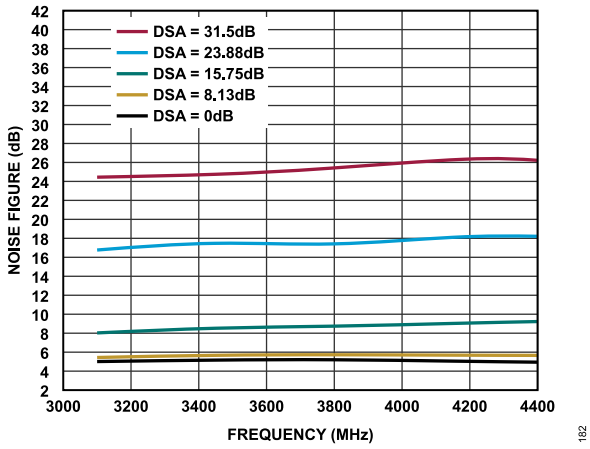

Figure 82. Noise Figure vs. Frequency at Various DSA Values

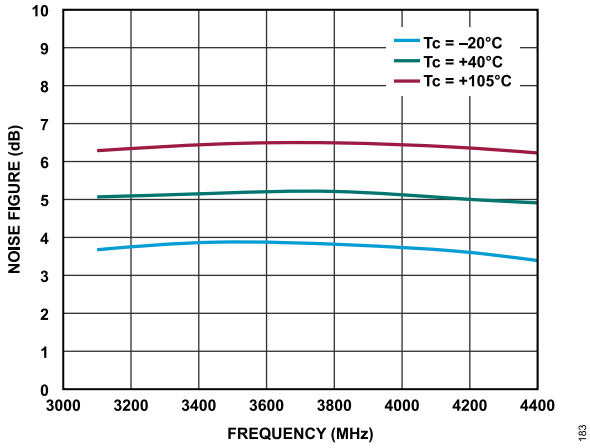

Figure 83. Noise Figure vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

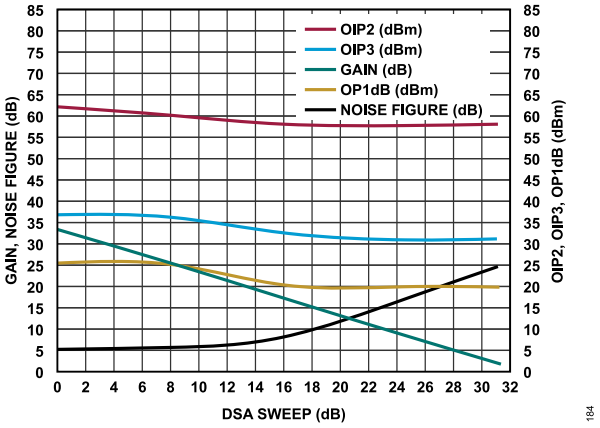

Figure 84. Gain, Noise Figure, OIP2, OIP3, OP1dB vs. DSA Sweep, Frequency = 3300 MHz

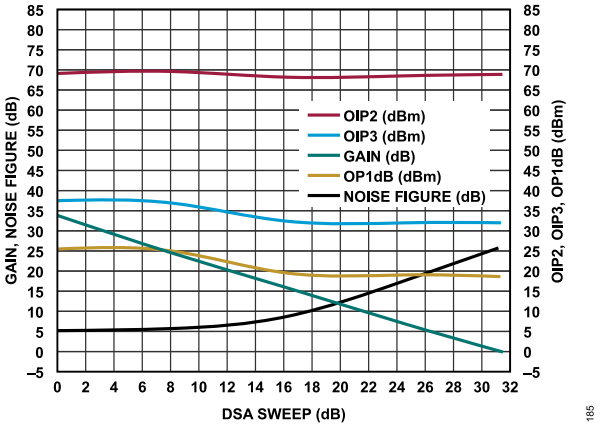

Figure 85. Gain, Noise Figure, OIP2, OIP3, OP1dB vs. DSA Sweep, Frequency = 3600 MHz

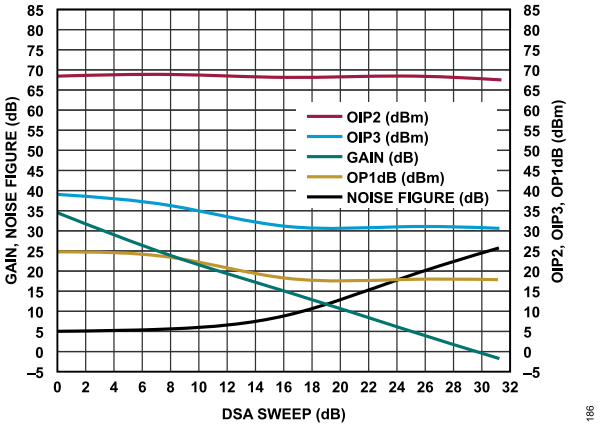

Figure 86. Gain, Noise Figure, OIP2, OIP3, OP1dB vs. DSA Sweep, Frequency = 4200 MHz

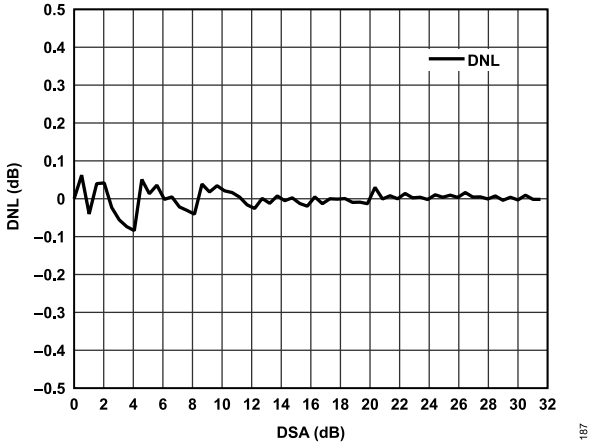

Figure 87. DSA Gain Step Error; Frequency = 3300 MHz

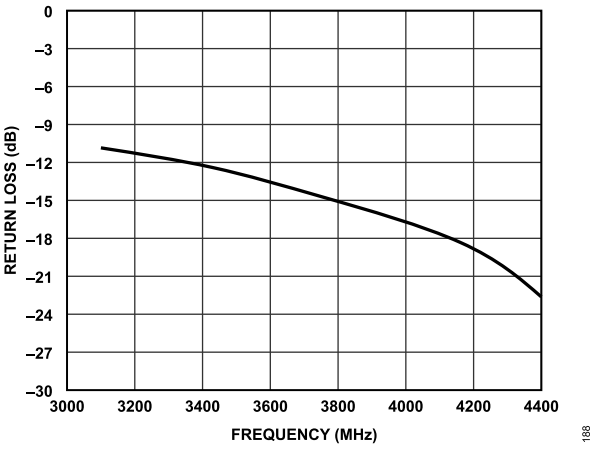

Figure 88. Return Loss of Differential RF Input S11 at 50 Ω Match

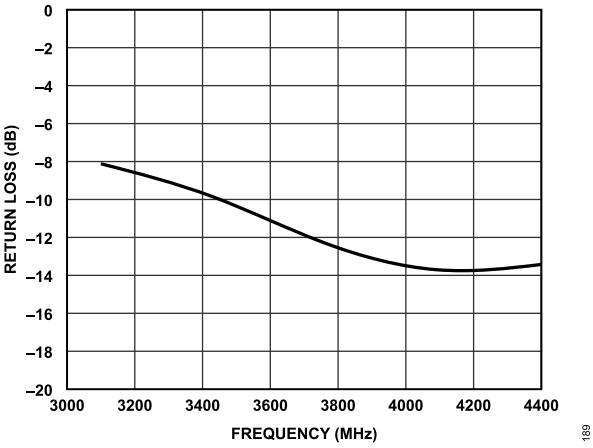

Figure 89. Return Loss of Single-Ended RF Output S22 at 50 Ω Match

TYPICAL PERFORMANCE CHARACTERISTICS

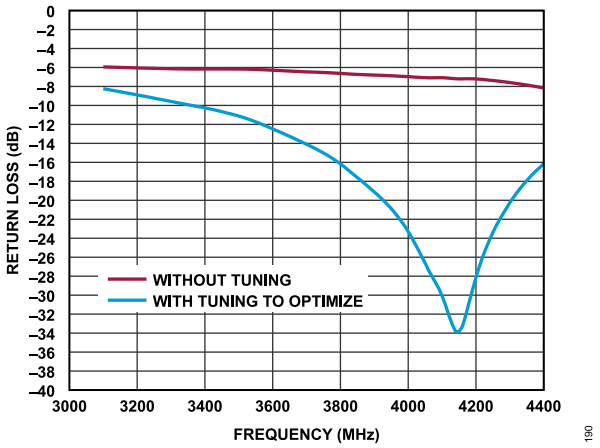

Figure 90. Return Loss of Differential RF Input S11 at 100 Ω Match; 0.8 pF in Shunt and 1.0 nH Series on Each Input

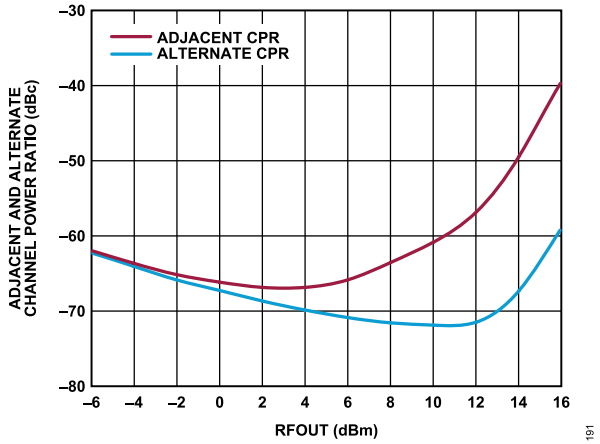

Figure 91. Adjacent and Alternate Channel Power Ratio vs. Output Power (RFOUT) by P_{IN} at 3800 MHz, LTE Test Model 1.1 (TM1.1) 5 MHz, DSA = 0 dB

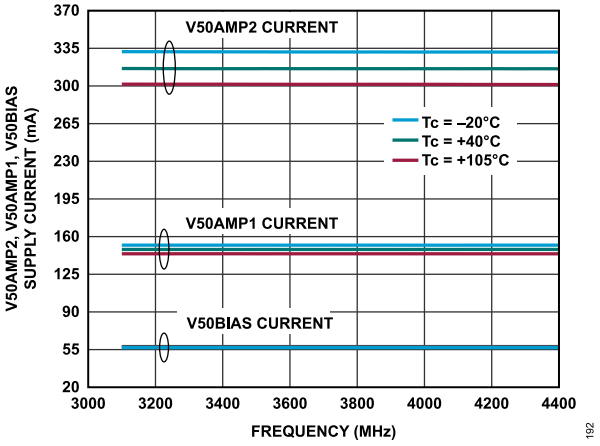

Figure 92. V50AMP1, V50AMP2, and V50BIAS Current vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

ADL6337-D

V_{50AMP1} = V_{50AMP2} = 5 V, T_A = 25°C, input power = −25 dBm (−25 dBm per tone for two tones), DSA attenuation= 0 dB, RS = RL = 50 Ω, TRM_AMP1_IP3_0 = TRM_AMP2_IP3_ = 1, TRM_AMP1_IREF_0_0 = TRM_AMP1_IREF_1 = TRM_AMP1_IREF_2 = TRM_AMP1_IREF_3 = 12, TRM_AMP2_IREF_0_0 = TRM_AMP2_IREF_1 = TRM_AMP2_IREF_2 = TRM_AMP2_IREF_3 =12, unless otherwise noted.

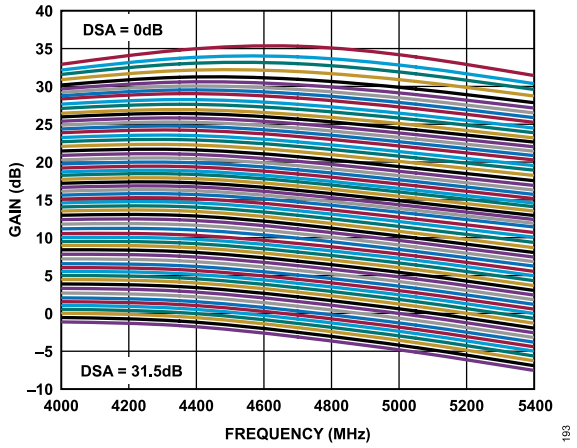

Figure 93. Gain vs. Frequency; 0.5 dB DSA Steps

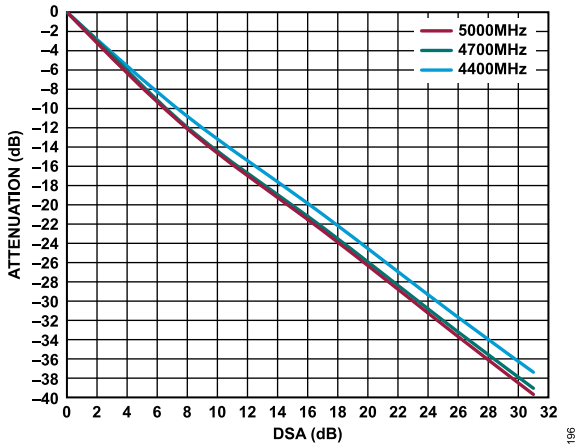

Figure 96. Attenuation vs. DSA at 3300 MHz, 3600 MHz, and 3800 MHz

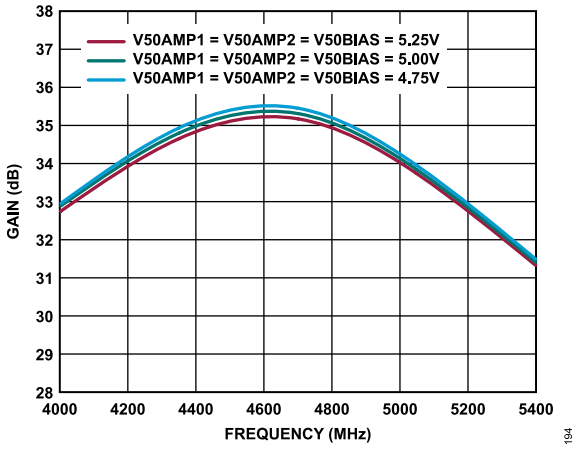

Figure 94. Gain vs. Frequency for Various Supplies

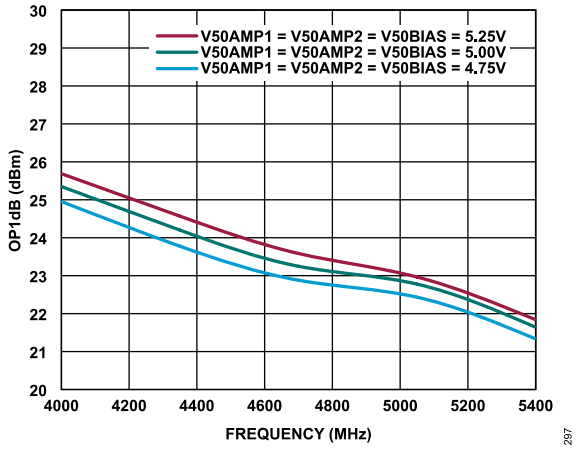

Figure 97. OP1dB vs. Frequency for Various Supplies

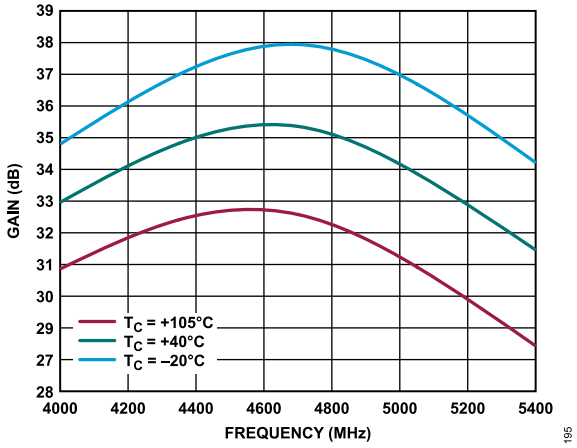

Figure 95. Gain vs. Frequency for Various Temperatures

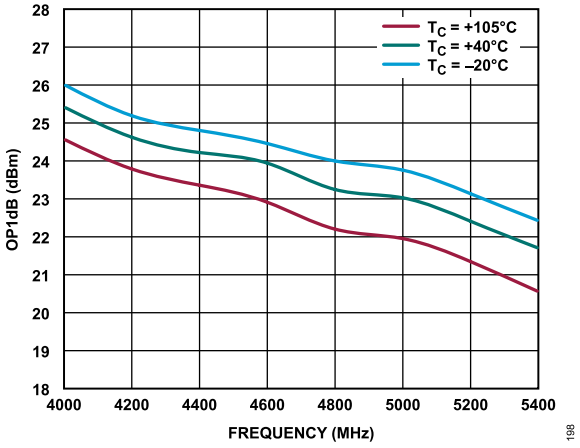

Figure 98. OP1dB vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

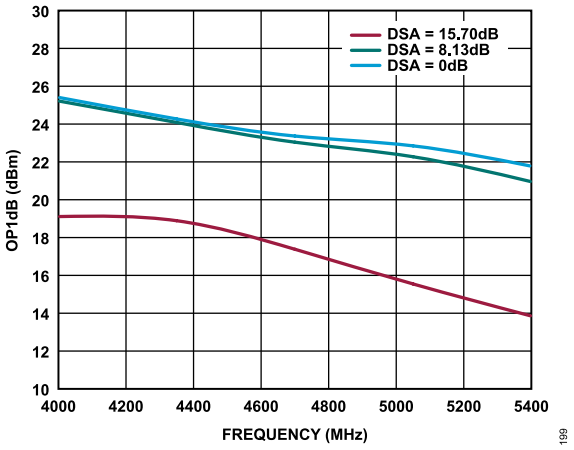

Figure 99. OP1dB vs. Frequency at Various DSA Values

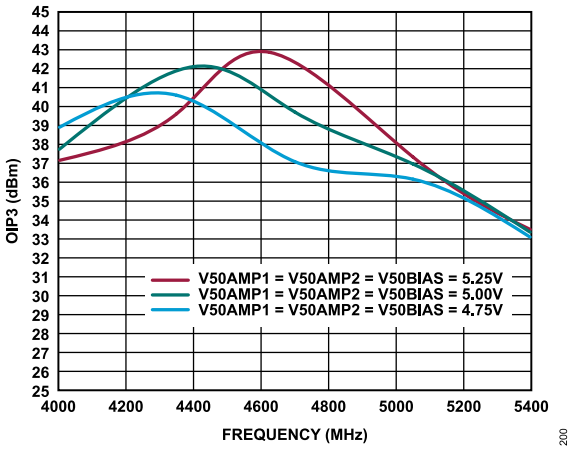

Figure 100. OIP3 vs. Frequency for Various Supplies

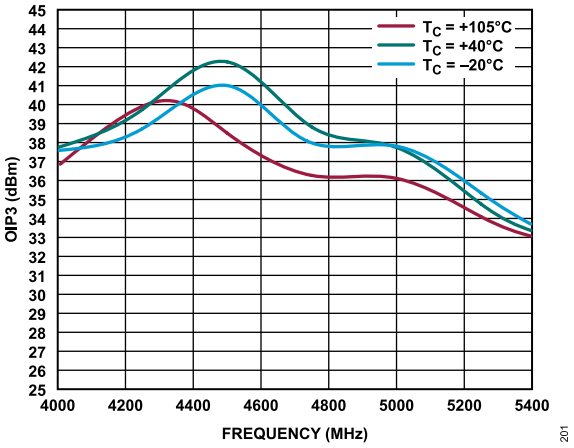

Figure 101. OIP3 vs. Frequency for Various Temperatures

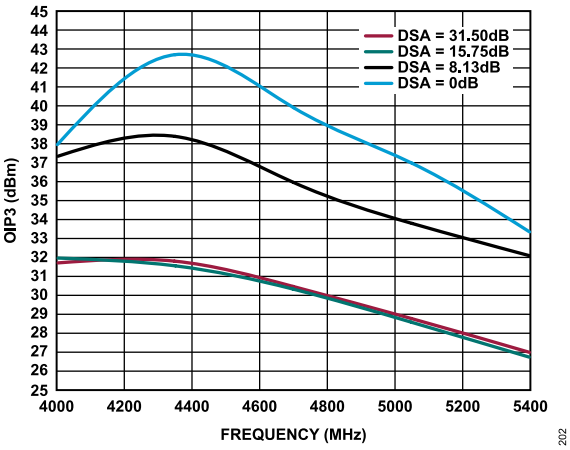

Figure 102. OIP3 vs. Frequency at Various DSA Values

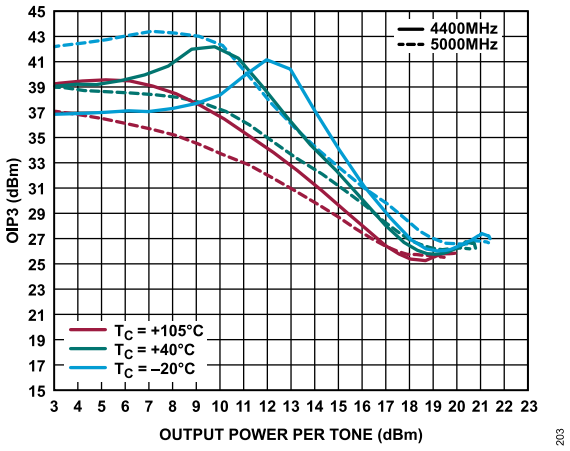

Figure 103. OIP3 vs. Output Power Per Tone for Various Temperatures at 4400 MHz and 5000 MHz

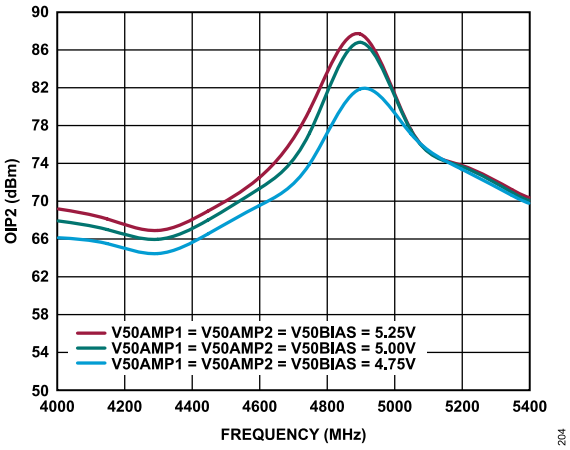

Figure 104. OIP2 vs. Frequency for Various Supplies

TYPICAL PERFORMANCE CHARACTERISTICS

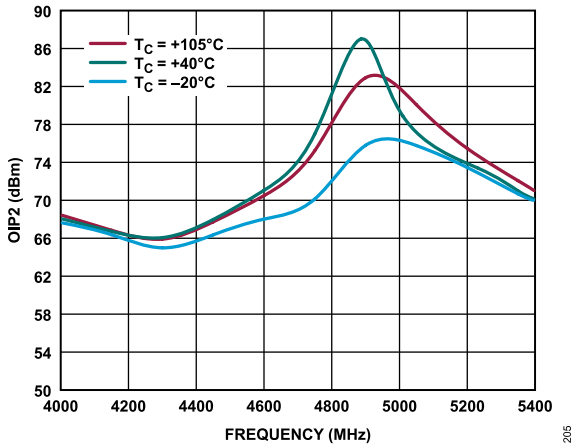

Figure 105. OIP2 vs. Frequency for Various Temperatures

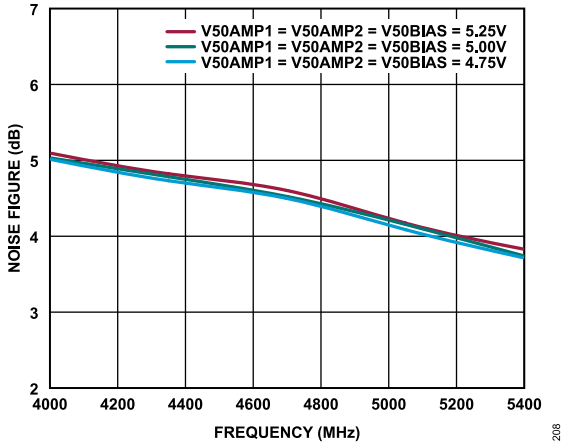

Figure 108. Noise Figure vs. Frequency for Various Supplies

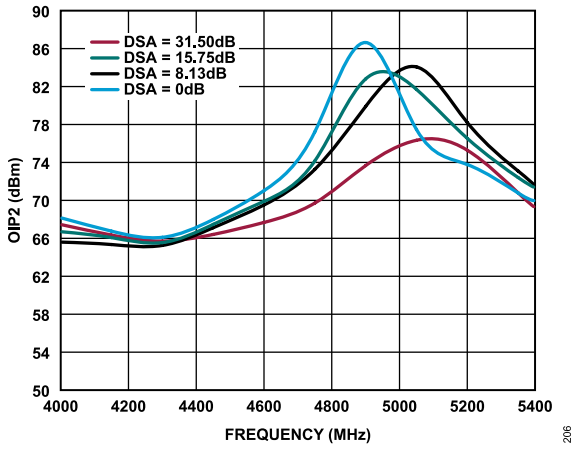

Figure 106. OIP2 vs. Frequency at Various DSA Values

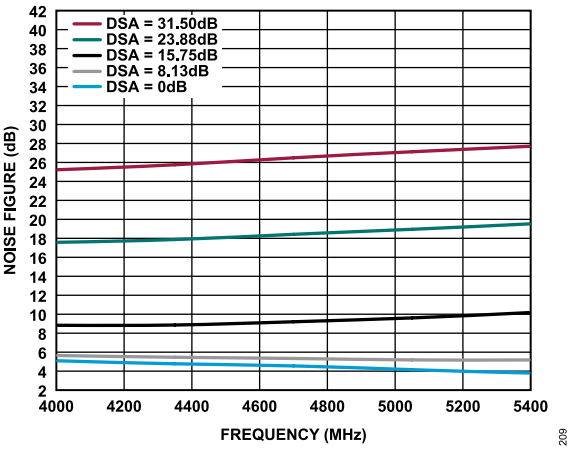

Figure 109. Noise Figure vs. Frequency at Various DSA Values

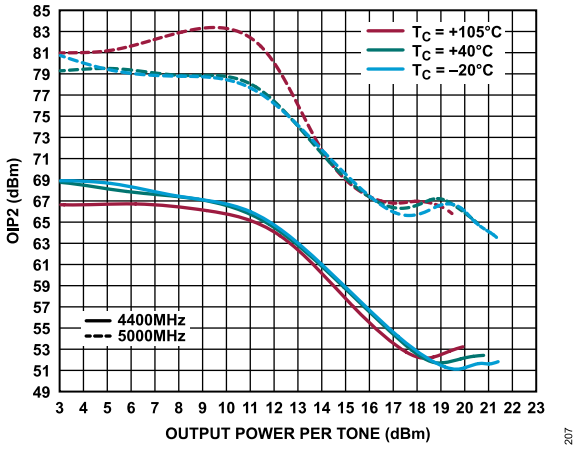

Figure 107. OIP2 vs. Output Power per Tone for Various Temperatures at 4400 MHz and 5000 MHz

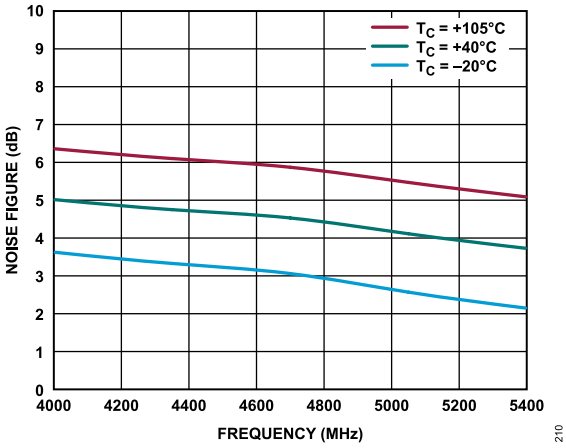

Figure 110. Noise Figure vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

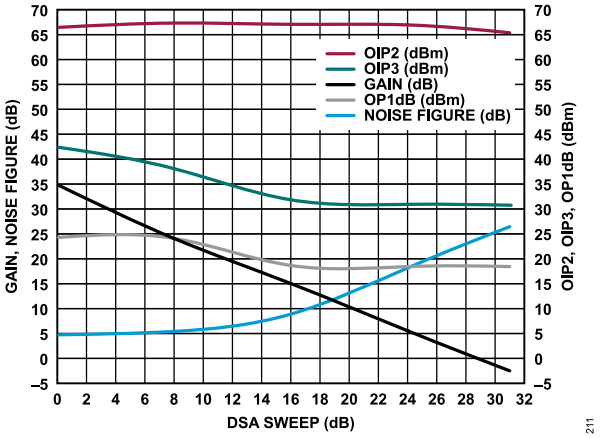

Figure 111. Gain, Noise Figure, OIP2, OIP3, OP1dB vs. DSA Sweep, Frequency = 4400 MHz

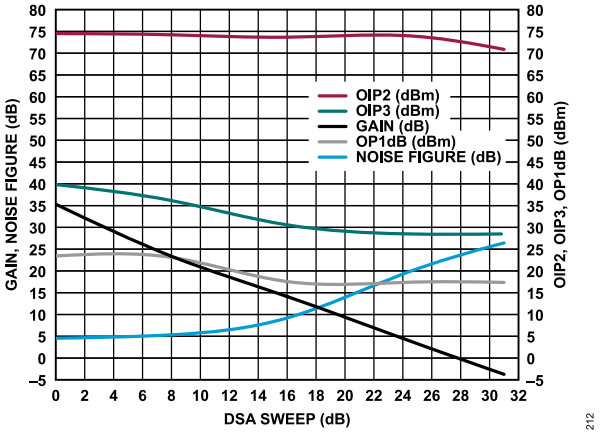

Figure 112. Gain, Noise Figure, OIP2, OIP3, OP1dB vs. DSA Sweep, Frequency = 4700 MHz

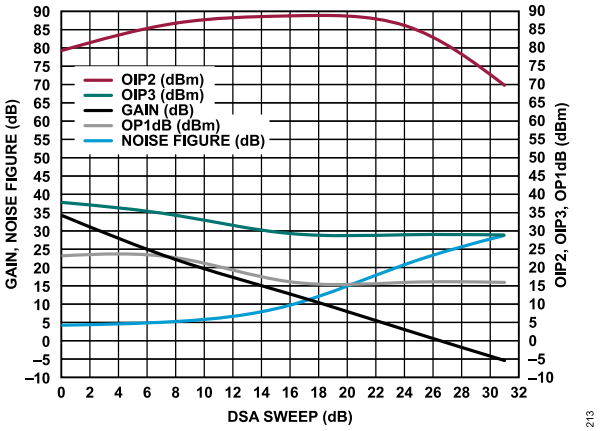

Figure 113. Gain, Noise Figure, OIP2, OIP3, OP1dB vs. DSA Sweep, Frequency = 5000 MHz

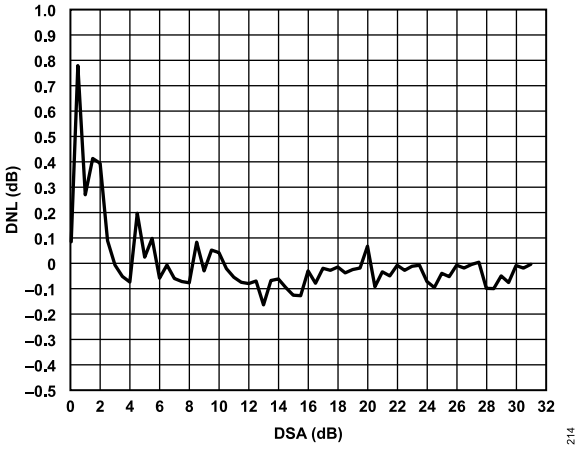

Figure 114. DSA Gain Step Error; Frequency = 4700 MHz

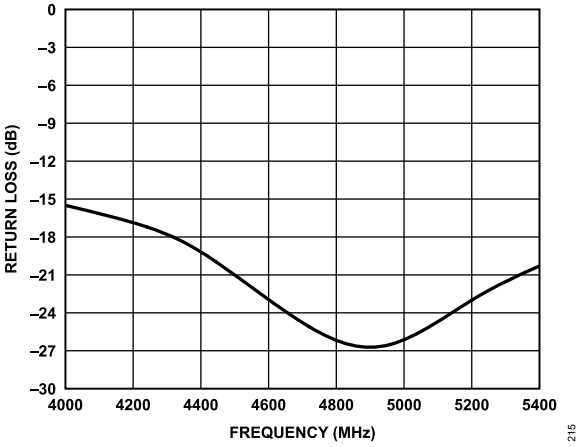

Figure 115. Return Loss of Differential RF Input S11 at 50 Ω Match

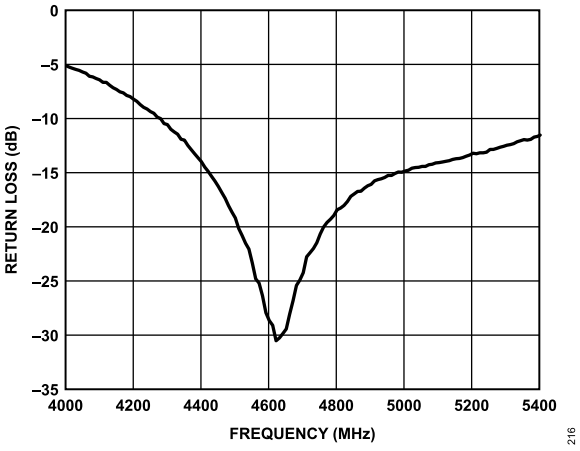

Figure 116. Return Loss of Single-Ended RF Output S22 at 50 Ω Match

TYPICAL PERFORMANCE CHARACTERISTICS

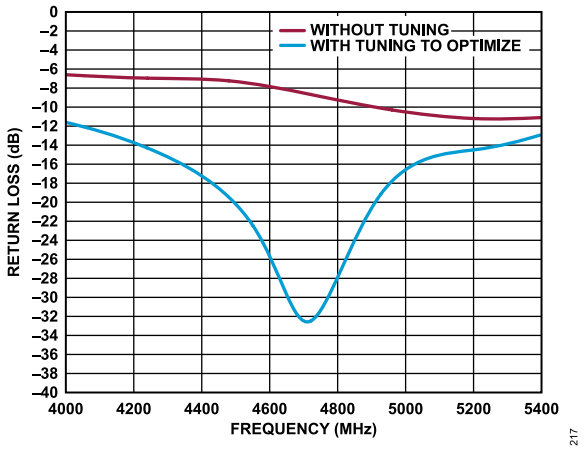

Figure 117. Return Loss of Differential RF Input S11 at 100 Ω Match; 0.6 pF in Shunt and 0.8 nH Series on Each Input

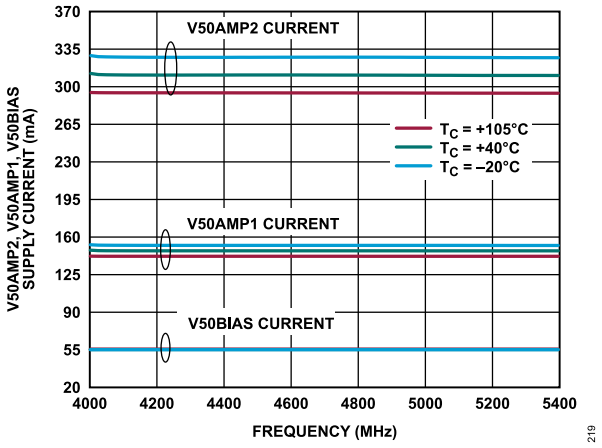

Figure 119. V50AMP1, V50AMP2, and V50BIAS Current vs. Frequency for Various Temperatures

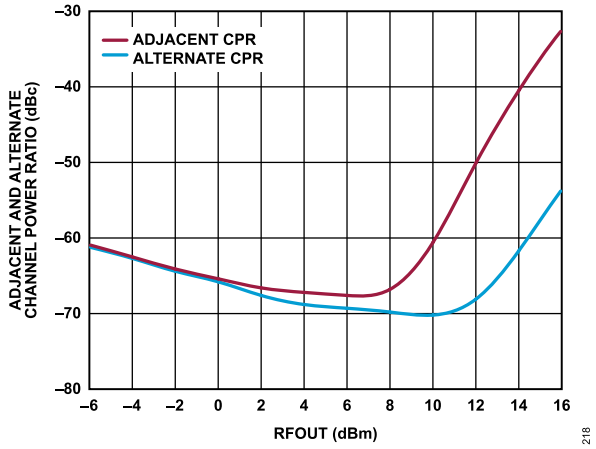

Figure 118. Adjacent and Alternate Channel Power Ratio vs. Output Power (RFOUT) by P_{IN} at 4700 MHz, LTE Test Model 1.1 (TM1.1) 5 MHz, DSA = 0 dB

THEORY OF OPERATION

A typical RF transmitter transmits RF power at a fixed output level. System gain varies over time, temperature, and process. Therefore, a gain adjustable block is needed to calibrate and compensate this variation. A VGA provides this programmable gain function.

The ADL6337 is a highly integrated RF VGA solution for transmit paths. It provides a single-chip solution that contains a balun for differential to single-ended signal conversion, digital attenuation, and gain stages while offering high dynamic range multicarrier transmitter designs.

The ADL6337 is a highly integrated 2-stage VGA used to interface an RF DAC to the power amplifier in the transmitter. It offers multiple gain control options with a 31.5 dB attenuation range in 0.5 dB steps integrating a RF Digital Step Attenuator (DSA1), a high linearity amplifier, followed by a second RF Digital Step Attenuator (DSA2), and a second high linearity amplifier.

Putting together the ADL6337 building blocks, the signal path through the device starts with converting the differential inputs to single ended by the integrated balun at the output.

The integrated building blocks of the ADL6337 are programmable via the SPI.

RF INPUT AND OUTPUT

The input impedance is 50 Ω differential and the output impedance is 50 Ω single-ended to allow the device to be driven by the DAC . 100 Ω differential inputs can be also achieved with external matching networks. See the Input and Output Port Matching section.

PROGRAMMABILITY GUIDE

Viewing the register map at the highest level, the registers are subdivided into the major functional blocks, as shown in Table 7. See the Register Summary section for a complete list of all the registers on the ADL6337.

Table 7. Memory Map Functional Groups

Register Address	Functional Blocks
0x000 to 0x011	SPI configuration
0x100	Function enable
0x102, 0x114, 0x115, 0c116	Four DSA preconfigurations settings (TXENP = 1)
0x103	DSA configuration (TXENP = 0)
0x104 to 0x106, 0x110 to 0x113	IREF and IP3 configuration
0x10A, 0x10B	DSA1 and DSA2 manual configuration
0x120	SPI supply control

The ADL6337 has a unique feature controlled by TXENP, Pin 1 (see Table 8). The TXENP pin can perform fast on/off switching of device operations for time division duplex (TDD) transmit applications. When TXENP is set to low (0 V), AMP1 and AMP2 are disabled (power-down mode) and current consumptions are reduced. Also, use this mode to adjust DSA level in Register 0x103. Its default attenuation level is the maximum (31.5 dB).

The normal operation mode of the ADL6337 uses the TXENP pin set high, but it is recommended that TXENP be set to low when configuring the registers. When ramping the TXENP pin high, normal operation starts, and the 0x100, 0x10A, 0x10B, 0x102, 0x104, 0x105, 0x106, 0x111, 0x112, 0x113, 0x110, 0x114, 0x115, and 0x116 registers are used for operation.

Register 0x100 comprises enable bits for the DSA1, AMP1, DSA2, AMP2, and IP3 tuning blocks (see Table 9). The default value of 0x07 in Register 0x100 allows for four DSA preconfiguration settings, selectable by ATTSEL1 (Pin 9) and ATTSEL2 (Pin 10). It is also called Attenuation State 0, 1, 2, and 3 (see Table 10).

The 0x102, 0x114, 0x115, and 0x116 registers can configure the DSA attenuation levels.

- Attenuation State 0:
  - ATTSEL2 (Pin 10) = low
  - ATTSEL1 (Pin 9) = low
- Attenuation State 1:
  - ATTSEL2 (Pin 10) = low
  - ATTSEL1 (Pin 9) = high
- Attenuation State 2:
  - ATTSEL2 (Pin 10) = high
  - ATTSEL1 (Pin 9) = low
- Attenuation State 3:
  - ATTSEL2 (Pin 10) = high
  - ATTSEL1 (Pin 9) = high

After the software reset asserts, the default settings for each mode are shown in Table 9. Parameters can be overwritten before or during the operations.

This feature allows for rapid RF performance switching using asynchronous external control with the ATTSEL1 and ATTSEL2 Pins. When the ATTSEL feature is not used and only one fixed attenuation level is used for operation, it is recommended to connect ATTSEL1 and ATTSEL2 to GND (0 V) and configure Register 0x102 for Attenuation State 0 to set the DSA attenuation level.

Note that the DSA1 and DSA2 attenuation levels cannot be configured individually in the four preconfiguration settings. The maximum attenuation level is 31.5 dB. If 20 dB attenuation is selected, the attenuation level in DSA2 is maximized first, and the rest of attenuation level is implemented in DSA1. It indicates that the attenuation levels are automatically allocated in the DSA1 and DSA2 blocks to maximize the noise figure performance. Note that the maximum attenuation level in DSA2 is 15.75 dB, which has the duplicated register value at 31 and 32 decimals in the 0x102, 0x114, 0x115, and 0x116 registers. The next attenuation (16.26 dB) in DSA1 starts at the 33 decimal value.

Setting DSA_MAN_EN_0[7] = 1 in Register 0x100 allows for individual control attenuation levels of DSA1 and DSA2 in Register 0x10A and Register 0x10B.

If the TXENP pin is held high when the 5 V supplies are applied, the device ramps up with the 5 V supplies. It is suggested that TXENP be held low during power-up.

ATTSEL1 and ATTSEL2 can be used to preset the DSA to any value from 0 dB to 31.5 dB by preprogramming the desired values via the SPI or using the default values provided in Table 10.

Table 8. TXENP Mode Selection

TXENP (Pin 1)	Operation Mode	Register to Use for Configuration	Description
0 (Low)	Power-down mode	0x103	To adjust DSA level manually. Default is the maximum attenuation level. AMP1 and AMP2 are disabled.
1 (High)	Normal operation mode	0x100	Enable AMP1, AMP2, LDO, etc. Enable bit to adjust DSA1 and DSA2 individually.
		0x10A, 0x10B	To adjust DSA1 and DSA2 levels individually at DSA_MAN_EN_0 0x100[7] = 1.
		0x102, 0x114, 0x115, 0x116	Four preconfiguration DSA attenuation settings by ATTSEL1 (Pin 9) and ATTSEL2 (Pin 10) at DSA_MAN_EN_0 0x100[7] = 0 (default).

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Table 8. TXENP Mode Selection (Continued)

TXENP (Pin 1)	Operation Mode	Register to Use for Configuration	Description
		0x110	IP3 Linearization Block Enable register. Use default to enable.
		0x104, 0x105, 0x106, 0x111, 0x112, 0x113	IP3 linearization trimming values for AMP1 and AMP2 (for example, 0x010).

Table 9. Register 0x100: Enable Register for Normal Operation

Bits	Bit Name	Description	Reset	Access
7	DSA_MAN_EN_0	DSA Manual Mode Enable When TXENP = 1. 0: Enable four preconfiguration settings via ATTSEL pins 1: Register 0x10A, 0x10B are used to configure DSA1 and DSA2 individually.	0x0	R/W
6	AMP2_IP3_OFF_0_0	Turn off AMP2 IP3 Currents ATTSEL00 When TXENP = 1. 0: Use default 1: Analog Devices internal	0x0	R/W
5	AMP1_IP3_OFF_0_0	Turn off AMP1 IP3 Currents ATTSEL00 When TXENP = 1. 0: Use default 1: Analog Devices internal	0x0	R/W
4	LDO33_EN_0	Not used.	0x0	R/W
3	EN_IBIASGEN_RESISTOR_0	Not used.	0x0	R/W
2	EN_IBIASGEN_0	Enable Bias Generator When TXENP = 1. 0: disable. 1: enable.	0x1	R/W
1	AMP2_EN_0	Enable Amp 2 When TXENP = 1. 0: disable. 1: enable.	0x1	R/W
0	AMP1_EN_0	Enable Amp 1 When TXENP = 1. 0: disable. 1: enable.	0x1	R/W

Table 10. Four Preconfiguration Settings for DSA

Attenuation State	ATTSEL2 (Pin 10)	ATTSEL1 (Pin 9)	Reg. Address	Register Name	Bits	Bit 7	Bit 6	Bits[5:0], DSA Setting 0 dB to 31.5 dB at 0.5 dB Step
0	0	0	0x102	SIG_PATH2_0	[5:0]	N/A	N/A	Default = 0.0 dB attenuation
1	0	1	0x114	DSA_ATTSEL_1	[5:0]	N/A	N/A	Default = 12.2 dB attenuation
2	1	0	0x115	DSA_ATTSEL_2	[5:0]	N/A	N/A	Default = 23.88 dB attenuation
3	1	1	0x116	DSA_ATTSEL_3	[5:0]	N/A	N/A	Default = 31.5 dB attenuation

LINEARITY AND PERFORMANCE OPTIMIZATION (REFERENCE ONLY)

The ADL6337 includes a linearity and performance optimization feature to change two types of bias current blocks: IREF and IP3.

The IREF adjustment feature is used for optimizing the output power and current consumptions. It can be individually tuned for each attenuation state (0, 1, 2, and 3) and for AMP1 and AMP2, which are controlled via ATTSEL1 and ATTSEL2. The enable and disable functions are controlled in Register 0x100[1:0] (seeTable 9), which are the main enable bits for AMP1 and AMP2. Table 11 shows a summary of IREF register address and bit names.

Use the IP3 feature to tune linearity performance. It can be enabled and disabled individually for AMP1 and AMP2 and for each attenuation state (0, 1, 2, and 3). See Table 12. All attenuation states, however, use the same optimized values for AMP1 and AMP2. Store the optimized values in Register 0x105[4:0] for AMP1 (see Table 13) and Register 0x106[4:0] for AMP2 (see Table 14). The Typical Performance Characteristics section uses the specific IREF and IP3 values to achieve the performance shown in Table 15.

Table 11. IREF Register Summary

	Attenuation State	ATTSEL2 Pin 10	ATTSEL1 Pin 9	AMP1		AMP2	
				Register Address	Bit Name	Register Address	Bit Name
IREF	0	0	0	0x104[3:0]	TRM_AMP1_IREF_0_0	0x104[7:4]	TRM_AMP2_IREF_0_0
	1	0	1	0x111[3:0]	TRM_AMP1_IREF_1	0x111[7:4]	TRM_AMP2_IREF_1
	2	1	0	0x112[3:0]	TRM_AMP1_IREF_2	0x112[7:4]	TRM_AMP2_IREF_2
	3	1	1	0x113[3:0]	TRM_AMP1_IREF_3	0x113[7:4]	TRM_AMP2_IREF_3

Table 12. IP3 Enable/Disable Register Bits

Attenuation State	ATTSEL2 Pin 10	ATTSEL1 Pin 9	AMP1		AMP1	
			Register Address	Bit Name	Register Address	Bit Name
0	0	0	0x100 [5]	AMP1_IP3_OFF_0_0	0x100 [6]	AMP2_IP3_OFF_0_0
1	0	1	0x110 [0]	AMP1_IP3_OFF_1	0x110 [4]	AMP2_IP3_OFF_1
2	1	0	0x110 [1]	AMP1_IP3_OFF_2	0x110 [5]	AMP2_IP3_OFF_2
3	1	1	0x110 [2]	AMP1_IP3_OFF_3	0x110 [6]	AMP2_IP3_OFF_3

Table 13. 0x105 IP3 Register for AMP1

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	TRM_AMP1_IP3_0	Amp 1 IP3 Trim When TXENP = 1.	0x0	R/W

Table 14. 0x106 IP3 Register for AMP2

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	TRM_AMP2_IP3_0	Amp 2 IP3 Trim When TXENP = 1.	0x5	R/W

Table 15. Optimized IREF and IP3 Values

Variant	Operating Frequency (MHz)	TRM_AMP1_IP3_0	TRM_AMP2_IP3_0	TRM_AMP1_IREF_0_0, TRM_AMP1_IREF_1 TRM_AMP1_IREF_2 TRM_AMP1_IREF_3	TRM_AMP2_IREF_0_0 TRM_AMP2_IREF_1 TRM_AMP2_IREF_2 TRM_AMP2_IREF_3
ADL6337-A	500 to 1000	2 (0x2)	3 (0x3)	13 (0xD)	11 (0xB)
ADL6337-B	1350 to 2800	5 (0x5)	5 (0x5)	12 (0xC)	11 (0xB)
ADL6337-C	3100 to 4400	6 (0x6)	6 (0x6)	11 (0xB)	11 (0xB)
ADL6337-D	4400 to 5200	1 (0x1)	1 (0x1)	12 (0xC)	12 (0xC)

SPI

The SPI of the ADL6337 allows device configuration for specific functions or operations via a 3- or 4-wire SPI mode. This interface consists of four control lines: SCLK, SDIO, SDO, and $\overline{CS}$ for 4-wire SPI mode. SCLK, SDIO, and $\overline{CS}$ are used for 3-wire SPI mode and the default setting is configured as 3-wire SPI mode. To enable 4-wire SPI mode, set SDOACTIVE[3] and SDOACTIVE_[4] in Register 0x000 to 1. The timing requirements for the 4-wire SPI port are shown in Figure 4.

It is recommended to assert the software reset every time when the power is ramped. There are two types of the software reset implemented in the ADL6337 (see Table 16). The first type resets only a specific chip to send 0x01 in Register 0x020 when multiple ADL6337 devices are connected (single-chip reset mode). In this case, only one device can be reset, and the reset is not asserted to the other devices. Defining the specific SPI chip address in the SPI transactions is also necessary. See the Configuring Multiple Chips to Share the SPI Bus section. Another way is to reset multiple ADL6337 devices simultaneously by sending 0x81 in Register 0x000 (broadcasting reset mode).

Table 16. Software Reset Type

Reset Type	Address	Data
Single-Chip Reset Mode	0x020	0x1
Broadcasting Reset Mode	0x000	0x81

The ADL6337 protocol consists of a read/write bit, six chip select ID bits (3 MSBs are always 0s), nine register address bits, followed by eight data bits. Both the address and data fields are organized with the MSB first and end with the LSB by default. The chip select ID bits are externally configured by the CS_A2, CS_A1, and CS_A0 pins.

The ADL6337 input logic level for the write cycle is with a 1.8 V logic level.

On a read cycle, the SDO pin is configurable for 1.8 V (default) or 3.3 V output levels by setting the SPI_1P8_3P3_CTRL bit (Register 0x120, Bit 0).

CONFIGURING MULTIPLE CHIPS TO SHARE THE SPI BUS

Up to eight ADL6337 devices can be addressed using the same 3- or 4-wire SPI, which means no extra $\overline{CS}$ line is needed for each device. For this capability, the chip address pins (CS_A2, CS_A1, CS_A0) of the ADL6337 are used to identify the chip with the SPI write chip address prefix. See the SPI interface port as shown in Figure 2.

The ADL6337 ignores any writes to addresses where the six MSBs are not equal to the chip address as set by the chip address pins. It only accepts access for addresses where the six MSB chip address prefix is equal to the chip address pins. The broadcasting software reset mode in Register 0x000 allows for an exception. All ADL6337 chips on the shared bus can accept a 0x81 software reset in Register 0x000 from the SPI host controller.

Figure 120 shows how to configure the chip address pins CS_CA2, CS_CA1, and CS_CA0 with the associated chip address prefix bits.

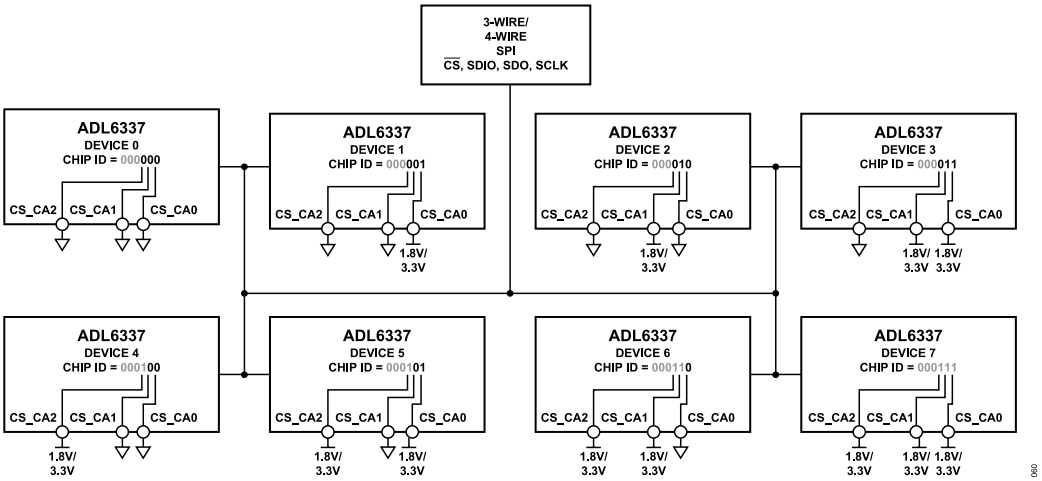

Figure 120. Configuring Multiple Chips to Share the SPI Bus

DEVICE SETUP

The recommended ADL6337 setup sequence is as follows:

1. Supply 5.0 V.
2. Set TXENP (Pin 1) to low (GND). The power-down mode is recommended to configure the ADL6337 via SPI.
3. Send the data in Table 17 via SPI.
4. Set TXENP (Pin 1) to high (5.0 V) to start the normal operation mode.

Table 17. SPI Sample Script for ADL6337-B

Address	Value	Note
0x000	0x81	Software reset
0x000	0x00	3-wire SPI mode
0x100	0x07	Enable register
0x102	0x00	DSA value 0 dB ATTSEL = 00
0x104	0xBC	IREF AMP2 = 11, AMP1 = 12 for ATTSEL = 00
0x105	0x05	IP3 value 5 for AMP1
0x106	0x05	IP3 value 5 for AMP2
0x111	0xBC	IREF AMP2 = 11, AMP1 = 12 for ATTSEL = 01
0x112	0xBC	IREF AMP2 = 11, AMP1 = 12 for ATTSEL = 10
0x113	0xBC	IREF AMP2 = 11, AMP1 = 12 for ATTSEL = 11
0x114	0x1F	DSA value 15.75 dB for ATTSEL = 01
0x115	0x21	DSA value 16.26 dB for ATTSEL = 10
0x116	0x3F	DSA value 31.50 dB for ATTSEL = 11

BASIC CONNECTIONS

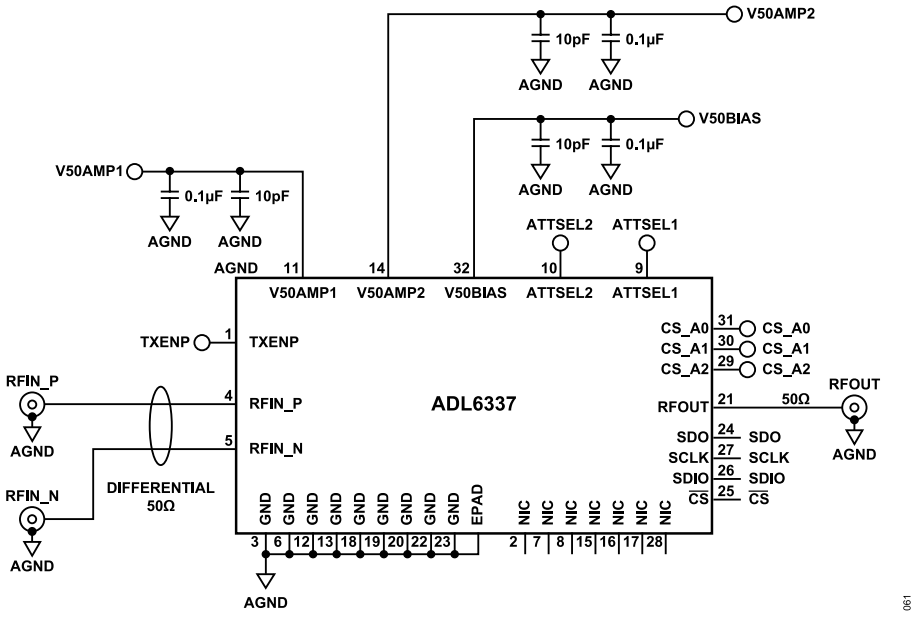

Figure 121. Basic Connections

Table 18. Basic Connections

Functional Blocks	Pin No.	Mnemonic	Description	Basic Connection
5 V	11, 14	V50AMP1, V50AMP2	Amplifiers, analog supply voltage, 5 V	Decouple this pin via 10 pF, 0.1 µF capacitors to ground. Ensure that the decoupling capacitors are located close to the pin.
Fast Attenuation	10, 9	ATTSEL1, ATTSEL2	Fast attenuation selection	
RF Input	4, 5	RFIN_P, RFIN_N	RF inputs	Differential RF input.
RF Output	21	RFOUT	RFOUT	RF output, single-ended.
Serial Port	25	$\overline{CS}$	Active-low chip select	1.8 V to 3.3 V tolerant logic levels.
	27	SCLK	SPI clock	1.8 V to 3.3 V tolerant logic levels.
	24	SDO	SPI data input	1.8 V to 3.3 V tolerant logic levels.
	26	SDIO	SPI data output	1.8 V to 3.3 V tolerant logic levels.
V50BIAS	32	V50BIAS	Bias circuitry power supply (5.0 V)	Decouple this pin via 10 pF, 0.1 µF capacitors to ground. Ensure that the decoupling capacitors are located close to the pin.
Chip Selection	29, 30, 31	CS_A2, CS_A1, CS_A0	SPI chip select (see the Configuring Multiple Chips to Share the SPI Bus section for information about the connections in a multiple chip operation; ground these pins if unused)	Chip selection.
Device Enable	1	TXENP	Active high for normal operation	
Ground	3, 6, 12, 13, 18, 19, 20, 22, 23	GND	Ground	Connect these pins to the ground of the printed circuit board.
EPAD	Exposed pad	Exposed pad	Exposed pad	Exposed Pad 1. The exposed pad must be connected to ground for electrical and thermal purposes.
NIC	2, 7, 8, 15, 16, 17, 28	NIC	NIC	No internal connection. These pins have no physical connection within the chip. They can be grounded or floated.

INPUT AND OUTPUT PORT MATCHING

The ADL6337 has four variants for four operating frequency ranges. Each variant has different input port matching schemes. The ADL6337-A requires external matching components for a 50 Ω input impedance to achieve the return loss specification, and external matching components are required for 100 Ω source matching. See Figure 122. The ADL6337-B, the ADL6337-C, and ADL6337-D do not require any external components to match the 50 Ω input impedance. However, the external matching components must match the single-ended 50 Ω load impedance only for the ADL6337-C and ADL6337-D. Additionally, the external matching components must match the 100 Ω input source impedance. See Figure 123, Figure 124, and Figure 125. Note that the matching components can be changed due to the board structures and materials.

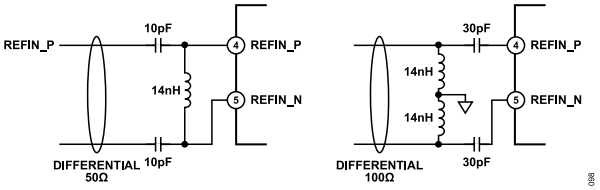

Figure 122. Input Matching Components for the ADL6337-A

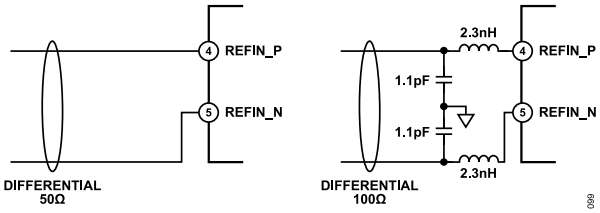

Figure 123. Input Matching Components for the ADL6337-B

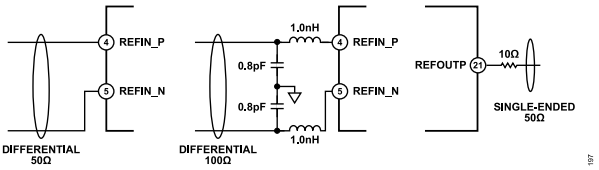

Figure 124. Input and Output Components for the ADL6337-C

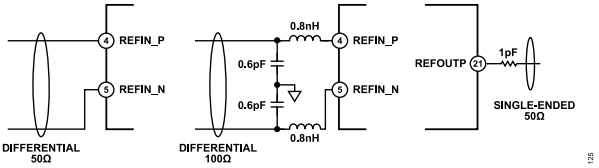

Figure 125. Input and Output Components for the ADL6337-D

REGISTER SUMMARY

Table 19. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x000	ADI_SPI_CONFIG	[7:0]	SOFTRESET_	LSB_FIRST_	ENDIAN_	SDOACTIVE_	SDOACTIVE	ENDIAN	LSB_FIRST	SOFTRESET	0x00	R/W
0x001	REG_0X0001	[7:0]	SINGLE_INSTRUCTION	CSB_STALL	PRIMARY_SUBORDINATE_RB	RESERVED		SOFT_RESET		PRIMARY_SUBORDINATE_TRANSFER	0x00	R/W
0x003	CHIPTYPE	[7:0]	CHIPTYPE								0x00	R
0x004	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x5B	R
0x005	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x00A	SCRATCHPAD	[7:0]	SCRATCHPAD								0x00	R/W
0x00B	SPI_REV	[7:0]	SPI_REV								0x00	R
0x010	FEOL	[7:0]	FEOL				RESERVED				0x00	R
0x011	BEOL_SIF	[7:0]	SIF				BEOL				0x02	R
0x012	VARIANT	[7:0]	VARIANT								0x14/0x15	R
0x020	SOFTRST_CHIP	[7:0]	RESERVED							SOFTRESET_CHIP	0x00	R/W
0x100	SIG_PATH0_0	[7:0]	DSA_MAN_EN_0	AMP2_IP3_OFF_0_0	AMP1_IP3_OFF_0_0	LDO33_EN_0	EN_IBIASGEN_RESISTOR_0	EN_IBIASGEN_0	AMP2_EN_0	AMP1_EN_0	0x07	R/W
0x102	SIG_PATH2_0	[7:0]	RESERVED		DSA_ATTEN_0_0						0x3F	R/W
0x103	SIG_PATH3_0	[7:0]	RESERVED		DSA_ATTEN_0_1						0x3F	R/W
0x104	SIG_PATH4_0	[7:0]	TRM_AMP2_IREF_0_0				TRM_AMP1_IREF_0_0				0x55	R/W
0x105	SIG_PATH5_0	[7:0]	RESERVED			TRM_AMP1_IP3_0					0x00	R/W
0x106	SIG_PATH6_0	[7:0]	RESERVED			TRM_AMP2_IP3_0					0x05	R/W
0x10A	SIG_PATHA_0	[7:0]	RESERVED			DSA1_MAN_ATTEN					0x00	R/W
0x10B	SIG_PATHB_0	[7:0]	RESERVED			DSA2_MAN_ATTEN					0x00	R/W
0x110	AMPS_IP3_ATTSEL	[7:0]	RESERVED	AMP2_IP3_OFF_3	AMP2_IP3_OFF_2	AMP2_IP3_OFF_1	RESERVED	AMP1_IP3_OFF_3	AMP1_IP3_OFF_2	AMP1_IP3_OFF_1	0x00	R/W
0x111	TRM_AMPS_IREF_1	[7:0]	TRM_AMP2_IREF_1				TRM_AMP1_IREF_1				0x55	R/W
0x112	TRM_AMPS_IREF_2	[7:0]	TRM_AMP2_IREF_2				TRM_AMP1_IREF_2				0x55	R/W
0x113	TRM_AMPS_IREF_3	[7:0]	TRM_AMP2_IREF_3				TRM_AMP1_IREF_3				0x55	R/W
0x114	DSA_ATTSEL_1	[7:0]	RESERVED		DSA_ATTEN_1						0x18	R/W
0x115	DSA_ATTSEL_2	[7:0]	RESERVED		DSA_ATTEN_2						0x30	R/W
0x116	DSA_ATTSEL_3	[7:0]	RESERVED		DSA_ATTEN_3						0x3F	R/W
0x120	DIG_CTRL	[7:0]	RESERVED							SPI_1P8_3P3_CTRL	0x00	R/W

REGISTER DETAILS

Address: 0x000, Reset: 0x00, Name: ADI_SPI_CONFIG

Table 20. Bit Descriptions for ADI_SPI_CONFIG

Bits	Bit Name	Description	Reset	Access
7	SOFTRESET_	Soft Reset for the Broadcasting Mode 0: Reset not asserted. 1: Reset asserted.	0x0	R/W
6	LSB_FIRST_	Least Significant Bit (LSB) First 0: Most Significant Bit (MSB) first 1: LSB first	0x0	R/W
5	ENDIAN_	Endian 0: Little Endian 1: Big Endian	0x0	R/W
4	SDOACTIVE_	SDO Active 0: SDO Inactive, 3-wire SPI Mode 1: SDO Active for 4-wire SPI Mode	0x0	R/W
3	SDOACTIVE	SDO Active 0: SDO Inactive, 3-wire SPI Mode 1: SDO Active for 4-wire SPI Mode	0x0	R/W
2	ENDIAN	Endian. 0: Little Endian 1: Big Endian	0x0	R/W
1	LSB_FIRST	LSB First 0: MSB first 1: LSB first.	0x0	R/W
0	SOFTRESET	Soft Reset for the Broadcasting Mode 0: Reset not asserted. 1: Reset asserted.	0x0	R/W

Address: 0x001, Reset: 0x00, Name: REG_0X0001

Table 21. Bit Descriptions for REG_0X0001

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INSTRUCTION	Single Instruction. ADI internal.	0x0	R/W
6	CSB_STALL	$\overline{CS}$ Stall. ADI internal.	0x0	R/W
5	PRIMARY_SUBORDINATE_RB	Primary Subordinate RB. ADI internal.	0x0	R/W
[4:3]	RESERVED	Reserved. ADI internal.	0x0	R
[2:1]	SOFT_RESET	Soft Reset. ADI internal.	0x0	R/W
0	PRIMARY_SUBORDINATE_TRANSFER	Primary Subordinate Transfer. ADI internal.	0x0	R/W

Address: 0x003, Reset: 0x00, Name: CHIPTYPE

Table 22. Bit Descriptions for CHIPTYPE

Bits	Bit Name	Description	Reset	Access
[7:0]	CHIPTYPE	Chip Type, Read Only	0x0	R

Address: 0x004, Reset: 0x00, Name: PRODUCT_ID_L

Table 23. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product_ID_L, Lower 8 Bits ADL6337	0x5B	R

Address: 0x005, Reset: 0x00, Name: PRODUCT_ID_H

REGISTER DETAILS

Table 24. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product_ID_L, Higher 8 Bits	0x0	R

Address: 0x00A, Reset: 0x00, Name: SCRATCHPAD

Table 25. Bit Descriptions for SCRATCHPAD

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCHPAD	Scratchpad	0x0	R/W

Address: 0x00B, Reset: 0x00, Name: SPI_REV

Table 26. Bit Descriptions for SPI_REV

Bits	Bit Name	Description	Reset	Access
[7:0]	SPI_REV	SPI Register Map Rev	0x0	R

Address: 0x010, Reset: 0x00, Name: FEOL

Table 27. Bit Descriptions for FEOL

Bits	Bit Name	Description	Reset	Access
[7:4]	FEOL	FEOL	0x0	R
[3:0]	RESERVED	Reserved	0x0	R

Address: 0x011, Reset: 0x00, Name: BEOL_SIF

Table 28. Bit Descriptions for BEOL_SIF

Bits	Bit Name	Description	Reset	Access
[7:4]	SIF	SIF Version	0x0	R
[3:0]	BEOL	BEOL Version 0x02: Variant A,Variant B, and Variant C	0x02	R

Address: 0x012, Reset: 0x00, Name: VARIANT

Table 29. Bit Descriptions for VARIANT

Bits	Bit Name	Description	Reset	Access
[7:0]	VARIANT	Variant 0x14: Variant A 0x15: Variant B 0x23: Variant C	 0x14 /0x15 /0x23	R

Address: 0x020, Reset: 0x00, Name: SOFTRST_CHIP

Table 30. Bit Descriptions for SOFTRST_CHIP

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved	0x0	R
0	SOFTRESET_CHIP	SoftReset for a Single Chip 0: Reset not asserted. 1: Reset asserted.	0x0	R/W

Address: 0x100, Reset: 0x07, Name: SIG_PATH0_0

Table 31. Bit Descriptions for SIG_PATH0_0

Bits	Bit Name	Description	Reset	Access
7	DSA_MAN_EN_0	DSA Manual Mode Enable When TXENP = 1 0: Enable 4-Predefine mode via ATTSEL pins. 1: Registers 0x10A, 0x10B are used to configure DSA1 and DSA2 individually.	0x0	R/W
6	AMP2_IP3_OFF_0_0	Turn Off AMP2 IP3 Currents ATTSEL00 When TXENP = 1 0: Use default	0x0	R/W

REGISTER DETAILS

Table 31. Bit Descriptions for SIG_PATH0_0 (Continued)

Bits	Bit Name	Description	Reset	Access
		1: Debug only		
5	AMP1_IP3_OFF_0_0	Turn Off AMP1 IP3 Currents ATTSEL00 When TXENP = 1 0: Use default 1: Debug only	0x0	R/W
4	LDO33_EN_0	Not used.	0x0	R/W
3	EN_IBIASGEN_RESISTOR_0	Not used.	0x0	R/W
2	EN_IBIASGEN_0	Enable Bias Generator When TXENP = 1 0: Disable 1: Enable	0x1	R/W
1	AMP2_EN_0	Enable Amp 2 When TXENP = 1 0: Disable 1: Enable	0x1	R/W
0	AMP1_EN_0	Enable Amp 1 When TXENP = 1 0: Disable 1: Enable	0x1	R/W

Address: 0x102, Reset: 0x3F, Name: SIG_PATH2_0

Table 32. Bit Descriptions for SIG_PATH2_0

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved	0x0	R
[5:0]	DSA_ATTEN_0_0	DSA Attenuator Setting ATTSEL00 When TXENP = 1 DSA2 000000 (0): 0.00 dB 000001 (1): 0.51 dB 000010 (2): 1.02 dB 000011 (3): 1.53 dB 000100 (4): 2.04 dB 000101 (5): 2.55 dB 000110 (6): 3.05 dB 000111 (7): 3.56 dB 001000 (8): 4.07 dB 001001 (9): 4.58 dB 001010 (10): 5.09 dB 001011 (11): 5.59 dB 001100 (12): 6.10 dB 001101 (13): 6.61 dB 001110 (14): 7.12 dB 001111 (15): 7.63 dB 010000 (16): 8.13 dB 010001 (17): 8.64 dB 010010 (18): 9.15 dB 010011 (19): 9.66 dB 010100 (20): 10.17 dB 010101 (21): 10.67 dB 010110 (22): 11.18 dB 010111 (23): 11.69 dB 011000 (24): 12.20 dB 011001 (25): 12.71 dB 011010 (26): 13.21 dB 011011 (27): 13.72 dB	0x3F	R/W

REGISTER DETAILS

Table 32. Bit Descriptions for SIG_PATH2_0 (Continued)

Bits	Bit Name	Description	Reset	Access
		011100 (28): 14.23 dB 011101 (29): 14.74 dB 011110 (30): 15.25 dB 011111 (31) and 100000 (32): 15.75 dB. Boundary state from DSA2 to DSA1 stage. DSA2 + DSA1 100001 (33): 16.26 dB 100010 (34): 16.77 dB 100011 (35): 17.28 dB 100100 (36): 17.79 dB 100101 (37): 18.30 dB 100110 (38): 18.80 dB 100111 (39): 19.31 dB 101000 (40): 19.82 dB 101001 (41): 20.33 dB 101010 (42): 20.84 dB 101011 (43): 21.34 dB 101100 (44): 21.85 dB 101101 (45): 22.36 dB 101110 (46): 22.87 dB 101111 (47): 23.38 dB 110000 (48): 23.88 dB 110001 (49): 24.39 dB 110010 (50): 24.90 dB 110011 (51): 25.41 dB 110100 (52): 25.92 dB 110101 (53): 26.42 dB 110110 (54): 26.93 dB 110111 (55): 27.44 dB 111000 (56): 27.95 dB 111001 (57): 28.46 dB 111010 (58): 28.96 dB 111011 (59): 29.47 dB 111100 (60): 29.98 dB 111101 (61): 30.49 dB 111110 (62): 31.00 dB 111111 (63): 31.50 dB		

Address: 0x103, Reset: 0x3F, Name: SIG_PATH3_0

Table 33. Bit Descriptions for SIG_PATH3_0

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	DSA_ATTEN_0_1	DSA Attenuator Setting ATTSEL00 When TXENP = 0 DSA2 000000 (0): 0.00 dB 000001 (1): 0.51 dB 000010 (2): 1.02 dB 000011 (3): 1.53 dB 000100 (4): 2.04 dB 000101 (5): 2.55 dB 000110 (6): 3.05 dB 000111 (7): 3.56 dB	0x3F	R/W

REGISTER DETAILS

Table 33. Bit Descriptions for SIG_PATH3_0 (Continued)

Bits	Bit Name	Description	Reset	Access
		001000 (8): 4.07 dB 001001 (9): 4.58 dB 001010 (10): 5.09 dB 001011 (11): 5.59 dB 001100 (12): 6.10 dB 001101 (13): 6.61 dB 001110 (14): 7.12 dB 001111 (15): 7.63 dB 010000 (16): 8.13 dB 010001 (17): 8.64 dB 010010 (18): 9.15 dB 010011 (19): 9.66 dB 010100 (20): 10.17 dB 010101 (21): 10.67 dB 010110 (22): 11.18 dB 010111 (23): 11.69 dB 011000 (24): 12.20 dB 011001 (25): 12.71 dB 011010 (26): 13.21 dB 011011 (27): 13.72 dB 011100 (28): 14.23 dB 011101 (29): 14.74 dB 011110 (30): 15.25 dB 011111 (31) and 100000 (32): 15.75 dB. Boundary state from DSA2 to DSA1 stage. DSA2 + DSA1 100001 (33): 16.26 dB 100010 (34): 16.77 dB 100011 (35): 17.28 dB 100100 (36): 17.79 dB 100101 (37): 18.30 dB 100110 (38): 18.80 dB 100111 (39): 19.31 dB 101000 (40): 19.82 dB 101001 (41): 20.33 dB 101010 (42): 20.84 dB 101011 (43): 21.34 dB 101100 (44): 21.85 dB 101101 (45): 22.36 dB 101110 (46): 22.87 dB 101111 (47): 23.38 dB 110000 (48): 23.88 dB 110001 (49): 24.39 dB 110010 (50): 24.90 dB 110011 (51): 25.41 dB 110100 (52): 25.92 dB 110101 (53): 26.42 dB 110110 (54): 26.93 dB 110111 (55): 27.44 dB 111000 (56): 27.95 dB 111001 (57): 28.46 dB 111010 (58): 28.96 dB 111011 (59): 29.47 dB		

REGISTER DETAILS

Table 33. Bit Descriptions for SIG_PATH3_0 (Continued)

Bits	Bit Name	Description	Reset	Access
		111100 (60): 29.98 dB 111101 (61): 30.49 dB 111110 (62): 31.00 dB 111111 (63): 31.50 dB		

Address: 0x104, Reset: 0x55, Name: SIG_PATH4_0

Table 34. Bit Descriptions for SIG_PATH4_0

Bits	Bit Name	Description	Reset	Access
[7:4]	TRM_AMP2_IREF_0_0	Amp 2 IREF Trim ATTSEL00 When TXENP = 1	0x5	R/W
[3:0]	TRM_AMP1_IREF_0_0	Amp 1 IREF Trim ATTSEL00 When TXENP = 1	0x5	R/W

Address: 0x105, Reset: 0x00, Name: SIG_PATH5_0

Table 35. Bit Descriptions for SIG_PATH5_0

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved	0x0	R
[4:0]	TRM_AMP1_IP3_0	Amp 1 IP3 Trim When TXENP = 1	0x0	R/W

Address: 0x106, Reset: 0x05, Name: SIG_PATH6_0

Table 36. Bit Descriptions for SIG_PATH6_0

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved	0x0	R
[4:0]	TRM_AMP2_IP3_0	Amp 2 IP3 Trim When TXENP = 1	0x5	R/W

Address: 0x10A, Reset: 0x00, Name: SIG_PATHA_0

Table 37. Bit Descriptions for SIG_PATHA_0

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	DSA1_MAN_ATTEN	DSA1 Attenuator Manual Setting 000000 (0): 0.00 dB 000001 (1): 0.51 dB 000010 (2): 1.02 dB 000011 (3): 1.53 dB 000100 (4): 2.04 dB 000101 (5): 2.55 dB 000110 (6): 3.05 dB 000111 (7): 3.56 dB 001000 (8): 4.07 dB 001001 (9): 4.58 dB 001010 (10): 5.09 dB 001011 (11): 5.59 dB 001100 (12): 6.10 dB 001101 (13): 6.61 dB 001110 (14): 7.12 dB 001111 (15): 7.63 dB 010000 (16): 8.13 dB 010001 (17): 8.64 dB 010010 (18): 9.15 dB 010011 (19): 9.66 dB 010100 (20): 10.17 dB 010101 (21): 10.67 dB	0x0	R/W

REGISTER DETAILS

Table 37. Bit Descriptions for SIG_PATHA_0 (Continued)

Bits	Bit Name	Description	Reset	Access
		010110 (22): 11.18 dB 010111 (23): 11.69 dB 011000 (24): 12.20 dB 011001 (25): 12.71 dB 011010 (26): 13.21 dB 011011 (27): 13.72 dB 011100 (28): 14.23 dB 011101 (29): 14.74 dB 011110 (30): 15.25 dB 011111 (31): 15.75 dB		

Address: 0x10B, Reset: 0x00, Name: SIG_PATHB_0

Table 38. Bit Descriptions for SIG_PATHB_0

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	DSA2_MAN_ATTEN	DSA2 Attenuator Manual Setting 000000 (0): 0.00 dB 000001 (1): 0.51 dB 000010 (2): 1.02 dB 000011 (3): 1.53 dB 000100 (4): 2.04 dB 000101 (5): 2.55 dB 000110 (6): 3.05 dB 000111 (7): 3.56 dB 001000 (8): 4.07 dB 001001 (9): 4.58 dB 001010 (10): 5.09 dB 001011 (11): 5.59 dB 001100 (12): 6.10 dB 001101 (13): 6.61 dB 001110 (14): 7.12 dB 001111 (15): 7.63 dB 010000 (16): 8.13 dB 010001 (17): 8.64 dB 010010 (18): 9.15 dB 010011 (19): 9.66 dB 010100 (20): 10.17 dB 010101 (21): 10.67 dB 010110 (22): 11.18 dB 010111 (23): 11.69 dB 011000 (24): 12.20 dB 011001 (25): 12.71 dB 011010 (26): 13.21 dB 011011 (27): 13.72 dB 011100 (28): 14.23 dB 011101 (29): 14.74 dB 011110 (30): 15.25 dB 011111 (31): 15.75 dB	0x0	R/W

Address: 0x110, Reset: 0x00, Name: AMPS_IP3_ATTSEL

REGISTER DETAILS

Table 39. Bit Descriptions for AMPS_IP3_ATTSEL

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
6	AMP2_IP3_OFF_3	Turn Off AMP2 IP3 Currents ATTSEL11	0x0	R/W
5	AMP2_IP3_OFF_2	Turn Off AMP2 IP3 Currents ATTSEL10	0x0	R/W
4	AMP2_IP3_OFF_1	Turn Off AMP2 IP3 Currents ATTSEL01	0x0	R/W
3	RESERVED	Reserved	0x0	R
2	AMP1_IP3_OFF_3	Turn Off AMP1 IP3 Currents ATTSEL11	0x0	R/W
1	AMP1_IP3_OFF_2	Turn Off AMP1 IP3 Currents ATTSEL10	0x0	R/W
0	AMP1_IP3_OFF_1	Turn Off AMP1 IP3 Currents ATTSEL01	0x0	R/W

Address: 0x111, Reset: 0x55, Name: TRM_AMPS_IREF_1

Table 40. Bit Descriptions for TRM_AMPS_IREF_1

Bits	Bit Name	Description	Reset	Access
[7:4]	TRM_AMP2_IREF_1	Amp 2 IREF Trim ATTSEL01	0x5	R/W
[3:0]	TRM_AMP1_IREF_1	Amp 1 IREF Trim ATTSEL01	0x5	R/W

Address: 0x112, Reset: 0x55, Name: TRM_AMPS_IREF_2

Table 41. Bit Descriptions for TRM_AMPS_IREF_2

Bits	Bit Name	Description	Reset	Access
[7:4]	TRM_AMP2_IREF_2	Amp 2 IREF Trim ATTSEL10	0x5	R/W
[3:0]	TRM_AMP1_IREF_2	Amp 1 IREF Trim ATTSEL10	0x5	R/W

Address: 0x113, Reset: 0x55, Name: TRM_AMPS_IREF_3

Table 42. Bit Descriptions for TRM_AMPS_IREF_3

Bits	Bit Name	Description	Reset	Access
[7:4]	TRM_AMP2_IREF_3	Amp 2 IREF Trim ATTSEL11	0x5	R/W
[3:0]	TRM_AMP1_IREF_3	Amp 1 IREF Trim ATTSEL11	0x5	R/W

Address: 0x114, Reset: 0x18, Name: DSA_ATTSEL_1

Table 43. Bit Descriptions for DSA_ATTSEL_1

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved	0x0	R
[5:0]	DSA_ATTEN_1	DSA Attenuator Setting ATTSEL01 When TXENP = 1 DSA2 000000 (0): 0.00 dB 000001 (1): 0.51 dB 000010 (2): 1.02 dB 000011 (3): 1.53 dB 000100 (4): 2.04 dB 000101 (5): 2.55 dB 000110 (6): 3.05 dB 000111 (7): 3.56 dB 001000 (8): 4.07 dB 001001 (9): 4.58 dB 001010 (10): 5.09 dB 001011 (11): 5.59 dB 001100 (12): 6.10 dB 001101 (13): 6.61 dB 001110 (14): 7.12 dB 001111 (15): 7.63 dB	0x18	R/W

REGISTER DETAILS

Table 43. Bit Descriptions for DSA_ATTSEL_1 (Continued)

Bits	Bit Name	Description	Reset	Access
		010000 (16): 8.13 dB 010001 (17): 8.64 dB 010010 (18): 9.15 dB 010011 (19): 9.66 dB 010100 (20): 10.17 dB 010101 (21): 10.67 dB 010110 (22): 11.18 dB 010111 (23): 11.69 dB 011000 (24): 12.20 dB 011001 (25): 12.71 dB 011010 (26): 13.21 dB 011011 (27): 13.72 dB 011100 (28): 14.23 dB 011101 (29): 14.74 dB 011110 (30): 15.25 dB 011111 (31) and 100000 (32): 15.75 dB. Boundary state from DSA2 to DSA1 stage. DSA2 + DSA1 100001 (33): 16.26 dB 100010 (34): 16.77 dB 100011 (35): 17.28 dB 100100 (36): 17.79 dB 100101 (37): 18.30 dB 100110 (38): 18.80 dB 100111 (39): 19.31 dB 101000 (40): 19.82 dB 101001 (41): 20.33 dB 101010 (42): 20.84 dB 101011 (43): 21.34 dB 101100 (44): 21.85 dB 101101 (45): 22.36 dB 101110 (46): 22.87 dB 101111 (47): 23.38 dB 110000 (48): 23.88 dB 110001 (49): 24.39 dB 110010 (50): 24.90 dB 110011 (51): 25.41 dB 110100 (52): 25.92 dB 110101 (53): 26.42 dB 110110 (54): 26.93 dB 110111 (55): 27.44 dB 111000 (56): 27.95 dB 111001 (57): 28.46 dB 111010 (58): 28.96 dB 111011 (59): 29.47 dB 111100 (60): 29.9 8dB 111101 (61): 30.49 dB 111110 (62): 31.00 dB 111111 (63): 31.50 dB		

Address: 0x115, Reset: 0x30, Name: DSA_ATTSEL_2

REGISTER DETAILS

Table 44. Bit Descriptions for DSA_ATTSEL_2

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved	0x0	R
[5:0]	DSA_ATTEN_2	DSA Attenuator Setting ATTSEL10 When TXENP = 1 DSA2 000000 (0): 0.00 dB 000001 (1): 0.51 dB 000010 (2): 1.02 dB 000011 (3): 1.53 dB 000100 (4): 2.04 dB 000101 (5): 2.55 dB 000110 (6): 3.05 dB 000111 (7): 3.56 dB 001000 (8): 4.07 dB 001001 (9): 4.58 dB 001010 (10): 5.09 dB 001011 (11): 5.59 dB 001100 (12): 6.10 dB 001101 (13): 6.61 dB 001110 (14): 7.12 dB 001111 (15): 7.63 dB 010000 (16): 8.13 dB 010001 (17): 8.64 dB 010010 (18): 9.15 dB 010011 (19): 9.66 dB 010100 (20): 10.17 dB 010101 (21): 10.67 dB 010110 (22): 11.18 dB 010111 (23): 11.69 dB 011000 (24): 12.20 dB 011001 (25): 12.71 dB 011010 (26): 13.21 dB 011011 (27): 13.72 dB 011100 (28): 14.23 dB 011101 (29): 14.74 dB 011110 (30): 15.25 dB 011111 (31) and 100000 (32): 15.75 dB. Boundary state from DSA2 to DSA1 stage. DSA2 + DSA1 100001 (33): 16.26 dB 100010 (34): 16.77 dB 100011 (35): 17.28 dB 100100 (36): 17.79 dB 100101 (37): 18.30 dB 100110 (38): 18.80 dB 100111 (39): 19.31 dB 101000 (40): 19.82 dB 101001 (41): 20.33 dB 101010 (42): 20.84 dB 101011 (43): 21.34 dB 101100 (44): 21.85 dB 101101 (45): 22.36 dB 101110 (46): 22.87 dB 101111 (47): 23.38 dB	0x30	R/W

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Table 44. Bit Descriptions for DSA_ATTSEL_2 (Continued)

Bits	Bit Name	Description	Reset	Access
		110000 (48): 23.88 dB 110001 (49): 24.39 dB 110010 (50): 24.90 dB 110011 (51): 25.41 dB 110100 (52): 25.92 dB 110101 (53): 26.42 dB 110110 (54): 26.93 dB 110111 (55): 27.44 dB 111000 (56): 27.95 dB 111001 (57): 28.46 dB 111010 (58): 28.96 dB 111011 (59): 29.47 dB 111100 (60): 29.98 dB 111101 (61): 30.49 dB 111110 (62): 31.00 dB 111111 (63): 31.50 dB		

Address: 0x116, Reset: 0x3F, Name: DSA_ATTSEL_3

Table 45. Bit Descriptions for DSA_ATTSEL_3

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	DSA_ATTEN_3	DSA Attenuator Setting ATTSEL11 When TXENP = 1 DSA2 000000 (0): 0.00 dB 000001 (1): 0.51 dB 000010 (2): 1.02 dB 000011 (3): 1.53 dB 000100 (4): 2.04 dB 000101 (5): 2.55 dB 000110 (6): 3.05 dB 000111 (7): 3.56 dB 001000 (8): 4.07 dB 001001 (9): 4.58 dB 001010 (10): 5.09 dB 001011 (11): 5.59 dB 001100 (12): 6.10 dB 001101 (13): 6.61 dB 001110 (14): 7.12 dB 001111 (15): 7.63 dB 010000 (16): 8.13 dB 010001 (17): 8.64 dB 010010 (18): 9.15 dB 010011 (19): 9.66 dB 010100 (20): 10.17 dB 010101 (21): 10.67 dB 010110 (22): 11.18 dB 010111 (23): 11.69 dB 011000 (24): 12.20 dB 011001 (25): 12.71 dB 011010 (26): 13.21 dB 011011 (27): 13.72 dB	0x3F	R/W

REGISTER DETAILS

Table 45. Bit Descriptions for DSA_ATTSEL_3 (Continued)

Bits	Bit Name	Description	Reset	Access
		011100 (28): 14.23 dB 011101 (29): 14.74 dB 011110 (30): 15.25d B 011111 (31): and 100000 (32): 15.75 dB. Boundary state from DSA2 to DSA1 stage. DSA2 + DSA1 100001 (33): 16.26 dB 100010 (34): 16.77 dB 100011 (35): 17.28 dB 100100 (36): 17.79 dB 100101 (37): 18.30 dB 100110 (38): 18.80 dB 100111 (39): 19.31 dB 101000 (40): 19.82 dB 101001 (41): 20.33 dB 101010 (42): 20.84 dB 101011 (43): 21.34 dB 101100 (44): 21.85 dB 101101 (45): 22.36 dB 101110 (46): 22.87 dB 101111 (47): 23.38 dB 110000 (48): 23.88 dB 110001 (49): 24.39 dB 110010 (50): 24.90 dB 110011 (51): 25.41 dB 110100 (52): 25.92 dB 110101 (53): 26.4 2dB 110110 (54): 26.93 dB 110111 (55): 27.44 dB 111000 (56): 27.95 dB 111001 (57): 28.46 dB 111010 (58): 28.96 dB 111011 (59): 29.47 dB 111100 (60): 29.98 dB 111101 (61): 30.49 dB 111110 (62): 31.00 dB 111111 (63): 31.50 dB		

Address: 0x120, Reset: 0x00, Name: DIG_CTRL

Table 46. Bit Descriptions for DIG_CTRL

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved	0x0	R
0	SPI_1P8_3P3_CTRL	SPI Supply Control 0: 1.8 V Read back. 1: 3.3 V Read back.	0x0	R/W