Data Sheet

# ADL8111

## 10 MHz to 8 GHz Bypass Amplifier

## FEATURES

- Small signal gain of 12.5 dB typical from 10 MHz to 500 MHz
- Broad operation from 10 MHz to 8000 MHz
- OIP3 of 34 dBm typical from 10 MHz to 500 MHz
- Internal amplifier state, output P1dB of 17 dBm typical from 5000 MHz to 8000 MHz
- Noise figure of 2.8 dB typical from 10 MHz to 500 MHz
- Low insertion loss of 2 dB typical for the internal bypass switch state from 10 MHz to 500 MHz
- Wide operating temperature range of −40°C to +85°C
- RoHS compliant, 6 mm × 6 mm, 28-terminal LGA
- ESD rating of ±750 V (Class 1B)

## APPLICATIONS

- Military
- Test instrumentation
- Communications

## FUNCTIONAL BLOCK DIAGRAM

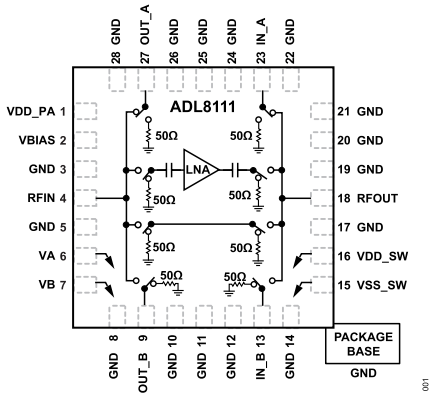


*Figure 1.*

## GENERAL DESCRIPTION

The ADL8111 is a low noise amplifier (LNA) with a nonreflective bypass switch that provides broadband operation from 10 MHz to 8000 MHz. The ADL8111 provides a low noise figure of 2.8 dB with a high output third-order intercept (OIP3) of 34 dBm simultaneously, which delivers a high dynamic range. The ADL8111 provides a gain of 12.5 dB that is stable over frequency, temperature, power supply, and from device to device.

The integration of an amplifier and two single-pole, quad-throw (SP4T) nonreflective switches allows multiple gain and linearity values. The addition of switches also offers high input intercept performance and prevents distortion on the high signal level applications.

The ADL8111 has a high electrostatic discharge (ESD) rating of ±750 V (Class 1B) and is fully specified for operation across a wide temperature range of −40°C to +85°C. The ADL8111 is offered in a 6 mm × 6 mm, 28-terminal land grid array (LGA) package.

## TABLE OF CONTENTS



## REVISION HISTORY

**11/2021—Rev. 0 to Rev. A**

Changes to Figure 1 ... 1
Added Figure 10; Renumbered Sequentially ... 6
Changes to Theory of Operation Section ... 20
Added Figure 84 ... 21
Changes to Applications Information Section ... 21
Changes to Figure 86 ... 23

**4/2019—Revision 0: Initial Version**

## SPECIFICATIONS

Drain bias voltage (VDD_PA) = +5 V, quiescent drain supply current ($I_{DQ\_PA}$) = 70 mA, negative bias voltage (VSS_SW) = −3.3 V, positive bias voltage (VDD_SW) = +3.3 V, and $T_A$ = 25°C, unless otherwise noted.

***Table 1.***

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| OVERALL FUNCTION | | | | | |
| Frequency Range | | 10 | | 5000 | MHz |
| INTERNAL AMPLIFIER STATE | | | | | |
| Small Signal Gain | | 11.2 | 12.5 | | dB |
| Gain Flatness | | | ±0.5 | | dB |
| Input Return Loss | | | 24 | | dB |
| Output Return Loss | | | 17 | | dB |
| Radio Frequency (RF) Settling Time | | | | | |
| | 50% VA/VB to 0.5 dB margin of final RFOUT | | 170 | | ns |
| | 50% VA/VB to 0.1 dB margin of final RFOUT | | 260 | | ns |
| Switching Speed | | | | | |
| Rise Time ($t_{RISE}$) and Fall Time ($t_{FALL}$) | 10% to 90% RFOUT | | 40 | | ns |
| Turn On Time ($t_{ON}$) and Turn Off Time ($t_{OFF}$) | 50% VA/VB to 90%/10% RF | | 160 | | ns |
| Output 1 dB Compression (P1dB) | | 17 | 19.5 | | dBm |
| Output Third-Order Intercept (OIP3) | | | 34 | | dBm |
| Noise Figure | | | 2.8 | | dB |
| VDD_PA | | 3.0 | 5.0 | 5.5 | V |
| INTERNAL BYPASS SWITCH STATE | | | | | |
| Insertion Loss | | | 2 | | dB |
| RF Settling Time | | | | | |
| | 50% VA/VB to 0.5 dB margin of final RFOUT | | 175 | | ns |
| | 50% VA/VB to 0.1 dB margin of final RFOUT | | 260 | | ns |
| Switching Speed | | | | | |
| $t_{RISE}/t_{FALL}$ | 10% to 90% RFOUT | | 60 | | ns |
| $t_{ON}/t_{OFF}$ | 50% VA/VB to 90%/10% RF | | 160 | | ns |
| Input Third-Order Intercept (IIP3) | | | 58 | | dBm |
| 0.5 dB Compression (P0.5dB) | | | 34 | | dBm |
| P1dB | | | 35 | | dBm |
| Return Loss On State | | | 18 | | dB |
| Return Loss Off State | | | 30 | | dB |
| VDD_SW | | 3.0 | 3.3 | 3.6 | V |
| VSS_SW | | −3.6 | −3.3 | −3.0 | V |
| EXTERNAL BYPASS A AND EXTERNAL BYPASS B STATES | | | | | |
| Insertion Loss | | | 1 | | dB |
| RF Settling Time | | | | | |
| | 50% VA/VB to 0.5 dB margin of final RFOUT | | 180 | | ns |
| | 50% VA/VB to 0.1 dB margin of final RFOUT | | 230 | | ns |
| Switching Speed | | | | | |
| $t_{RISE}/t_{FALL}$ | 10% to 90% RFOUT | | 70 | | ns |
| $t_{ON}/t_{OFF}$ | 50% VA/VB to 90%/10% RF | | 175 | | ns |
| IIP3 | | | 59 | | dBm |
| P0.5dB | | | 35.5 | | dBm |
| P1dB | | | 36 | | dBm |
| Return Loss On State | | | 22 | | dB |
| Return Loss Off State | | | 25 | | dB |
| VDD_SW | | 3.0 | 3.3 | 3.6 | V |

## SPECIFICATIONS

*Table 1.*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VSS_SW | | −3.6 | −3.3 | −3.0 | V |

VDD_PA = +5 V, $I_{DQ\_PA}$ = 70 mA, VSS_SW = −3.3 V, VDD_SW = +3.3 V, and $T_A$ = 25°C, unless otherwise noted.

*Table 2.*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| OVERALL FUNCTION | | | | | |
| Frequency Range | | 5000 | | 8000 | MHz |
| INTERNAL AMPLIFIER STATE | | | | | |
| Small Signal Gain | | 10.6 | 11.5 | | dB |
| Gain Flatness | | | ±1 | | dB |
| Input Return Loss | | | 14 | | dB |
| Output Return Loss | | | 16 | | dB |
| P1dB | | | 17 | | dBm |
| OIP3 | | | 32 | | dBm |
| Noise Figure | | | 4.5 | | dB |
| VDD_PA | | 3.0 | 5.0 | 5.5 | V |
| INTERNAL BYPASS SWITCH STATE | | | | | |
| Insertion Loss | | | 2.7 | | dB |
| IIP3[1] | | | 58 | | dBm |
| P0.5dB | | | 34 | | dBm |
| Return Loss On State | | | 18 | | dB |
| Return Loss Off State | | | 22 | | dB |
| VDD_SW | | 3.0 | 3.3 | 3.6 | V |
| VSS_SW | | −3.6 | −3.3 | −3.0 | V |
| EXTERNAL BYPASS A AND EXTERNAL BYPASS B STATES[2] | | | | | |
| Insertion Loss | | | 1.5 | | dB |
| IIP3 | | | 57.5 | | dBm |
| P0.5dB | | | 34.5 | | dBm |
| Return Loss On State | | | 17 | | dB |
| Return Loss Off State | | | 20 | | dB |
| VDD_SW | | 3.0 | 3.3 | 3.6 | V |
| VSS_SW | | −3.6 | −3.3 | −3.0 | V |

[1] IIP3 and compression data for the internal bypass and the External Bypass B states is the same as the External Bypass A state data.

[2] External Bypass A and External Bypass B were tested with an external 50 Ω transmission line on the evaluation board.

*Table 3. Total Supply Current by $V_{DD}$*

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Supply Current | | | | |
| VDD_PA = 5 V | | 70 | | mA |
| VDD_SW = +3.3 V | | 30 | | µA |
| VSS_SW = −3.3 V | | 30 | | µA |

*Table 4. Logic Control Voltage*

| Digital Control Inputs | Min | Typ | Max | Unit | Current |
|---|---|---|---|---|---|
| Low | 0 | | 0.8 | V | <1 µA typical |
| High | 1.4 | | VDD_SW + 0.3 | V | <1 µA typical |

## ABSOLUTE MAXIMUM RATINGS

*Table 5.*

| Parameter | Rating |
|---|---|
| VDD_PA | +7 V dc |
| VDD_SW Range | −0.3 V to +3.7 V |
| VSS_SW Range | −3.7 V to +0.3 V |
| Control Voltage (VA, VB) Range | −0.3 V to VDD + 0.3 V |
| RF Input Power (RFIN) − Internal Amplifier State | 20 dBm |
| RFIN − Internal Bypass, External Bypass A, External Bypass B | 31 dBm |
| RFIN (IN_A, OUT_A, IN_B, and OUT_B) Termination Path (VDD_SW, VA, VB = 3.3 V, VSS = −3.3 V, $T_A$ = 85°C, and Frequency = 2 GHz) | 28 dBm |
| Hot Switch Power Level (IN_A, OUT_A, IN_B, and OUT_B), VDD_SW = 3.3 V, TA = 85°C, and Frequency = 2 GHz | 30 dBm |
| Hot Switch Power Level (Internal Amplifier State) | 20 dBm |
| Continuous Power Dissipation, $P_{DISS}$ ($T_A$ = 85°C, Derate 6.8 mW/°C Above 85°C) | 0.61 W |
| Channel Temperature | 175°C |
| Maximum Peak Reflow Temperature (Moisture Sensitivity Level 3, MSL3)[1] | 260°C |
| Storage Temperature Range | −40°C to +125°C |
| Operating Temperature Range | −40°C to +85°C |
| ESD Sensitivity (Human Body Model) | Class 1B (Passed ±750 V) |

[1] See the Ordering Guide section for additional information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to the printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JC}$ is the junction to case thermal resistance.

*Table 6. Thermal Resistance*

| Package Type | $\theta_{JC}$ | Unit |
|---|---|---|
| CC-28-3[1] | 148 | °C/W |

[1] $\theta_{JC}$ was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the ground paddle to the PCB, and the ground paddle is held constant at an 85°C operating temperature.

## POWER DERATING CURVES

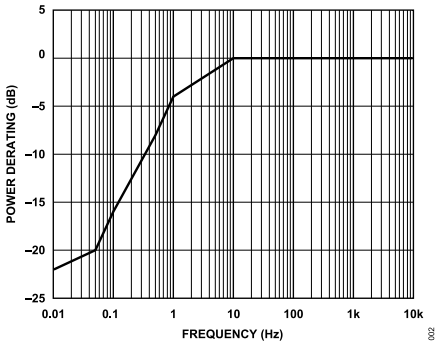


*Figure 2. Power Derating for RFIN Port*

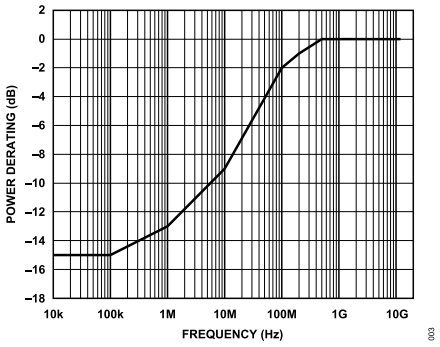


*Figure 3. Power Derating for Terminated Path*

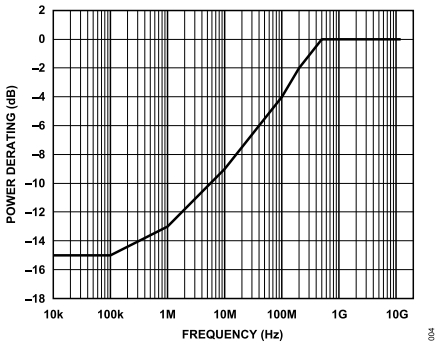


*Figure 4. Power Derating for Hot Switching Power*

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

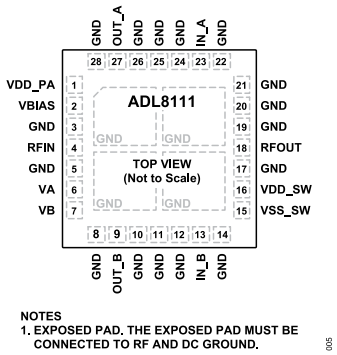


*Figure 5. Pin Configuration—Top View Not to Scale*

*Table 7. Pin Function Descriptions*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | VDD_PA | Drain Bias Voltage. See Table 2. |
| 2 | VBIAS | Current Mirror Bias Resistor Pin. Use this pin to set the current to the internal resistor by the external resistor. See Figure 9 for the interface schematic. |
| 3, 5, 8, 10 to 12, 14, 17, 19 to 22, 24 to 26, 28 | GND | RF and DC Ground. See Figure 6 for the interface schematic. |
| 4 | RFIN | RF Input. These pins are dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. |
| 6, 7 | VA, VB | Control Input. See Table 2, Table 4, and Table 5. See Figure 8 and Figure 7 for the interface schematics. |
| 9, 13 | OUT_B, IN_B | These pins are dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. |
| 15 | VSS_SW | Negative Bias Voltage. See Table 2. |
| 16 | VDD_SW | Positive Bias Voltage. See Table 2. |
| 18 | RFOUT | RF Output. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. |
| 23, 27 | IN_A, OUT_A | These pins are dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. |
| | EPAD | Exposed Pad. The exposed pad must be connected to RF and dc ground. |

## INTERFACE SCHEMATICS


*Figure 6. GND Interface Schematic*

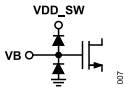


*Figure 7. VB Interface Schematic*

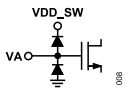


*Figure 8. VA Interface Schematic*

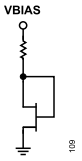


*Figure 9. VBIAS Interface Schematic*

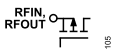


*Figure 10. RFIN and RFOUT Interface Schematic*

## TYPICAL PERFORMANCE CHARACTERISTICS

### EXTERNAL BYPASS A STATE

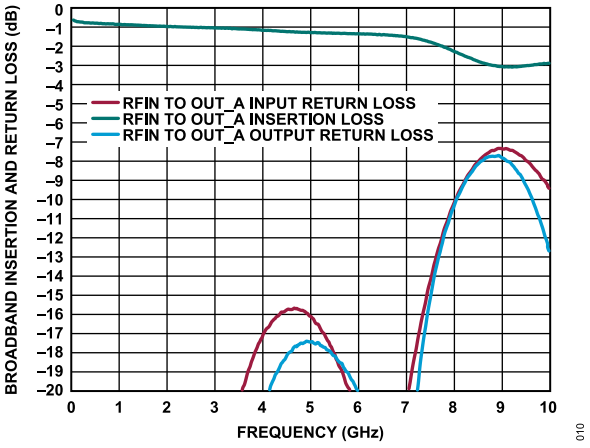


*Figure 11. Broadband Insertion and Return Loss vs. Frequency, State = External Bypass A, Path = RFIN to OUT_A (Refer to Figure 76 for the Test Circuit)*

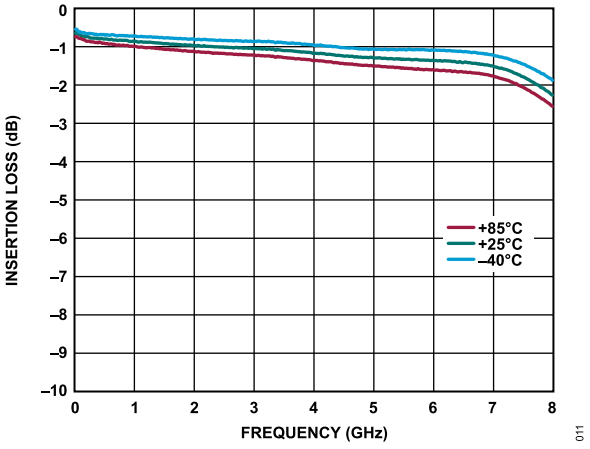


*Figure 12. Insertion Loss Over Temperature vs. Frequency, State = External Bypass A, Path = RFIN to OUT_A (Refer to Figure 76 for the Test Circuit)*

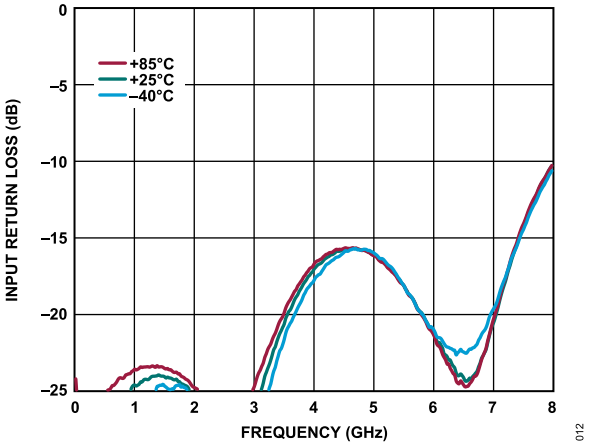


*Figure 13. Input Return Loss Over Temperature vs. Frequency, State = External Bypass A, Path = RFIN to OUT_A (Refer to Figure 76 for the Test Circuit)*

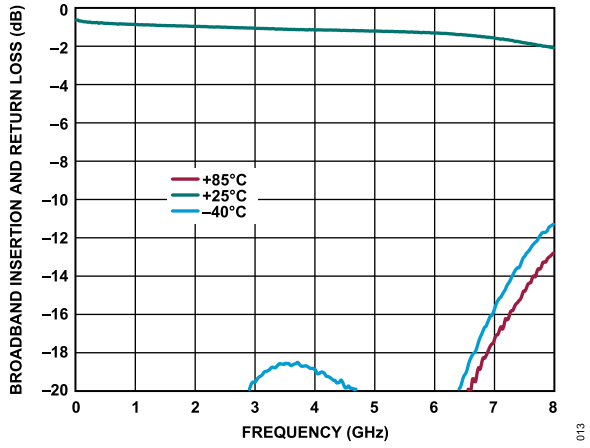


*Figure 14. Broadband Insertion and Return Loss vs. Frequency, State = External Bypass A, Path = IN_A to RFOUT (Refer to Figure 76 for the Test Circuit)*

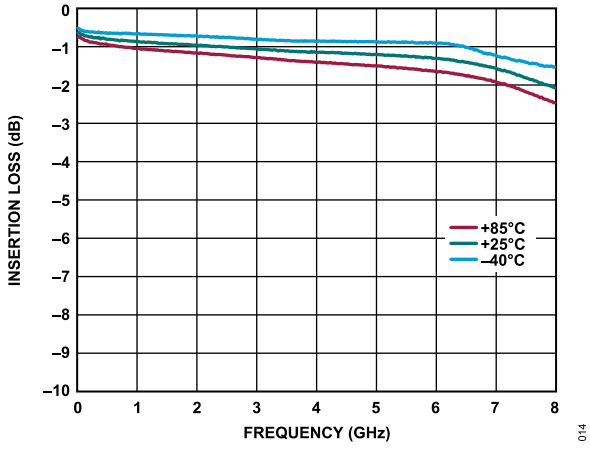


*Figure 15. Insertion Loss Over Temperature vs. Frequency, State = External Bypass A, Path = IN_A to RFOUT (Refer to Figure 76 for the Test Circuit)*

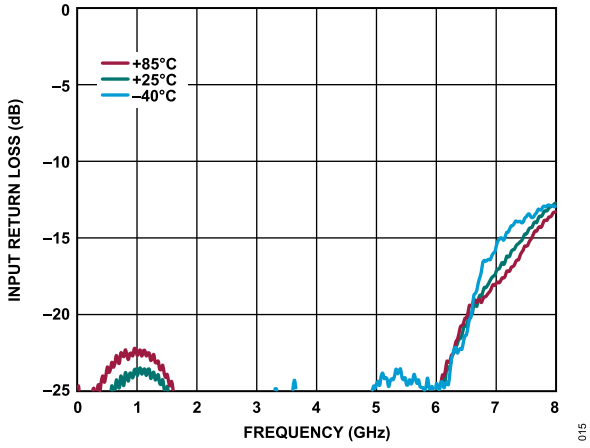


*Figure 16. Input Return Loss Over Temperature vs. Frequency, State = External Bypass A, Path = IN_A to RFOUT (Refer to Figure 76 for the Test Circuit)*

## TYPICAL PERFORMANCE CHARACTERISTICS

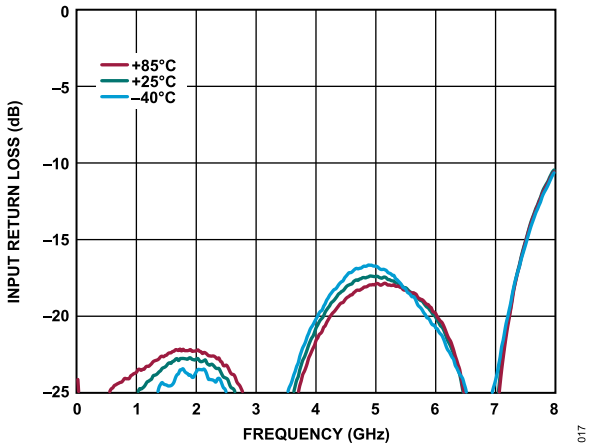


*Figure 17. Input Return Loss Over Temperature vs. Frequency, State = External Bypass A, Path = RFIN to OUT_A (Refer to Figure 76 for the Test Circuit)*

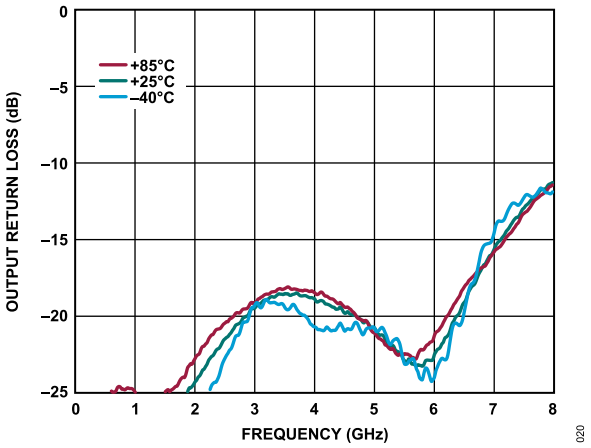


*Figure 20. Output Return Loss Over Temperature vs. Frequency, State = External Bypass A, Path = IN_A to RFOUT (Refer to Figure 76 for the Test Circuit)*

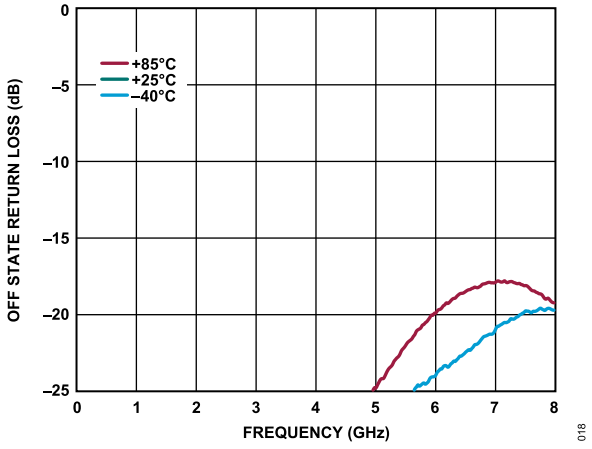


*Figure 18. Off State Return Loss vs. Frequency Over Temperature, State = External Bypass A, Path = OUT_B (Refer to Figure 76 for the Test Circuit)*

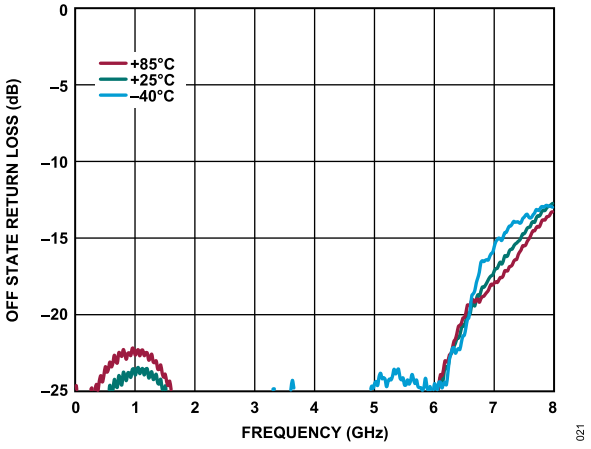


*Figure 21. Off State Return Loss vs. Frequency Over Temperature, State = External Bypass A, Path = IN_B (Refer to Figure 76 for the Test Circuit)*

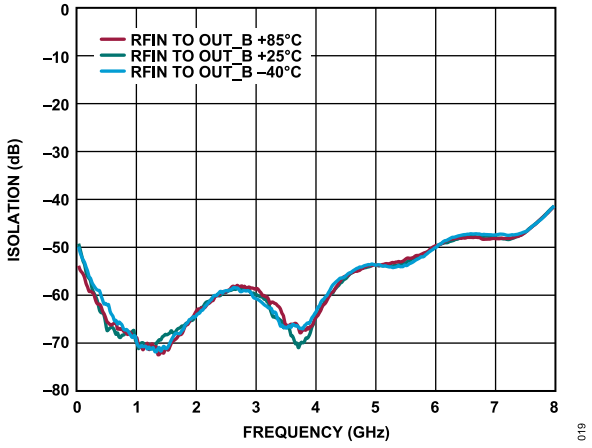


*Figure 19. Isolation vs. Frequency Over Temperature, State = External Bypass A (Refer to Figure 76 for the Test Circuit)*

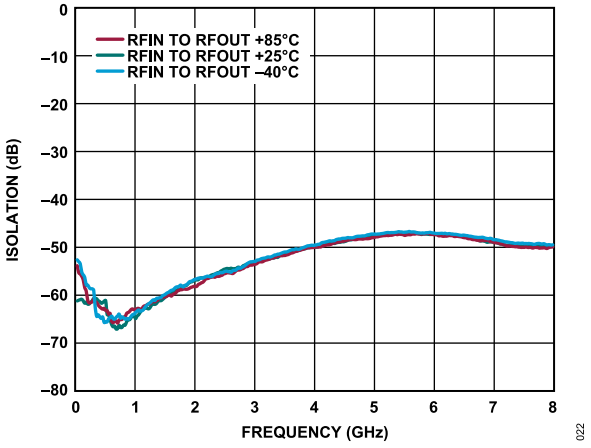


*Figure 22. Isolation vs. Frequency Over Temperature, State = External Bypass A (Refer to Figure 76 for the Test Circuit)*

## TYPICAL PERFORMANCE CHARACTERISTICS

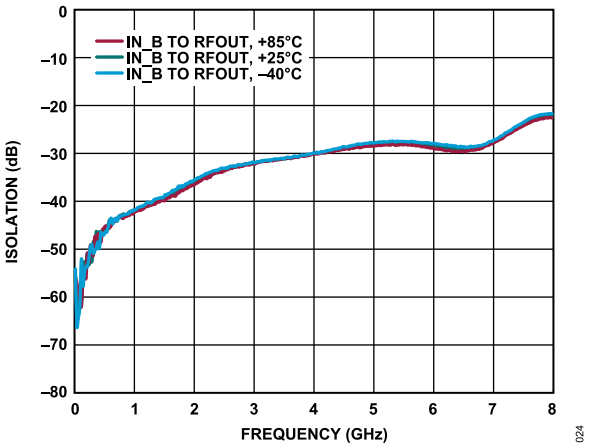


*Figure 23. Isolation vs. Frequency Over Temperature, State = External Bypass A (Refer to Figure 76 for the Test Circuit)*

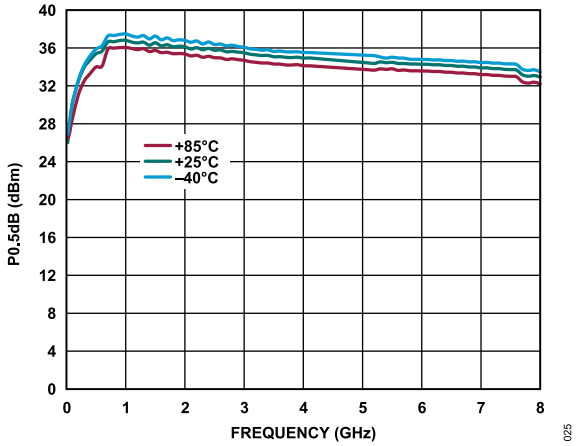


*Figure 24. P0.5dB vs. Frequency Over Temperature, State = External Bypass A, Path = RFIN to OUT_A or IN_A to RFOUT (Refer to Figure 76 for the Test Circuit)*

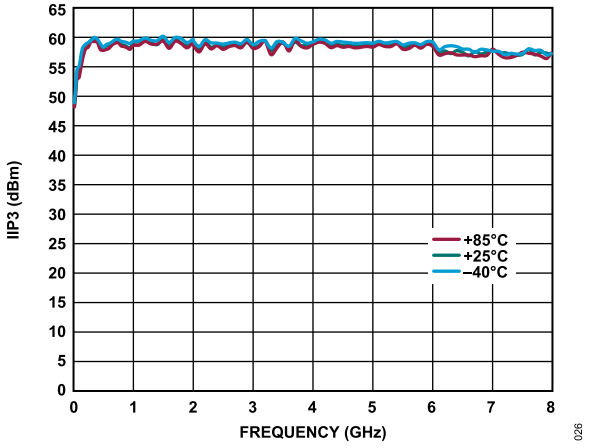


*Figure 25. IIP3 vs. Frequency Over Temperature, State = External Bypass A, Path = RFIN to OUT_A or IN_A to RFOUT (Refer to Figure 76 for the Test Circuit)*

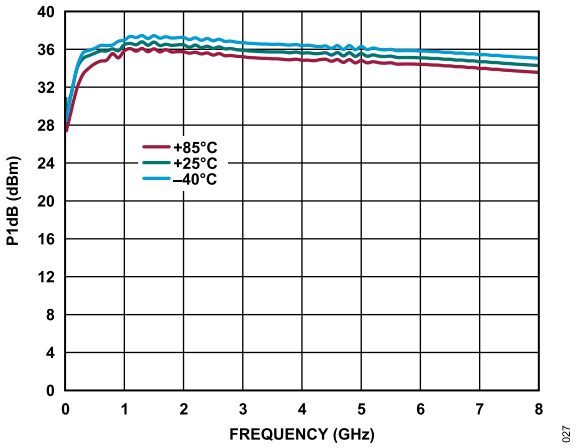


*Figure 26. P1dB Compression vs. Frequency Over Temperature, State = External Bypass A, Path = RFIN to OUT_A or IN_A to RFOUT (Refer to Figure 76 for the Test Circuit)*

## TYPICAL PERFORMANCE CHARACTERISTICS

### INTERNAL AMPLIFIER STATE

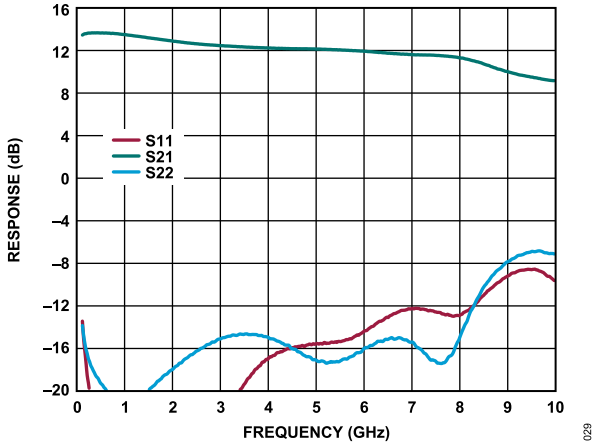


Figure 27. Broadband Gain and Return Loss vs. Frequency (100 MHz to 10 GHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)

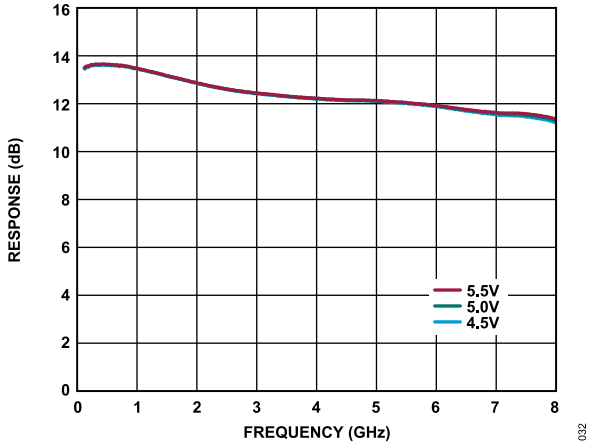


Figure 30. Gain vs Frequency Over VDD (100 MHz to 10 GHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)

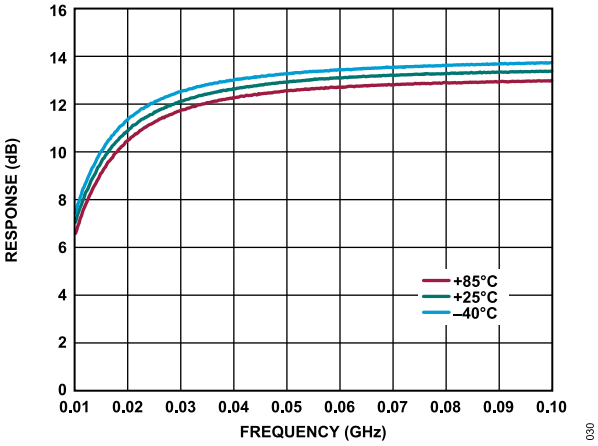


Figure 28. Gain Over Temperature vs. Frequency (10 MHz to 100 MHz) State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)

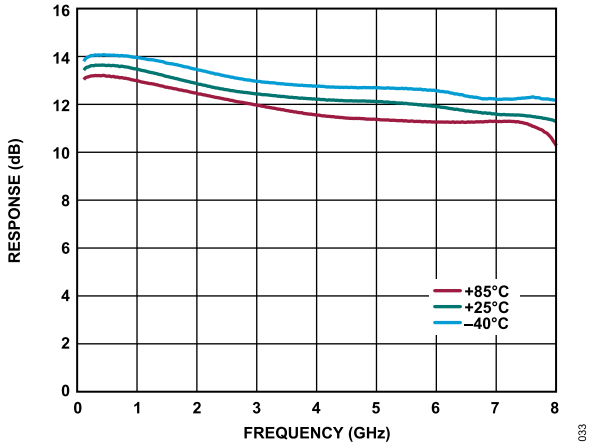


Figure 31. Gain vs. Frequency Over Temperature (100 MHz to 10 GHz) State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)

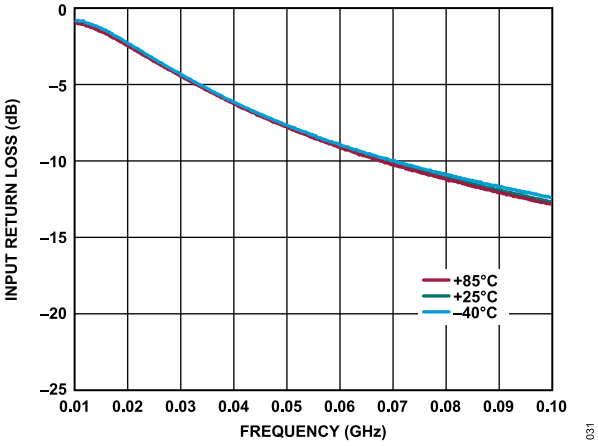


Figure 29. Input Return Loss vs. Frequency (10 MHz to 100 MHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)

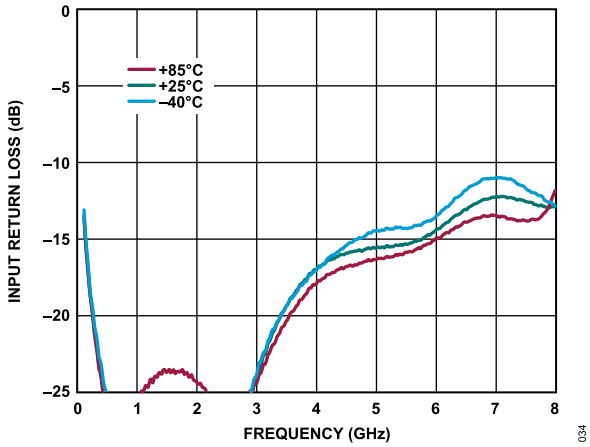


Figure 32. Input Return Loss vs. Frequency Over Temperature (100 MHz to 8 GHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)

## TYPICAL PERFORMANCE CHARACTERISTICS

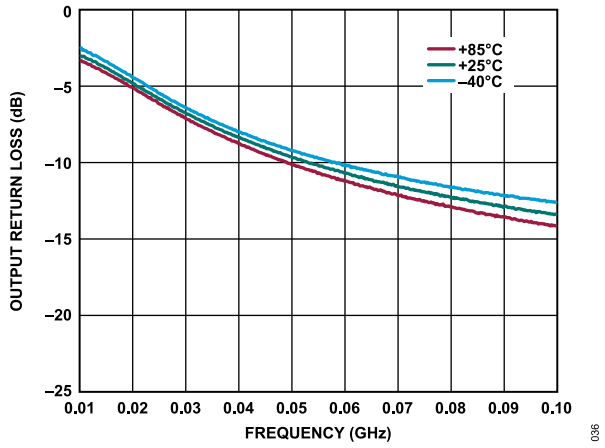


Figure 33. Output Return Loss vs. Frequency (10 MHz to 100 MHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)

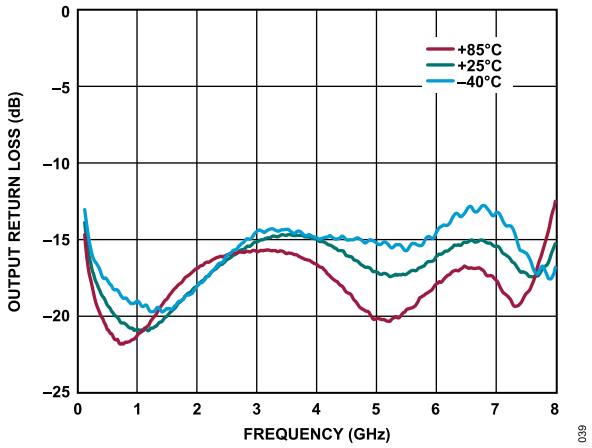


Figure 36. Output Return Loss vs. Frequency Over Temperature (100 MHz to 8 GHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)

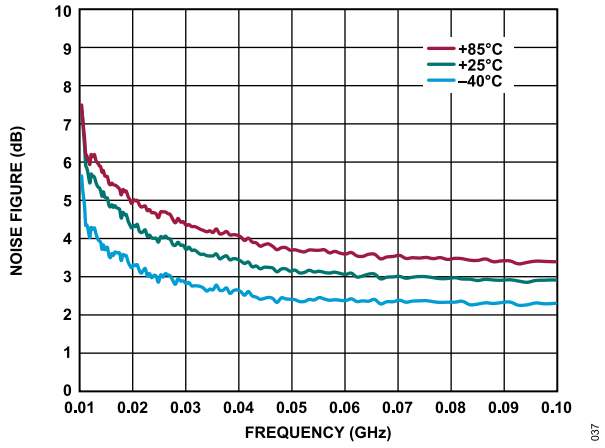


Figure 34. Noise Figure vs. Frequency Over Temperature (10 MHz to 100 MHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)

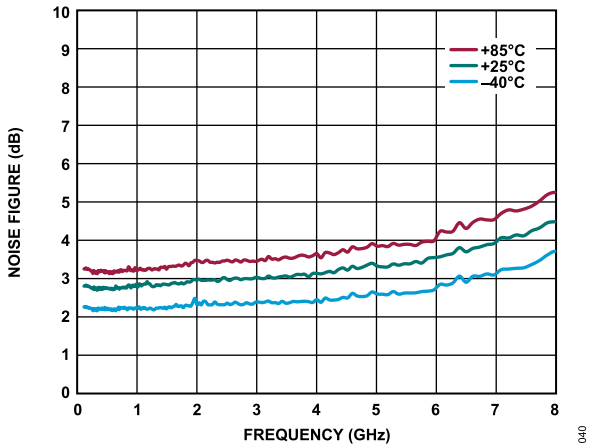


Figure 37. Noise Figure vs. Frequency Over Temperature (100 MHz to 8 GHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)

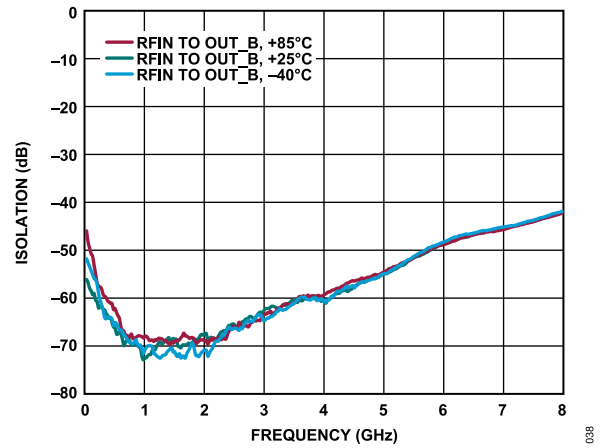


Figure 35. Isolation vs. Frequency Over Temperature, State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)

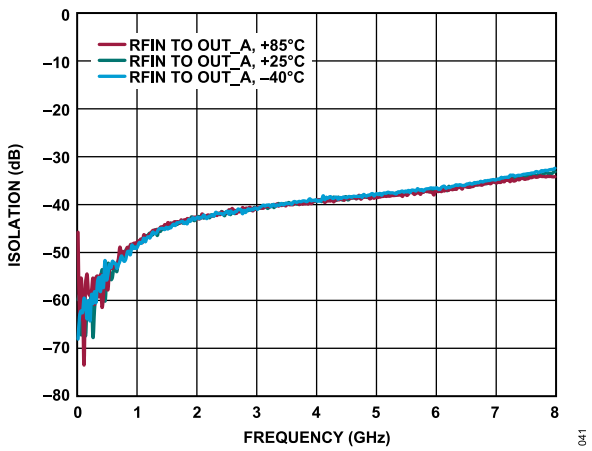


Figure 38. Isolation vs. Frequency Over Temperature (100 MHz to 8 GHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)

## TYPICAL PERFORMANCE CHARACTERISTICS

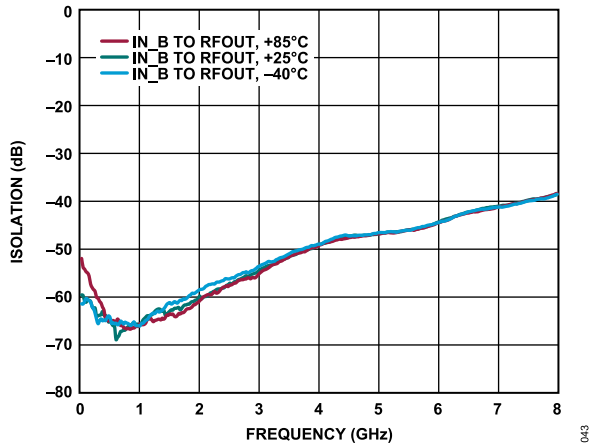


*Figure 39. Isolation vs. Frequency Over Temperature (100 MHz to 8 GHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)*

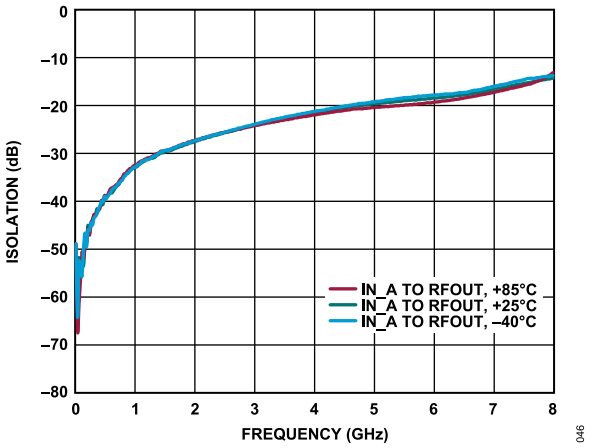


*Figure 42. Isolation vs. Frequency Over Temperature (100 MHz to 8 GHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)*

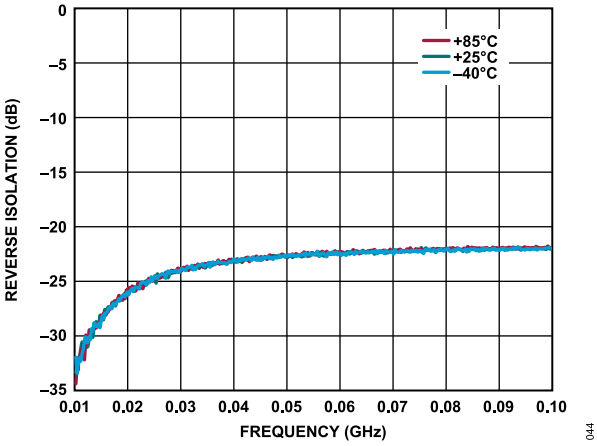


*Figure 40. Reverse Isolation vs. Frequency Over Temperature (100 MHz to 8 GHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)*

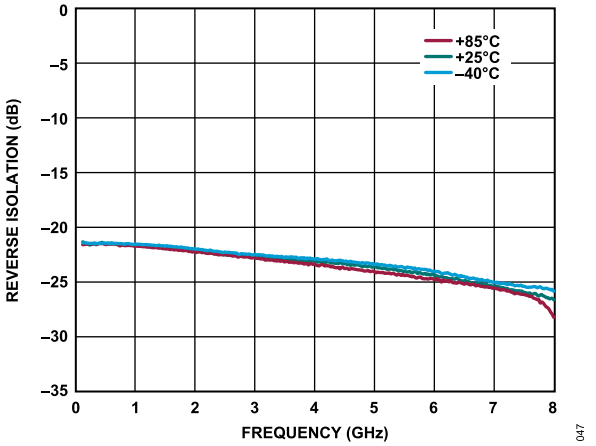


*Figure 43. Reverse Isolation vs. Frequency Over Temperature (100 MHz to 8 GHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)*

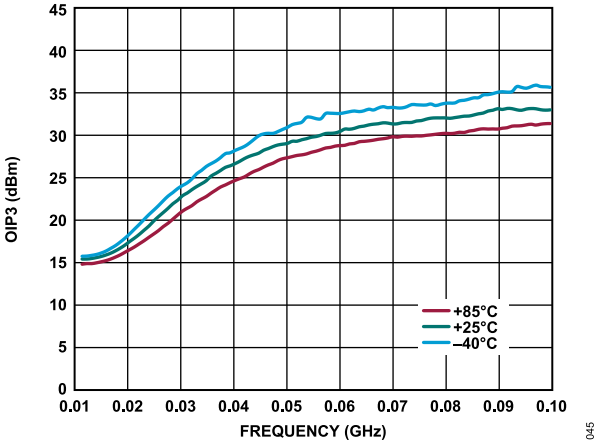


*Figure 41. OIP3 vs. Frequency Over Temperature (10 MHz to 100 MHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)*

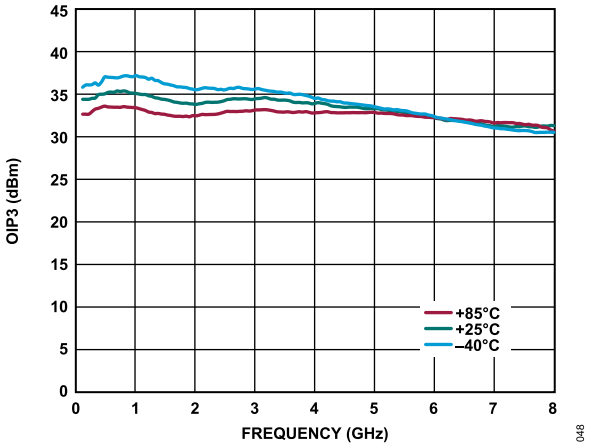


*Figure 44. OIP3 vs. Frequency Over Temperature (100 MHz to 8 GHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)*

## TYPICAL PERFORMANCE CHARACTERISTICS

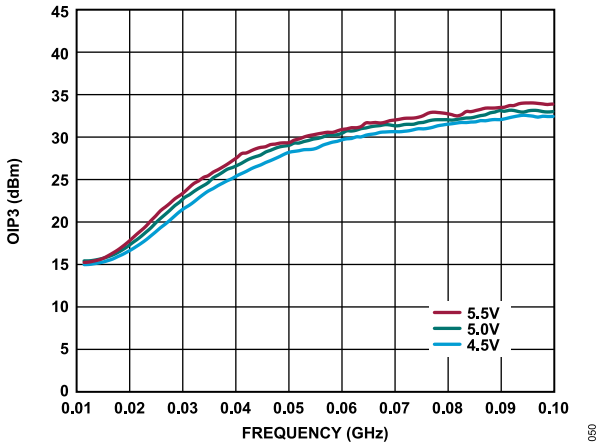


*Figure 45. OIP3 vs. Frequency Over VDD (10 MHz to 100 MHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)*

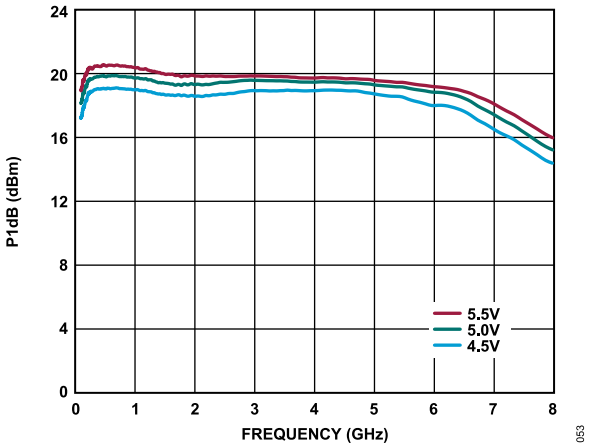


*Figure 48. P1dB vs. Frequency Over VDD (100 MHz to 8 GHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)*

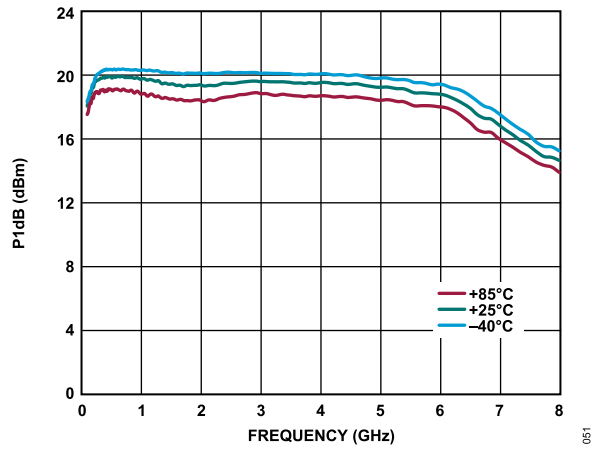


*Figure 46. P1dB vs. Frequency Over Temperature (100 MHz to 8 GHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)*

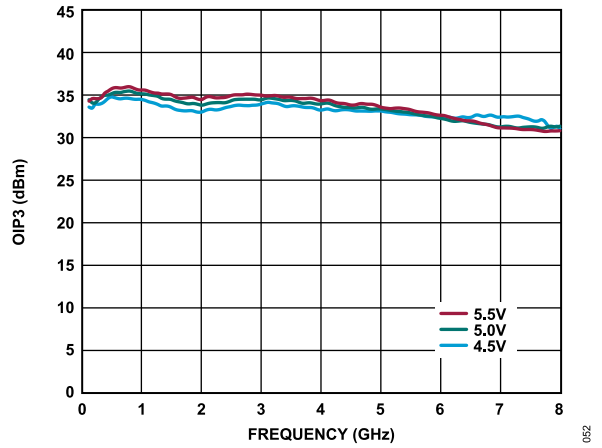


*Figure 47. OIP3 vs. Frequency Over VDD (100 MHz to 8 GHz), State = Internal Amplifier (Refer to Figure 77 for the Test Circuit)*

## TYPICAL PERFORMANCE CHARACTERISTICS

### INTERNAL BYPASS STATE

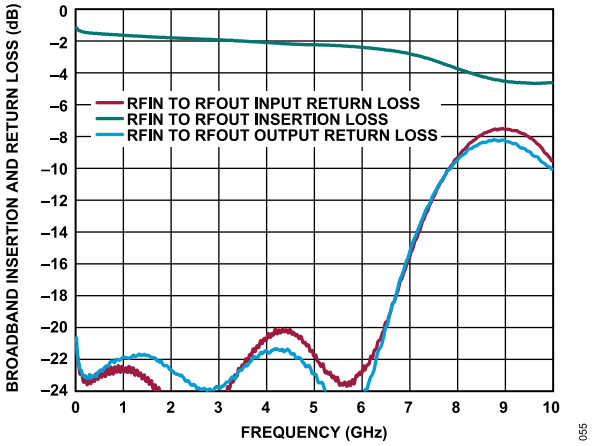


Figure 49. Broadband Insertion and Return Loss vs. Frequency, State = Internal Bypass (Refer to Figure 78 for the Test Circuit)

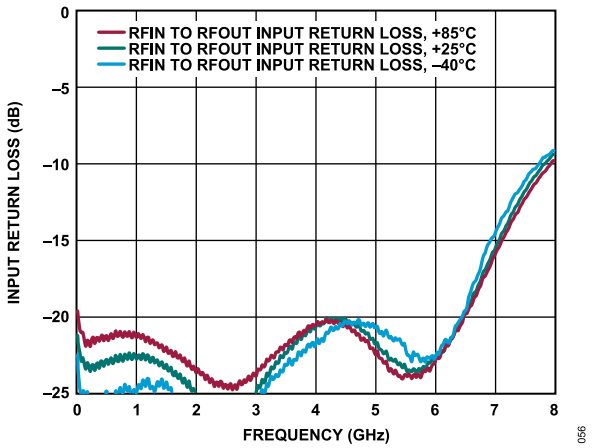


Figure 50. Input Return Loss Over Temperature vs. Frequency, State = Internal Bypass (Refer to Figure 78 for the Test Circuit)

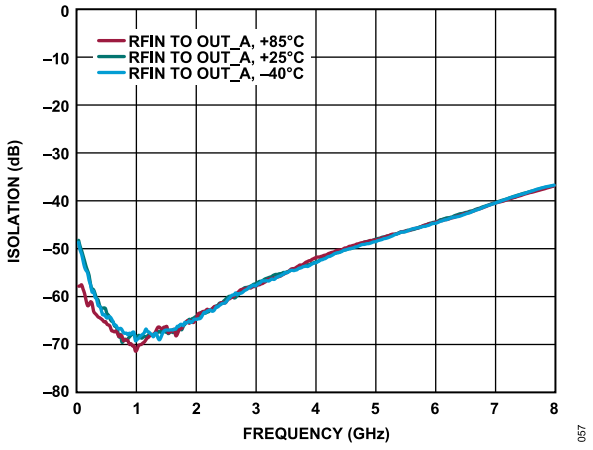


Figure 51. Isolation vs. Frequency Over Temperature, State = Internal Bypass (Refer to Figure 78 for the Test Circuit)

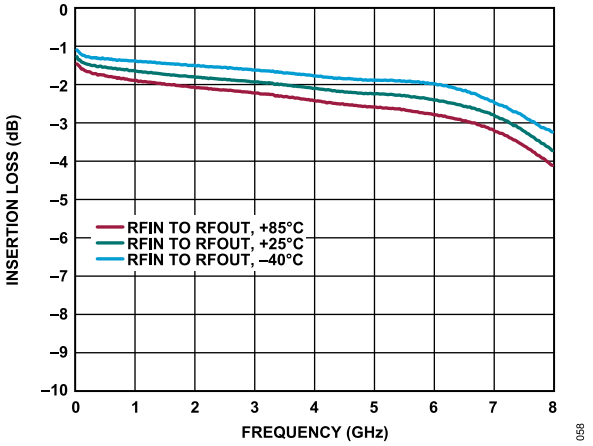


Figure 52. Insertion Loss Over Temperature vs. Frequency, State = Internal Bypass (Refer to Figure 78 for the Test Circuit)

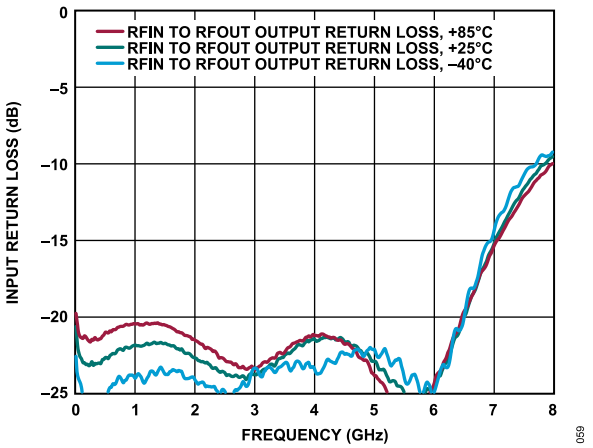


Figure 53. Output Return Loss Over Temperature vs. Frequency, State = Internal Bypass (Refer to Figure 78 for the Test Circuit)

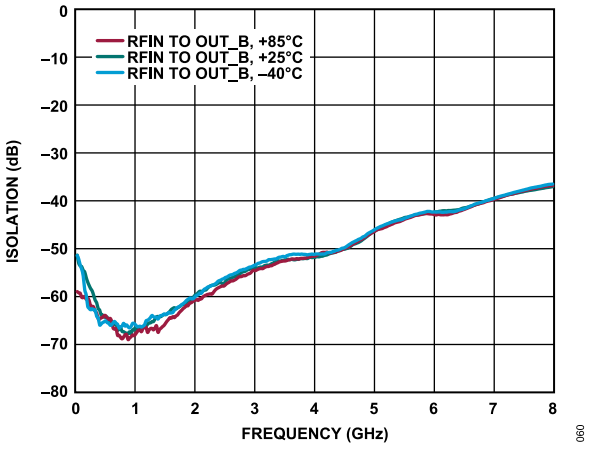


Figure 54. Isolation vs. Frequency Over Temperature, State = Internal Bypass (Refer to Figure 78 for the Test Circuit)

## TYPICAL PERFORMANCE CHARACTERISTICS

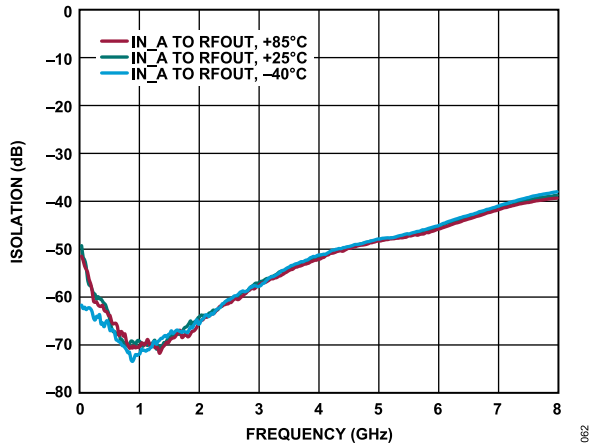


*Figure 55. Isolation vs. Frequency Over Temperature, State = Internal Bypass (Refer to Figure 78 for the Test Circuit)*

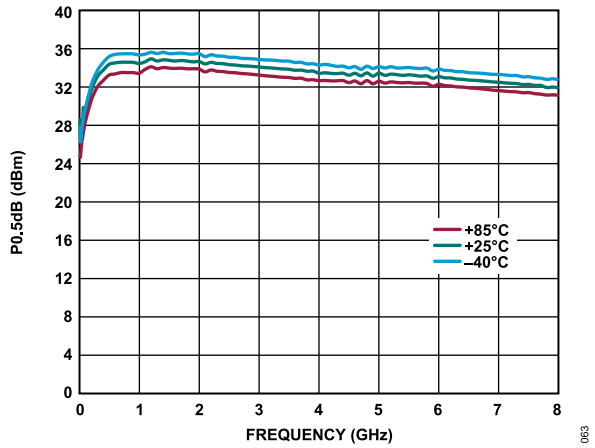


*Figure 56. P0.5dB vs. Frequency Over Temperature, State = Internal Bypass, Path = RFIN to RFOUT (Refer to Figure 78 for the Test Circuit)*

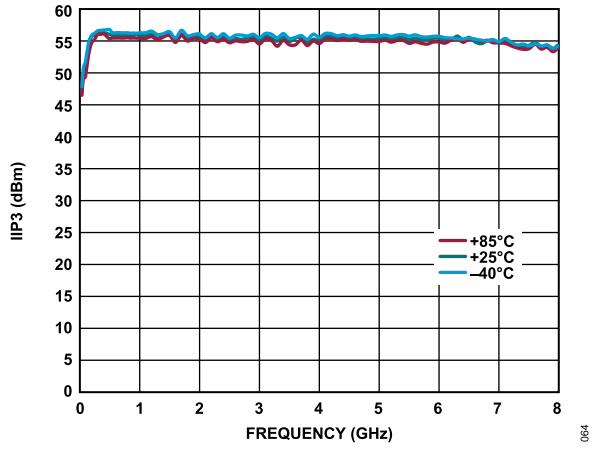


*Figure 57. IIP3 vs. Frequency Over Temperature, State = Internal Bypass, Path = RFIN to RFOUT (Refer to Figure 78 for the Test Circuit)*

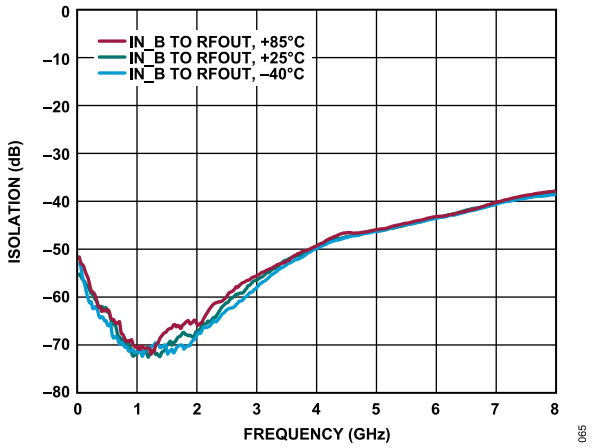


*Figure 58. Isolation vs. Frequency Over Temperature, State = Internal Bypass (Refer to Figure 78 for the Test Circuit)*

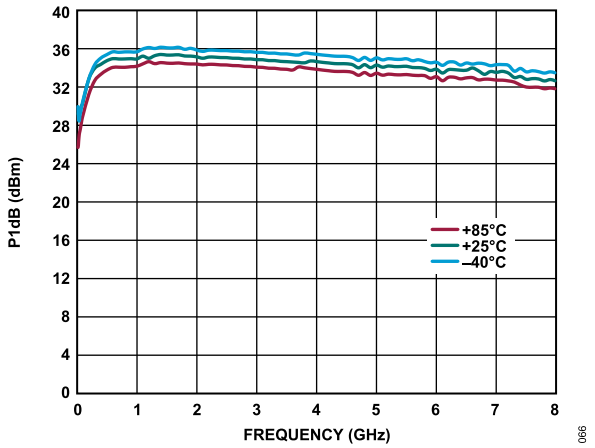


*Figure 59. P1dB vs. Frequency Over Temperature, State = Internal Bypass, Path = RFIN to RFOUT (Refer to Figure 78 for the Test Circuit)*

## TYPICAL PERFORMANCE CHARACTERISTICS

### EXTERNAL BYPASS B STATE

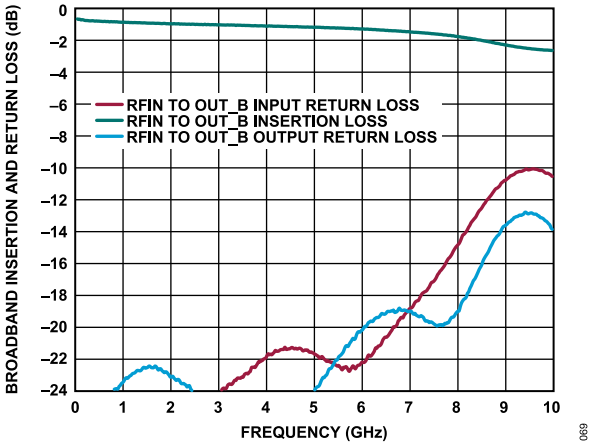


*Figure 60. Broadband Insertion and Return Loss vs. Frequency, State = External Bypass B, Path = RFIN to OUT_B (Refer to Figure 79 for the Test Circuit)*

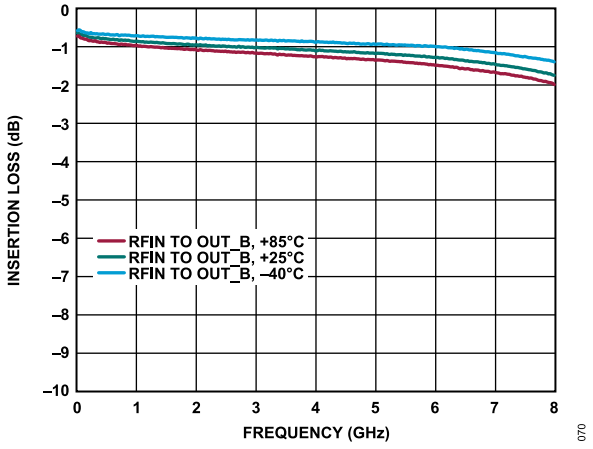


*Figure 61. Insertion Loss Over Temperature vs. Frequency, State = External Bypass B, Path = RFIN to OUT_B (Refer to Figure 79 for the Test Circuit)*

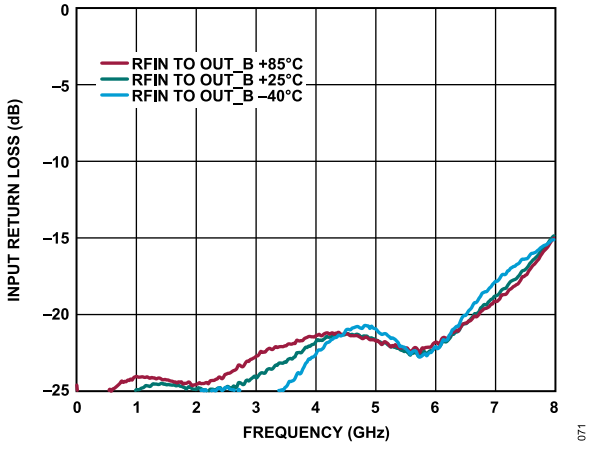


*Figure 62. Input Return Loss Over Temperature vs. Frequency, State = External Bypass B, Path = RFIN to OUT_B (Refer to Figure 79 for the Test Circuit)*

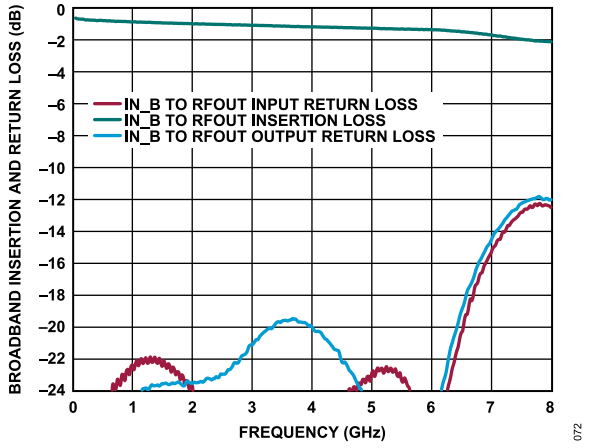


*Figure 63. Broadband Insertion and Return Loss vs. Frequency, State = External Bypass B, Path = IN_B to RFOUT (Refer to Figure 79 for the Test Circuit)*

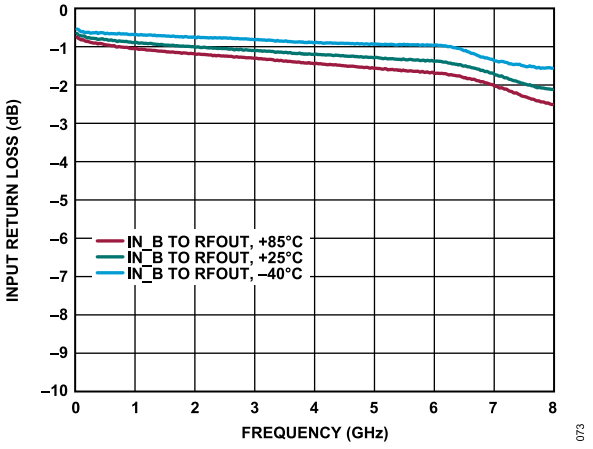


*Figure 64. Insertion Loss Over Temperature vs. Frequency, State = External Bypass B, Path = IN_B to RFOUT (Refer to Figure 79 for the Test Circuit)*

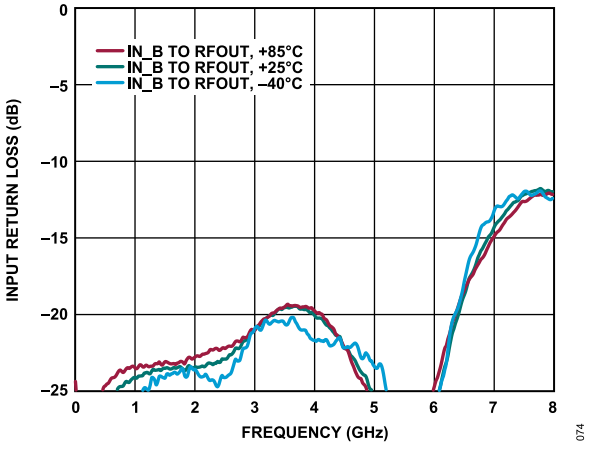


*Figure 65. Input Return Loss Over Temperature vs. Frequency, State = External Bypass B, Path = IN_B to RFOUT (Refer to Figure 79 for the Test Circuit)*

## TYPICAL PERFORMANCE CHARACTERISTICS

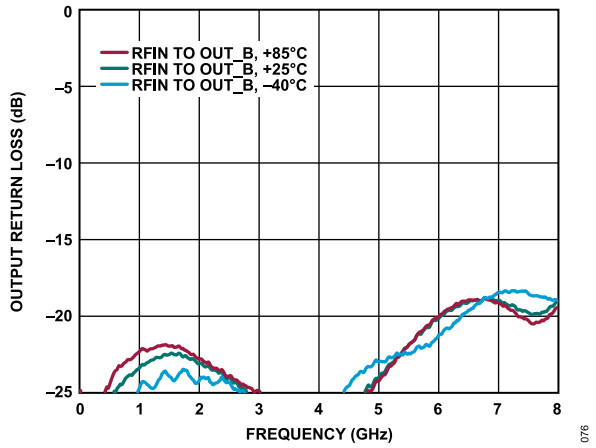


*Figure 66. Output Return Loss Over Temperature vs. Frequency, State = External Bypass B, Path = RFIN to OUT_B (Refer to Figure 79 for the Test Circuit)*

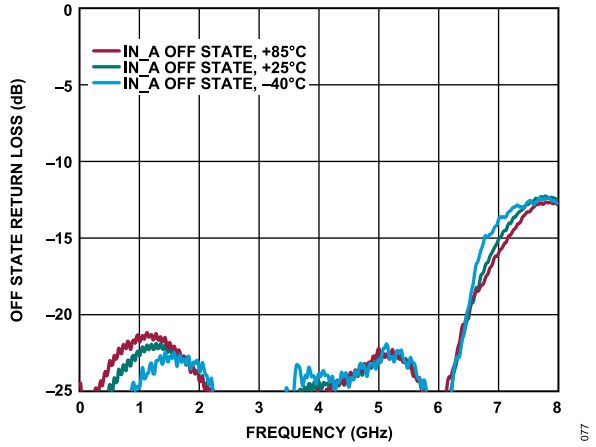


*Figure 67. Off State Return Loss vs. Frequency Over Temperature, State = External Bypass B, Path = IN_A (Refer to Figure 79 for the Test Circuit)*

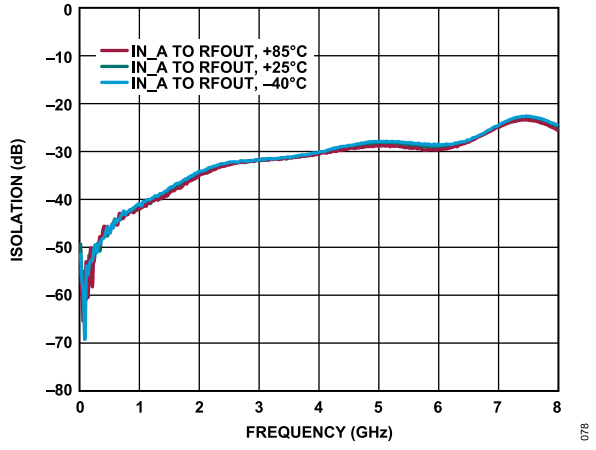


*Figure 68. Isolation vs. Frequency Over Temperature, State = External Bypass B (Refer to Figure 79 for the Test Circuit)*

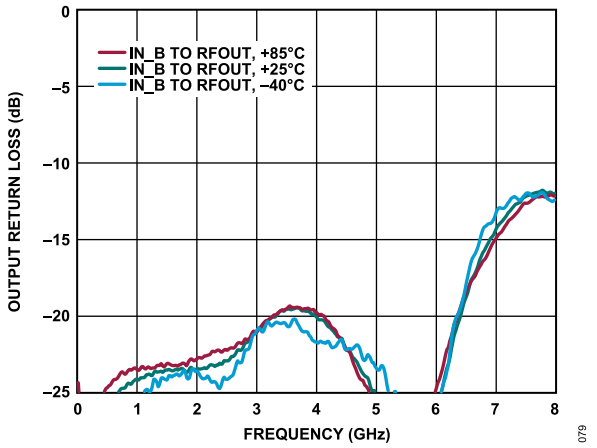


*Figure 69. Output Return Loss Over Temperature vs. Frequency, State = External Bypass B, Path = IN_B to RFOUT (Refer to Figure 79 for the Test Circuit)*

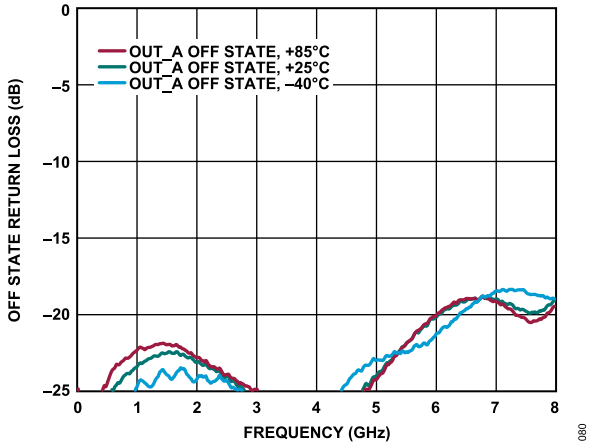


*Figure 70. Off State Return Loss vs. Frequency Over Temperature, State = External Bypass B, Path = OUT_A (Refer to Figure 79 for the Test Circuit)*

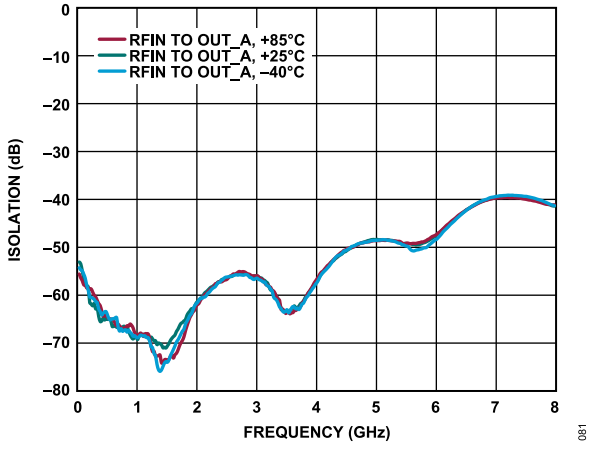


*Figure 71. Isolation vs. Frequency Over Temperature, State = External Bypass B (Refer to Figure 79 for the Test Circuit)*

## TYPICAL PERFORMANCE CHARACTERISTICS

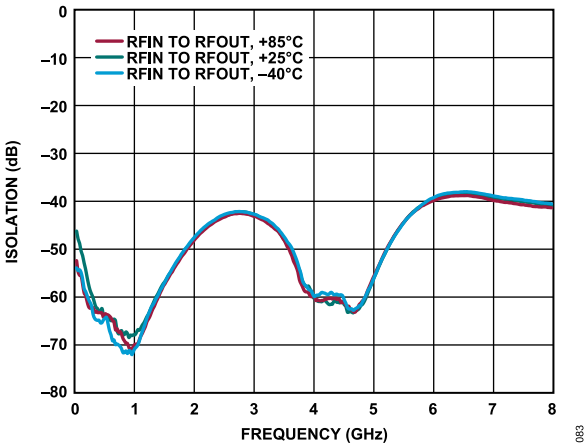


Figure 72. Isolation vs. Frequency Over Temperature, State = External Bypass B (Refer to Figure 79 for the Test Circuit)

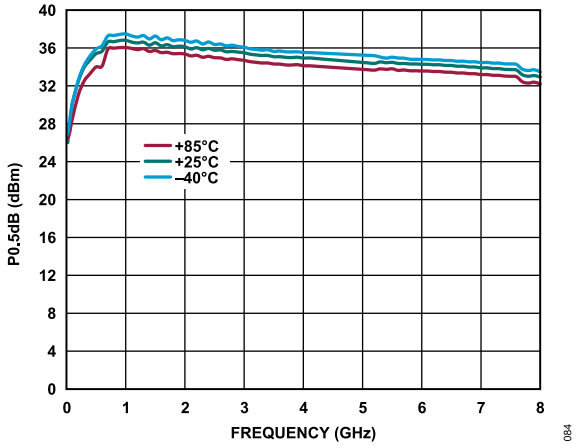


Figure 73. P0.5dB vs. Frequency Over Temperature, State = External Bypass B, Path = RFIN to OUT_B or IN_B to RFOUT (Refer to Figure 79 for the Test Circuit)

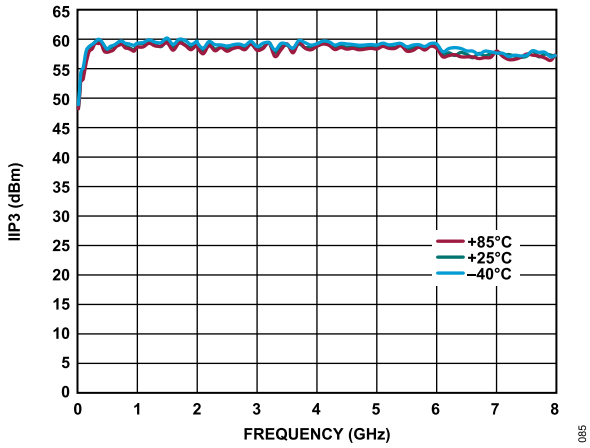


Figure 74. IIP3 vs. Frequency Over Temperature, State = External Bypass B, Path = RFIN to OUT_B or IN_B to RFOUT (Refer to Figure 79 for the Test Circuit)

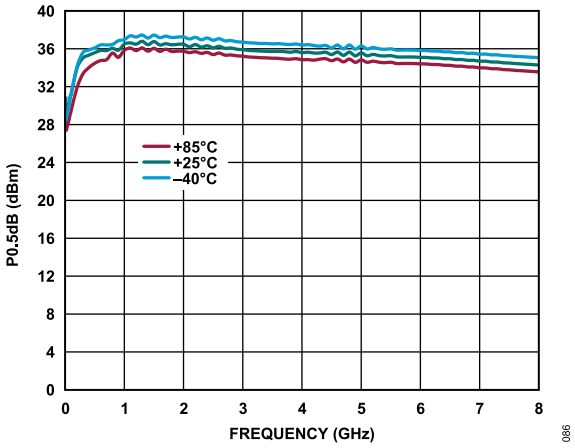


Figure 75. P0.5dB vs. Frequency Over Temperature, State = External Bypass B, Path = RFIN to OUT_B or IN_B to RFOUT (Refer to Figure 79 for the Test Circuit)

## TEST CIRCUITS

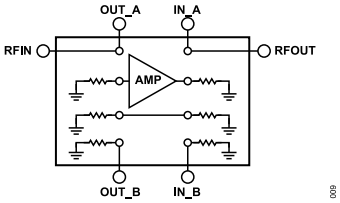


*Figure 76. External Bypass A State*

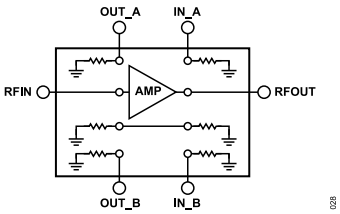


*Figure 77. Internal Amplifier State*

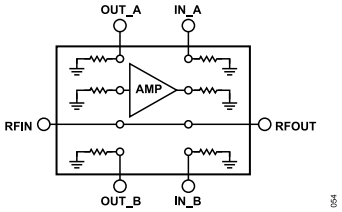


*Figure 78. Internal Bypass State*

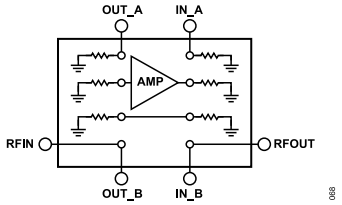


*Figure 79. External Bypass B State*

## THEORY OF OPERATION

The ADL8111 integrates an amplifier with two switching networks located at the RF input and output. The amplifier, which is internally ac-coupled on its input and output, uses a gallium arsenide (GaAs) LNA die from the HMC8411. The switching network employs robust silicon-on-insulator (SOI) technology for fast switching and a short settling time. This integrated solution has four different signal path states available: an internal amplifier, an internal bypass, External Bypass A, and External Bypass B. Signal path states are controlled through the digital pins, VA and VB, using 1.4 V high and 0 V low logic (see Figure 80 to Figure 83). The internal amplifier is biased up by applying 5 V to VDD_PA, and the internal switches are biased up by applying +3.3 V and −3.3 V to VDD_SW and VSS_SW, respectively. DC bias to the switches is independent of the LNA. Turning off bias to VDD_PA to the LNA provides better isolation between RF ports.

### SIGNAL PATH STATES FOR DIGITAL CONTROL INPUTS

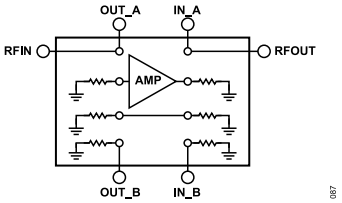


*Figure 80. External Bypass A, VA = 0 V and VB = 0 V*

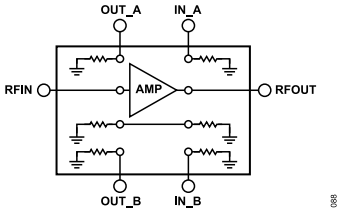


*Figure 81. Internal Amplifier, VA = 0 V and VB = 3.3 V*

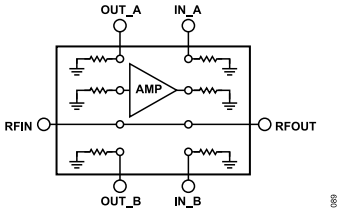


*Figure 82. Internal Bypass, VA = 3.3 V and VB = 0 V*

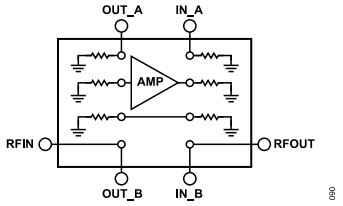


*Figure 83. External Bypass B, VA = 3.3 V and VB = 3.3 V*

*Table 8. Truth Table*

| | Digital Control Inputs | | |
|---|---|---|---|
| **State Name** | **VA** | **VB** | **Signal Path State** |
| External Bypass A | Low | Low | RFIN to OUT_A, IN_A to RFOUT |
| Internal Amplifier | Low | High | RFIN to RFOUT through amplifier path |
| Internal Bypass | High | Low | RFIN to RFOUT through bypass path |
| External Bypass B | High | High | RFIN to OUT_B, IN_B to RFOUT |

## APPLICATIONS INFORMATION

The basic connections for operating the ADL8111 are shown in Figure 86, which is also the schematic for the evaluation board. A 5 V dc bias is supplied to the amplifier on VDD_PA, +3.3 V dc bias supply to VDD_SW and −3.3 V dc bias supply to VSS_SW.

VA and VB are digital inputs set path states shown in Table 7. High logic state is set at 1.4 V and low logic state is set at 0 V.

The LNA within the ADL8111 operates in self-biased mode where the VBIAS pin is connected to a 560 Ω external resistor to achieve a 70 mA supply current. Refer to Table 9 for the recommended resistor values to achieve different $I_{DQ}$ currents.

Figure 84 shows the time domain response at RFOUT to switching voltages on VA and VB when RFIN is driven by a steady level of approximately 2.5 dBm at 200 MHz. Both of the External Bypass connections paths (External Bypass A, External Bypass B) are left open.

With VA and VB low and high respectively, the ADL8111 is in Internal Amplifier Mode and the observed output level is approximately $4V_{PP}$ or 16 dBm. With VA high and VB low, device switches to Internal Bypass Mode, and the output drops correspondingly. With VA and VB both low or both high, the device switches to either External Bypass A or External Bypass B. Since these two paths are left open in this case, no signal appears at the output for both cases.

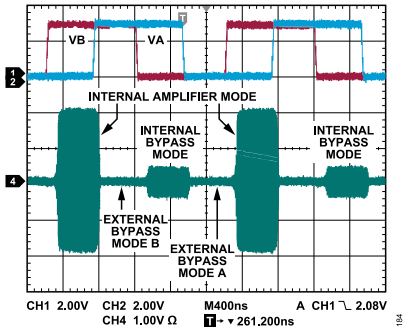


*Figure 84. Time Domain Response of RFOUT to Switching of VA and VB Voltages with a Continuous 2.5 dBm RF Input on RFIN*

## RECOMMENDED BIAS SEQUENCING

### During Power-Up

The recommended bias sequence during power-up follows:

1. Set VDD_SW = 3.3 V.
2. Set VSS_SW = −3.3 V.
3. Set VDD_PA = 5 V.
4. Apply the RF signal.

### During Power-Down

The recommended bias sequence during power-down follows:

1. Turn off the RF signal.
2. Set VDD_PA = 0 V.
3. Set VSS_SW = 0 V.
4. Set VDD_SW = 0 V.

The bias conditions, VDD_PA = 5 V at $I_{DQ}$ = 70 mA, is the recommended operating point to achieve optimum performance. The data used in this data sheet was taken with the recommended bias condition. Using the HMC8411 with different bias conditions can provide different performance than what is shown in the Typical Performance Characteristics section.

*Table 9. Recommended Bias Resistor Values at VDD_PA = 5 V*

| $R_{BIAS}$ (Ω) | $I_{DQ}$ (mA) |
|---|---|
| 226 | 85 |
| 560 | 70 |
| 1.1 k | 55 |

## EVALUATION PCB

The ADL8111-EVALZ is the evaluation board for the ADL8111 with fully populated components as shown in Figure 85 and its schematic shown in Figure 86. The board is fabricated with four layers using Rogers 4350. Signal lines have characteristic impedance of 50 Ω. Package ground leads and the exposed paddle are soldered to the ground plane. Adequate amounts of via holes connect the top and bottom ground planes. The evaluation board is available from Analog Devices, Inc., upon request. Gerber files can be found on the ADL8111 product webpage.

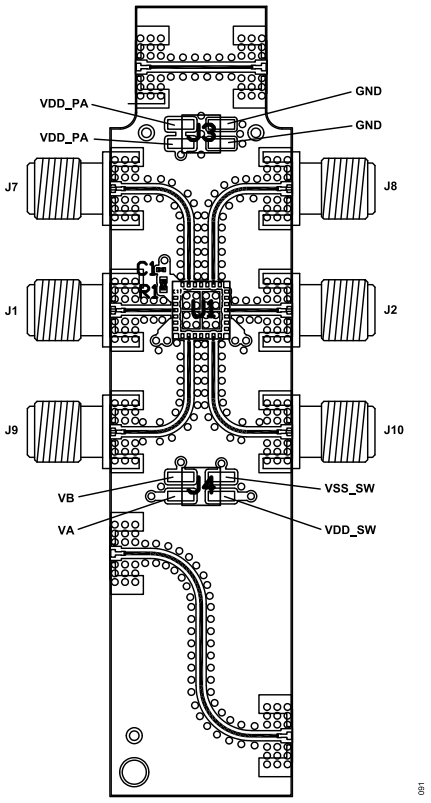


*Figure 85. ADL8111-EVALZ Evaluation Board PCB*

## EVALUATION PCB

### EVALUATION BOARD SCHEMATIC

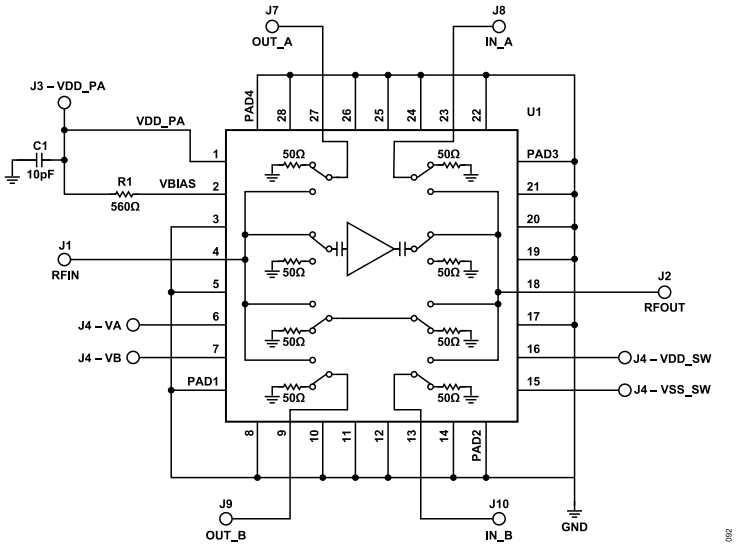


*Figure 86. ADL8111-EVALZ Evaluation Board Schematic*

*Table 10. Bill of Material for Evaluation PCB ADL8111-EVALZ*

| Item | Description |
|---|---|
| J1, J2, J7, J8, J9, J10 | SRI SMA RF connectors |
| J3, J4 | DC header pins |
| U1 | ADL8111 |
| C1 | 10 pF, 5% tolerance, 0201, ceramic capacitor |
| R1 | 560 Ω, 1/16 W, 0402, thick film resistor |