Data Sheet

ADL8142

GaAs, pHEMT, MMIC, Low Noise Amplifier, 23 GHz to 31 GHz

FEATURES

- Low noise figure: 1.6 dB typical at 27 GHz to 31 GHz
- Single positive supply (self biased)
- High gain: 27 dB typical at 27 GHz to 31 GHz
- High OIP3: 21.5 dBm typical at 27 GHz to 31 GHz
- RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP

APPLICATIONS

- Satellite communication
- Telecommunications
- Civilian radar

GENERAL DESCRIPTION

The ADL8142 is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT), low noise wideband amplifier that operates from 23 GHz to 31 GHz. The ADL8142 provides a typical gain of 27 dB, a 1.6 dB typical noise figure, and a typical output third-order intercept (OIP3) of 21.5 dBm at 27 GHz to 31 GHz, requiring only 25 mA from a 2 V supply voltage. Note that the OIP3 can be improved with larger drain currents. The ADL8142 also features inputs and outputs that are ac-coupled and internally matched to 50 Ω, making it ideal for high capacity microwave radio applications.

The ADL8142 is housed in a RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP.

FUNCTIONAL BLOCK DIAGRAM

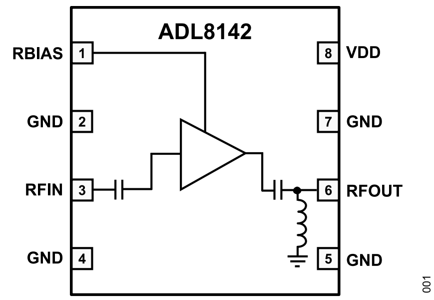

Figure 1.

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REVISION HISTORY

2/2023—Rev. A to Rev. B

Change to Gain Variation over Temperature Parameter, Table 1....3
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11/2022—Rev. 0 to Rev. A

Change to Features Section....1
Change to General Description Section....1
Change to IP3 Parameter, Table 2....3
Changes to Figure 67....19

4/2022—Revision 0: Initial Version

SPECIFICATIONS

23 GHZ TO 27 GHZ FREQUENCY RANGE

Supply voltage (V_{DD}) = 2 V, quiescent current (I_{DQ}) = 25 mA, bias resistance (R_{BIAS}) = 634 Ω, and T_C = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	23		27	GHz	
GAIN		29		dB	
Gain Variation over Temperature		0.026		dB/°C	
NOISE FIGURE		1.8		dB	
RETURN LOSS					
Input (S11)		10.5		dB	
Output (S22)		16		dB	
OUTPUT					
Power for 1 dB Compression (P1dB)		8.5		dBm	
Saturated Power (P_{SAT})		10		dBm	
IP3		17.5		dBm	Measurement taken at output power (P_{OUT}) per tone = −4 dBm
Second-Order Intercept (IP2)		25		dBm	Measurement taken at P_{OUT} per tone = −4 dBm
POWER ADDED EFFICIENCY (PAE)		18		%	Measured at P_{SAT}

27 GHZ TO 31 GHZ FREQUENCY RANGE

V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 634 Ω, and T_C = 25°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	27		31	GHz	
GAIN	24.5	27		dB	
Gain Variation over Temperature		0.019		dB/°C	
NOISE FIGURE		1.6		dB	
RETURN LOSS					
S11		13		dB	
S22		15		dB	
OUTPUT					
P1dB	7.5	10		dBm	
P_{SAT}		11		dBm	
IP3		21.5		dBm	Measurement taken at P_{OUT} per tone = −4 dBm
IP2		35		dBm	Measurement taken at P_{OUT} per tone = −4 dBm
PAE		21		%	Measured at P_{SAT}

DC SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit
SUPPLY CURRENT				
I_{DQ}		25		mA
Amplifier Current (I_{DQ_AMP})		23		mA
RBIAS Current (I_{RBIAS})		2		mA
SUPPLY VOLTAGE				
V_{DD}	1.5	2	3.5	V

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD}	4.5 V
RF Input Power (RFIN)	20 dBm
Pulsed RFIN (Duty Cycle = 10%, Pulse Width = 100 µs)	22 dBm
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C (Derate 5.99 mW/°C Above 85°C)	0.54 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−40°C to +85°C
Nominal Junction (T_A = 85°C, V_{DD} = 2 V, I_{DQ} = 25 mA, Input Power (P_{IN}) = Off)	93.4°C
Maximum Junction	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-8-30		
Quiescent, T_{BASE} = 25°C	134.3	°C/W
Worst Case[1], T_{BASE} = 85°C	167	°C/W

[1] Worst case across all specified operating conditions.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

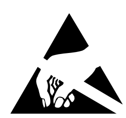
Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8142

Table 6. ADL8142, 8-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±250	1A

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

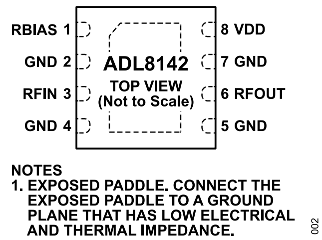


Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDD to set the I_{DQ}. See Figure 64 and Table 8 for more details. See Figure 3 for the interface schematic.
2, 4, 5, 7	GND	Ground. Connect the GND pins to a ground plane that has low electrical and thermal impedance. See Figure 6 for the interface schematic.
3	RFIN	RF Input. The RFIN pin is ac-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
6	RFOUT	RF Output. The RFOUT pin is ac-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.
8	VDD	Drain Bias. Connect the VDD pin to the supply voltage. See Figure 5 for the interface schematic.
	EXPOSED PADDLE	Exposed Paddle. Connect the exposed paddle to a ground plane that has low electrical and thermal impedance.

INTERFACE SCHEMATICS

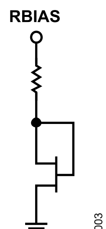


Figure 3. RBIAS Interface Schematic

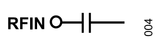


Figure 4. RFIN Interface Schematic

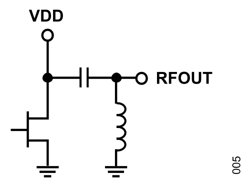


Figure 5. RFOUT/VDD Interface Schematic

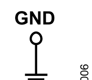


Figure 6. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

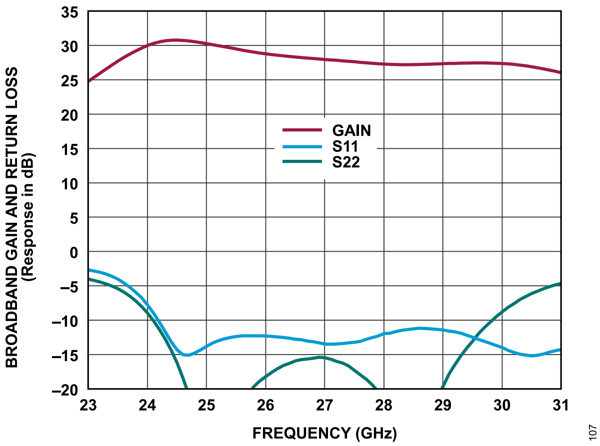


Figure 7. Broadband Gain and Return Loss vs. Frequency, V_{DD} = 2 V, I_{DQ} = 25 mA

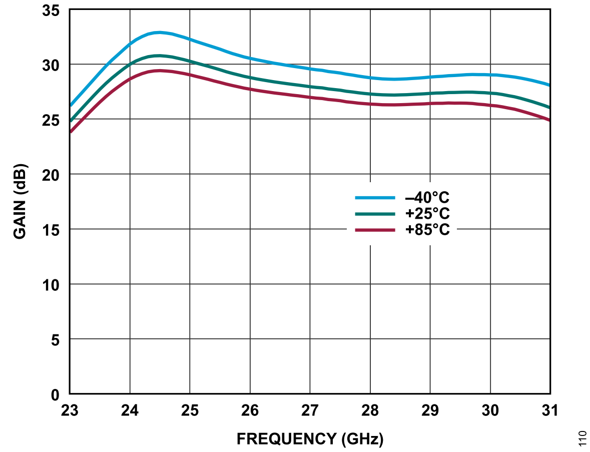


Figure 10. Gain vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 634 Ω

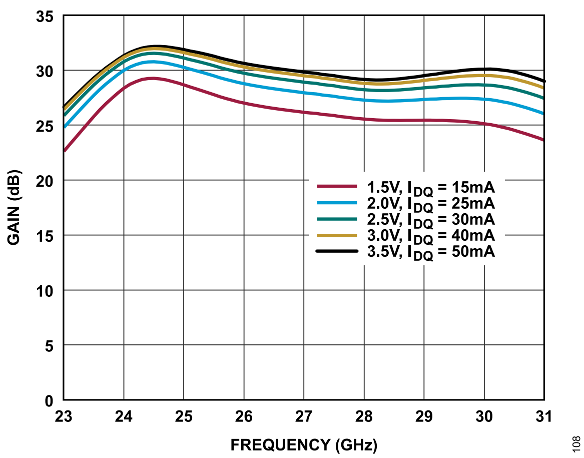


Figure 8. Gain vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 634 Ω

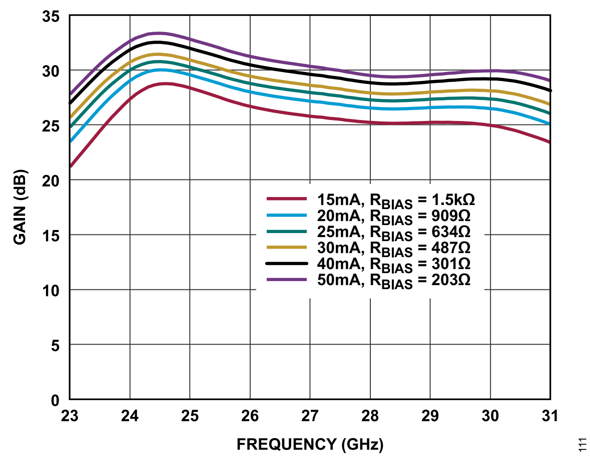


Figure 11. Gain vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

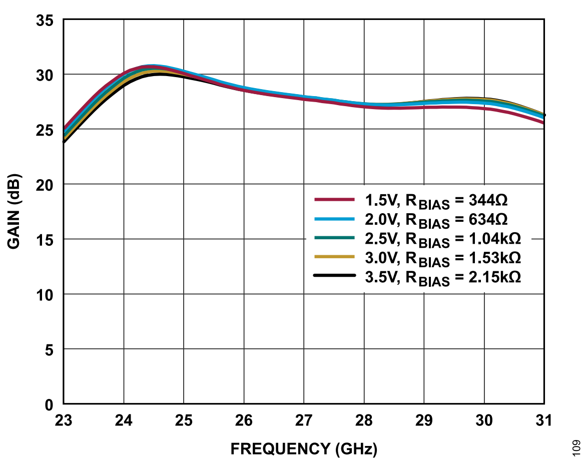


Figure 9. Gain vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

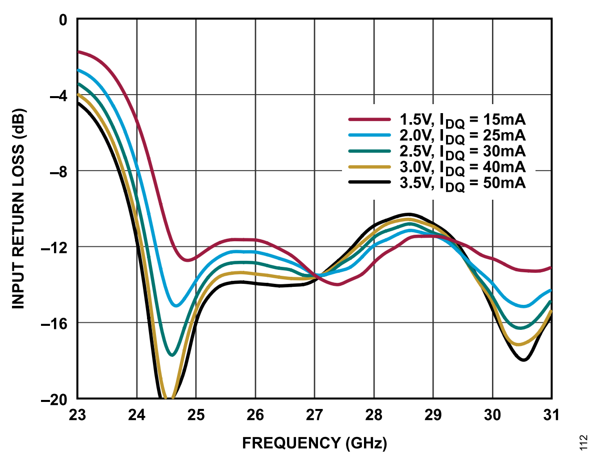


Figure 12. Input Return Loss vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 634 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

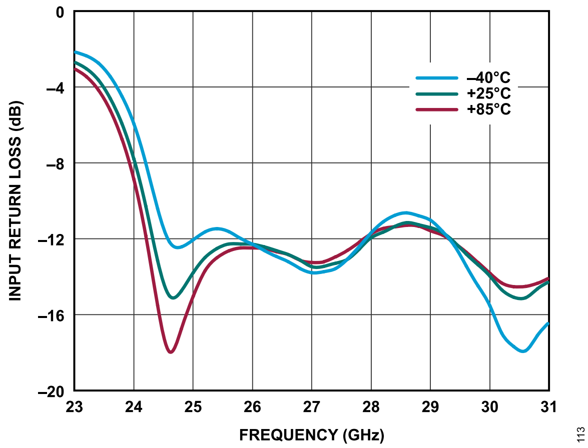


Figure 13. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 634 Ω

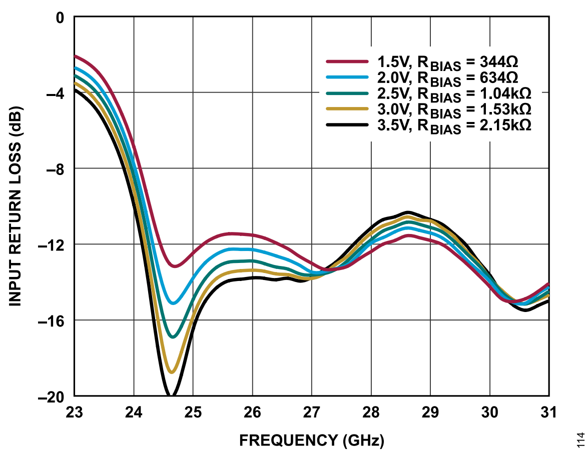


Figure 14. Input Return Loss vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

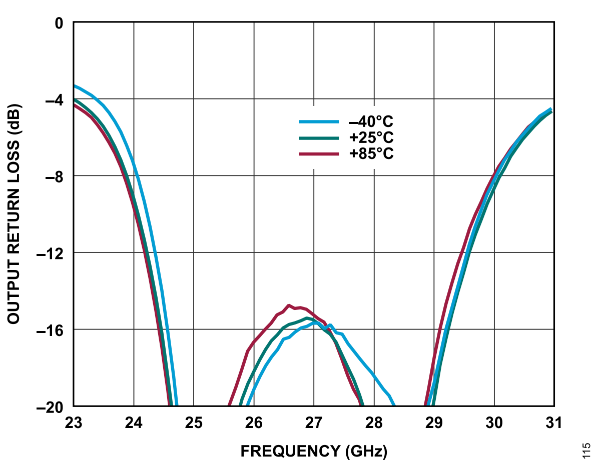


Figure 15. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 634 Ω

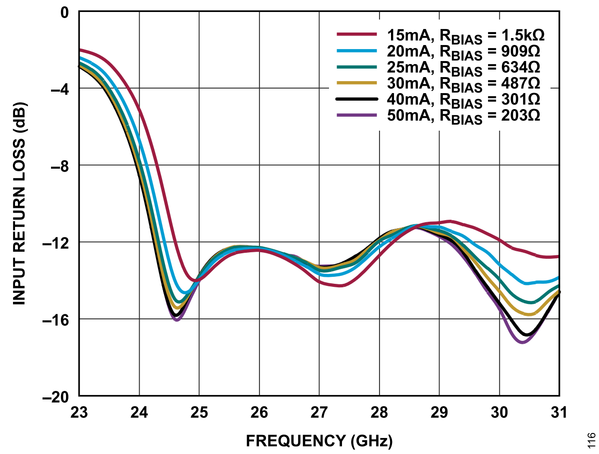


Figure 16. Input Return Loss vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

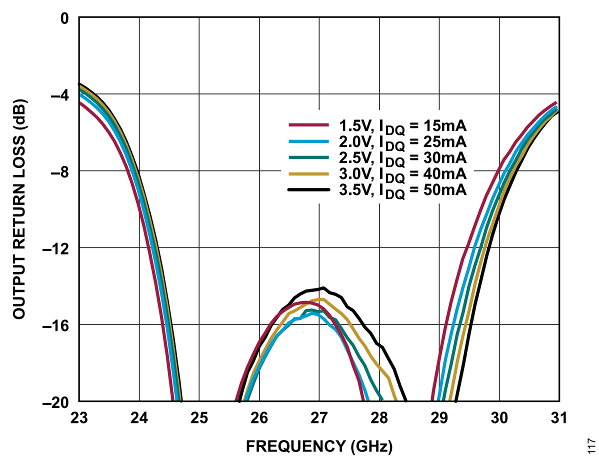


Figure 17. Output Return Loss vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 634 Ω

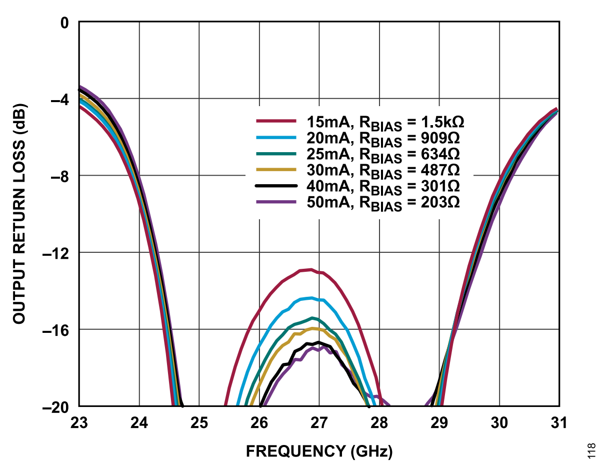


Figure 18. Output Return Loss vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

TYPICAL PERFORMANCE CHARACTERISTICS

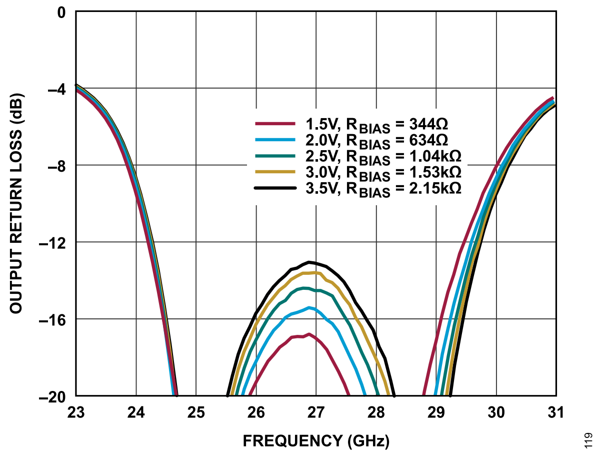


Figure 19. Output Return Loss vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

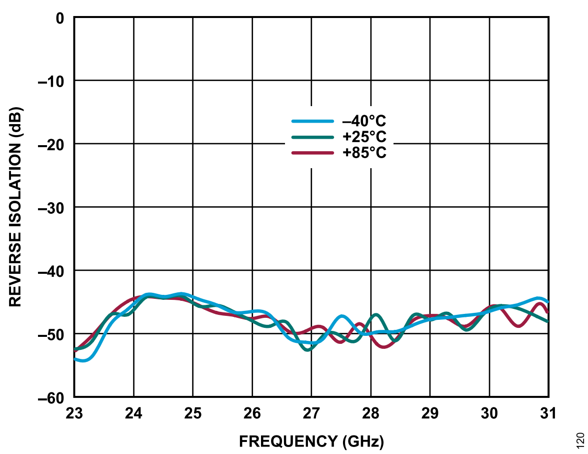


Figure 20. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 634 Ω

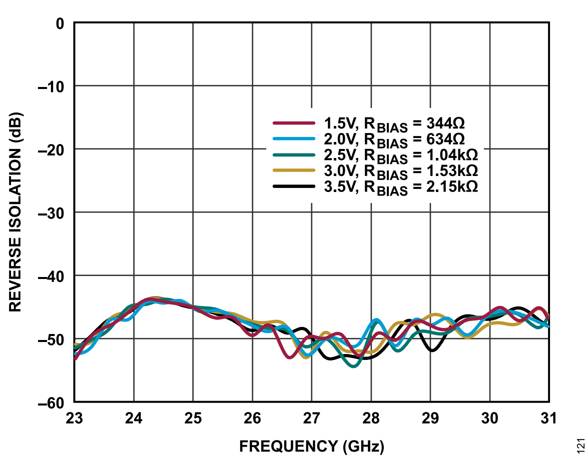


Figure 21. Reverse Isolation vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

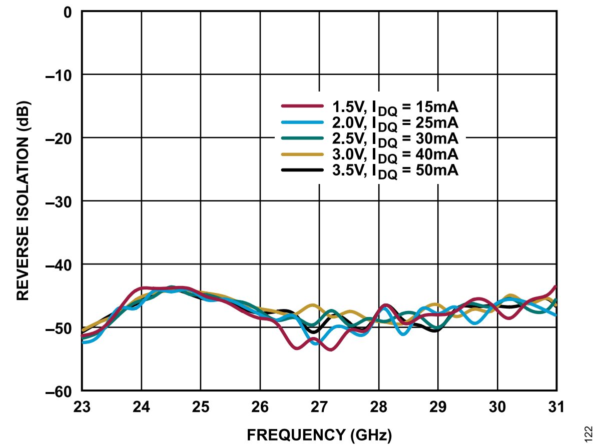


Figure 22. Reverse Isolation vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 634 Ω

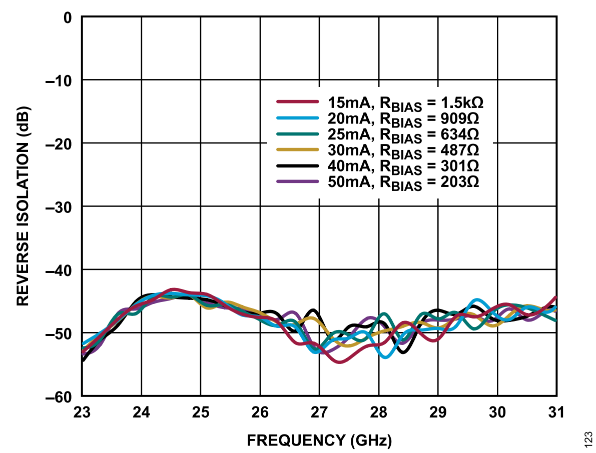


Figure 23. Reverse Isolation vs. Frequency for Various R_{BIAS} Values and I_{DQ}, V_{DD} = 2 V

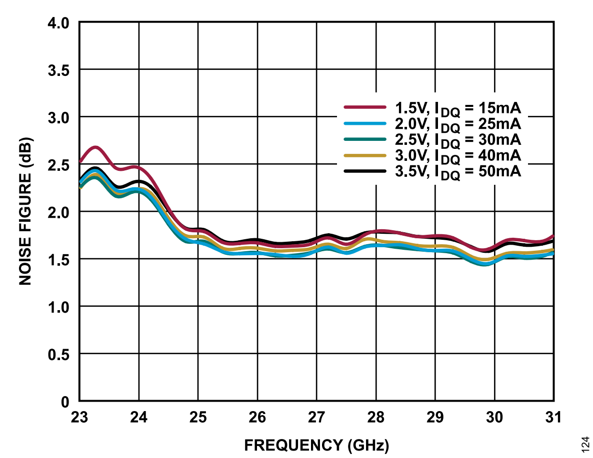


Figure 24. Noise Figure vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 634 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

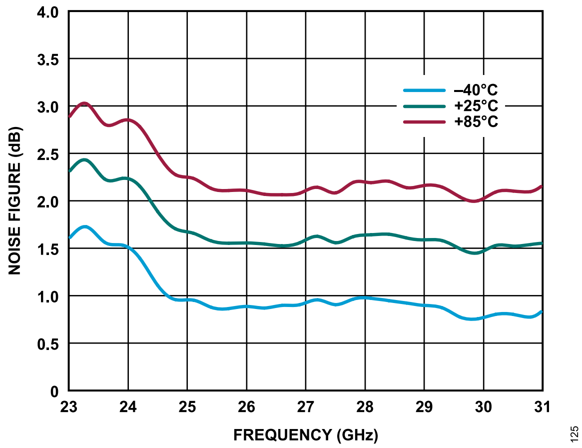


Figure 25. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 634 Ω

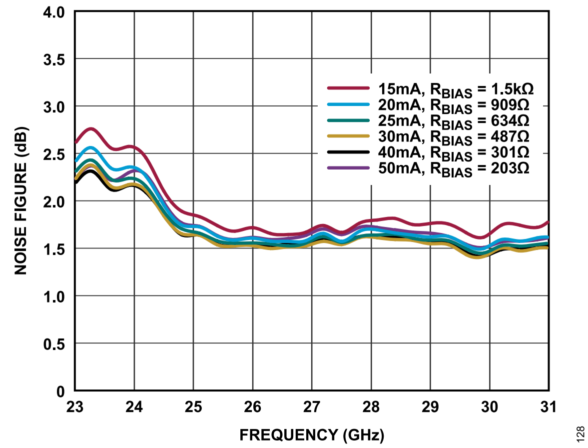


Figure 28. Noise Figure vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

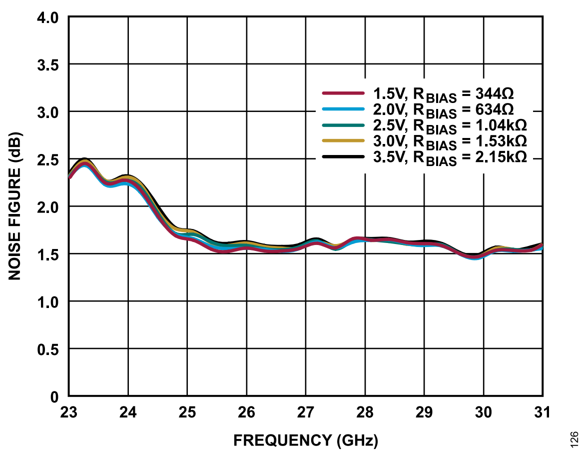


Figure 26. Noise Figure vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

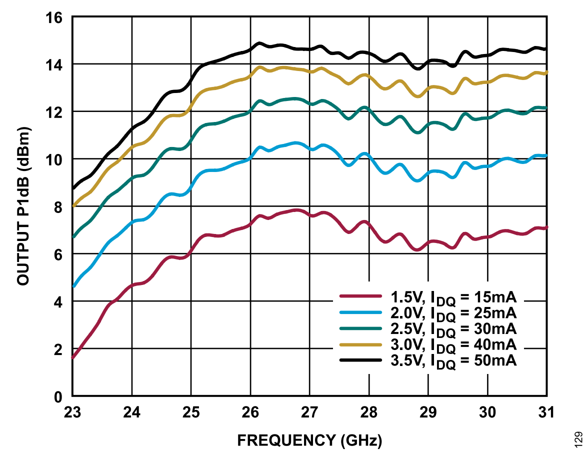


Figure 29. OP1dB vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 634 Ω

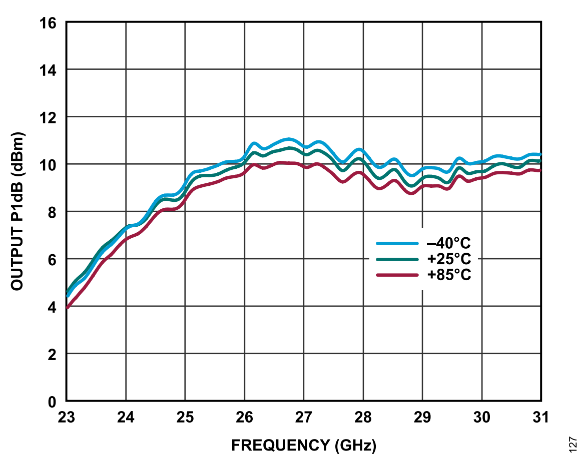


Figure 27. OP1dB vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 634 Ω

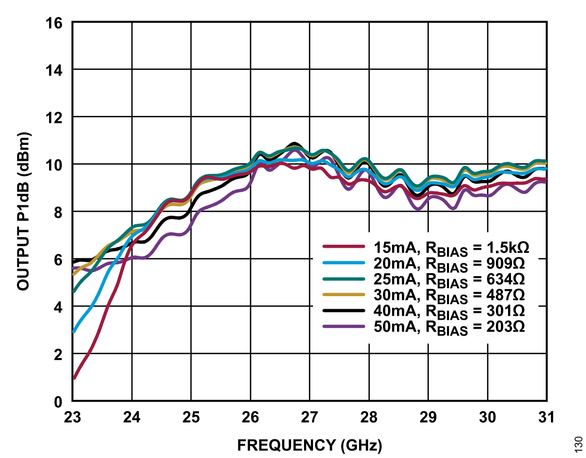


Figure 30. OP1dB vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

TYPICAL PERFORMANCE CHARACTERISTICS

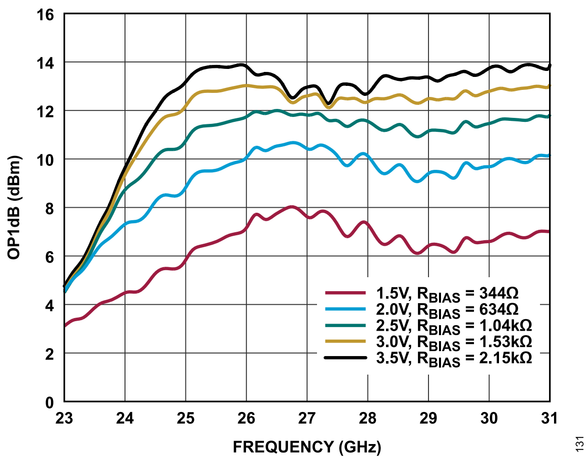


Figure 31. OP1dB vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

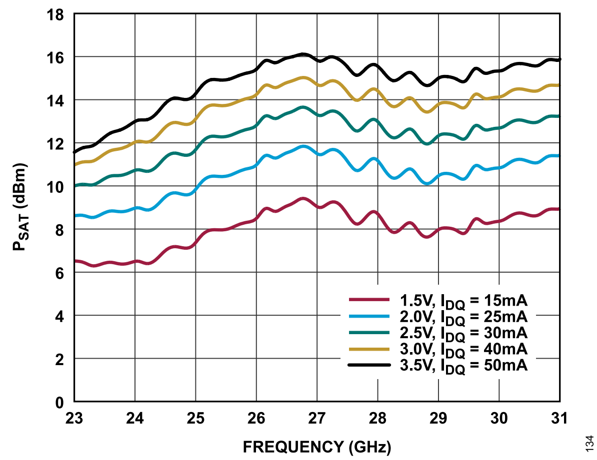


Figure 34. P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 634 Ω

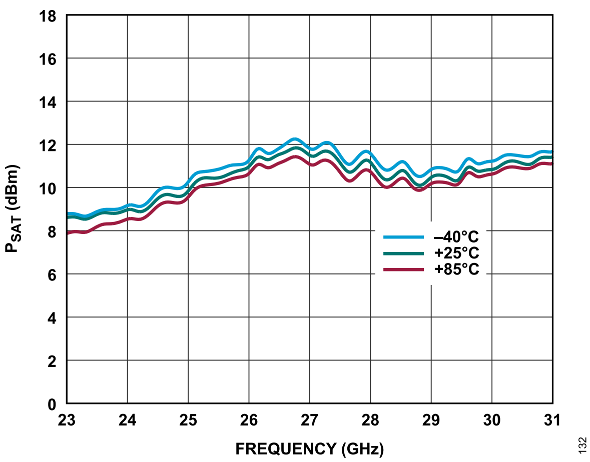


Figure 32. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 634 Ω

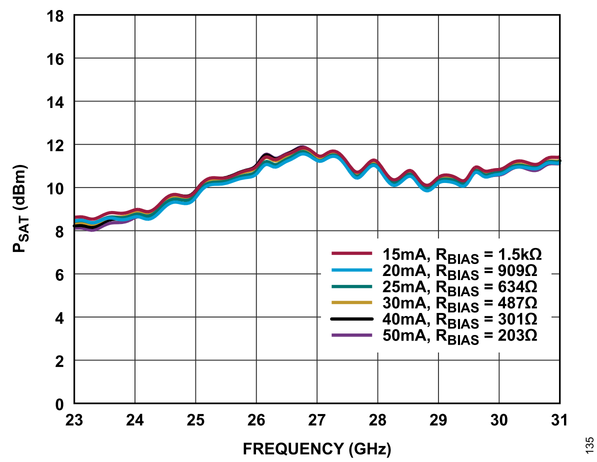


Figure 35. P_{SAT} vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

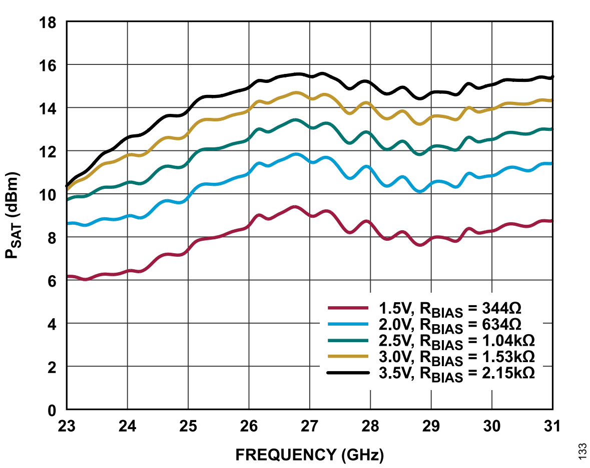


Figure 33. P_{SAT} vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

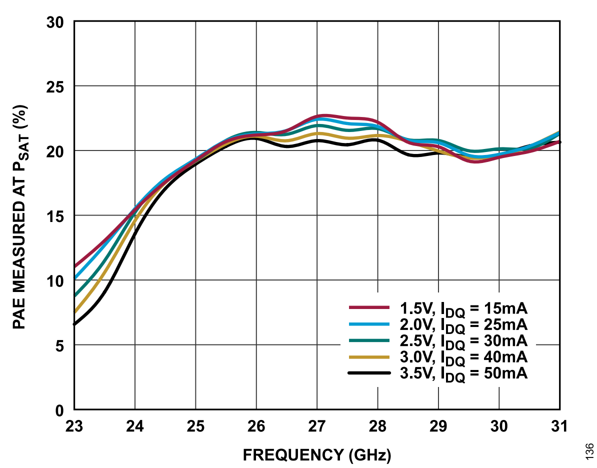


Figure 36. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 634 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

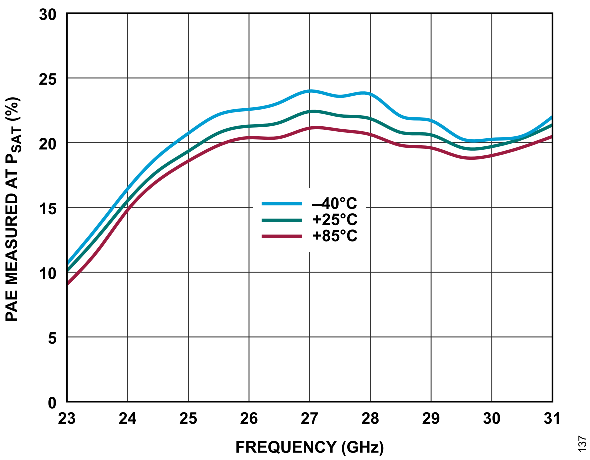


Figure 37. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 634 Ω

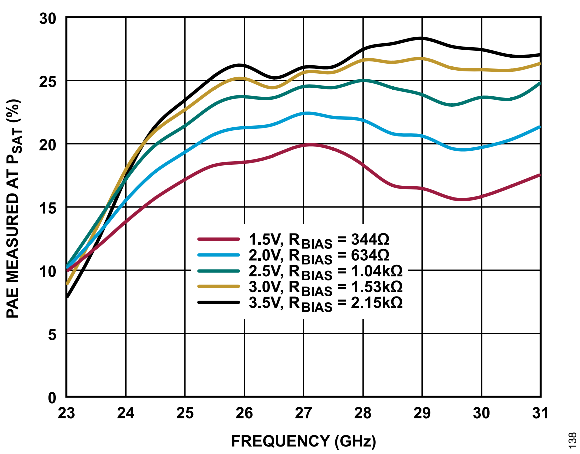


Figure 38. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

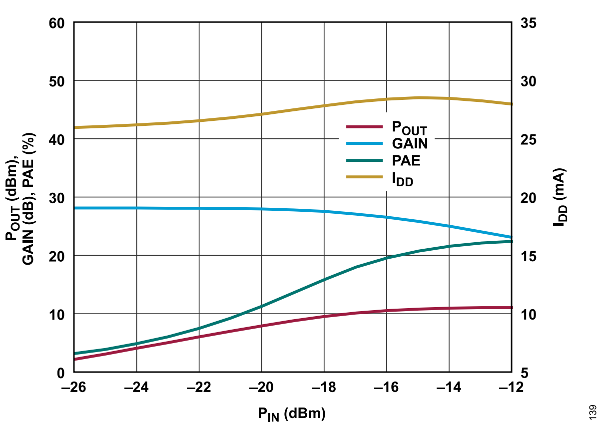


Figure 39. P_{OUT}, Gain, PAE, and Power Supply Current (I_{DD}) vs. P_{IN} at 27 GHz, V_{DD} = 2 V, R_{BIAS} = 634 Ω

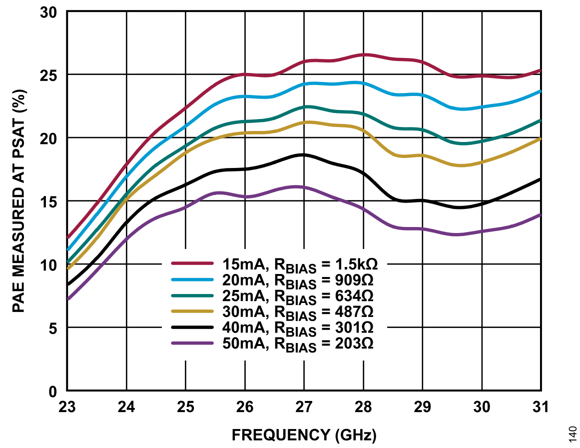


Figure 40. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

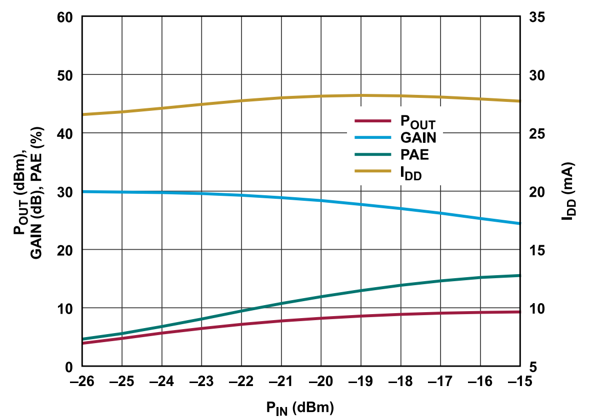


Figure 41. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 24 GHz, V_{DD} = 2 V, R_{BIAS} = 634 Ω

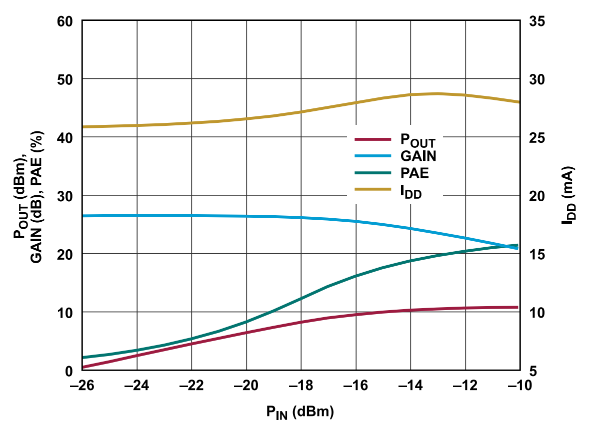


Figure 42. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 31 GHz, V_{DD} = 2 V, R_{BIAS} = 634 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

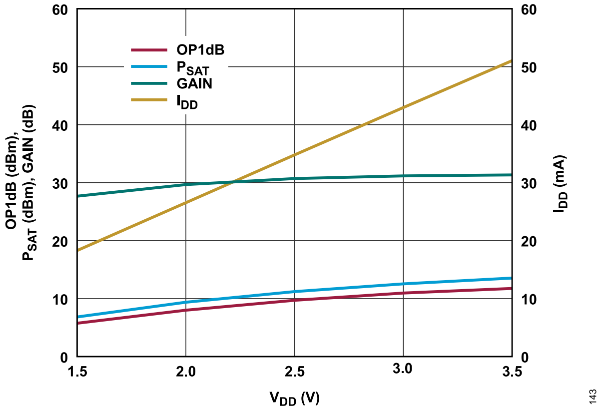


Figure 43. OP1dB, P_{SAT}, Gain, and I_{DD} vs. Supply Voltage at 24 GHz, R_{BIAS} = 634 Ω

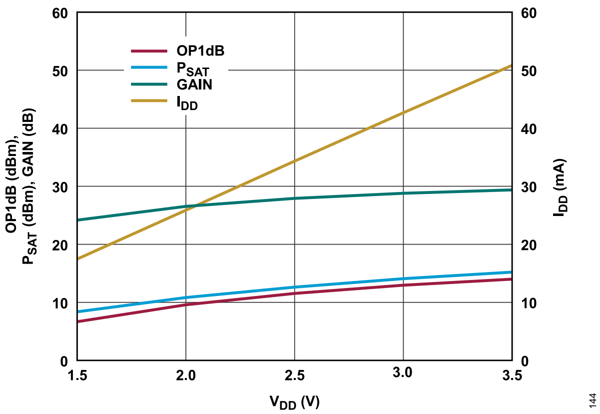


Figure 44. OP1dB, P_{SAT}, Gain, and I_{DD} vs. Supply Voltage at 31 GHz, R_{BIAS} = 634 Ω

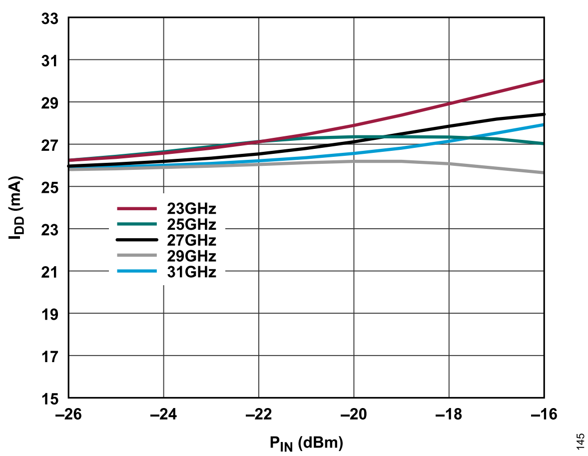


Figure 45. I_{DD} vs. P_{IN} for Various Frequencies, V_{DD} = 2 V

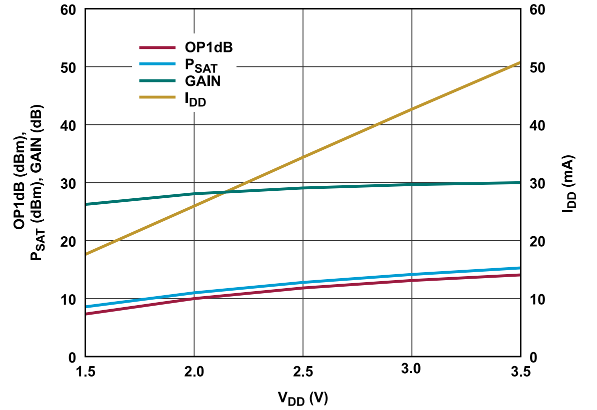


Figure 46. OP1dB, P_{SAT}, Gain, and I_{DD} vs. Supply Voltage at 27 GHz, R_{BIAS} = 634 Ω

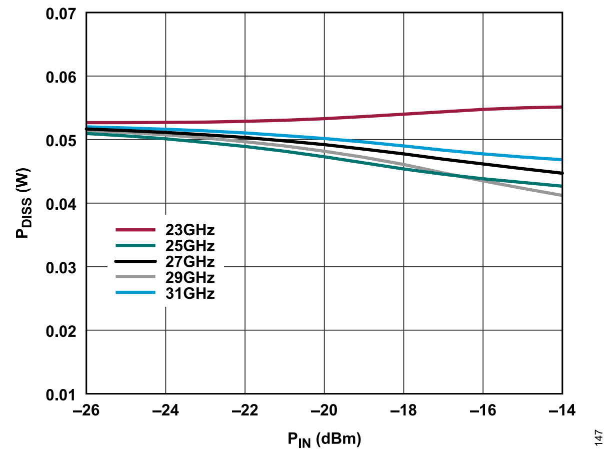


Figure 47. P_{DISS} vs. P_{IN} at Various Frequencies

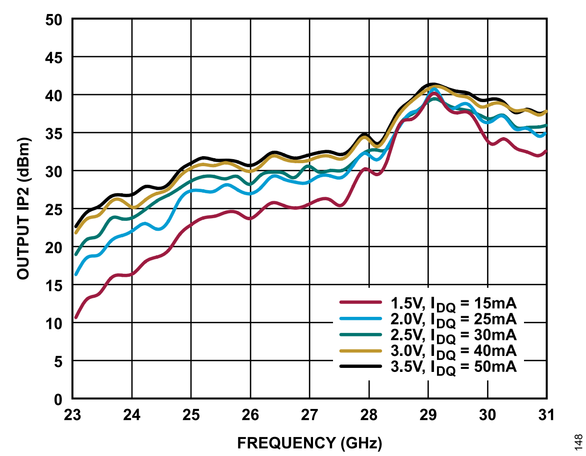


Figure 48. OIP2 vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 634 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

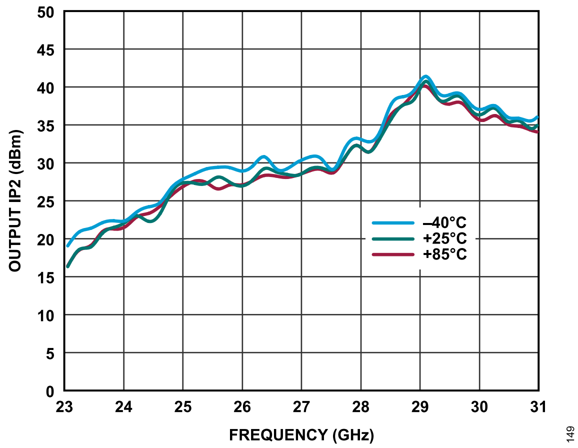


Figure 49. OIP2 vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 634 Ω

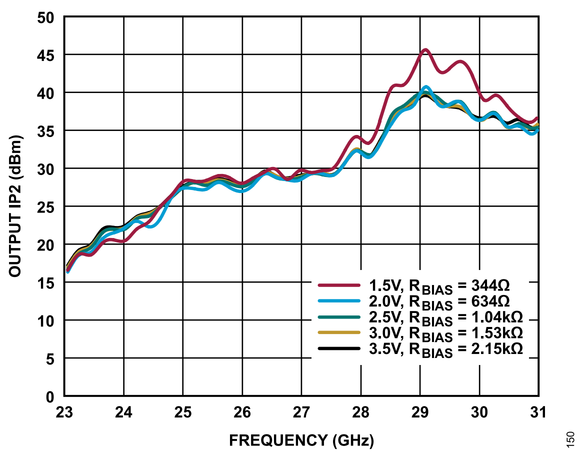


Figure 50. OIP2 vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

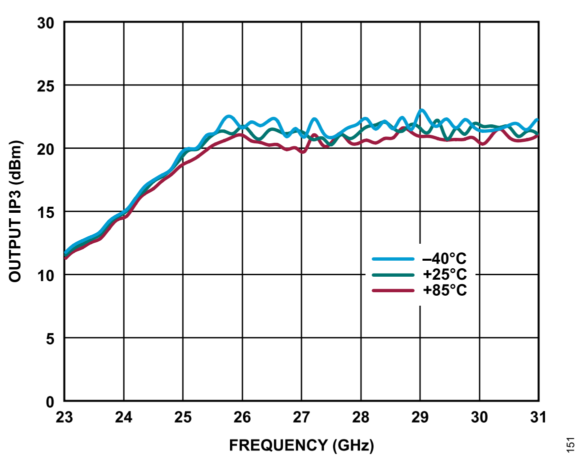


Figure 51. OIP3 vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 634 Ω

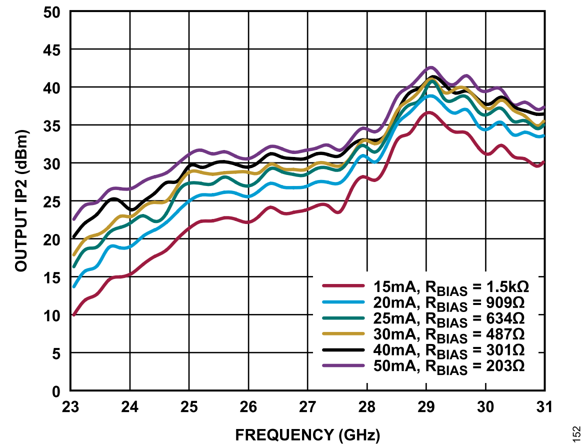


Figure 52. OIP2 vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

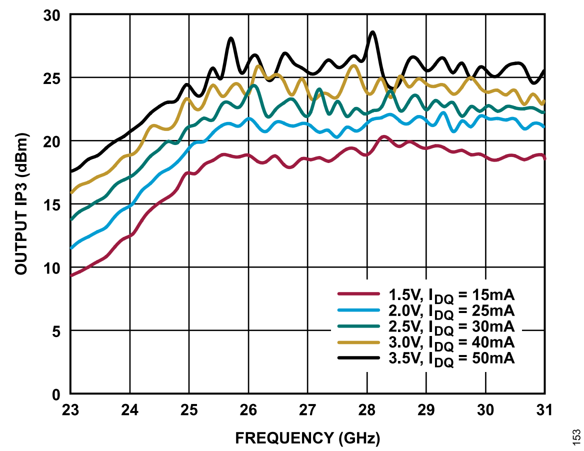


Figure 53. OIP3 vs. Frequency for Various Supply Voltages and I_{DQ}, R_{BIAS} = 634 Ω

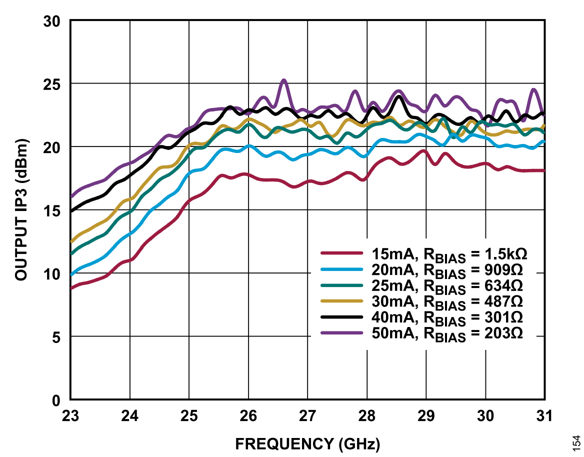


Figure 54. OIP3 vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

TYPICAL PERFORMANCE CHARACTERISTICS

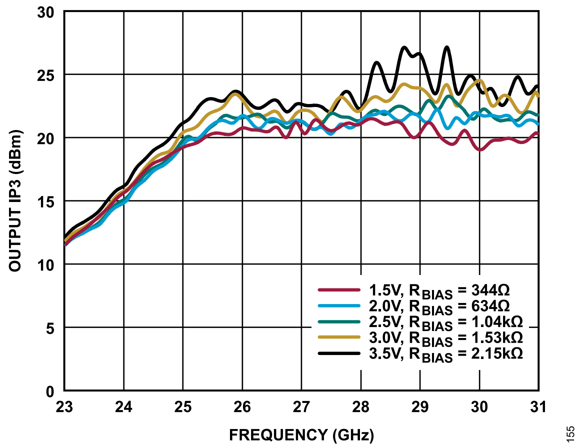


Figure 55. OIP3 vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

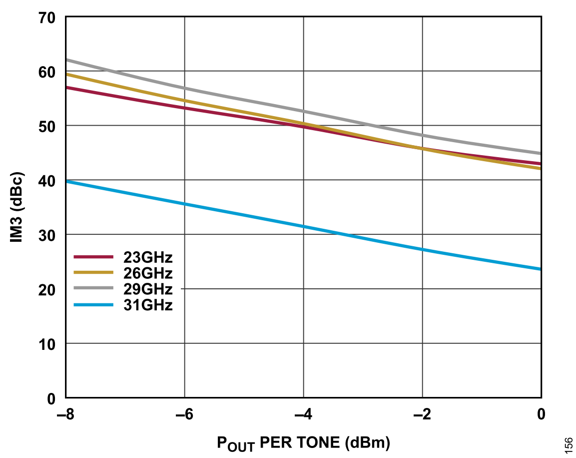


Figure 56. Third-Order Intermodulation (IM3) vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 2 V, R_{BIAS} = 634 Ω

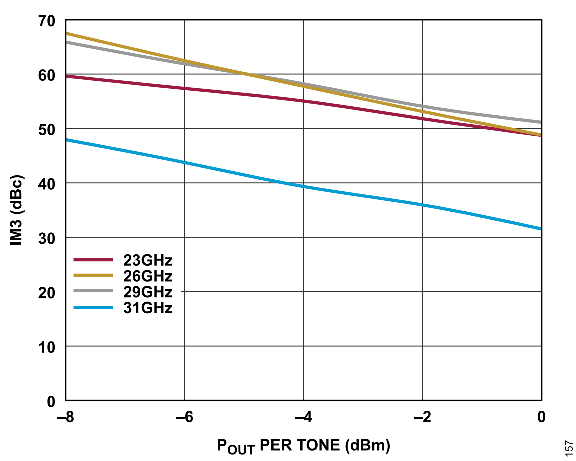


Figure 57. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 3 V, R_{BIAS} = 634 Ω

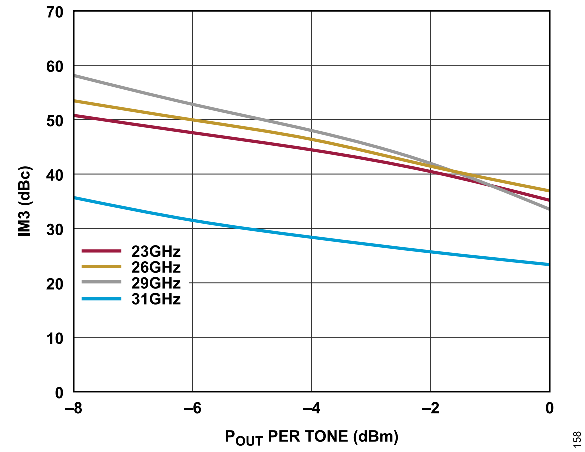


Figure 58. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 1.5 V, R_{BIAS} = 634 Ω

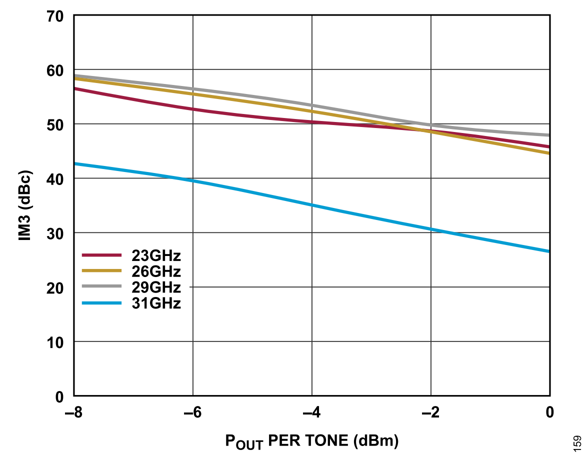


Figure 59. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 2.5 V, R_{BIAS} = 634 Ω

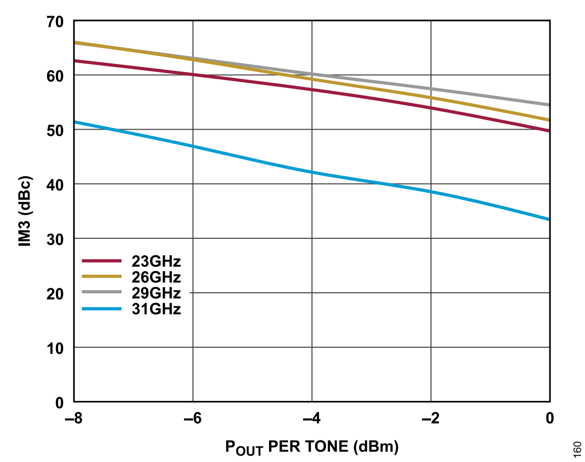


Figure 60. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 3.5 V, R_{BIAS} = 634 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

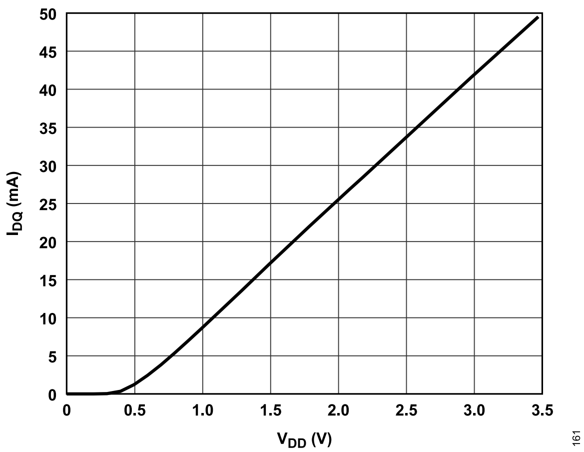


Figure 61. I_{DQ} vs. V_{DD}, R_{BIAS} = 634 Ω

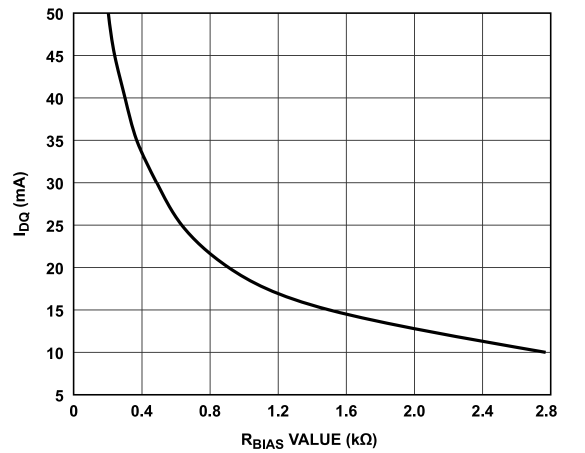


Figure 62. I_{DQ} vs. R_{BIAS} Value, V_{DD} = 2 V

THEORY OF OPERATION

The ADL8142 is a GaAs, MMIC, pHEMT, low noise wideband amplifier with an integrated bias inductor and ac-coupling capacitors. The simplified schematic is shown in Figure 63.

To adjust the drain bias current, connect an external resistor between the RBIAS and VDD pins.

The ADL8142 has ac-coupled, single-ended input and output ports with impedances that are nominally equal to 50 Ω over the 23 GHz to 31 GHz frequency range. No external matching components are required. While the RF output path is ac-coupled, there is a dc path to ground on the RFOUT side of the ac coupling capacitor.

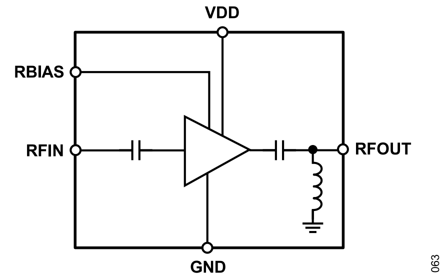


Figure 63. Simplified Schematic

APPLICATIONS INFORMATION

The basic connections for operating the ADL8142 over the specified frequency range are shown in Figure 64. No external biasing inductor is required, allowing the 2 V supply to be connected to the VDD pin. It is recommended to use 0.1 µF and 100 pF power supply decoupling capacitors. The power supply decoupling capacitors shown in Figure 64 represent the configuration used to characterize and qualify the ADL8142.

To set I_{DQ}, connect a resistor (R2) between the RBIAS and VDD pins. A default value of 634 Ω is recommended, which results in a nominal I_{DQ} of 25 mA. The RBIAS pin also draws a current that varies with the value of R_{BIAS}, and this current is typically a few mA. Do not leave the RBIAS pin open.

The RFIN and RFOUT pins are internally ac-coupled. If the RFOUT pin is connected to a dc bias level other than 0 V, ac-couple this pin because of the internal dc path to ground on RFOUT.

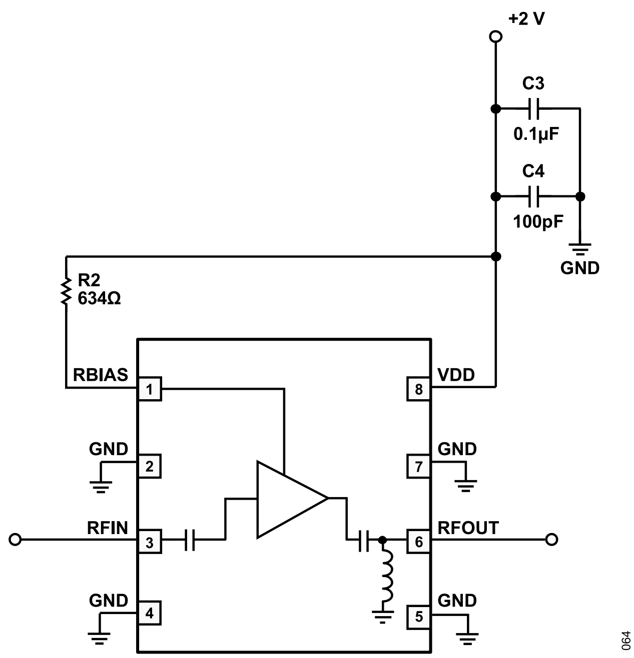


Figure 64. Typical Application Circuit

RECOMMENDED BIAS SEQUENCING

See the ADL8142-EVALZ user guide for the recommended bias sequencing information.

Table 8. Recommended Bias Resistor Values for V_{DD} = 2 V

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
203	50	45	5
301	40	36.2	3.8
487	30	27.5	2.5
634	25	23.0	2.0
909	20	18.5	1.5
1500	15	14.1	0.9

USING RBIAS AS A FAST ENABLE AND DISABLE FUNCTION

The RBIAS pin can be used as a fast enable and disable control input. In the schematic in Figure 65, a single-pole, double throw switch is used to switch the voltage on the RBIAS resistor between 0 V and 2.5 V. When the voltage on the RBIAS pin is equal to 0 V, I_{DQ} reduces to less than 1 mA with P_{IN} set to −20 dBm. The response time of this circuit is shown in Figure 66.

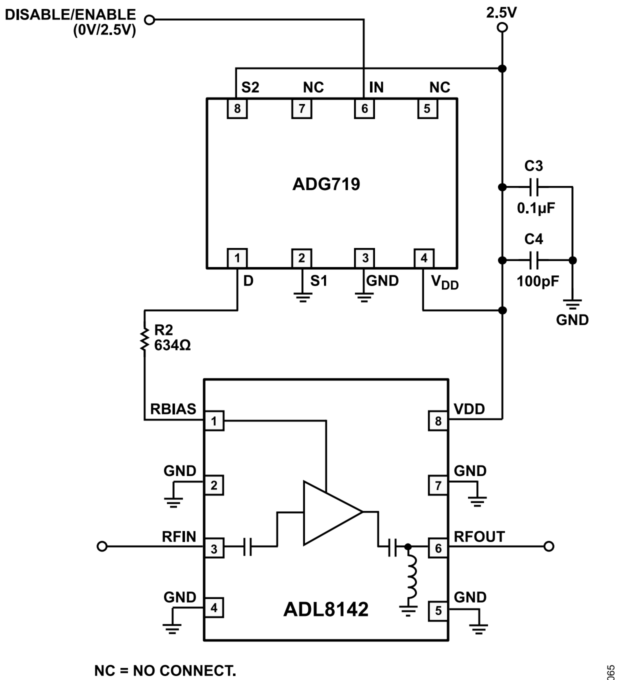


Figure 65. Fast Enable and Disable Using a 0 V to 2.5 V Pulse on the RBIAS Resistor

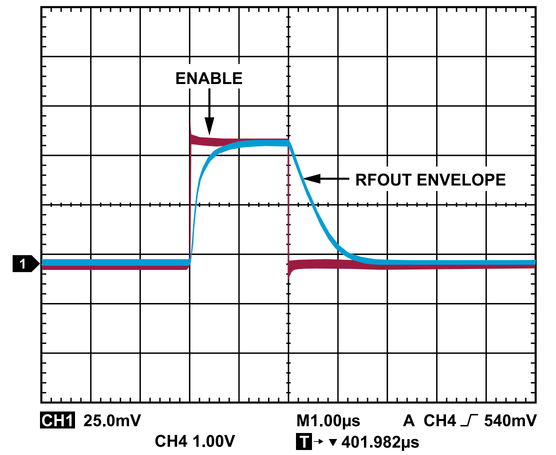


Figure 66. On and/or Off Response of the RF Output Envelope When the IN Pin of the ADG719 Is Pulsed, P_{OUT} = 6 dBm at 27 GHz

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 67 shows a recommended power management circuit that uses the LT3083 low dropout (LDO) regulator. With the IN and $V_{CONTROL}$ pins tied together, the minimum input voltage (V_{IN}) is 3.6 V when an output voltage (V_{OUT}) of 2 V is required along with a current draw of up to 3 A. Assuming that the ADL8142 is being used in a large array, a single LT3083 can easily provide power to the low noise amplifiers in a 64-element array. For applications that require a lower dropout voltage, LT3033 can be used.

Table 9 provides recommended resistor values to set the other V_{DD} voltages. In each case, the minimum external supply is the minimum dropout voltage from the $V_{CONTROL}$ input to V_{OUT}.

Table 9. Recommended Resistor Values for the Various LDO Output Voltages

LDO V_{OUT} (V)	R1 (kΩ)	Minimum V_{DD} (V)
1.5	30.1	3.1
2	40.2	3.6
2.5	49.9	4.1
3.3	66.5	4.9

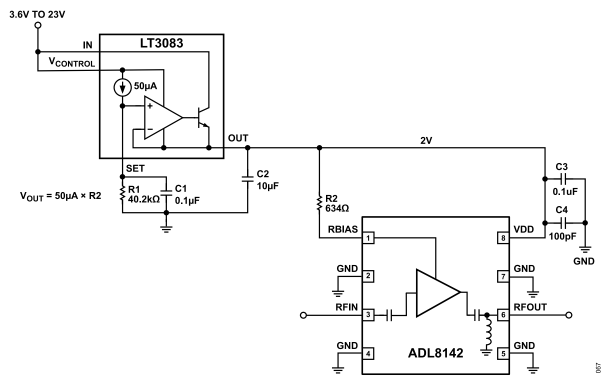


Figure 67. Recommended Power Management Circuit