5.7 kV rms, Signal Isolated CAN FD Transceiver

Data Sheet

ADM3056E

FEATURES

- 5.7 kV rms (8000 V_{PEAK}) signal isolated CAN transceiver
- 1.7 V to 5.5 V supply range for V_{DD1}
- 4.5 V to 5.5 V supply range for V_{DD2}
- ISO 11898-2:2016 compliant CAN FD
- Data rates up to 12 Mbps for CAN FD
- Low loop propagation delay of 150 ns maximum
- Extended common-mode range of ±25 V
- Bus fault protection (CANH, CANL) of ±40 V
- Low power standby supporting remote wake request
- Extra isolated signal for control (for example, termination switches)
- Slope control for reduced EMI
- Safety and regulatory approvals (pending)
  - VDE Certificate of Conformity, VDE V 0884-10
    - V_{IORM} = 849 V_{PEAK}
    - V_{IOSM} = 8000 V_{PEAK} (test: V_{PEAK} = 12.8 kV)
  - UL: 5700 V rms for 1 minute per UL 1577
  - CSA Component Acceptance 5A at 5 kV rms
    - IEC 60950, IEC 61010
- 8.3 mm creepage/clearance with 16-lead SOIC package
- High common-mode transient immunity: ≥75 kV/µs
- Industrial temperature range: −40°C to +125°C

APPLICATIONS

- CANOpen, DeviceNet, and other CAN bus implementations
- Solar inverters and battery management
- Motor and process control
- Industrial automation
- Transport and infrastructure

FUNCTIONAL BLOCK DIAGRAM

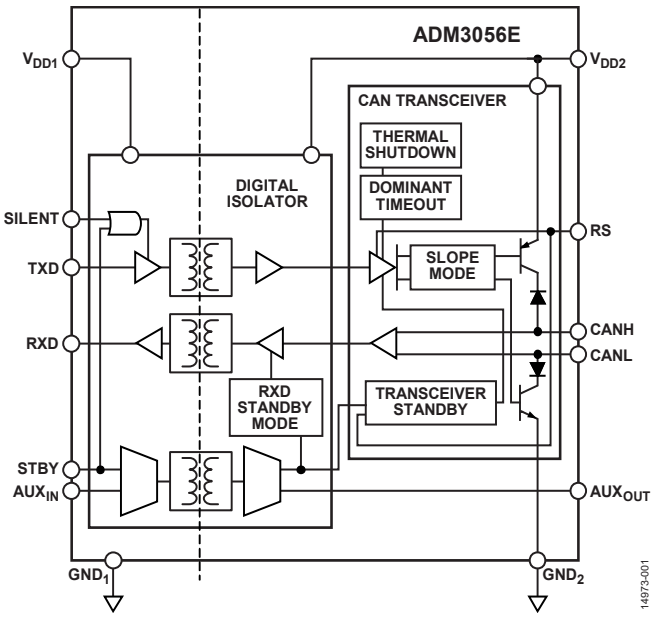

Figure 1.

GENERAL DESCRIPTION

The ADM3056E is a 5.7 kV rms isolated controller area network (CAN) physical layer transceiver. The ADM3056E fully meets the CAN flexible data rate (CAN FD) CAN FD ISO 11898-2:2016 requirements and is further capable of supporting data rates as high as 12 Mbps.

The device employs Analog Devices, Inc., *i*Coupler® technology to combine a highly robust 3-channel isolator and a CAN transceiver into a single SOIC, surface-mount package. The ADM3056E provides galvanic isolation between the CAN controller and physical layer bus.

Safety and regulatory approvals (pending) for 5.7 kV rms isolation voltage, 849 V_{PEAK} working insulation voltage, 8 kV surge, and 8.3 mm creepage and clearance, ensure that the ADM3056E meets isolation requirements for high voltage applications.

Low propagation delays through the isolation support longer bus cables. Slope control mode is available for the standard CAN at low data rates. Standby mode can minimize power consumption when the bus is idle, or if the node goes offline. Silent mode allows the TXD input to be ignored for listen only functionality.

Dominant timeout functionality protects against bus lock up in a fault condition, and current limiting and thermal shutdown features protect against output short circuits. The device is fully specified over the −40°C to +125°C industrial temperature range and is available in a 16-lead, increased creepage, wide-body SOIC package.

Rev. 0 Document Feedback

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REVISION HISTORY

12/2018—Revision 0: Initial Version

SPECIFICATIONS

All voltages are relative to their respective ground. 1.7 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, −40°C ≤ ambient temperature (T_A) ≤ +125°C, and STBY is low, unless otherwise noted. Typical specifications are at V_{DD1} = V_{DD2} = 5 V and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
Bus Side	I_{DD2}					
Standby Mode				3.5	mA	STBY high, AUX_{IN} low, load resistance (R_L) = 60 Ω
Recessive State (or Silent)			9	10	mA	TXD and/or SILENT high, R_L = 60 Ω
Dominant State			63	75	mA	Fault condition, see the Theory of Operation section, R_L = 60 Ω
70% Dominant/30% Recessive						Worst case, see the Theory of Operation section, R_L = 60 Ω
1 Mbps			38	45	mA	
5 Mbps			43	50	mA	
12 Mbps			52	65	mA	
Logic Side *i*Coupler Current	I_{DD1}					
Normal Mode				5	mA	TXD high, low, or switching; AUX_{IN} low
Standby Mode			1.6	2	mA	STBY high
DRIVER						
Differential Outputs						See Figure 21
Recessive State, Normal Mode						TXD high, termination resistor (R_L) and common-mode filter capacitor (C_F) open
CANH, CANL Voltage	V_{CANL}, V_{CANH}	2.0		3.0	V	
Differential Output Voltage	V_{OD}	−500		+50	mV	
Dominant State, Normal Mode						TXD and SILENT low, C_F open
CANH Voltage	V_{CANH}	2.75		4.5	V	50 Ω ≤ R_L ≤ 65 Ω
CANL Voltage	V_{CANL}	0.5		2.0	V	50 Ω ≤ R_L ≤ 65 Ω
Differential Output Voltage	V_{OD}	1.5		3.0	V	50 Ω ≤ R_L ≤ 65 Ω
		1.4		3.3	V	45 Ω ≤ R_L ≤ 70 Ω
		1.5		5.0	V	R_L = 2240 Ω
Standby Mode						STBY high, R_L and C_F open
CANH, CANL Voltage	V_{CANL}, V_{CANH}	−0.1		+0.1	V	
Differential Output Voltage	V_{OD}	−200		+200	mV	
Output Symmetry (V_{DD2} − V_{CANH} − V_{CANL})	V_{SYM}	−0.55		+0.55	V	R_L = 60 Ω, C_F = 4.7 nF, RS low
Short-Circuit Current	$\|I_{SC}\|$					R_L open
Absolute						
CANH				115	mA	V_{CANH} = −3 V
CANL				115	mA	V_{CANL} = 18 V
Steady State						
CANH				115	mA	V_{CANH} = −24 V
CANL				115	mA	V_{CANL} = 24 V
Logic Inputs (TXD, SILENT, STBY, AUX_{IN})						
Input Voltage						
High	V_{IH}	0.65 × V_{DD1}			V	
Low	V_{IL}			0.35 × V_{DD1}	V	
Complementary Metal-Oxide Semiconductor (CMOS) Logic Input Currents	$\|I_{IH}\|$, $\|I_{IL}\|$			10	µA	Input high or low

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RECEIVER						
Differential Inputs						
Differential Input Voltage Range	V_{ID}					See Figure 22, RXD capacitance (C_{RXD}) open, −25 V < V_{CANL}, and V_{CANH} < +25 V
Recessive		−1.0		+0.5	V	
		−1.0		+0.4	V	STBY high
Dominant		0.9		5.0	V	
		1.15		5.0	V	STBY high
Input Voltage Hysteresis	V_{HYS}		150		mV	
Unpowered Input Leakage Current	$\lvert I_{IN\ (OFF)}\rvert$			10	µA	V_{CANH}, V_{CANL} = 5 V, V_{DD2} = 0 V
CANH, CANL Input Resistance	R_{INH}, R_{INL}	6		25	kΩ	
Differential Input Resistance	R_{DIFF}	20		100	kΩ	
Input Resistance Matching	m_R	−0.03		+0.03		$m_R = 2 \times (R_{INH} - R_{INL})/(R_{INH} + R_{INL})$
CANH, CANL Input Capacitance	C_{INH}, C_{INL}		35		pF	
Differential Input Capacitance	C_{DIFF}		12		pF	
Logic Outputs (RXD, AUX_{OUT})						
Output Voltage						
Logic Low	V_{OL}		0.2	0.4	V	Output current (I_{OUT}) = 2 mA
Logic High	V_{OH}					I_{OUT} = −2 mA
RXD		V_{DD1} − 0.2			V	
AUX_{OUT}		2.4			V	
Short-Circuit Current	I_{OS}					Output voltage (V_{OUT}) = GND_1 or V_{DD1}
RXD		7		85	mA	
COMMON-MODE TRANSIENT IMMUNITY[1]						Common-mode voltage (V_{CM}) ≥ 1 kV, transient magnitude ≥ 800 V
Input High, Recessive	$\lvert CM_H\rvert$	75	100		kV/µs	AUX_{IN} high, TXD high, or CANH, CANL recessive
Input Low, Dominant	$\lvert CM_L\rvert$	75	100		kV/µs	AUX_{IN} low, TXD low, or CANH, CANL dominant
SLOPE CONTROL						
Input Voltage for Standby Mode	V_{STB}	4.0			V	
Current for Slope Control Mode	I_{SLOPE}			−240	µA	RS voltage (V_{RS}) = 0 V
Slope Control Mode Voltage	V_{SLOPE}	2.1			V	RS current (I_{RS}) = 10 µA
Input Voltage for High Speed Mode	V_{HS}			1	V	

[1] $\lvert CM_H\rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining AUX_{OUT} ≥ 2.4 V, CANH, CANL recessive, or RXD ≥ V_{DD1} − 0.2 V. $\lvert CM_L\rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining AUX_{OUT} ≤ 0.4 V, CANH, CANL dominant, or RXD ≤ 0.4 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

All voltages are relative to their respective ground. 1.7 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, −40°C ≤ T_A ≤ +125°C, and STBY low, unless otherwise noted. Typical specifications are at V_{DD1} = V_{DD2} = 5 V and T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DRIVER						SILENT low, see Figure 2 TXD pin bit time (t_{BIT_TXD}) = 200 ns, see Figure 23 RS pin pull-down resistance (R_{SLOPE}) = 0 Ω R_L = 60 Ω, C_L = 100 pF
Maximum Data Rate		12			Mbps	
Propagation Delay from TXD to Bus (Recessive to Dominant)	t_{TXD_DOM}		35	60	ns	
Propagation Delay from TXD to Bus (Dominant to Recessive)	t_{TXD_REC}		46	70	ns	
Transmit Dominant Timeout	t_{DT}	1175			µs	TXD low, see Figure 5
RECEIVER						SILENT low, see Figure 2 and Figure 23 R_L = 60 Ω, C_L = 100 pF C_{RXD} = 15 pF
Falling Edge Loop Propagation Delay (TXD to RXD)	t_{LOOP_FALL}					
Full Speed Mode				150	ns	R_{SLOPE} = 0 Ω, t_{BIT_TXD} = 200 ns
Slope Control Mode				300	ns	R_{SLOPE} = 47 kΩ, t_{BIT_TXD} = 1 µs
Rising Edge Loop Propagation Delay (TXD to RXD)	t_{LOOP_RISE}					
Full Speed Mode				150	ns	R_{SLOPE} = 0 Ω, t_{BIT_TXD} = 200 ns
Slope Control Mode				300	ns	R_{SLOPE} = 47 kΩ, t_{BIT_TXD} = 1 µs
Loop Delay Symmetry (Minimum Recessive Bit Width)	t_{BIT_RXD}					
2 Mbps		450		550	ns	t_{BIT_TXD} = 500 ns
5 Mbps		160		220	ns	t_{BIT_TXD} = 200 ns
8 Mbps		85		140	ns	t_{BIT_TXD} = 125 ns
12 Mbps		50		91.6	ns	t_{BIT_TXD} = 83.3 ns
CANH, CANL SLEW RATE	|SR|		7		V/µs	R_{SLOPE} = 47 kΩ
STANDBY						
Minimum Pulse Width Detected (Receiver Filter Time)	t_{FILTER}	1		5	µs	STBY high, see Figure 4
Wake-Up Pattern Detection Reset Time	t_{WUPR}	1175		4000	µs	STBY high, see Figure 4
Normal Mode to Standby Mode Time	t_{STBY_ON}			25	µs	Not shown in timing figures
Standby Mode to Normal Mode Time	t_{STBY_OFF}			25	µs	Time until RXD valid, not shown in timing figures
AUXILIARY SIGNAL						
Maximum Switching Rate	f_{AUX}	20			kHz	
AUX_{IN} to AUX_{OUT} Propagation Delay	t_{AUX}			25	µs	Not shown in timing figures
SILENT MODE						
Normal Mode to Silent Mode Time	t_{SILENT_ON}		40	100	ns	TXD low, R_{SLOPE} = 0 Ω, see Figure 3
Silent Mode to Normal Mode Time	t_{SILENT_OFF}		50	100	ns	TXD low, R_{SLOPE} = 0 Ω, see Figure 3

Timing Diagrams

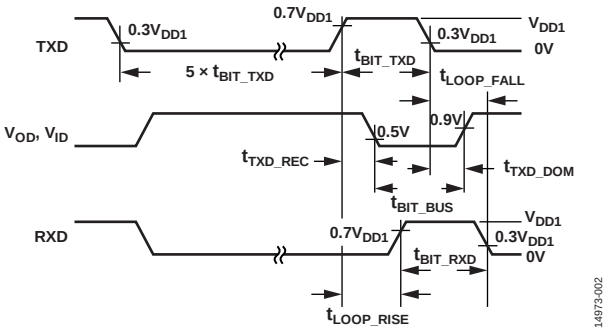

Figure 2. Driver/Receiver Timing Diagram

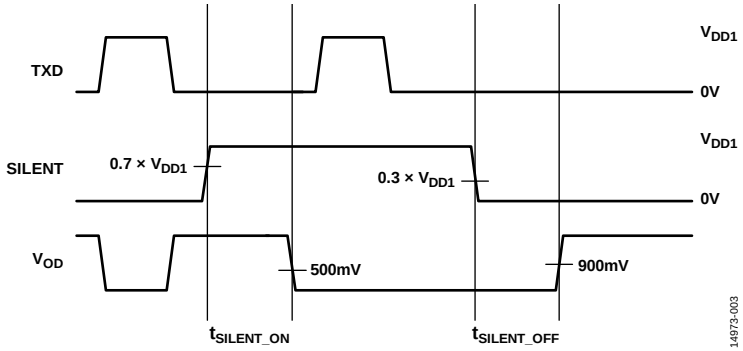

Figure 3. Silent Mode Timing Diagram

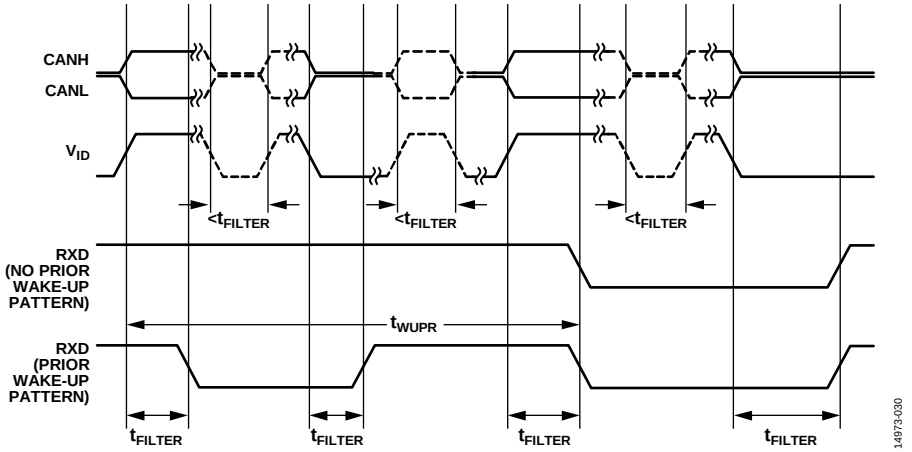

Figure 4. Wake-Up Pattern Detection and Filtered RXD in Standby Timing Diagram

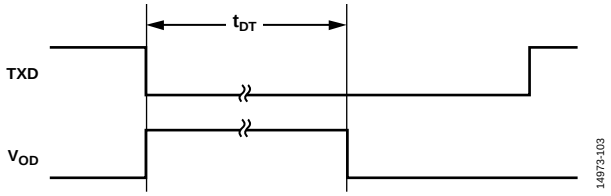

Figure 5. Dominant Timeout

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 3.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5700	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	8.3	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303 Part 1
Material Group		I		Material Group (DIN VDE 0110, 1/89, Table 1)

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		1.5		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	

[1] The device is considered a 2-terminal device. Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

See Table 9 and the Insulation Lifetime section for the recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

The ADuM3056E is approved by the organizations listed in Table 5.

Table 5.

UL (Pending)[1]	CSA (Pending)	VDE (Pending)[2]	CQC (Pending)
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Certified under CQC11-471543-2012
Single Protection, 5700 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2	Reinforced insulation, 849 V_{PEAK}, V_{IOTM} = 8 kV_{PEAK}	GB4943.1-2011: Basic insulation at 830 V rms (1174 V_{PEAK})
	Basic insulation at 830 V rms (1174 V_{PEAK})		Reinforced insulation at 415 V rms (587 V_{PEAK})
	Reinforced insulation at 415 V rms (587 V_{PEAK})		
	IEC 60601-1 Edition 3.1:		
	Basic insulation (1 mean of patient protection (MOPP)), 519 V rms (734 V_{PEAK})		
	Reinforced insulation (2 MOPP), 261 V rms (369 V_{PEAK})		
	CSA 61010-1-12 and IEC 61010-1 third edition		
	Basic insulation at: 300 V rms mains, 830 V secondary (1174 V_{PEAK})		
	Reinforced insulation at: 300 V rms mains, 415 V secondary (587 V_{PEAK})		
File E214100	File 205078	File 2471900-4880-0001	File (pending)

[1] In accordance with UL 1577, each ADM3056E is proof tested by applying an insulation test voltage ≥ 6840 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-10, each ADM3056E is proof tested by applying an insulation test voltage ≥ 1592 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS (PENDING)

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data.

Table 6.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to IV	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V_{PEAK}
Input to Output Test Voltage, Method A		$V_{pd(m)}$		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1274	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1019	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	8000	V_{PEAK}
Impulse	1.2 µs rise time, 50 µs, 50% fall time in air, to the preferred sequence	$V_{IMPULSE}$	8000	V_{PEAK}
Surge Isolation Voltage				
Basic	$V_{PEAK} = 12.8$ kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	9800	V_{PEAK}
Reinforced	$V_{PEAK} = 12.8$ kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	8000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 6)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	1.73	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

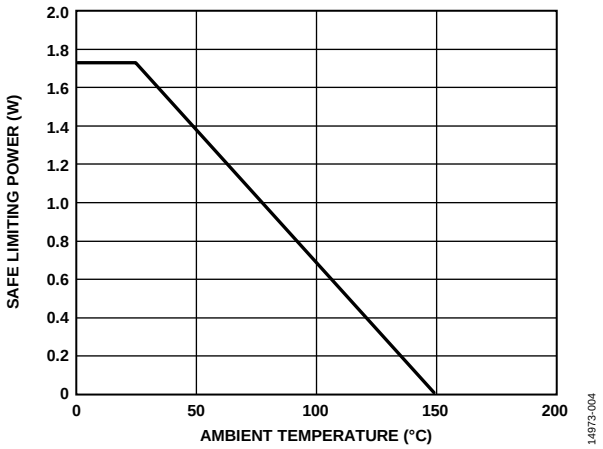

Figure 6. Thermal Derating Curve, Dependence of Safety Limiting Power Values with Ambient Temperature per DIN V VDE V 0884-10

ABSOLUTE MAXIMUM RATINGS

Pin voltages with respect to GND_X on same side, unless otherwise stated.

Table 7.

Parameter	Rating
V_{DD1}, V_{DD2}	−0.5 V to +6 V
Logic Side Input/Output (TXD, RXD, AUX_{IN}, SILENT, STBY)	−0.5 V to V_{DD1} + 0.5 V
CANH, CANL	−40 V to +40 V
AUX_{OUT}, RS	−0.5 V to V_{DD2} + 0.5 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Maximum)	150°C
Electrostatic Discharge (ESD)	
IEC 61000-4-2, CANH/CANL	
Across Isolation Barrier with Respect to GND_1	±8 kV
Contact Discharge with Respect to GND_2	±8 kV
Air Discharge with Respect to GND_2	±15 kV
Human Body Model (All Pins, 1.5 kΩ, 100 pF)	4 kV
Moisture Sensitivity Level (MSL)	3

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
RI-16-2[1]	72	°C/W

[1] θ_{JA} is derived by simulation of the device on a 4-layer board in an enclosure with no airflow. See the Thermal Analysis section for thermal model definitions.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 9. Maximum Continuous Working Voltage[1]

Parameter	Insulation Rating (20-Year Lifetime)[2]	VDE 0884-11 Lifetime Conditions Fulfilled
AC Voltage		
Bipolar Waveform		
Basic Insulation	849 V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
Reinforced Insulation	707 V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
Unipolar Waveform		
Basic Insulation	1697 V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
Reinforced Insulation	1356 V_{PEAK}	Lifetime limited by package creepage per IEC 60664-1
DC Voltage		
Basic Insulation	1660 V_{PEAK}	Lifetime limited by package creepage per IEC 60664-1
Reinforced Insulation	830 V_{PEAK}	Lifetime limited by package creepage per IEC 60664-1

[1] The maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

[2] Insulation capability without regard to creepage limitations. Working voltage may be limited by the PCB creepage when considering rms voltages for components soldered to a PCB (assumes Material Group I up to 1250 V rms), or by the SOIC_IC package creepage of 8.3 mm, when considering rms voltages for Material Group II.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

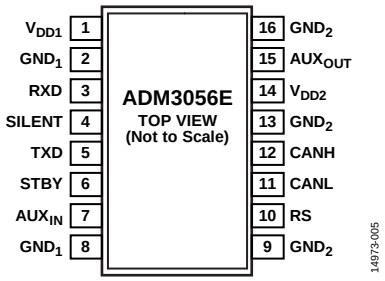

Figure 7. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply, Logic Side, 1.7 V to 5.5 V. This pin requires 0.1 µF and 0.01 µF decoupling capacitors.
2, 8	GND_1	Ground, Logic Side.
3	RXD	Receiver Output Data.
4	SILENT	Silent Mode Select. Active with input high. Bring this input low or leave the pin unconnected (internal pull-down) for normal mode.
5	TXD	Transmitter Input Data. This pin has a weak internal pull-up resistor to V_{DD1}.
6	STBY	Standby Mode Select. Active with input high. Bring this input low or leave the pin unconnected (internal pull-down) for normal mode.
7	AUX_{IN}	Auxiliary Channel Input. This pin sets the AUX_{OUT} output.
9, 13, 16	GND_2	Ground, Bus Side.
10	RS	Slope Control Pin. Short this pin to ground for full speed operation or use a weak pull-down (for example, 47 kΩ) for slope control mode. An input high signal places the CAN transceiver in standby.
11	CANL	CAN Low Input/Output.
12	CANH	CAN High Input/Output.
14	V_{DD2}	Power Supply, Bus Side, 4.5 V to 5.5 V. This pin requires 0.1 µF and 0.01 µF decoupling capacitors.
15	AUX_{OUT}	Isolated Auxiliary Channel Output per Auxiliary Input in Normal Mode. The state of AUX_{OUT} is latched when STBY is high. By default, AUX_{OUT} is low at startup or when V_{DD1} is unpowered.

OPERATIONAL TRUTH TABLE

Table 11. Truth Table

Power		Inputs[1, 2]						Outputs		
V_{DD1}	V_{DD2}	TXD	SILENT	STBY	AUX_{IN}	RS	Mode	RXD	AUX_{OUT}	CANH/CANL
On	On	Low	Low	Low	Low	Low/ pull-down	Normal/ slope mode	Low	Low	Dominant[3]
On	On	Low	Low	Low	High	Low/ pull-down	Normal/ slope mode	Low	High	Dominant[3]
On	On	High	Low	Low	Low	Low/ pull-down	Normal/ slope mode	High/per bus	Low	Recessive/set by bus
On	On	High	Low	Low	High	Low/ pull-down	Normal/ slope mode	High/per bus	High	Recessive/set by bus
On	On	X	High	Low	Low	X	Listen only	High/per bus	Low	Recessive/set by bus
On	On	X	High	Low	High	X	Listen only	High/per bus	High	Recessive/set by bus
On	On	X	X	High	X	X	Standby[4]	High/WUP[5]/ filtered	Last state	High-Z, biased to GND_2/ set by bus
On	On	X	X	X	Low	High	Standby[4]	High/WUP[5]/ filtered	Low	High-Z, based to GND_2/ set by bus
On	On	X	X	X	High	High	Standby[4]	High/WUP[5]/ filtered	High	High-Z, biased to GND_2/ set by bus
Off	On	Z	Z	Z	Z	Low/ pull-down	Normal/ slope mode	Indeterminate	Low	Recessive/set by bus
On	Off	X	X	X	X	X	Transceiver off	High	Indeterminate	High-Z

[1] Z means high impedance within one diode drop of ground.
[2] X means don't care.
[3] Limited by t_{DT}.
[4] RS can only set the transceiver to standby mode. It does not control the digital isolator.
[5] WUP means remote wake-up pattern.

TYPICAL PERFORMANCE CHARACTERISTICS

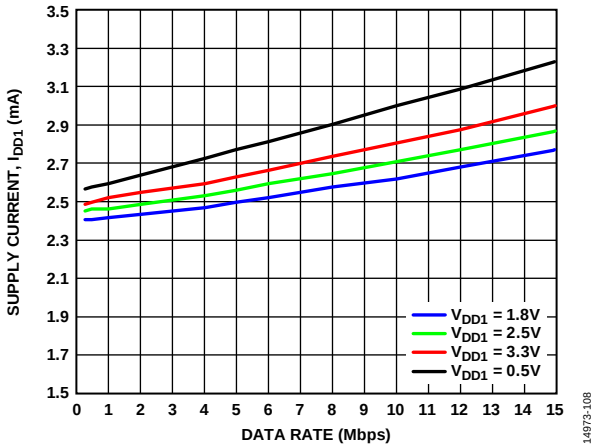

Figure 8. Supply Current, I_{DD1} vs. Data Rate, AUX_{IN} Low

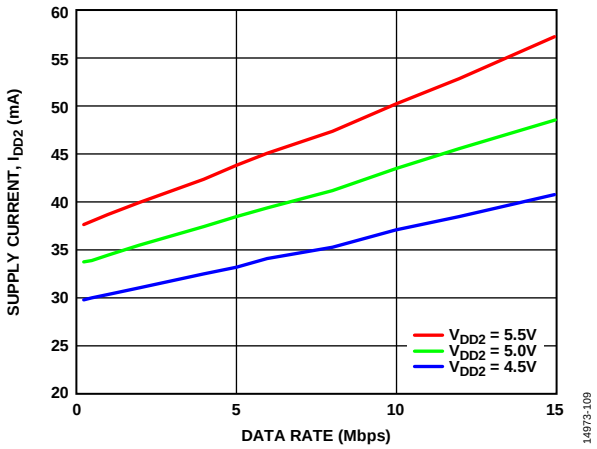

Figure 9. Supply Current, I_{DD2} vs. Data Rate

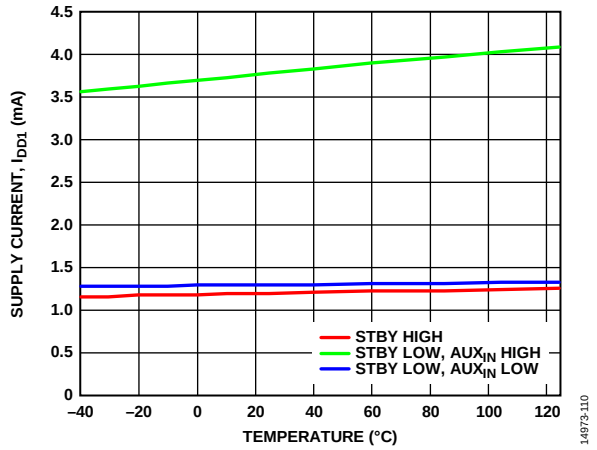

Figure 10. Supply Current, I_{DD1} vs. Temperature (Inputs Idle, V_{DD1} = 5 V)

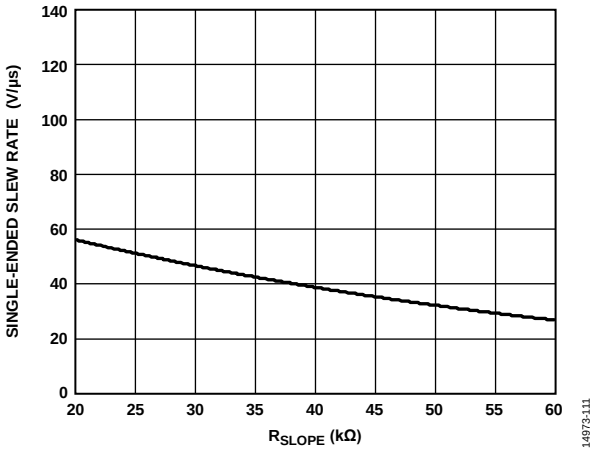

Figure 11. Single-Ended Slew Rate vs. R_{SLOPE}

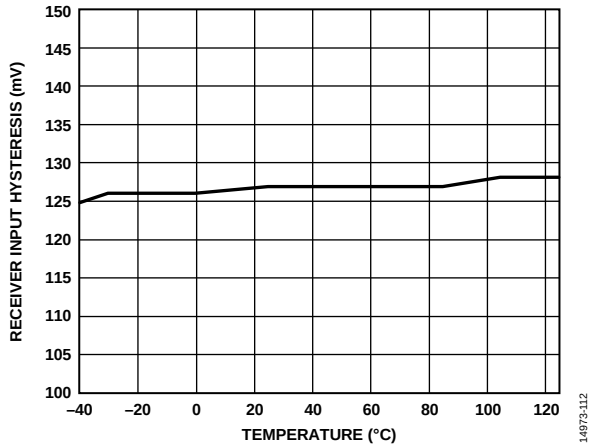

Figure 12. Receiver Input Hysteresis vs. Temperature

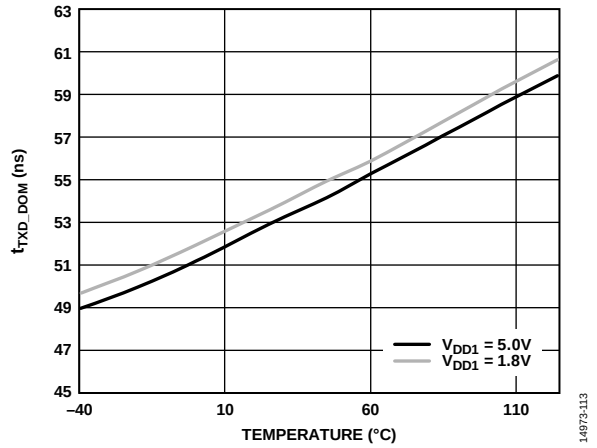

Figure 13. t_{TXD_DOM} vs. Temperature (R_{SLOPE} = 0 Ω)

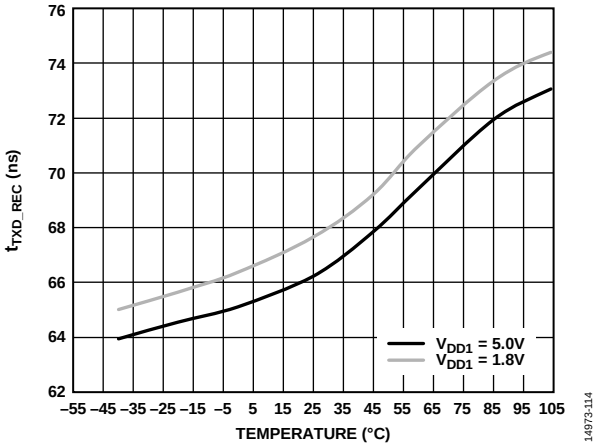

Figure 14. t_{TXD_REC} vs. Temperature (R_{SLOPE} = 0 Ω)

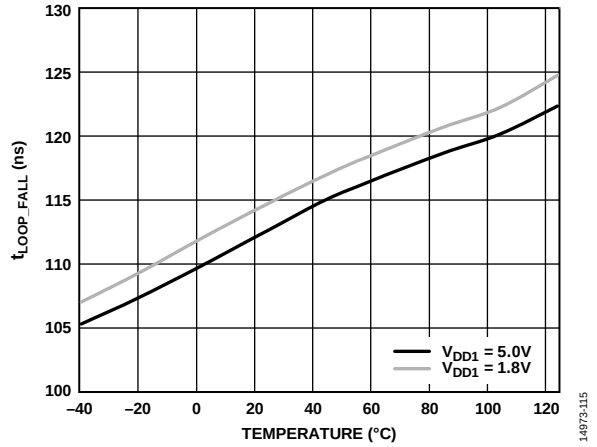

Figure 15. t_{LOOP_FALL} vs. Temperature (R_{SLOPE} = 0 Ω)

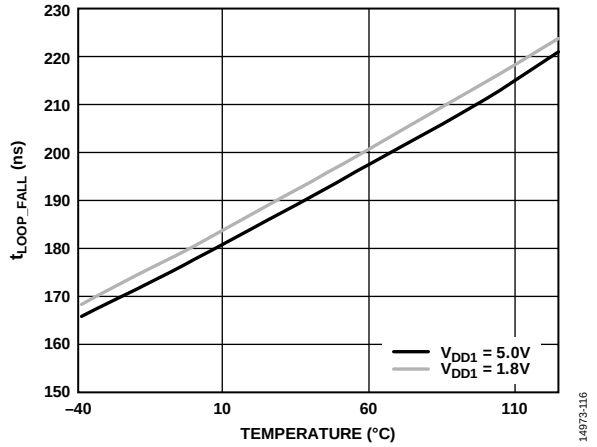

Figure 16. t_{LOOP_FALL} vs. Temperature (R_{SLOPE} = 47 kΩ)

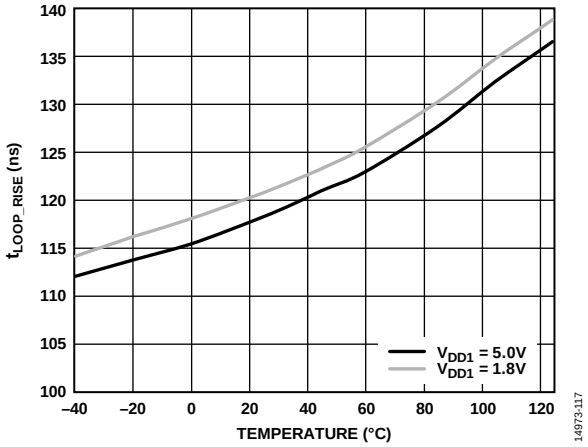

Figure 17. t_{LOOP_RISE} vs. Temperature (R_{SLOPE} = 0 Ω)

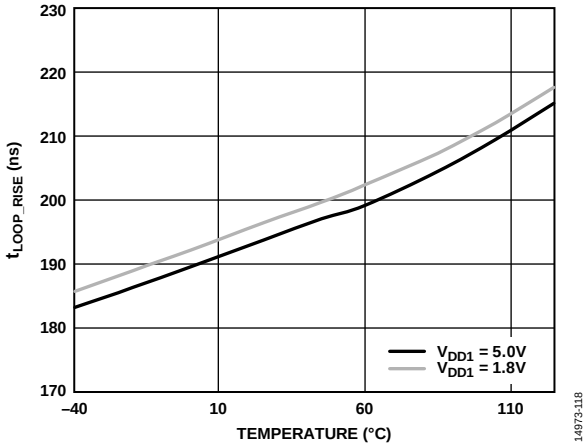

Figure 18. t_{LOOP_RISE} vs. Temperature (R_{SLOPE} = 47 kΩ)

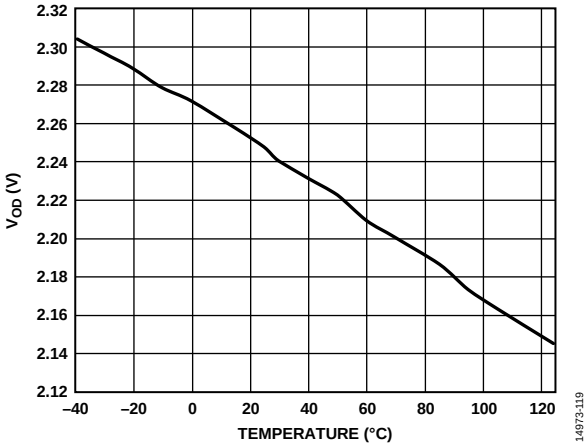

Figure 19. V_{OD} vs. Temperature

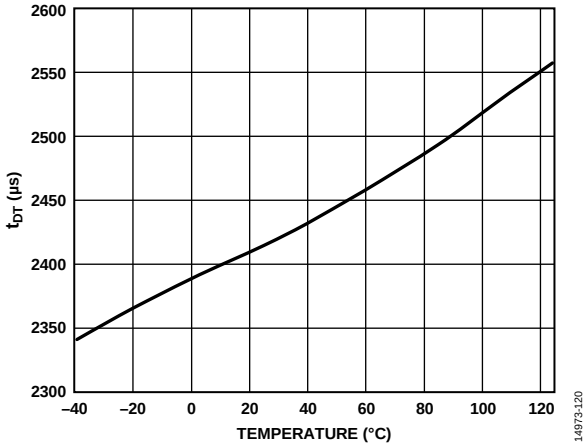

Figure 20. t_{DT} vs. Temperature

TEST CIRCUITS

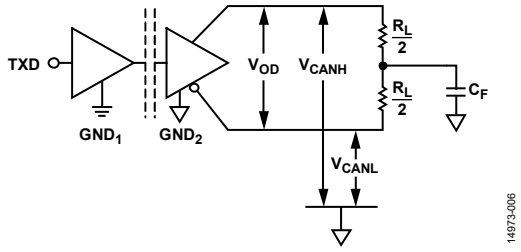

Figure 21. Driver Voltage Measurement

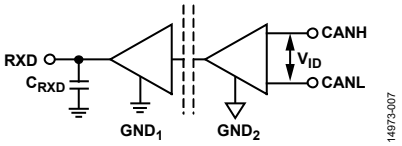

Figure 22. Receiver Voltage Measurement

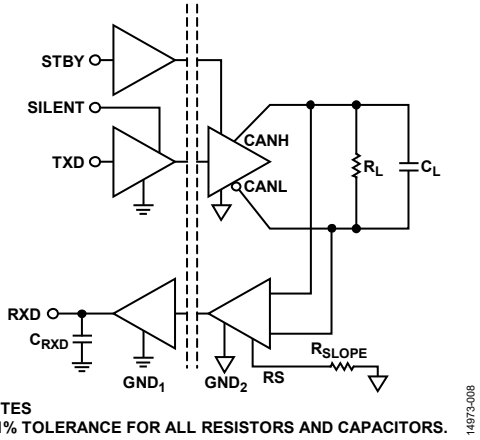

Figure 23. Switching Characteristics Measurements

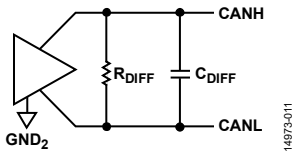

Figure 24. R_{DIFF} and C_{DIFF} Measured in Recessive State, Bus Disconnected

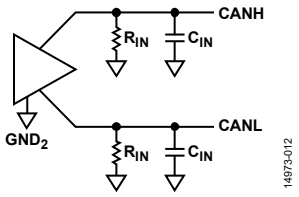

Figure 25. R_{IN} and C_{IN} Measured in Recessive State, Bus Disconnected

TERMINOLOGY

I_{DD1}
I_{DD1} is the current drawn by the V_{DD1} pin. This pin powers the logic side *i*Coupler digital isolator.

I_{DD2}
I_{DD2} is the current drawn by the V_{DD2} pin. This pin powers the bus side *i*Coupler digital isolator and transceiver.

V_{OD} and V_{ID}
V_{OD} and V_{ID} are the differential voltages from the transmitter or at the receiver on the CANH and CANL pins.

t_{TXD_DOM}
t_{TXD_DOM} is the propagation delay from a low signal on TXD to transition the bus to a dominant state. See Figure 2 for level definitions.

t_{TXD_REC}
t_{TXD_REC} is the propagation delay from a high signal on TXD to transition the bus to a recessive state. See Figure 2 for level definitions.

t_{LOOP_FALL}
t_{LOOP_FALL} is the propagation delay from a low signal on TXD to the bus dominant and transitions low on the RXD. See Figure 2 for level definitions.

t_{LOOP_RISE}
t_{LOOP_RISE} is the propagation delay from a high signal on TXD to the bus recessive and transitions high on the RXD. See Figure 2 for level definitions.

t_{BIT_TXD}
t_{BIT_TXD} is the bit time on the TXD pin as transmitted by the CAN controller. See Figure 2 for level definitions.

t_{BIT_BUS}
t_{BIT_BUS} is the bit time as transmitted by the transceiver to the bus. When compared with a given t_{BIT_TXD}, a measure of bit symmetry from the TXD digital isolation channel and CAN transceiver can be determined. See Figure 2 for level definitions.

t_{BIT_RXD}
t_{BIT_RXD} is the bit time on the RXD output pin, which can be compared with t_{BIT_TXD} for a round trip measure of pulse width distortion through the TXD digital isolation channel, the CAN transceiver, and back through the RXD isolation channel. See Figure 2 for level definitions.

Wake-Up Pattern
The wake-up pattern is the remote transmitted pattern required to trigger the low speed data transmission by the CAN transceiver while in standby mode. The pattern does not take the transceiver out of standby mode, and its effect on the transceiver times out. See Figure 4 for additional information.

THEORY OF OPERATION

CAN TRANSCEIVER OPERATION

The ADM3056E facilitates galvanically isolated communication between a CAN controller and the CAN bus. The CAN controller and the ADM3056E communicate with standard 1.8 V, 2.5 V, 3.3 V, or 5.0 V CMOS levels.

The CAN bus has two states: dominant and recessive. The recessive state is present on the bus when the differential voltage between CANH and CANL is less than 0.5 V. In the recessive state, the CANH and CANL pins are set to high impedance and are loosely biased to a single-ended voltage of 2.5 V. A dominant state is present on the bus when the differential voltage between CANH and CANL is greater than 1.5 V. The transceiver transmits a dominant state by driving the single-ended voltage of the CANH pin to 3.5 V and the CANL pin to 1.5 V. The recessive and dominant states correspond to CMOS high on the RXD pin and CMOS low on the TXD pin, respectively.

A dominant state from another node overwrites a recessive state on the bus. A CAN frame can be set for higher priority by using a longer string of dominant bits to gain control of the CAN bus during the arbitration phase. While transmitting, a CAN transceiver also reads back the state of the bus. When a CAN controller receives a dominant state while transmitting a recessive state during arbitration, the CAN controller surrenders the bus to the node still transmitting the dominant state. The node that gains control during the arbitration phase reads back only its own transmission. This interaction between recessive and dominant states allows competing nodes to negotiate for control of the bus while avoiding contention between nodes.

Industrial applications can have long cable runs. These long runs can have differences in local earth potential. Different sources may also power nodes. The ADM3056E transceiver has a ±25 V common-mode range (CMR) that exceeds the ISO 11898-2:2016 requirement and further increases the tolerance to ground variation.

See the AN-1123 Application Note for additional information on CAN.

SIGNAL ISOLATION

The ADM3056E device provides galvanic signal isolation implemented on the logic side of the interface. The RXD and TXD isolation channels transmit with an on off keying (OOK) architecture on *i*Coupler digital isolation technology.

The low propagation delay isolation, quick transceiver conversion speeds, and integrated form factor are critical for longer cable lengths and higher data speeds and reducing the total solution board space. The ADM3056E isolated transceiver reduces solution board space while increasing data transfer rates over discrete solutions.

The V_{DD1} pin powers the logic side signal isolation. The voltage on this pin scales the digital interface logic from 1.7 V to 5.5 V, depending on the supply voltage to the V_{DD1} pin.

TheV_{DD2} supply pin powers the bus side digital isolator and CAN transceiver and must be supplied with a nominal 5 V supply.

STANDBY MODE

The STBY pin engages a reduced power standby mode that modifies the operation of both the CAN transceiver and digital isolation channels. Standby mode disables the TXD signal isolation channel and sets the transmitter output to a high impedance state loosely biased to GND_2. While in standby mode, the receiver filters bus data and responds only after the remote wake-up sequence is received.

When entering or exiting standby mode, the TXD input must be kept high and the RXD output must be ignored for the full t_{STBY_ON} and t_{STBY_OFF} times.

REMOTE WAKE UP

The ADM3056E responds to the remote wake-up sequence as defined in ISO 11898-2:2016. When the CAN transceiver is presented with the defined slow speed, high to low to high sequence within the low wake-up pattern detection reset time (t_{WUPR}), low speed data transmission is allowed.

Receipt of the remote wake-up pattern does not bring the ADM3056E out of standby mode. The ADM3056E STBY pin must be brought low externally to exit standby mode. After the ADM3056E receives the remote wake-up pattern, the transceiver continues to receive low speed data until standby mode is exited.

SILENT MODE

Asserting the SILENT pin disables the TXD digital isolation channel. Any inputs to the TXD pin are ignored in this mode, and the transceiver presents a recessive bus state. The operation of the RXD channel is unaffected. The RXD channel continues to output data received from the internal CAN transceiver monitoring the bus.

Silent mode is useful when paired with a CAN controller using automatic baud rate detection. A CAN controller must be set to the same data rate as all attached nodes. The CAN controller produces an error frame and ties up the bus with a dominant state when the received data rate is different from expected. Other CAN nodes then echo this error frame. While in silent mode, the error frames produced by the CAN controller are kept from interrupting bus traffic, and the controller can continue listening to bus traffic.

RS

The RS pin sets the transceiver in one of three different modes of operation: high speed, slope control, or standby. This pin cannot be left floating.

For high speed mode, connect the RS pin directly to GND_2. Ensure that the transition time of the CAN bus signals is as short as possible to allow higher speed signaling. A shielded cable is recommended to avoid electromagnetic interference (EMI) problems in high speed mode.

Slope control mode allows the use of unshielded twisted pair wires or parallel pair wires as bus lines. Slow the signal rise and fall transition times to reduce EMI and ringing in slope control mode. Adjust the rise and fall slopes by adding a resistor (R_{SLOPE}) connected from RS to GND_2. The slope is proportional to the current output at the RS pin.

The RS pin can also set the CAN transceiver to standby mode, which occurs when the pin is driven to a voltage above V_{STB}. In standby mode, high speed data is filtered, and the CANH and CANL lines are biased to GND_2.

The RS pin can only set the CAN transceiver to standby mode. The state of the RS pin does not modify the operation of digital isolation channels or the auxiliary channel.

AUXILIARY CHANNEL

The auxiliary channel is available for low speed data transmission at up to 20 kHz (or 40 kbps nonreturn-to-zero format) when STBY is not asserted. The data rate limit of the channel allows the data channel to be shared by the STBY signal.

In standby mode, or when STBY is driven high, the operation of the channel is modified to share the multiplexed signal path with the STBY signal (see Figure 1). The AUX_{OUT} pin remains latched in the state when STBY is asserted. Periodic pulses (<25 µs wide) are sent to indicate that the logic side is powered and remains in standby mode.

In applications where AUX_{OUT} may be shorted to GND_2 or V_{DD2}, add a series resistance to the output channel.

INTEGRATED AND CERTIFIED IEC EMC SOLUTION

Typically, designers must add protection against harsh operating environments while also making the device as small as possible. To reduce board space and the design effort needed to meet the system level ESD standards, the ADM3056E has robust protection circuitry on chip for the CANH and CANL pins.

FAULT PROTECTION

High voltage miswire events commonly occur when the system power supply is connected directly to the CANH and the CANL bus lines during assembly. Supplies may also be shorted by accidental damage to the fieldbus cables while the system is operating. Accounting for inductive kickback and switching effects, the ADM3056E isolated transceiver CAN bus lines are protected against these miswire or shorting events in systems with up to nominal 24 V supplies. The CANH and CANL signal lines can withstand a continuous supply short with respect to GND_2 or between the CAN bus lines without damage. This level of protection applies when the device is either powered or unpowered.

FAIL-SAFE FEATURES

In cases where the TXD input pin is allowed to float, to prevent bus traffic interruption, the TXD input channel has an internal pull-up to the V_{DD1} pin. The pull-up holds the transceiver in the recessive state.

The ADM3056E features a dominant timeout (t_{DT} in Table 2). A TXD line shorted to ground or malfunctioning CAN controller are examples of how a single node can indefinitely prevent further bus traffic. The dominant timeout limits how long the transceiver can transmit in the dominant state. When the TXD pin is presented with a logic high, normal TXD functionality is restored.

The t_{DT} minimum also inherently creates a minimum data rate. Under normal operation, the CAN protocol allows five consecutive bits of the same polarity before stuffing a bit of the opposite polarity into the transmitting bit sequence. When an error is detected, the CAN controller purposely violates the bit stuffing rules by producing six consecutive dominant bits. At any given data rate, the CAN controller must transmit as many as 11 consecutive dominant bits to effectively limit the ADM3056E minimum data rate to 9600 bps.

THERMAL SHUTDOWN

The ADM3056E contains thermal shutdown circuitry that protects the device from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. The circuitry disables the driver outputs when the die temperature reaches 175°C. When the die has cooled, the drivers are enabled again.

APPLICATIONS INFORMATION

RADIATED EMISSIONS AND PCB LAYOUT

The ADM3056E isolated CAN transceiver is designed to pass EN55022 Class B by 6 dB on a simple 2-layer PCB design. Stitching capacitance or surface-mount technology (SMT) safety capacitors are not required to meet this emissions level.

PCB LAYOUT

The ADM3056E digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 26). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. The recommended bypass capacitor value is between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 must also be considered, unless the ground pair on each package side is connected close to the package.

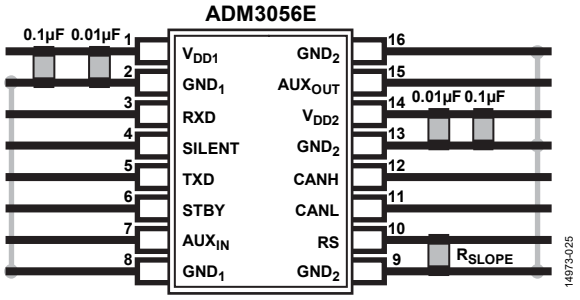

Figure 26. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this coupling can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

Note that the total lead length between the ends of the low equivalent series resistance (ESR) capacitor and the input power supply pin must not exceed 2 mm. Installing the bypass capacitor with traces more than 2 mm in length may result in data corruption.

THERMAL ANALYSIS

The ADM3056E consists of three internal die attached to a split lead frame with two die attach pads. For the purposes of thermal analysis, the die are treated as a thermal unit, with the highest junction temperature reflected in the θ_{JA} value from Table 8. The θ_{JA} value is based on measurements taken with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADM3056E can operate at full load across the full temperature range without derating the output current.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the ADM3056E isolator is presented in Table 3 for the 16-lead SOIC with increased creepage package.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling have shown that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as dc stress, which causes very little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are typically based on 60 Hz sinusoidal stress to reflect isolation from the line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as is shown in Equation 2. For insulation wear out with the polyimide materials used in these products, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\,RMS}{}^2 + V_{DC}{}^2} \quad (1)$$

or

$$V_{AC\,RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2} \quad (2)$$

where:
V_{RMS} is the total rms working voltage.
$V_{AC\,RMS}$ is the time varying portion of the working voltage.
V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V ac rms and a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance, and lifetime of a device, see Figure 27 and the following equations.

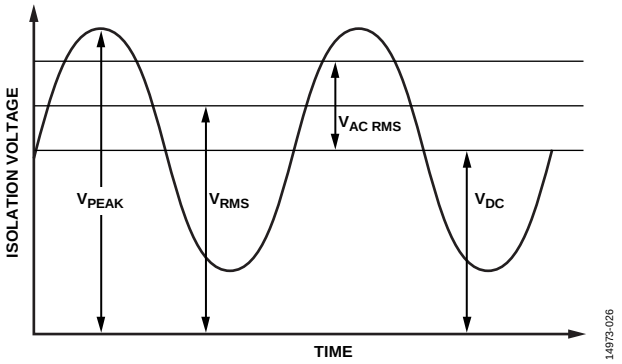

Figure 27. Critical Voltage Example

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\,RMS}{}^2 + V_{DC}{}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

$$V_{RMS} = 466 \text{ V}$$

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 2.

$$V_{AC\,RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2}$$

$$V_{AC\,RMS} = \sqrt{466^2 - 400^2}$$

$$V_{AC\,RMS} = 240 \text{ V rms}$$

In this case, the ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage in Table 9 for the SOIC_IC package, for the expected lifetime, which is less than a 60 Hz sine wave, and it is well within the limit for a 50-year service life.

Note that the dc working voltage limit is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.