

## FEATURES

Electronics industries alliance (EIA) RS-485/RS-422 compliant

Data rate options

**ADM4850/ADM4854:** 115 kbps

**ADM4851/ADM4855:** 500 kbps

**ADM4852/ADM4856:** 2.5 Mbps

**ADM4853/ADM4857:** 10 Mbps

Half-duplex and full duplex options

Reduced slew rates for low electromagnetic interference (EMI)

True fail-safe receiver inputs

5  $\mu$ A (maximum) supply current in shutdown mode

Up to 256 transceivers on one bus

Outputs high-Z when disabled or powered off

-7 V to +12 V bus common-mode range

Thermal shutdown and short-circuit protection

Pin-compatible with the MAX308x

Specified over the -40°C to +85°C temperature range

Available in 8-lead SOIC, 8-lead LFCSP, and 8-lead MSOP

Qualified for automotive applications

## APPLICATIONS

Low power RS-485 applications

EMI sensitive systems

DTE to DCE interfaces

Industrial control

Packet switching

Local area networks

Level translators

## GENERAL DESCRIPTION

The [ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857](#) are differential line transceivers suitable for high speed, half-duplex and full duplex data communication on multipoint bus transmission lines. They are designed for balanced data transmission and comply with EIA Standards RS-485 and RS-422. The [ADM4850/ADM4851/ADM4852/ADM4853](#) are half-duplex transceivers that share differential lines and have separate enable inputs for the driver and receiver. The full duplex [ADM4854/ADM4855/ADM4856/ADM4857](#) transceivers have dedicated differential line driver outputs and receiver inputs.

The devices have a 1/8-unit load receiver input impedance, which allows up to 256 transceivers on one bus. Because only one driver must be enabled at any time, the output of a disabled or powered down driver is three-stated to avoid overloading the bus. The receiver inputs have a true fail-safe feature, which ensures a logic high output level when the inputs are open or shorted.

Rev. F

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## FUNCTIONAL BLOCK DIAGRAMS

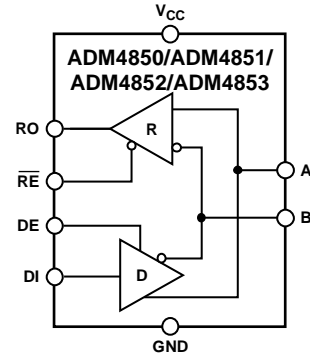


Figure 1. [ADM4850/ADM4851/ADM4852/ADM4853](#) Functional Block Diagram

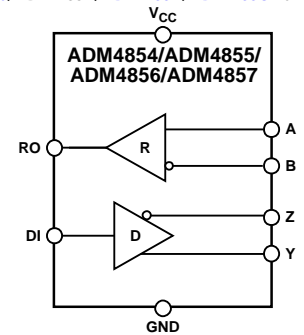


Figure 2. [ADM4854/ADM4855/ADM4856/ADM4857](#) Functional Block Diagram

This guarantees that the receiver outputs are in a known state before communication begins and when communication ends. The driver outputs are slew rate limited to reduce EMI and data errors caused by reflections from improperly terminated buses. Excessive power dissipation caused by bus contention or by output shorting is prevented with a thermal shutdown circuit. The devices are fully specified over the commercial and industrial temperature ranges and are available in 8-lead SOIC ([ADM4850](#) through [ADM4857](#)), 8-lead LFCSP ([ADM4850/ADM4852/ADM4853](#)), and 8-lead MSOP ([ADM4850](#) only) packages.

Table 1. Selection Table

Device No.	Half-Duplex/Full Duplex	Data Rate
<a href="#">ADM4850</a>	Half	115 kbps
<a href="#">ADM4851</a>	Half	500 kbps
<a href="#">ADM4852</a>	Half	2.5 Mbps
<a href="#">ADM4853</a>	Half	10 Mbps
<a href="#">ADM4854</a>	Full	115 kbps
<a href="#">ADM4855</a>	Full	500 kbps
<a href="#">ADM4856</a>	Full	2.5 Mbps
<a href="#">ADM4857</a>	Full	10 Mbps

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**REVISION HISTORY**

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Added Figure 6, Renumbered Sequentially ..... 8

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Changes to Table 3 and Table 4 ..... 4

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Changes to Table 7 ..... 6

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**10/04—Revision 0: Initial Version**

## SPECIFICATIONS

$V_{CC} = 5\text{ V} \pm 5\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 2.

Parameter		Min	Typ	Max	Unit	Test Conditions/Comments
<b>DRIVER</b>						
Differential Output Voltage	$V_{OD}$			$V_{CC}$	V	$R = \infty$ , see Figure 19 <sup>1</sup>
		2.0		5	V	$R = 50\ \Omega$ (RS-422), see Figure 19
		1.5		5	V	$R = 27\ \Omega$ (RS-485), see Figure 19
Differential Output Voltage over Common-Mode Range	$ V_{OD3} $	1.5		5	V	$V_{TST} = -7\text{ V to } +12\text{ V}$ , see Figure 20
$\Delta V_{OD} $ for Complementary Output States				0.2	V	$R = 27\ \Omega$ or $50\ \Omega$ , see Figure 19
Common-Mode Output Voltage	$V_{OC}$			3	V	$R = 27\ \Omega$ or $50\ \Omega$ , see Figure 19
$\Delta V_{OC} $ for Complementary Output States				0.2	V	$R = 27\ \Omega$ or $50\ \Omega$ , see Figure 19
Output Short-Circuit Current						$-7\text{ V} < V_{OUT} < +12\text{ V}$
$V_{OUT} = \text{High}$		-200		+200	mA	
$V_{OUT} = \text{Low}$		-200		+200	mA	
<b>DRIVER INPUT LOGIC</b>						
CMOS Input Logic Threshold						
Low				0.8	V	
High		2.0			V	
CMOS Logic Input Current (DI)				$\pm 1$	$\mu\text{A}$	
DE Input Resistance to GND			220		k $\Omega$	
<b>RECEIVER</b>						
Differential Input Threshold Voltage	$V_{TH}$	-200	-125	-30	mV	$-7\text{ V} < V_{OC} < +12\text{ V}$
Input Hysteresis			20		mV	$-7\text{ V} < V_{OC} < +12\text{ V}$
Input Resistance (A, B)		96	150		k $\Omega$	$-7\text{ V} < V_{OC} < +12\text{ V}$
Input Current (A, B)				0.125	mA	$V_{IN} = 12\text{ V}$
				-0.1	mA	$V_{IN} = -7\text{ V}$
CMOS Logic Input Current ( $\overline{RE}$ )				$\pm 1$	$\mu\text{A}$	
CMOS Output Voltage						
Low				0.4	V	$I_{OUT} = 4\text{ mA}$
High		4.0			V	$I_{OUT} = -4\text{ mA}$
Output Short-Circuit Current		7		85	mA	$V_{OUT} = \text{GND or } V_{CC}$
Three-State Output Leakage Current				$\pm 2$	$\mu\text{A}$	$0.4\text{ V} \leq V_{OUT} \leq 2.4\text{ V}$
<b>POWER SUPPLY CURRENT</b>						
115 kbps Options (ADM4850/ADM4854)				5	$\mu\text{A}$	$DE = 0\text{ V}, \overline{RE} = V_{CC}$ (shutdown)
			36	60	$\mu\text{A}$	$DE = 0\text{ V}, \overline{RE} = 0\text{ V}$
			100	160	$\mu\text{A}$	$DE = V_{CC}$
500 kbps Options (ADM4855)				5	$\mu\text{A}$	$DE = 0\text{ V}, \overline{RE} = V_{CC}$ (shutdown)
			80	120	$\mu\text{A}$	$DE = 0\text{ V}, \overline{RE} = 0\text{ V}$
			120	200	$\mu\text{A}$	$DE = V_{CC}$
2.5 Mbps Options (ADM4852/ADM4856)				5	$\mu\text{A}$	$DE = 0\text{ V}, \overline{RE} = V_{CC}$ (shutdown)
			250	400	$\mu\text{A}$	$DE = 0\text{ V}, \overline{RE} = 0\text{ V}$
			320	500	$\mu\text{A}$	$DE = V_{CC}$
10 Mbps Options (ADM4853/ADM4857)				5	$\mu\text{A}$	$DE = 0\text{ V}, \overline{RE} = V_{CC}$ (shutdown)
			250	400	$\mu\text{A}$	$DE = 0\text{ V}, \overline{RE} = 0\text{ V}$
			320	500	$\mu\text{A}$	$DE = V_{CC}$

<sup>1</sup> Guaranteed by design.

## ADM4850/ADM4854 TIMING SPECIFICATIONS

$V_{CC} = 5\text{ V} \pm 5\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
<b>DRIVER</b>						
Maximum Data Rate		115			kbps	
Propagation Delay	$t_{PLH}, t_{PHL}$	600		2500	ns	$R_{LDIFF} = 54\ \Omega$ , $C_{L1} = C_{L2} = 100\text{ pF}$ , see Figure 21 and Figure 25
Skew	$t_{SKEW}$			70	ns	$R_{LDIFF} = 54\ \Omega$ , $C_{L1} = C_{L2} = 100\text{ pF}$ , see Figure 21 and Figure 25
Rise/Fall Times	$t_{R}, t_{F}$	600		2400	ns	$R_{LDIFF} = 54\ \Omega$ , $C_{L1} = C_{L2} = 100\text{ pF}$ , see Figure 21 and Figure 25
Enable Time	$t_{ZH}, t_{ZL}$			2000	ns	$R_L = 500\ \Omega$ , $C_L = 100\text{ pF}$ , see Figure 22 and Figure 27 (ADM4850 only)
Disable Time	$t_{LZ}, t_{HZ}$			2000	ns	$R_L = 500\ \Omega$ , $C_L = 15\text{ pF}$ , see Figure 22 and Figure 27 (ADM4850 only)
Enable Time from Shutdown			4000		ns	$R_L = 500\ \Omega$ , $C_L = 100\text{ pF}$ , see Figure 22 (ADM4850 only)
<b>RECEIVER</b>						
Propagation Delay	$t_{PLH}, t_{PHL}$	400		1000	ns	$C_L = 15\text{ pF}$ , see Figure 23 and Figure 26
Differential Skew	$t_{SKEW}$			255	ns	$C_L = 15\text{ pF}$ , see Figure 23 and Figure 26
Enable Time	$t_{ZH}, t_{ZL}$		5	50	ns	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , see Figure 24 and Figure 28 (ADM4850 only)
Disable Time	$t_{LZ}, t_{HZ}$		20	50	ns	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , see Figure 24 and Figure 28 (ADM4850 only)
Enable Time from Shutdown			4000		ns	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , see Figure 24 (ADM4850 only)
Time to Shutdown		50	330	3000	ns	ADM4850 only <sup>1</sup>

<sup>1</sup> The half-duplex device is put into shutdown mode by driving  $\overline{RE}$  high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

## ADM4851/ADM4855 TIMING SPECIFICATIONS

$V_{CC} = 5\text{ V} \pm 5\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
<b>DRIVER</b>						
Maximum Data Rate		500			kbps	
Propagation Delay	$t_{PLH}, t_{PHL}$	250		600	ns	$R_{LDIFF} = 54\ \Omega$ , $C_{L1} = C_{L2} = 100\text{ pF}$ , see Figure 21 and Figure 25
Skew	$t_{SKEW}$			40	ns	$R_{LDIFF} = 54\ \Omega$ , $C_{L1} = C_{L2} = 100\text{ pF}$ , see Figure 21 and Figure 25
Rise/Fall Times	$t_{R}, t_{F}$	200		600	ns	$R_{LDIFF} = 54\ \Omega$ , $C_{L1} = C_{L2} = 100\text{ pF}$ , see Figure 21 and Figure 25
Enable Time	$t_{ZH}, t_{ZL}$			1000	ns	$R_L = 500\ \Omega$ , $C_L = 100\text{ pF}$ , see Figure 22 and Figure 27 (ADM4851 only)
Disable Time	$t_{LZ}, t_{HZ}$			1000	ns	$R_L = 500\ \Omega$ , $C_L = 100\text{ pF}$ , see Figure 22 and Figure 27 (ADM4851 only)
Enable Time from Shutdown			4000		ns	$R_L = 500\ \Omega$ , $C_L = 100\text{ pF}$ , see Figure 22 (ADM4851 only)
<b>RECEIVER</b>						
Propagation Delay	$t_{PLH}, t_{PHL}$	400		1000	ns	$C_L = 15\text{ pF}$ , see Figure 23 and Figure 26
Differential Skew	$t_{SKEW}$			250	ns	$C_L = 15\text{ pF}$ , see Figure 23 and Figure 26
Enable Time	$t_{ZH}, t_{ZL}$		5	50	ns	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , see Figure 24 and Figure 28 (ADM4851 only)
Disable Time	$t_{LZ}, t_{HZ}$		20	50	ns	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , see Figure 24 and Figure 28 (ADM4851 only)
Enable Time from Shutdown			4000		ns	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , see Figure 24 (ADM4851 only)
Time to Shutdown		50	330	3000	ns	ADM4851 only <sup>1</sup>

<sup>1</sup> The half-duplex device is put into shutdown mode by driving  $\overline{RE}$  high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

**ADM4852/ADM4856 TIMING SPECIFICATIONS**

$V_{CC} = 5\text{ V} \pm 5\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
<b>DRIVER</b>						
Maximum Data Rate		2.5			Mbps	
Propagation Delay	$t_{PLH}, t_{PHL}$	50		180	ns	$R_{LDIFF} = 54\ \Omega, C_{L1} = C_{L2} = 100\text{ pF}$ , see Figure 21 and Figure 25
Skew	$t_{SKEW}$			50	ns	$R_{LDIFF} = 54\ \Omega, C_{L1} = C_{L2} = 100\text{ pF}$ , see Figure 21 and Figure 25
Rise/Fall Times	$t_R, t_F$			140	ns	$R_{LDIFF} = 54\ \Omega, C_{L1} = C_{L2} = 100\text{ pF}$ , see Figure 21 and Figure 25
Enable Time	$t_{ZH}, t_{ZL}$			180	ns	$R_L = 500\ \Omega, C_L = 100\text{ pF}$ , see Figure 22 and Figure 27 (ADM4852 only)
Disable Time	$t_{LZ}, t_{HZ}$			180	ns	$R_L = 500\ \Omega, C_L = 100\text{ pF}$ , see Figure 22 and Figure 27 (ADM4852 only)
Enable Time from Shutdown			4000		ns	$R_L = 500\ \Omega, C_L = 100\text{ pF}$ , see Figure 22 (ADM4852 only)
<b>RECEIVER</b>						
Propagation Delay	$t_{PLH}, t_{PHL}$	55		190	ns	$C_L = 15\text{ pF}$ , see Figure 23 and Figure 26
Differential Skew	$t_{SKEW}$			50	ns	$C_L = 15\text{ pF}$ , see Figure 23 and Figure 26
Enable Time	$t_{ZH}, t_{ZL}$		5	50	ns	$R_L = 1\text{ k}\Omega, C_L = 15\text{ pF}$ , see Figure 24 and Figure 28 (ADM4852 only)
Disable Time	$t_{LZ}, t_{HZ}$		20	50	ns	$R_L = 1\text{ k}\Omega, C_L = 15\text{ pF}$ , see Figure 24 and Figure 28 (ADM4852 only)
Enable Time from Shutdown			4000		ns	$R_L = 1\text{ k}\Omega, C_L = 15\text{ pF}$ , see Figure 24 (ADM4852 only)
Time to Shutdown		50	330	3000	ns	ADM4852 only <sup>1</sup>

<sup>1</sup> The half-duplex device is put into shutdown mode by driving  $\overline{RE}$  high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

**ADM4853/ADM4857 TIMING SPECIFICATIONS**

$V_{CC} = 5\text{ V} \pm 5\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
<b>DRIVER</b>						
Maximum Data Rate		10			Mbps	
Propagation Delay	$t_{PLH}, t_{PHL}$	0		30	ns	$R_{LDIFF} = 54\ \Omega, C_{L1} = C_{L2} = 100\text{ pF}$ , see Figure 21 and Figure 25
Skew	$t_{SKEW}$			10	ns	$R_{LDIFF} = 54\ \Omega, C_{L1} = C_{L2} = 100\text{ pF}$ , see Figure 21 and Figure 25
Rise/Fall Times	$t_R, t_F$			30	ns	$R_{LDIFF} = 54\ \Omega, C_{L1} = C_{L2} = 100\text{ pF}$ , see Figure 21 and Figure 25
Enable Time	$t_{ZH}, t_{ZL}$			35	ns	$R_L = 500\ \Omega, C_L = 100\text{ pF}$ , see Figure 22 and Figure 27 (ADM4853 only)
Disable Time	$t_{LZ}, t_{HZ}$			35	ns	$R_L = 500\ \Omega, C_L = 100\text{ pF}$ , see Figure 22 and Figure 27 (ADM4853 only)
Enable Time from Shutdown			4000		ns	$R_L = 500\ \Omega, C_L = 100\text{ pF}$ , see Figure 22 (ADM4853 only)
<b>RECEIVER</b>						
Propagation Delay	$t_{PLH}, t_{PHL}$	55		190	ns	$C_L = 15\text{ pF}$ , see Figure 23 and Figure 26
Differential Skew	$t_{SKEW}$			30	ns	$C_L = 15\text{ pF}$ , see Figure 23 and Figure 26
Enable Time	$t_{ZH}, t_{ZL}$		5	50	ns	$R_L = 1\text{ k}\Omega, C_L = 15\text{ pF}$ , see Figure 24 and Figure 28 (ADM4853 only)
Disable Time	$t_{LZ}, t_{HZ}$		20	50	ns	$R_L = 1\text{ k}\Omega, C_L = 15\text{ pF}$ , see Figure 24 and Figure 28 (ADM4853 only)
Enable Time from Shutdown			4000		ns	$R_L = 1\text{ k}\Omega, C_L = 15\text{ pF}$ , see Figure 24 (ADM4853 only)
Time to Shutdown		50	330	3000	ns	ADM4853 only <sup>1</sup>

<sup>1</sup> The half-duplex device is put into shutdown mode by driving  $\overline{RE}$  high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

## ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
$V_{CC}$ to GND	6 V
Digital Input/Output Voltage (DE, $\overline{RE}$ , DI, RO)	-0.3 V to $V_{CC} + 0.3$ V
Driver Output/Receiver Input Voltage	-9 V to +14 V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +125°C
$\theta_{JA}$ Thermal Impedance	
8-Lead SOIC	110°C/W
8-Lead LFCSP	62°C/W
8-Lead MSOP	133.1°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

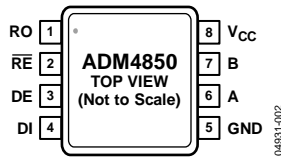


Figure 3. ADM4850, 8-Lead MSOP, Pin Configuration

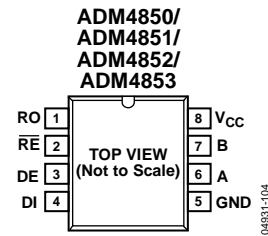
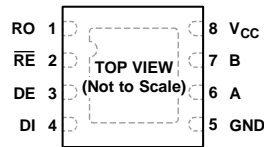


Figure 4. ADM4850/ADM4851/ADM4852/ADM4853, 8-Lead SOIC, Pin Configuration

Table 8. ADM4850/ADM4851/ADM4852/ADM4853, 8-Lead MSOP and 8-Lead SOIC, Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output. When RO is enabled and $(A - B) \geq -30$ mV, RO is high. When RO is enabled and $(A - B) \leq -200$ mV, RO is low.
2	$\overline{RE}$	Receiver Output Enable. A low level on $\overline{RE}$ enables the receiver output (RO). A high level on $\overline{RE}$ places RO into a high impedance state.
3	DE	Driver Output Enable. A high level on DE enables the driver differential outputs (A and B). A low level on DE places the driver differential outputs into a high impedance state.
4	DI	Driver Input. When the driver is enabled, a logic low on DI forces A low and B high, whereas a logic high on DI forces A high and B low.
5	GND	Ground.
6	A	Noninverting Receiver Input A/Noninverting Driver Output A.
7	B	Inverting Receiver Input B/Inverting Driver Output B.
8	$V_{CC}$	5 V Power Supply.

### ADM4850/ADM4852/ADM4853



#### NOTES

1. THE EXPOSED PADDLE ON THE UNDERSIDE OF THE PACKAGE SHOULD BE SOLDERED TO THE GROUND PLANE TO INCREASE THE RELIABILITY OF THE SOLDER JOINTS AND TO MAXIMIZE THE THERMAL CAPABILITY OF THE PACKAGE.

04831-029

Figure 5. ADM4850/ADM4852/ADM4853, 8-Lead LFCSP, Pin Configuration

Table 9. ADM4850/ADM4852/ADM4853, 8-Lead LFCSP, Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output. When RO is enabled and $(A - B) \geq -30$ mV, RO is high. When RO is enabled and $(A - B) \leq -200$ mV, RO is low.
2	$\overline{RE}$	Receiver Output Enable. A low level on $\overline{RE}$ enables the receiver output (RO). A high level on $\overline{RE}$ places RO into a high impedance state.
3	DE	Driver Output Enable. A high level on DE enables the driver differential outputs (A and B). A low level places the driver differential outputs into a high impedance state.
4	DI	Driver Input. When the driver is enabled, a logic low on DI forces A low and B high, whereas a logic high on DI forces A high and B low.
5	GND	Ground.
6	A	Noninverting Receiver Input A/Noninverting Driver Output A.
7	B	Inverting Receiver Input B/Inverting Driver Output B.
8	$V_{CC}$ EPAD	5 V Power Supply. Exposed Pad. The exposed paddle on the underside of the package must be soldered to the ground plane to increase the reliability of the solder joints and to maximize the thermal capability of the package.

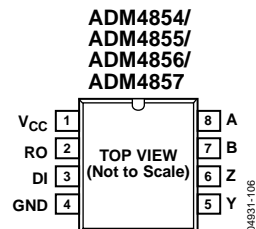


Figure 6. ADM4854/ADM4855/ADM4856/ADM4857, 8-Lead SOIC, Pin Configuration

Table 10. ADM4854/ADM4855/ADM4856/ADM4857, 8-Lead SOIC, Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{CC}$	5 V Power Supply.
2	RO	Receiver Output. When RO is enabled and $(A - B) \geq -30$ mV, RO is high. When RO is enabled and $(A - B) \leq -200$ mV, RO is low.
3	DI	Driver Input. When the driver is enabled, a logic low on DI forces Y low and Z high, whereas a logic high on DI forces Y high and Z low.
4	GND	Ground.
5	Y	Noninverting Driver Output.
6	Z	Inverting Driver Output.
7	B	Inverting Receiver Input.
8	A	Noninverting Receiver Input.



### TYPICAL PERFORMANCE CHARACTERISTICS

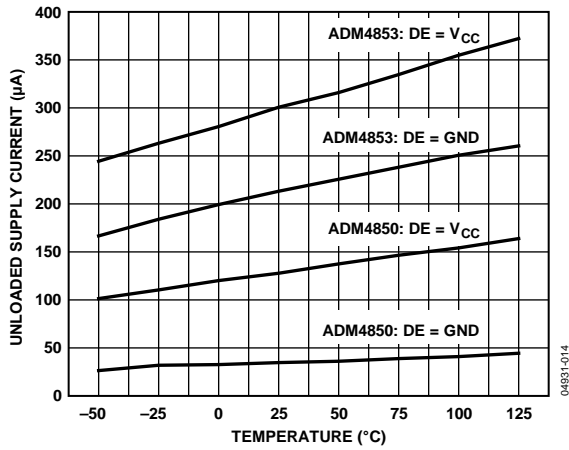


Figure 7. Unloaded Supply Current vs. Temperature (ADM4850/ADM4853)

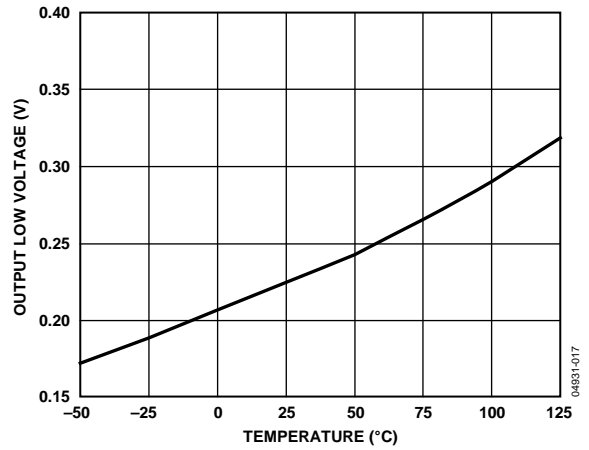


Figure 10. Receiver Output Low Voltage vs. Temperature

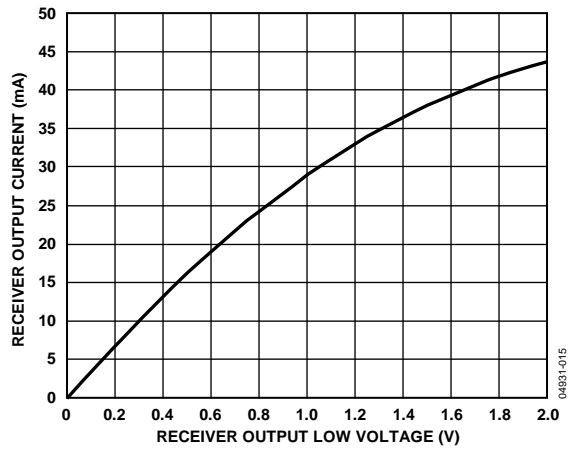


Figure 8. Receiver Output Current vs. Receiver Output Low Voltage

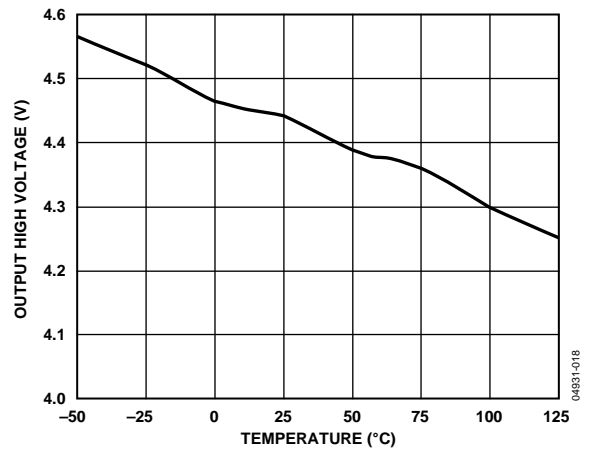


Figure 11. Receiver Output High Voltage vs. Temperature

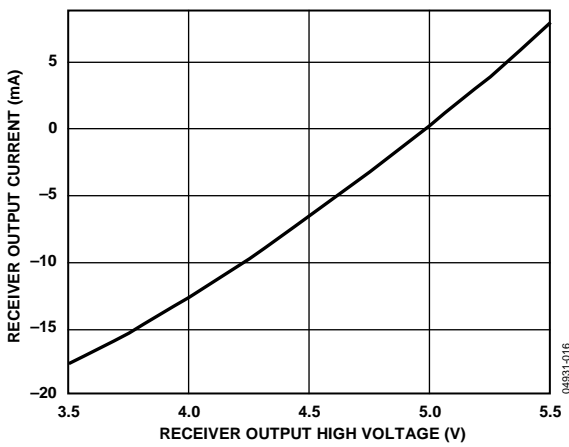


Figure 9. Receiver Output Current vs. Receiver Output High Voltage

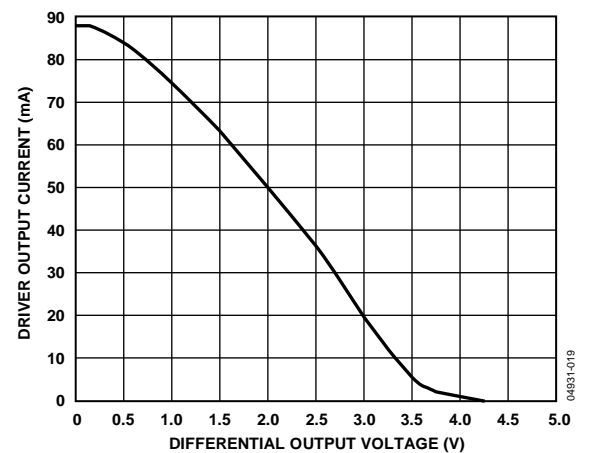


Figure 12. Driver Output Current vs. Differential Output Voltage

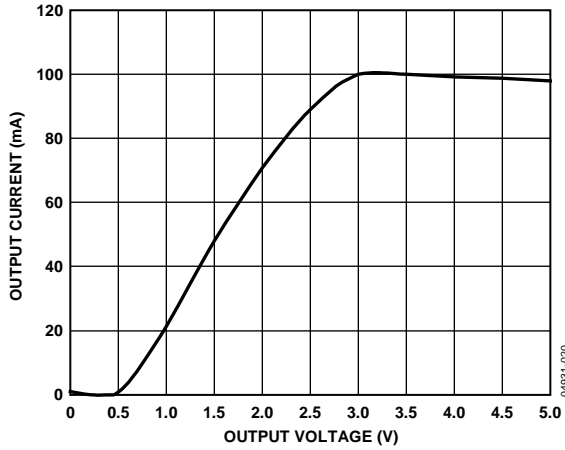


Figure 13. Output Current vs. Driver Output Low Voltage

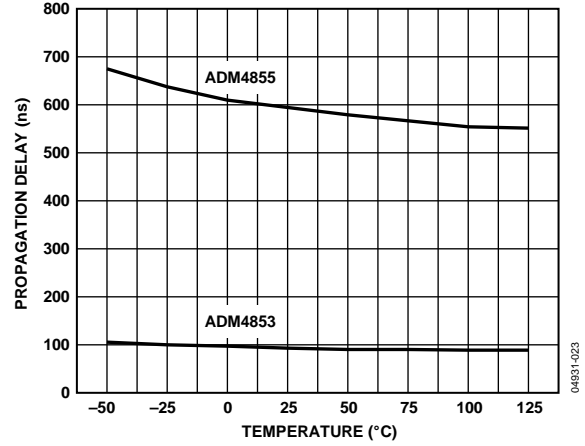


Figure 16. Receiver Propagation Delay vs. Temperature (ADM4853/ADM4855)

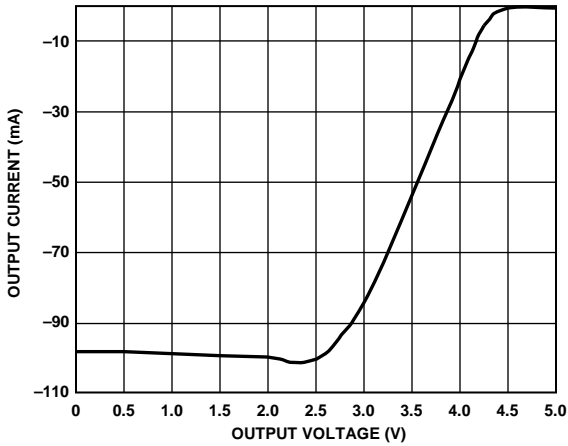


Figure 14. Output Current vs. Driver Output High Voltage

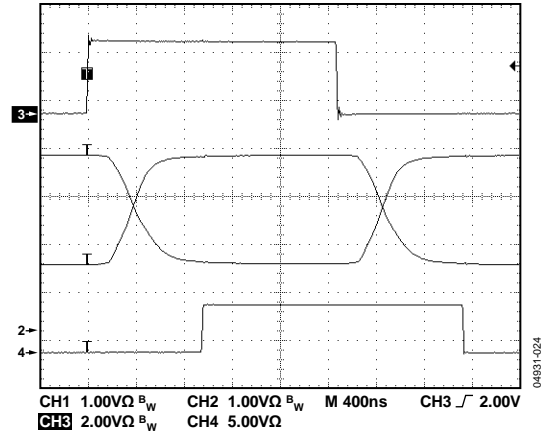


Figure 17. Driver/Receiver Propagation Delay (ADM4855, 500 kbps)

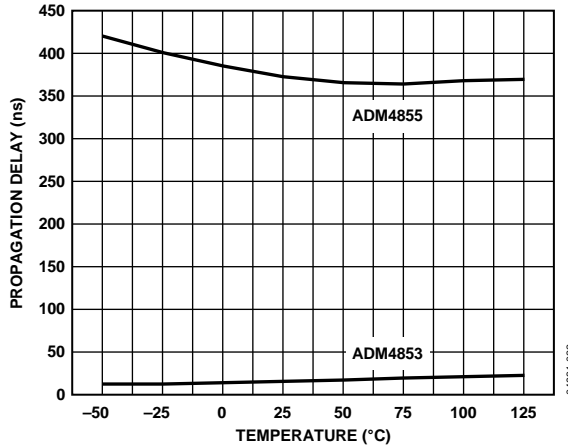


Figure 15. Driver Propagation Delay vs. Temperature (ADM4853/ADM4855)

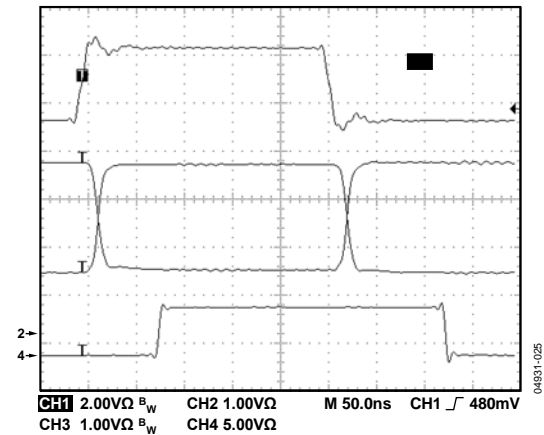


Figure 18. Driver/Receiver Propagation Delay (ADM4857, 4 Mbps)

TEST CIRCUITS

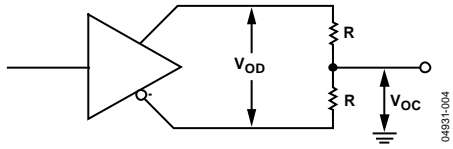


Figure 19. Driver Voltage Measurement

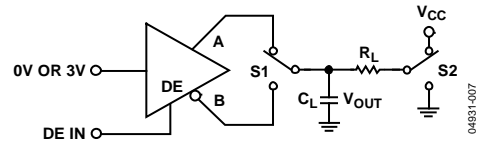


Figure 22. Driver Enable/Disable (ADM4850/ADM4852/ADM4853)

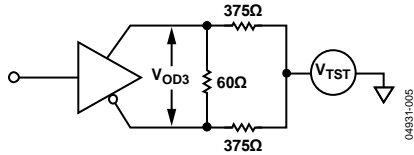


Figure 20. Driver Voltage Measurement over Common-Mode Voltage Range

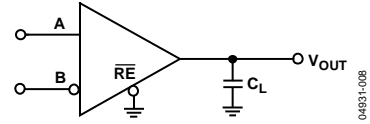


Figure 23. Receiver Propagation Delay

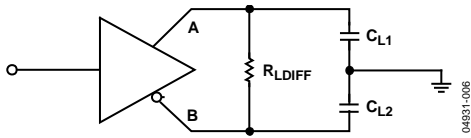


Figure 21. Driver Propagation Delay

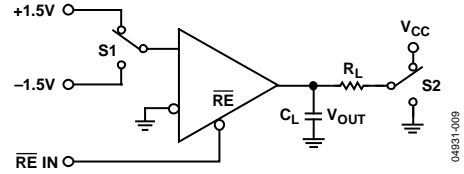


Figure 24. Receiver Enable/Disable (ADM4850/ADM4852/ADM4853)

### SWITCHING CHARACTERISTICS

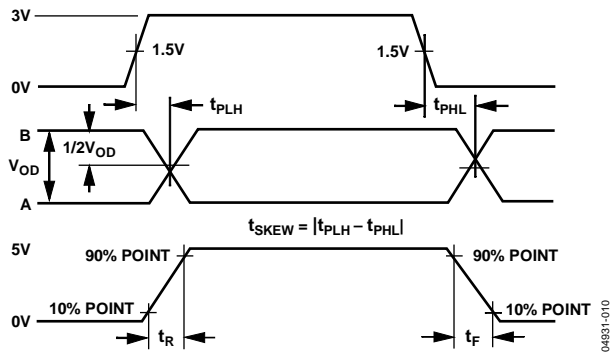


Figure 25. Driver Propagation Delay, Rise/Fall Timing

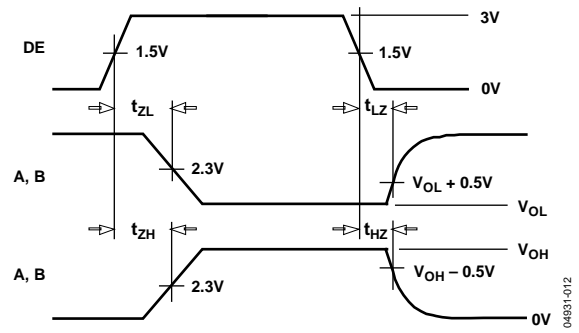


Figure 27. Driver Enable/Disable Timing

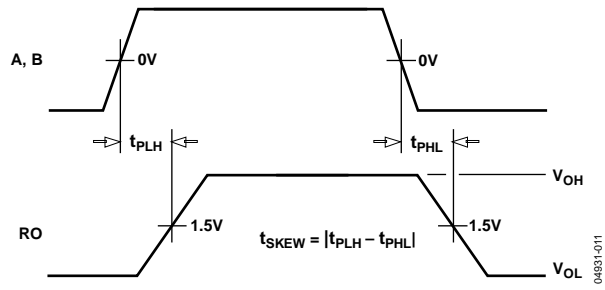


Figure 26. Receiver Propagation Delay

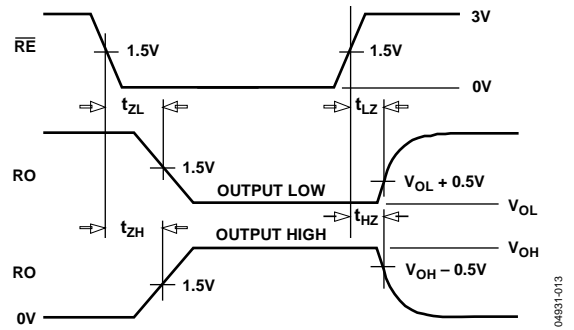


Figure 28. Receiver Enable/Disable Timing

## THEORY OF OPERATION

The [ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857](#) are high speed RS-485/RS-422 transceivers offering enhanced performance over industry-standard devices. All devices in the family contain one driver and one receiver but offer a choice of performance options. The devices feature true fail-safe operation, which guarantees a logic high receiver output when the receiver inputs are open circuit or short-circuit, or when they are connected to a terminated transmission line with all drivers disabled (see the Fail-Safe Operation section).

### SLEW RATE CONTROL

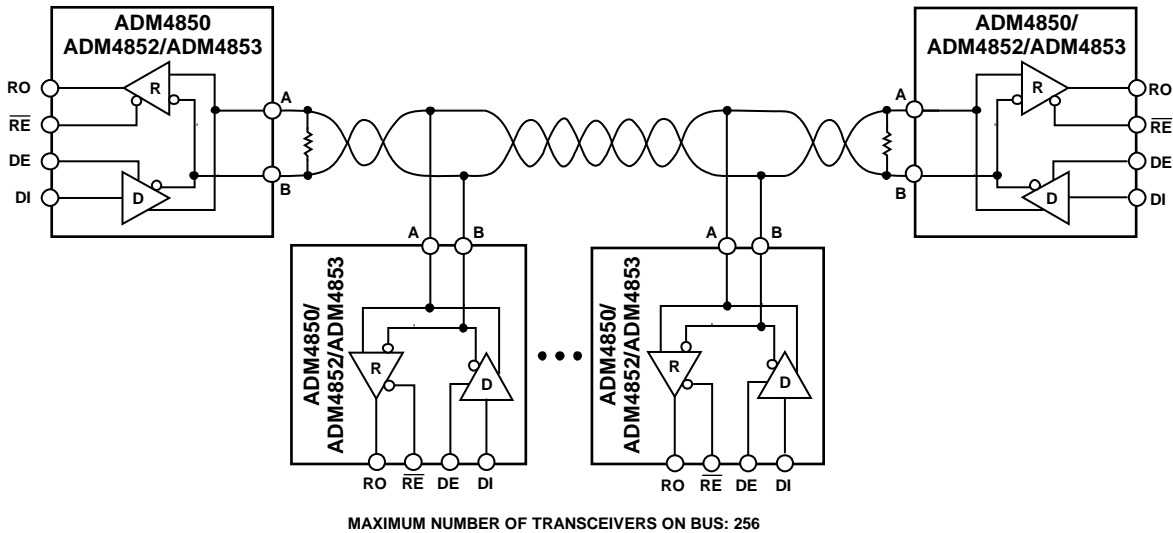
The [ADM4850](#) and [ADM4854](#) feature a controlled slew rate driver that minimizes EMI and reduces reflections caused by incorrectly terminated cables, allowing error free data transmission rates up to 115 kbps. The [ADM4851](#) and [ADM4855](#) offer a higher limit on driver output slew rate, allowing data transmission rates up to 500 kbps. The driver slew rates of the [ADM4852/ADM4856](#) and the [ADM4853/ADM4857](#) are not limited, offering data transmission rates up to 2.5 Mbps and 10 Mbps, respectively.

### RECEIVER INPUT FILTERING

The receivers of all the devices incorporate input hysteresis. In addition, the receivers of the 115 kbps [ADM4850](#) and [ADM4854](#) and the 500 kbps [ADM4851](#) and [ADM4855](#) incorporate input filtering, which enhances noise immunity with differential signals that have very slow rise and fall times. However, it causes the propagation delay to increase by 20%.

### HALF-DUPLEX/FULL DUPLEX OPERATION

Half-duplex operation implies that the transceiver can transmit and receive, but it can do only one of these at any given time. However, with full duplex operation, the transceiver can transmit and receive simultaneously. The [ADM4850/ADM4851/ADM4852/ADM4853](#) are half-duplex devices in which the driver and the receiver share differential bus terminals. The [ADM4854/ADM4855/ADM4856/ADM4857](#) are full duplex devices that have dedicated driver output and receiver input pins. Figure 29 and Figure 30 show typical half-duplex and full duplex topologies.



**NOTES**

1. THE ADM4851 IS A HALF-DUPLEX RS-485 TRANSCEIVER, BUT IT DOES NOT HAVE THE DRIVER ENABLE (DE) AND THE RECEIVER ENABLE ( $\overline{RE}$ ) PINS.

Figure 29. Typical Half-Duplex RS-485 Network Topology

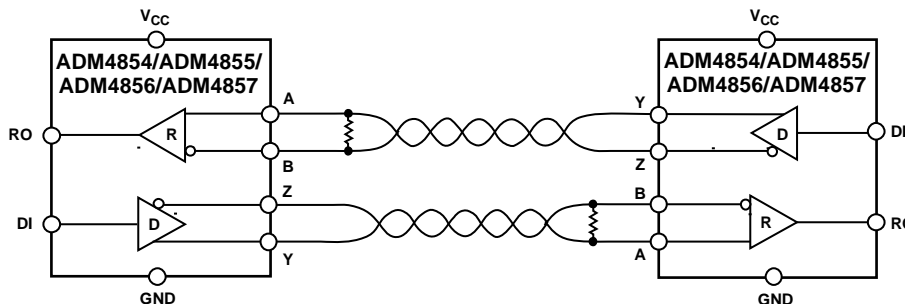


Figure 30. Typical Full Duplex Point-to-Point RS-485 Network Topology

### HIGH RECEIVER INPUT IMPEDANCE

The input impedance of the [ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857](#) receivers is 96 k $\Omega$ , which is eight times higher than the standard RS-485 unit load of 12 k $\Omega$ . This 96 k $\Omega$  impedance enables a standard driver to drive 32 unit loads or to be connected to 256 [ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857](#) receivers. An RS-485 bus, driven by a single standard driver, can be connected to a combination of [ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857](#) devices and standard unit load receivers, up to an equivalent of 32 standard unit loads.

### THREE-STATE BUS CONNECTION

The half-duplex devices ([ADM4850/ADM4852/ADM4853](#)) have a driver enable pin (DE) that enables the driver outputs when taken high, or puts the driver outputs into a high impedance state when taken low. Similarly, the half-duplex devices have an active low receiver enable pin (RE). Taking this pin low enables the receiver, whereas taking it high puts the receiver outputs into a high impedance state, which allows several driver outputs to be connected to an RS-485 bus. Note that only one driver must be enabled at a time, but that many receivers can be enabled.

### SHUTDOWN MODE

The [ADM4850/ADM4852/ADM4853](#) have a low power shutdown mode, which is enabled by taking  $\overline{\text{RE}}$  high and DE low. If shutdown mode is not used, the fact that DE is active high and  $\overline{\text{RE}}$  is active low offers a convenient way of switching the device between transmit and receive by tying DE and  $\overline{\text{RE}}$  together.

If DE is driven low and  $\overline{\text{RE}}$  is driven high for less than 50 ns, the devices are guaranteed not to enter shutdown mode. If DE is driven low and  $\overline{\text{RE}}$  is driven high for at least 3000 ns, the devices are guaranteed to enter shutdown mode.

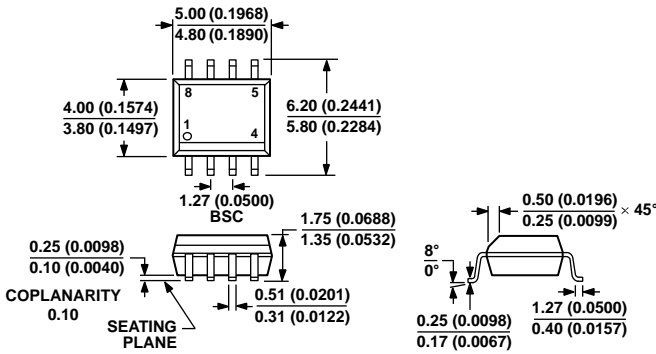
### FAIL-SAFE OPERATION

The [ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857](#) offer true fail-safe operation while remaining fully compliant with the  $\pm 200$  mV EIA/TIA-485 standard. A logic high receiver output generates when the receiver inputs are shorted together or open circuit, or when they are connected to a terminated transmission line with all drivers disabled. This logic high is done by setting the receiver threshold between  $-30$  mV and  $-200$  mV. If the differential receiver input voltage ( $A - B$ ) is greater than or equal to  $-30$  mV, RO is logic high. If ( $A - B$ ) is less than or equal to  $-200$  mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the differential input voltage of the receiver is pulled to 0 V by the internal circuitry of the [ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857](#), which results in a logic high with 30 mV minimum noise margin.

### CURRENT LIMIT AND THERMAL SHUTDOWN

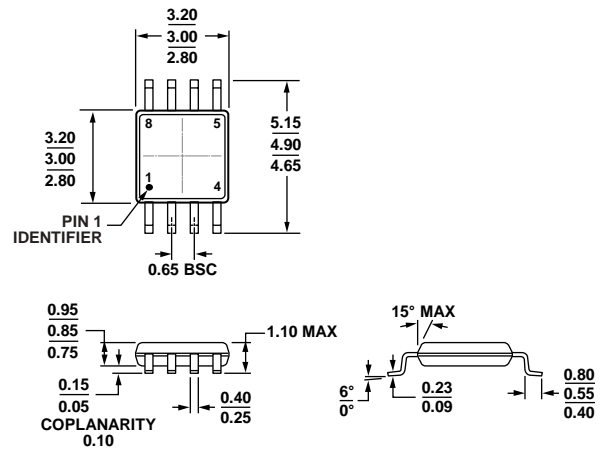
The [ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857](#) incorporate two protection mechanisms to guard the drivers against short circuits, bus contention, or other fault conditions. The first is a current limiting output stage, which protects the driver against short circuits over the entire common-mode voltage range by limiting the output current to approximately 70 mA. Under extreme fault conditions where the current limit is not effective, a thermal shutdown circuit puts the driver outputs into a high impedance state if the die temperature exceeds 150°C, and does not turn them back on until the temperature falls to 130°C.

# OUTLINE DIMENSIONS



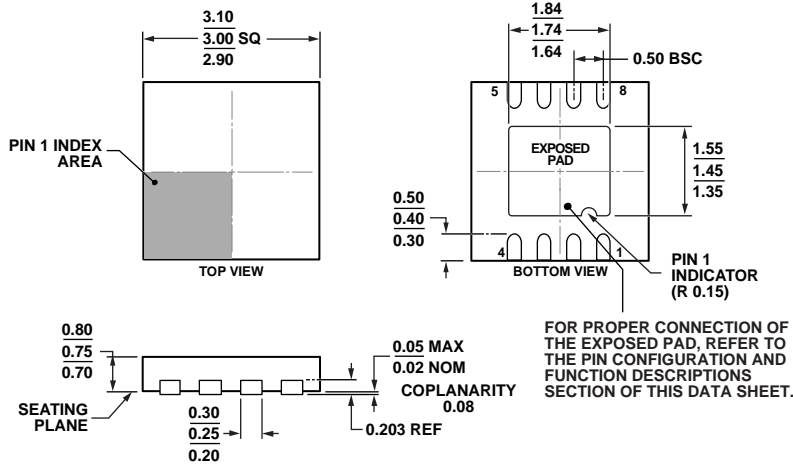
COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 31. 8-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-8)  
 Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 32. 8-Lead Mini Small Outline Package [MSOP] (RM-8)  
 Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-229-WEED

Figure 33. 8-Lead Lead Frame Chip Scale Package [LFCSP] 3 mm x 3 mm Body and 0.75 mm Package Height (CP-8-13)  
 Dimensions shown in millimeters