5 V, Slew Rate Limited, Half-Duplex and Full Duplex RS-485/RS-422 Transceivers

Data Sheet

ADM4850 to ADM4857

FEATURES

- Electronics industries alliance (EIA) RS-485/RS-422 compliant
- Data rate options
  - ADM4850/ADM4854: 115 kbps
  - ADM4851/ADM4855: 500 kbps
  - ADM4852/ADM4856: 2.5 Mbps
  - ADM4853/ADM4857: 10 Mbps
- Half-duplex and full duplex options
- Reduced slew rates for low electromagnetic interference (EMI)
- True fail-safe receiver inputs
- 5 µA (maximum) supply current in shutdown mode
- Up to 256 transceivers on one bus
- Outputs high-Z when disabled or powered off
- −7 V to +12 V bus common-mode range
- Thermal shutdown and short-circuit protection
- Pin-compatible with the MAX308x
- Specified over the −40°C to +85°C temperature range
- Available in 8-lead SOIC, 8-lead LFCSP, and 8-lead MSOP
- Qualified for automotive applications

APPLICATIONS

- Low power RS-485 applications
- EMI sensitive systems
- DTE to DCE interfaces
- Industrial control
- Packet switching
- Local area networks
- Level translators

GENERAL DESCRIPTION

The ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857 are differential line transceivers suitable for high speed, half-duplex and full duplex data communication on multipoint bus transmission lines. They are designed for balanced data transmission and comply with EIA Standards RS-485 and RS-422. The ADM4850/ADM4851/ADM4852/ADM4853 are half-duplex transceivers that share differential lines and have separate enable inputs for the driver and receiver. The full duplex ADM4854/ADM4855/ADM4856/ADM4857 transceivers have dedicated differential line driver outputs and receiver inputs.

The devices have a 1/8-unit load receiver input impedance, which allows up to 256 transceivers on one bus. Because only one driver must be enabled at any time, the output of a disabled or powered down driver is three-stated to avoid overloading the bus. The receiver inputs have a true fail-safe feature, which ensures a logic high output level when the inputs are open or shorted.

FUNCTIONAL BLOCK DIAGRAMS

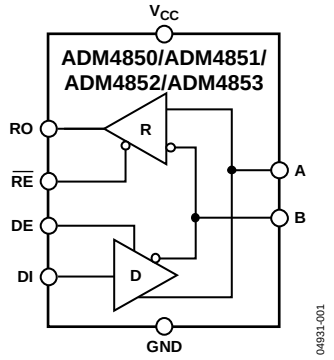

Figure 1. ADM4850/ADM4851/ADM4852/ADM4853 Functional Block Diagram

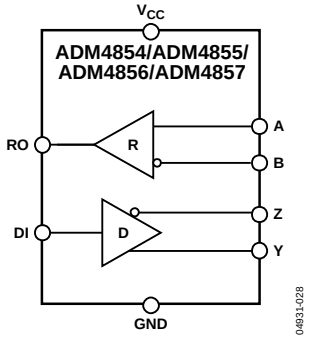

Figure 2. ADM4854/ADM4855/ADM4856/ADM4857 Functional Block Diagram

This guarantees that the receiver outputs are in a known state before communication begins and when communication ends. The driver outputs are slew rate limited to reduce EMI and data errors caused by reflections from improperly terminated buses. Excessive power dissipation caused by bus contention or by output shorting is prevented with a thermal shutdown circuit. The devices are fully specified over the commercial and industrial temperature ranges and are available in 8-lead SOIC (ADM4850 through ADM4857), 8-lead LFCSP (ADM4850/ADM4852/ADM4853), and 8-lead MSOP (ADM4850 only) packages.

Table 1. Selection Table

Device No.	Half-Duplex/Full Duplex	Data Rate
ADM4850	Half	115 kbps
ADM4851	Half	500 kbps
ADM4852	Half	2.5 Mbps
ADM4853	Half	10 Mbps
ADM4854	Full	115 kbps
ADM4855	Full	500 kbps
ADM4856	Full	2.5 Mbps
ADM4857	Full	10 Mbps

Rev. F

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagrams ... 1
Revision History ... 2
Specifications ... 3
ADM4850/ADM4854 Timing Specifications ... 4
ADM4851/ADM4855 Timing Specifications ... 4
ADM4852/ADM4856 Timing Specifications ... 5
ADM4853/ADM4857 Timing Specifications ... 5
Absolute Maximum Ratings ... 6
ESD Caution ... 6
Pin Configurations and Function Descriptions ... 7
Typical Performance Characteristics ... 9
Test Circuits ... 11
Switching Characteristics ... 12
Theory of Operation ... 13
Slew Rate Control ... 13
Receiver Input Filtering ... 13
Half-Duplex/Full Duplex Operation ... 13
High Receiver Input Impedance ... 14
Three-State Bus Connection ... 14
Shutdown Mode ... 14
Fail-Safe Operation ... 14
Current Limit and Thermal Shutdown ... 14
Outline Dimensions ... 15
Ordering Guide ... 16
Automotive Product ... 16

REVISION HISTORY

5/16—Rev. E to Rev. F

Changes to Figure 1 ... 1
Reformatted and Changes to Pin Configuration and Function Descriptions Section ... 7
Added Figure 6, Renumbered Sequentially ... 8

2/16—Rev. D to Rev. E

Changes to Figure 1 and General Description Section ... 1
Changes to Table 2 ... 3
Changes to Table 3 and Table 4 ... 4
Changes to Table 5 and Table 6 ... 5
Changes to Figure 3, Figure 4, and Table 8 Caption ... 7
Added Table 9; Renumbered Sequentially ... 7
Changes to Figure 5 and Table 10 Caption ... 8
Changes to Figure 6 Caption ... 9
Changes to Figure 14 Caption and Figure 15 Caption ... 10
Changes to Figure 21 Caption and Figure 23 Caption ... 11
Changed Circuit Description Section to Theory of Operation Section ... 13
Changes to Figure 28 ... 13
Changes to the Three-State Bus Connection Section and the Shutdown Mode Section ... 14
Updated Outline Dimensions ... 15
Changes to Ordering Guide ... 16

1/12—Rev. C to Rev. D

Change to Features Section ... 1
Changes to Ordering Guide ... 15
Added Automotive Products Section ... 15

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Change to Table 8, Pin 3 Description ... 7
Changes to Figure 29 ... 12
Changes to Ordering Guide ... 15

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Changes to Table 2 ... 3
Changes to Table 7 ... 6
Inserted Figure 4; Renumbered Sequentially ... 7
Moved Typical Performance Characteristics Section ... 8
Changes to Figure 24 and Figure 27 ... 11
Changes to Figure 29 ... 12
Change to Shutdown Mode Section ... 13
Updated Outline Dimensions ... 14
Changes to Ordering Guide ... 15

4/09—Rev. 0 to Rev. A

Changes to Ordering Guide ... 15

10/04—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter		Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Differential Output Voltage	V_{OD}			V_{CC}	V	R = ∞, see Figure 19[1]
		2.0		5	V	R = 50 Ω (RS-422), see Figure 19
		1.5		5	V	R = 27 Ω (RS-485), see Figure 19
Differential Output Voltage over Common-Mode Range	$\|V_{OD3}\|$	1.5		5	V	V_{TST} = −7 V to +12 V, see Figure 20
$\Delta\|V_{OD}\|$ for Complementary Output States				0.2	V	R = 27 Ω or 50 Ω, see Figure 19
Common-Mode Output Voltage	V_{OC}			3	V	R = 27 Ω or 50 Ω, see Figure 19
$\Delta\|V_{OC}\|$ for Complementary Output States				0.2	V	R = 27 Ω or 50 Ω, see Figure 19
Output Short-Circuit Current						−7 V < V_{OUT} < +12 V
V_{OUT} = High		−200		+200	mA	
V_{OUT} = Low		−200		+200	mA	
DRIVER INPUT LOGIC						
CMOS Input Logic Threshold						
Low				0.8	V	
High		2.0			V	
CMOS Logic Input Current (DI)				±1	μA	
DE Input Resistance to GND			220		kΩ	
RECEIVER						
Differential Input Threshold Voltage	V_{TH}	−200	−125	−30	mV	−7 V < V_{OC} < +12 V
Input Hysteresis			20		mV	−7 V < V_{OC} < +12 V
Input Resistance (A, B)		96	150		kΩ	−7 V < V_{OC} < +12 V
Input Current (A, B)				0.125	mA	V_{IN} = 12 V
				−0.1	mA	V_{IN} = −7 V
CMOS Logic Input Current ($\overline{RE}$)				±1	μA	
CMOS Output Voltage						
Low				0.4	V	I_{OUT} = 4 mA
High		4.0			V	I_{OUT} = −4 mA
Output Short-Circuit Current		7		85	mA	V_{OUT} = GND or V_{CC}
Three-State Output Leakage Current				±2	μA	0.4 V ≤ V_{OUT} ≤ 2.4 V
POWER SUPPLY CURRENT						
115 kbps Options (ADM4850/ADM4854)				5	μA	DE = 0 V, $\overline{RE}$ = V_{CC} (shutdown)
			36	60	μA	DE = 0 V, $\overline{RE}$ = 0 V
			100	160	μA	DE = V_{CC}
500 kbps Options (ADM4855)				5	μA	DE = 0 V, $\overline{RE}$ = V_{CC} (shutdown)
			80	120	μA	DE = 0 V, $\overline{RE}$ = 0 V
			120	200	μA	DE = V_{CC}
2.5 Mbps Options (ADM4852/ADM4856)				5	μA	DE = 0 V, $\overline{RE}$ = V_{CC} (shutdown)
			250	400	μA	DE = 0 V, $\overline{RE}$ = 0 V
			320	500	μA	DE = V_{CC}
10 Mbps Options (ADM4853/ADM4857)				5	μA	DE = 0 V, $\overline{RE}$ = V_{CC} (shutdown)
			250	400	μA	DE = 0 V, $\overline{RE}$ = 0 V
			320	500	μA	DE = V_{CC}

[1] Guaranteed by design.

ADM4850/ADM4854 TIMING SPECIFICATIONS

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate		115			kbps	
Propagation Delay	t_{PLH}, t_{PHL}	600		2500	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 21 and Figure 25
Skew	t_{SKEW}			70	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 21 and Figure 25
Rise/Fall Times	t_R, t_F	600		2400	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 21 and Figure 25
Enable Time	t_{ZH}, t_{ZL}			2000	ns	R_L = 500 Ω, C_L = 100 pF, see Figure 22 and Figure 27 (ADM4850 only)
Disable Time	t_{LZ}, t_{HZ}			2000	ns	R_L = 500 Ω, C_L = 15 pF, see Figure 22 and Figure 27 (ADM4850 only)
Enable Time from Shutdown			4000		ns	R_L = 500 Ω, C_L = 100 pF, see Figure 22 (ADM4850 only)
RECEIVER						
Propagation Delay	t_{PLH}, t_{PHL}	400		1000	ns	C_L = 15 pF, see Figure 23 and Figure 26
Differential Skew	t_{SKEW}			255	ns	C_L = 15 pF, see Figure 23 and Figure 26
Enable Time	t_{ZH}, t_{ZL}		5	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 and Figure 28 (ADM4850 only)
Disable Time	t_{LZ}, t_{HZ}		20	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 and Figure 28 (ADM4850 only)
Enable Time from Shutdown			4000		ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 (ADM4850 only)
Time to Shutdown		50	330	3000	ns	ADM4850 only[1]

[1] The half-duplex device is put into shutdown mode by driving $\overline{RE}$ high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

ADM4851/ADM4855 TIMING SPECIFICATIONS

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate		500			kbps	
Propagation Delay	t_{PLH}, t_{PHL}	250		600	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 21 and Figure 25
Skew	t_{SKEW}			40	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 21 and Figure 25
Rise/Fall Times	t_R, t_F	200		600	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 21 and Figure 25
Enable Time	t_{ZH}, t_{ZL}			1000	ns	R_L = 500 Ω, C_L = 100 pF, see Figure 22 and Figure 27 (ADM4851 only)
Disable Time	t_{LZ}, t_{HZ}			1000	ns	R_L = 500 Ω, C_L = 100 pF, see Figure 22 and Figure 27 (ADM4851 only)
Enable Time from Shutdown			4000		ns	R_L = 500 Ω, C_L = 100 pF, see Figure 22 (ADM4851 only)
RECEIVER						
Propagation Delay	t_{PLH}, t_{PHL}	400		1000	ns	C_L = 15 pF, see Figure 23 and Figure 26
Differential Skew	t_{SKEW}			250	ns	C_L = 15 pF, see Figure 23 and Figure 26
Enable Time	t_{ZH}, t_{ZL}		5	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 and Figure 28 (ADM4851 only)
Disable Time	t_{LZ}, t_{HZ}		20	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 and Figure 28 (ADM4851 only)
Enable Time from Shutdown			4000		ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 (ADM4851 only)
Time to Shutdown		50	330	3000	ns	ADM4851 only[1]

[1] The half-duplex device is put into shutdown mode by driving $\overline{RE}$ high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

ADM4852/ADM4856 TIMING SPECIFICATIONS

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate		2.5			Mbps	
Propagation Delay	t_{PLH}, t_{PHL}	50		180	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 21 and Figure 25
Skew	t_{SKEW}			50	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 21 and Figure 25
Rise/Fall Times	t_R, t_F			140	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 21 and Figure 25
Enable Time	t_{ZH}, t_{ZL}			180	ns	R_L = 500 Ω, C_L = 100 pF, see Figure 22 and Figure 27 (ADM4852 only)
Disable Time	t_{LZ}, t_{HZ}			180	ns	R_L = 500 Ω, C_L = 100 pF, see Figure 22 and Figure 27 (ADM4852 only)
Enable Time from Shutdown			4000		ns	R_L = 500 Ω, C_L = 100 pF, see Figure 22 (ADM4852 only)
RECEIVER						
Propagation Delay	t_{PLH}, t_{PHL}	55		190	ns	C_L = 15 pF, see Figure 23 and Figure 26
Differential Skew	t_{SKEW}			50	ns	C_L = 15 pF, see Figure 23 and Figure 26
Enable Time	t_{ZH}, t_{ZL}		5	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 and Figure 28 (ADM4852 only)
Disable Time	t_{LZ}, t_{HZ}		20	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 and Figure 28 (ADM4852 only)
Enable Time from Shutdown			4000		ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 (ADM4852 only)
Time to Shutdown		50	330	3000	ns	ADM4852 only[1]

[1] The half-duplex device is put into shutdown mode by driving $\overline{RE}$ high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

ADM4853/ADM4857 TIMING SPECIFICATIONS

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate		10			Mbps	
Propagation Delay	t_{PLH}, t_{PHL}	0		30	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 21 and Figure 25
Skew	t_{SKEW}			10	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 21 and Figure 25
Rise/Fall Times	t_R, t_F			30	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 21 and Figure 25
Enable Time	t_{ZH}, t_{ZL}			35	ns	R_L = 500 Ω, C_L = 100 pF, see Figure 22 and Figure 27 (ADM4853 only)
Disable Time	t_{LZ}, t_{HZ}			35	ns	R_L = 500 Ω, C_L = 100 pF, see Figure 22 and Figure 27 (ADM4853 only)
Enable Time from Shutdown			4000		ns	R_L = 500 Ω, C_L = 100 pF, see Figure 22 (ADM4853 only)
RECEIVER						
Propagation Delay	t_{PLH}, t_{PHL}	55		190	ns	C_L = 15 pF, see Figure 23 and Figure 26
Differential Skew	t_{SKEW}			30	ns	C_L = 15 pF, see Figure 23 and Figure 26
Enable Time	t_{ZH}, t_{ZL}		5	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 and Figure 28 (ADM4853 only)
Disable Time	t_{LZ}, t_{HZ}		20	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 and Figure 28 (ADM4853 only)
Enable Time from Shutdown			4000		ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 24 (ADM4853 only)
Time to Shutdown		50	330	3000	ns	ADM4853 only[1]

[1] The half-duplex device is put into shutdown mode by driving $\overline{RE}$ high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
V_{CC} to GND	6 V
Digital Input/Output Voltage (DE, $\overline{RE}$, DI, RO)	−0.3 V to V_{CC} + 0.3 V
Driver Output/Receiver Input Voltage	−9 V to +14 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
θ_{JA} Thermal Impedance	
8-Lead SOIC	110°C/W
8-Lead LFCSP	62°C/W
8-Lead MSOP	133.1°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

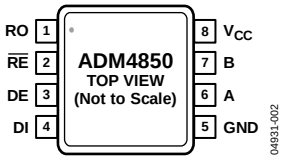

Figure 3. ADM4850, 8-Lead MSOP, Pin Configuration

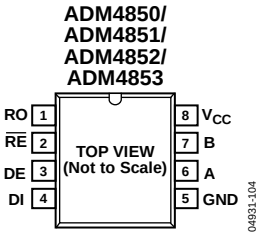

Figure 4. ADM4850/ADM4851/ADM4852/ADM4853, 8-Lead SOIC, Pin Configuration

Table 8. ADM4850/ADM4851/ADM4852/ADM4853, 8-Lead MSOP and 8-Lead SOIC, Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output. When RO is enabled and (A − B) ≥ −30 mV, RO is high. When RO is enabled and (A − B) ≤ −200 mV, RO is low.
2	$\overline{RE}$	Receiver Output Enable. A low level on $\overline{RE}$ enables the receiver output (RO). A high level on $\overline{RE}$ places RO into a high impedance state.
3	DE	Driver Output Enable. A high level on DE enables the driver differential outputs (A and B). A low level on DE places the driver differential outputs into a high impedance state.
4	DI	Driver Input. When the driver is enabled, a logic low on DI forces A low and B high, whereas a logic high on DI forces A high and B low.
5	GND	Ground.
6	A	Noninverting Receiver Input A/Noninverting Driver Output A.
7	B	Inverting Receiver Input B/Inverting Driver Output B.
8	V_{CC}	5 V Power Supply.

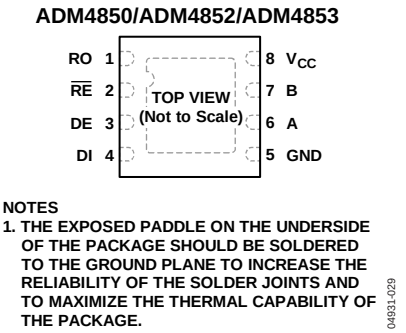

Figure 5. ADM4850/ADM4852/ADM4853, 8-Lead LFCSP, Pin Configuration

Table 9. ADM4850/ADM4852/ADM4853, 8-Lead LFCSP, Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output. When RO is enabled and (A − B) ≥ −30 mV, RO is high. When RO is enabled and (A − B) ≤ −200 mV, RO is low.
2	$\overline{RE}$	Receiver Output Enable. A low level on $\overline{RE}$ enables the receiver output (RO). A high level on $\overline{RE}$ places RO into a high impedance state.
3	DE	Driver Output Enable. A high level on DE enables the driver differential outputs (A and B). A low level places the driver differential outputs into a high impedance state.
4	DI	Driver Input. When the driver is enabled, a logic low on DI forces A low and B high, whereas a logic high on DI forces A high and B low.
5	GND	Ground.
6	A	Noninverting Receiver Input A/Noninverting Driver Output A.
7	B	Inverting Receiver Input B/Inverting Driver Output B.
8	V_{CC}	5 V Power Supply.
	EPAD	Exposed Pad. The exposed paddle on the underside of the package must be soldered to the ground plane to increase the reliability of the solder joints and to maximize the thermal capability of the package.

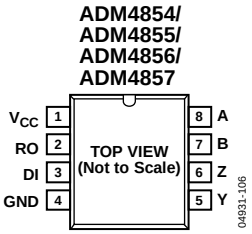

Figure 6. ADM4854/ADM4855/ADM4856/ADM4857, 8-Lead SOIC, Pin Configuration

Table 10. ADM4854/ADM4855/ADM4856/ADM4857, 8-Lead SOIC, Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{CC}	5 V Power Supply.
2	RO	Receiver Output. When RO is enabled and (A − B) ≥ −30 mV, RO is high. When RO is enabled and (A − B) ≤ −200 mV, RO is low.
3	DI	Driver Input. When the driver is enabled, a logic low on DI forces Y low and Z high, whereas a logic high on DI forces Y high and Z low.
4	GND	Ground.
5	Y	Noninverting Driver Output.
6	Z	Inverting Driver Output.
7	B	Inverting Receiver Input.
8	A	Noninverting Receiver Input.

TYPICAL PERFORMANCE CHARACTERISTICS

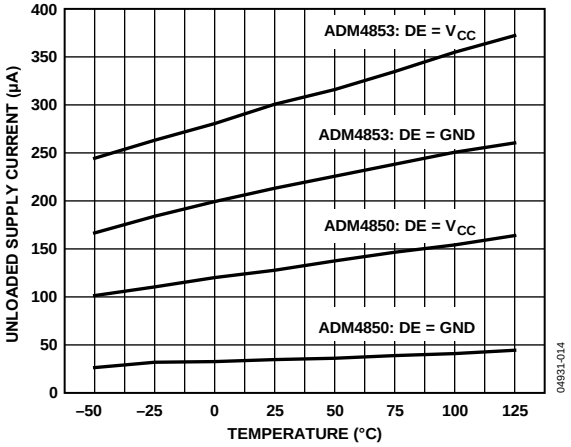

Figure 7. Unloaded Supply Current vs. Temperature (ADM4850/ADM4853)

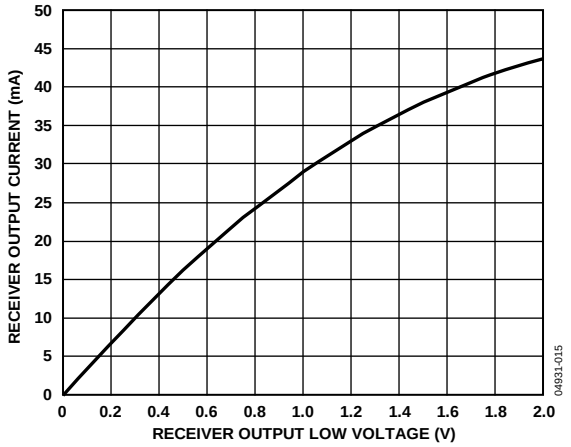

Figure 8. Receiver Output Current vs. Receiver Output Low Voltage

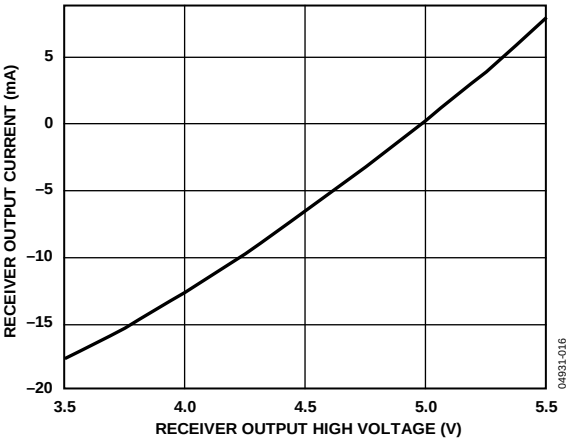

Figure 9. Receiver Output Current vs. Receiver Output High Voltage

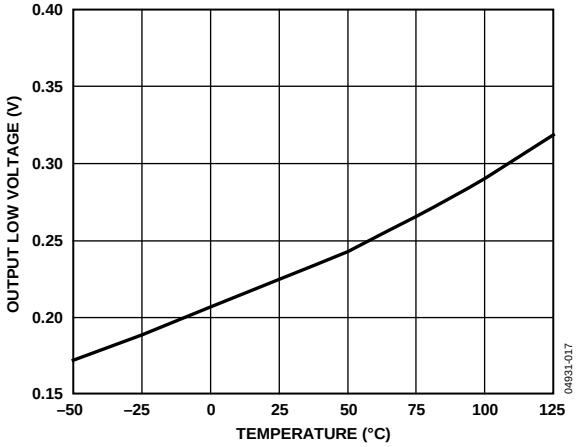

Figure 10. Receiver Output Low Voltage vs. Temperature

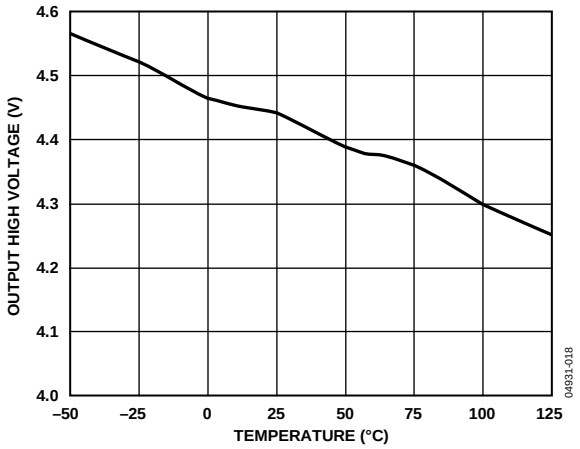

Figure 11. Receiver Output High Voltage vs. Temperature

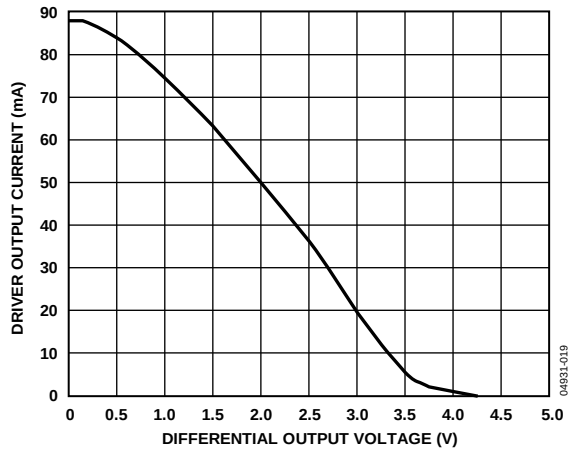

Figure 12. Driver Output Current vs. Differential Output Voltage

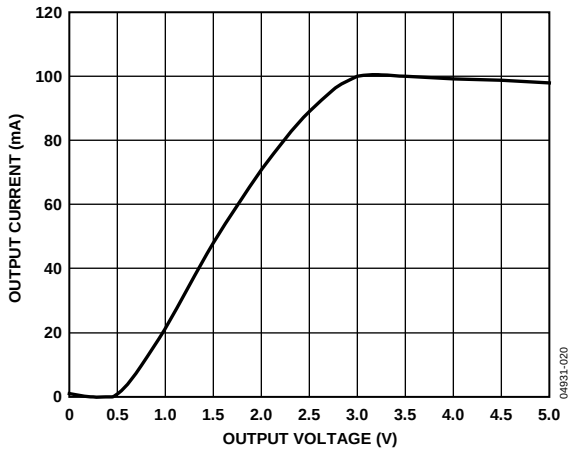

Figure 13. Output Current vs. Driver Output Low Voltage

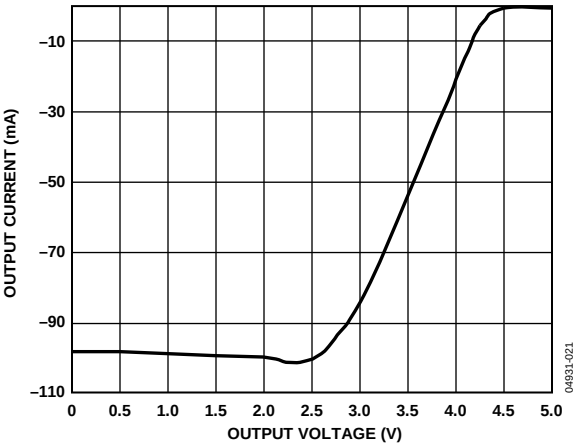

Figure 14. Output Current vs. Driver Output High Voltage

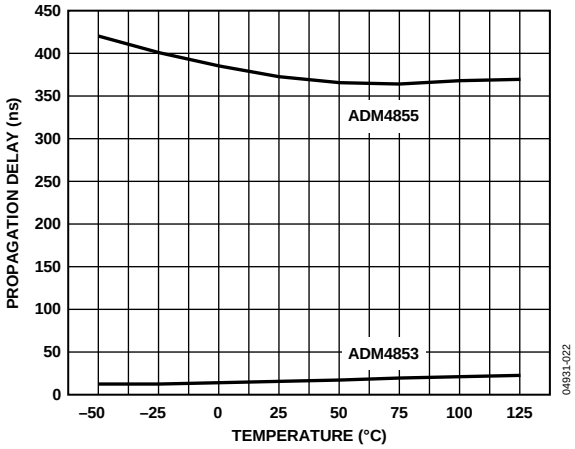

Figure 15. Driver Propagation Delay vs. Temperature (ADM4853/ADM4855)

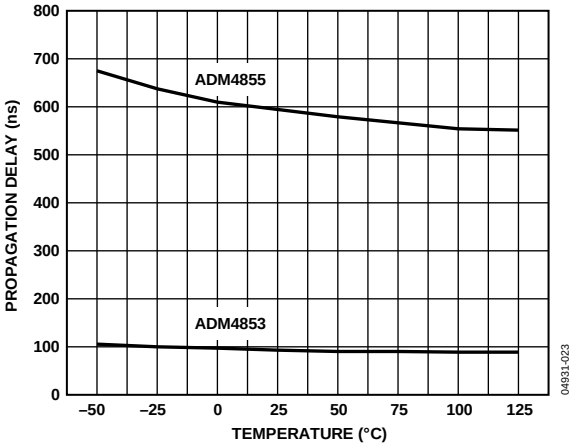

Figure 16. Receiver Propagation Delay vs. Temperature (ADM4853/ADM4855)

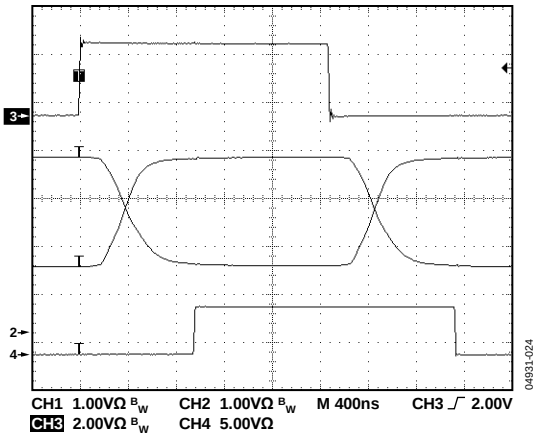

Figure 17. Driver/Receiver Propagation Delay (ADM4855, 500 kbps)

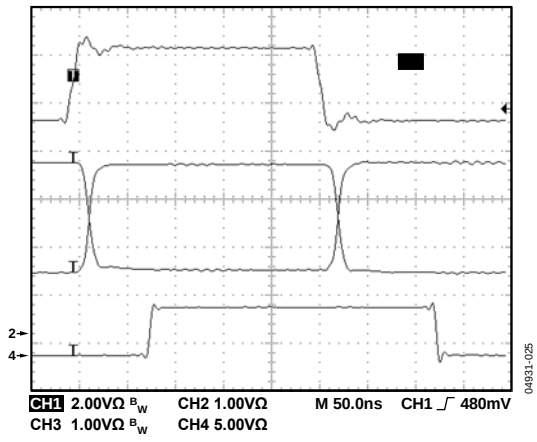

Figure 18. Driver/Receiver Propagation Delay (ADM4857, 4 Mbps)

TEST CIRCUITS

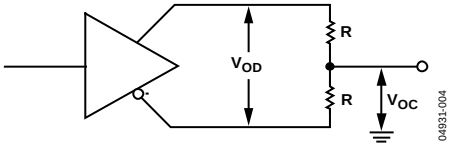

Figure 19. Driver Voltage Measurement

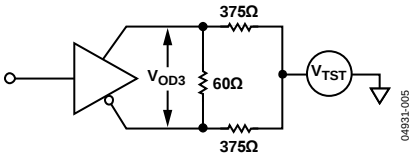

Figure 20. Driver Voltage Measurement over Common-Mode Voltage Range

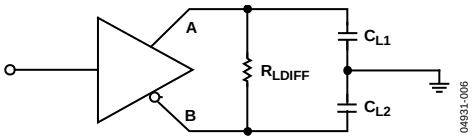

Figure 21. Driver Propagation Delay

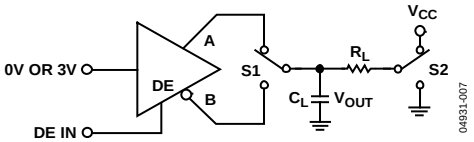

Figure 22. Driver Enable/Disable (ADM4850/ADM4852/ADM4853)

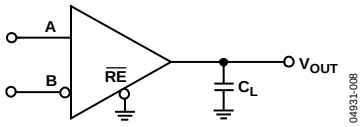

Figure 23. Receiver Propagation Delay

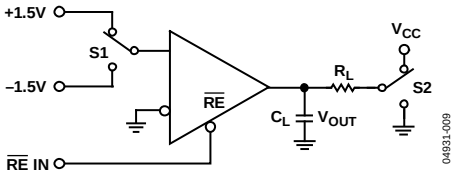

Figure 24. Receiver Enable/Disable (ADM4850/ADM4852/ADM4853)

SWITCHING CHARACTERISTICS

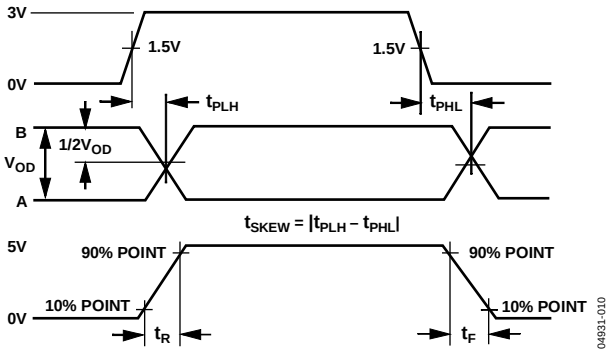

Figure 25. Driver Propagation Delay, Rise/Fall Timing

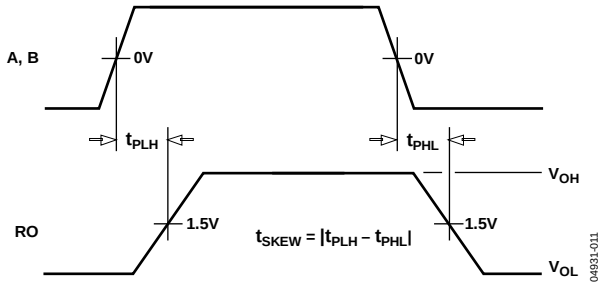

Figure 26. Receiver Propagation Delay

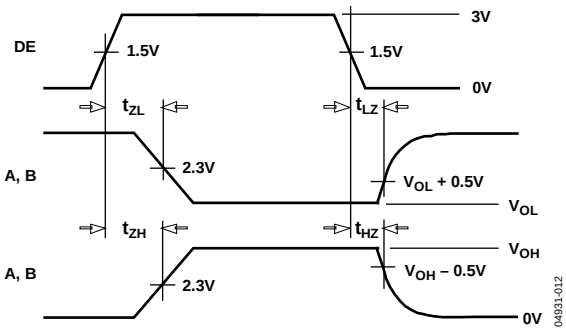

Figure 27. Driver Enable/Disable Timing

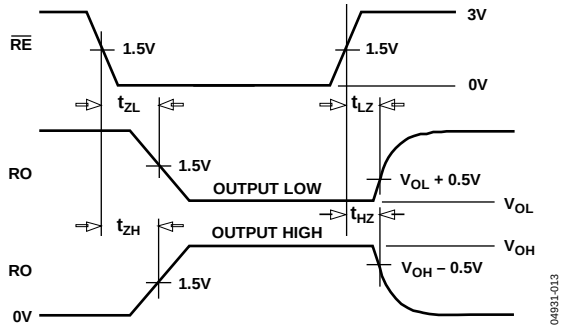

Figure 28. Receiver Enable/Disable Timing

THEORY OF OPERATION

The ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857 are high speed RS-485/RS-422 transceivers offering enhanced performance over industry-standard devices. All devices in the family contain one driver and one receiver but offer a choice of performance options. The devices feature true fail-safe operation, which guarantees a logic high receiver output when the receiver inputs are open circuit or short-circuit, or when they are connected to a terminated transmission line with all drivers disabled (see the Fail-Safe Operation section).

SLEW RATE CONTROL

The ADM4850 and ADM4854 feature a controlled slew rate driver that minimizes EMI and reduces reflections caused by incorrectly terminated cables, allowing error free data transmission rates up to 115 kbps. The ADM4851 and ADM4855 offer a higher limit on driver output slew rate, allowing data transmission rates up to 500 kbps. The driver slew rates of the ADM4852/ADM4856 and the ADM4853/ADM4857 are not limited, offering data transmission rates up to 2.5 Mbps and 10 Mbps, respectively.

RECEIVER INPUT FILTERING

The receivers of all the devices incorporate input hysteresis. In addition, the receivers of the 115 kbps ADM4850 and ADM4854 and the 500 kbps ADM4851 and ADM4855 incorporate input filtering, which enhances noise immunity with differential signals that have very slow rise and fall times. However, it causes the propagation delay to increase by 20%.

HALF-DUPLEX/FULL DUPLEX OPERATION

Half-duplex operation implies that the transceiver can transmit and receive, but it can do only one of these at any given time. However, with full duplex operation, the transceiver can transmit and receive simultaneously. The ADM4850/ADM4851/ADM4852/ADM4853 are half-duplex devices in which the driver and the receiver share differential bus terminals. The ADM4854/ADM4855/ADM4856/ADM4857 are full duplex devices that have dedicated driver output and receiver input pins. Figure 29 and Figure 30 show typical half-duplex and full duplex topologies.

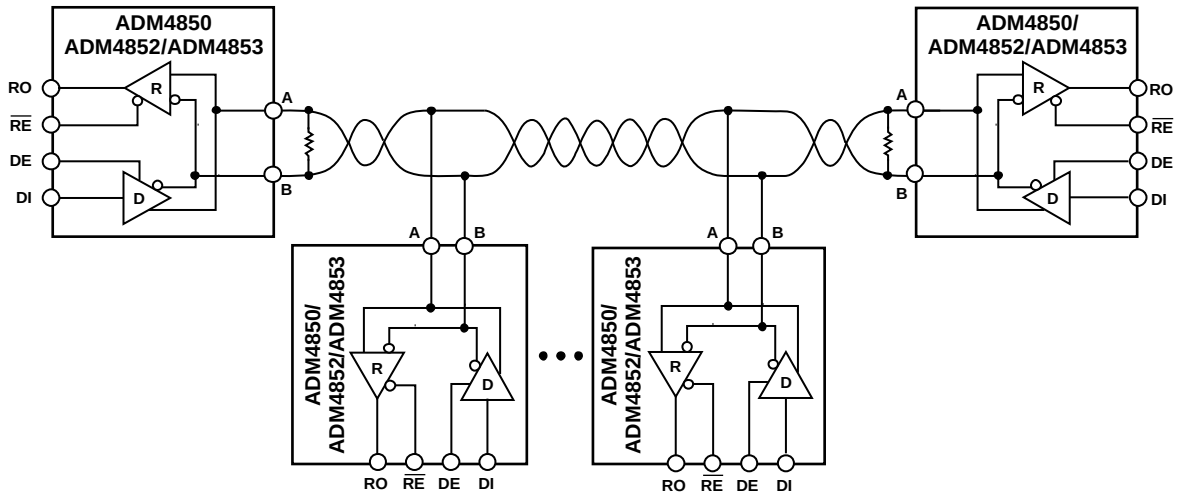

Figure 29. Typical Half-Duplex RS-485 Network Topology

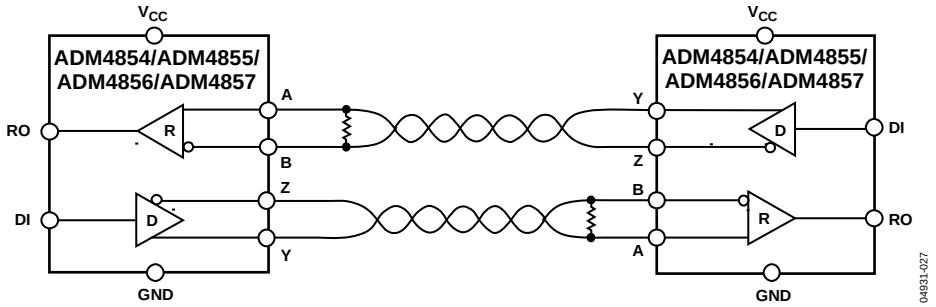

Figure 30. Typical Full Duplex Point-to-Point RS-485 Network Topology

HIGH RECEIVER INPUT IMPEDANCE

The input impedance of the ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857 receivers is 96 kΩ, which is eight times higher than the standard RS-485 unit load of 12 kΩ. This 96 kΩ impedance enables a standard driver to drive 32 unit loads or to be connected to 256 ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857 receivers. An RS-485 bus, driven by a single standard driver, can be connected to a combination of ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857 devices and standard unit load receivers, up to an equivalent of 32 standard unit loads.

THREE-STATE BUS CONNECTION

The half-duplex devices (ADM4850/ADM4852/ADM4853) have a driver enable pin (DE) that enables the driver outputs when taken high, or puts the driver outputs into a high impedance state when taken low. Similarly, the half-duplex devices have an active low receiver enable pin ($\overline{RE}$). Taking this pin low enables the receiver, whereas taking it high puts the receiver outputs into a high impedance state, which allows several driver outputs to be connected to an RS-485 bus. Note that only one driver must be enabled at a time, but that many receivers can be enabled.

SHUTDOWN MODE

The ADM4850/ADM4852/ADM4853 have a low power shutdown mode, which is enabled by taking $\overline{RE}$ high and DE low. If shutdown mode is not used, the fact that DE is active high and $\overline{RE}$ is active low offers a convenient way of switching the device between transmit and receive by tying DE and $\overline{RE}$ together.

If DE is driven low and $\overline{RE}$ is driven high for less than 50 ns, the devices are guaranteed not to enter shutdown mode. If DE is driven low and $\overline{RE}$ is driven high for at least 3000 ns, the devices are guaranteed to enter shutdown mode.

FAIL-SAFE OPERATION

The ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857 offer true fail-safe operation while remaining fully compliant with the ±200 mV EIA/TIA-485 standard. A logic high receiver output generates when the receiver inputs are shorted together or open circuit, or when they are connected to a terminated transmission line with all drivers disabled. This logic high is done by setting the receiver threshold between −30 mV and −200 mV. If the differential receiver input voltage (A − B) is greater than or equal to −30 mV, RO is logic high. If (A − B) is less than or equal to −200 mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the differential input voltage of the receiver is pulled to 0 V by the internal circuitry of the ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857, which results in a logic high with 30 mV minimum noise margin.

CURRENT LIMIT AND THERMAL SHUTDOWN

The ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ADM4855/ADM4856/ADM4857 incorporate two protection mechanisms to guard the drivers against short circuits, bus contention, or other fault conditions. The first is a current limiting output stage, which protects the driver against short circuits over the entire common-mode voltage range by limiting the output current to approximately 70 mA. Under extreme fault conditions where the current limit is not effective, a thermal shutdown circuit puts the driver outputs into a high impedance state if the die temperature exceeds 150°C, and does not turn them back on until the temperature falls to 130°C.

OUTLINE DIMENSIONS

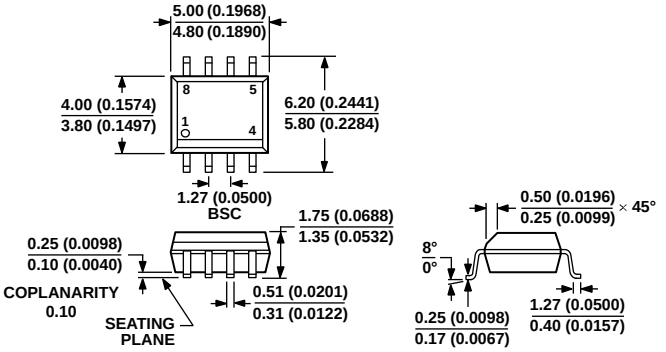

Figure 31. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

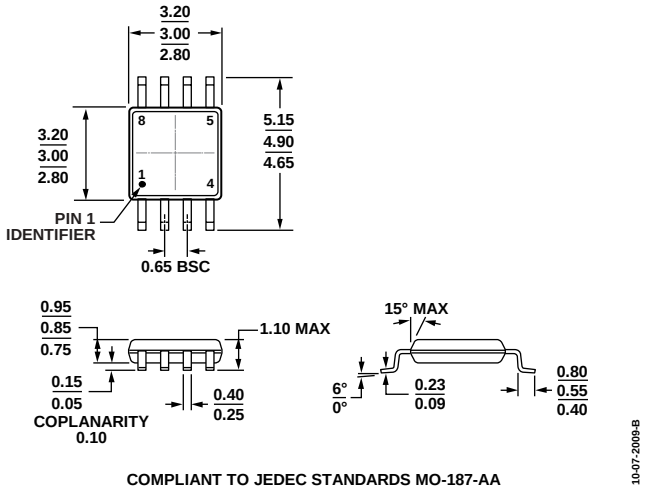

Figure 32. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

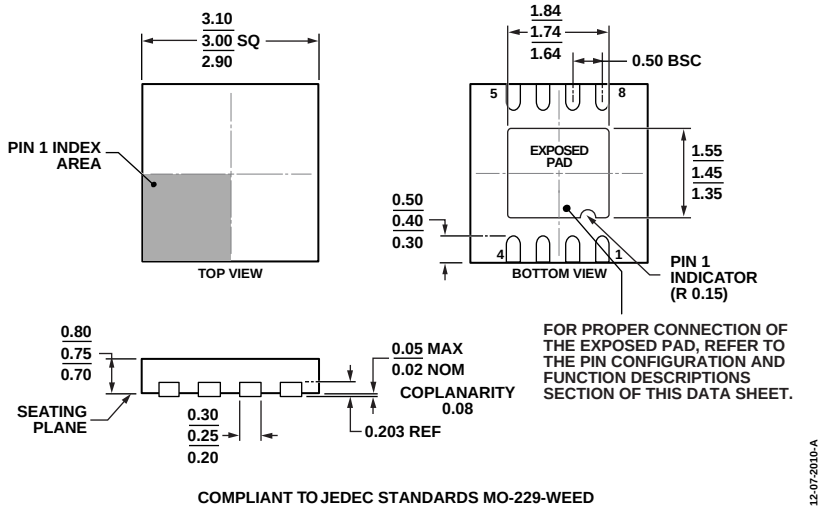

Figure 33. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-13)
Dimensions shown in millimeters