Dual, 3 V, CMOS, LVDS High Speed Differential Driver

ADN4663

FEATURES

±15 kV ESD protection on output pins
600 Mbps (300 MHz) switching rates
Flow-through pinout simplifies PCB layout
300 ps typical differential skew
700 ps maximum differential skew
1.5 ns maximum propagation delay
3.3 V power supply
±355 mV differential signaling
Low power dissipation: 23 mW typical
Interoperable with existing 5 V LVDS receivers
Conforms to TIA/EIA-644 LVDS standard
Industrial operating temperature range (−40°C to +85°C)
Available in surface-mount (SOIC) package

APPLICATIONS

Backplane data transmission
Cable data transmission
Clock distribution

FUNCTIONAL BLOCK DIAGRAM

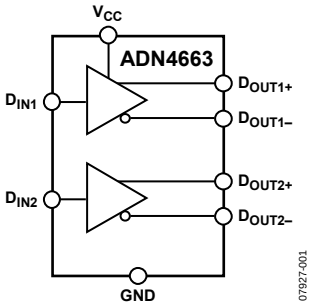

Figure 1.

GENERAL DESCRIPTION

The ADN4663 is a dual, CMOS, low voltage differential signaling (LVDS) line driver offering data rates of over 600 Mbps (300 MHz), and ultralow power consumption. It features a flow-through pinout for easy PCB layout and separation of input and output signals.

The device accepts low voltage TTL/CMOS logic signals and converts them to a differential current output of typically ±3.1 mA for driving a transmission medium such as a twisted-pair cable. The transmitted signal develops a differential voltage of typically ±355 mV across a termination resistor at the receiving end, and this is converted back to a TTL/CMOS logic level by a line receiver.

The ADN4663 and a companion receiver offer a new solution to high speed point-to-point data transmission, and a low power alternative to emitter-coupled logic (ECL) or positive emitter-coupled logic (PECL).

Rev. 0

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REVISION HISTORY

1/09—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V; R_L = 100 Ω; C_L = 15 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1, 2]	Symbol	Min	Typ	Max	Unit	Test Conditions
LVDS OUTPUTS (D_{OUTx+}, D_{OUTx-})						
Differential Output Voltage	V_{OD}	250	355	450	mV	See Figure 2 and Figure 4
Change in Magnitude of V_{OD} for Complementary Output States	ΔV_{OD}		1	35	|mV|	See Figure 2 and Figure 4
Offset Voltage	V_{OS}	1.125	1.2	1.375	V	See Figure 2 and Figure 4
Change in Magnitude of V_{OS} for Complementary Output States	ΔV_{OS}		3	25	|mV|	See Figure 2 and Figure 4
Output High Voltage	V_{OH}		1.4	1.6	V	See Figure 2 and Figure 4
Output Low Voltage	V_{OL}	0.90	1.1		V	See Figure 2 and Figure 4
INPUTS (D_{IN1}, D_{IN2})						
Input High Voltage	V_{IH}	2.0		V_{CC}	V	
Input Low Voltage	V_{IL}	GND		0.8	V	
Input High Current	I_{IH}	−10	±2	+10	µA	V_{IN} = 3.3 V or 2.4 V
Input Low Current	I_{IL}	−10	±1	+10	µA	V_{IN} = GND or 0.5 V
Input Clamp Voltage	V_{CL}	−1.5	−0.6		V	I_{CL} = −18 mA
LVDS OUTPUT PROTECTION (D_{OUTx+}, D_{OUTx-})						
Output Short-Circuit Current[3]	I_{OS}		−5.7	−8.0	mA	$D_{INx} = V_{CC}$, D_{OUTx+} = 0 V or D_{INx} = GND, D_{OUTx-} = 0 V
LVDS OUTPUT LEAKAGE (D_{OUTx+}, D_{OUTx-})						
Power-Off Leakage	I_{OFF}	−10	±1	+10	µA	$V_{OUT} = V_{CC}$ or GND, V_{CC} = 0 V
POWER SUPPLY						
Supply Current, Unloaded	I_{CC}		8	14	mA	No load, $D_{INx} = V_{CC}$ or GND
Supply Current, Loaded	I_{CCL}		10	20	mA	$D_{INx} = V_{CC}$ or GND
ESD PROTECTION						
D_{OUTx+}, D_{OUTx-} Pins			±15		kV	Human body model
All Pins Except D_{OUTx+}, D_{OUTx-}			±4		kV	Human body model

[1] Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD}, ΔV_{OD}, and ΔV_{OS}.
[2] The ADN4663 is a current mode device and functions within data sheet specifications only when a resistive load is applied to the driver outputs. Typical range is 90 Ω to 110 Ω.
[3] Output short-circuit current (I_{OS}) is specified as magnitude only; minus sign indicates direction only.

AC CHARACTERISTICS

V_{CC} = 3.0 V to 3.6 V; R_L = 100 Ω; C_L[1] = 15 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[2]	Symbol	Min	Typ	Max	Unit	Conditions/Comments[3, 4]
Differential Propagation Delay High to Low	t_{PHLD}	0.3	0.8	1.5	ns	See Figure 3 and Figure 4
Differential Propagation Delay Low to High	t_{PLHD}	0.3	1.1	1.5	ns	See Figure 3 and Figure 4
Differential Pulse Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$[5]	t_{SKD1}	0	0.3	0.7	ns	See Figure 3 and Figure 4
Channel-to-Channel Skew[6]	t_{SKD2}	0	0.4	0.8	ns	See Figure 3 and Figure 4
Differential Part-to-Part Skew[7]	t_{SKD3}	0		1.0	ns	See Figure 3 and Figure 4
Differential Part-to-Part Skew[8]	t_{SKD4}	0		1.2	ns	See Figure 3 and Figure 4
Rise Time	t_{TLH}	0.2	0.5	1.0	ns	See Figure 3 and Figure 4
Fall Time	t_{THL}	0.2	0.5	1.0	ns	See Figure 3 and Figure 4
Maximum Operating Frequency[9]	f_{MAX}		350		MHz	See Figure 3

[1] C_L includes probe and jig capacitance.
[2] AC parameters are guaranteed by design and characterization.
[3] Generator waveform for all tests, unless otherwise specified: f = 50 MHz, Z_O = 50 Ω, $t_{TLH} \leq 1$ ns, and $t_{THL} \leq 1$ ns.
[4] All input voltages are for one channel, unless otherwise specified. Other inputs are set to GND.
[5] $t_{SKD1} = \lvert t_{PHLD} - t_{PLHD} \rvert$ is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
[6] t_{SKD2} is the differential channel-to-channel skew of any event on the same device.
[7] t_{SKD3}, differential part-to-part skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
[8] t_{SKD4}, differential part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperatures and voltage ranges, and across process distribution. t_{SKD4} is defined as |maximum − minimum| differential propagation delay.
[9] f_{MAX} generator input conditions: $t_{TLH} = t_{THL} < 1$ ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output criteria: duty cycle = 45% to 55%, $V_{OD} > 250$ mV, all channels switching.

Test Circuits and Timing Diagrams

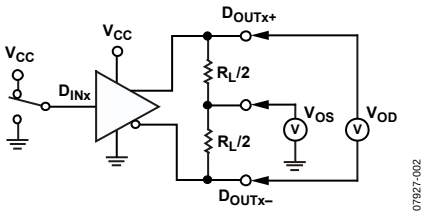

Figure 2. Test Circuit for Driver V_{OD} and V_{OS}

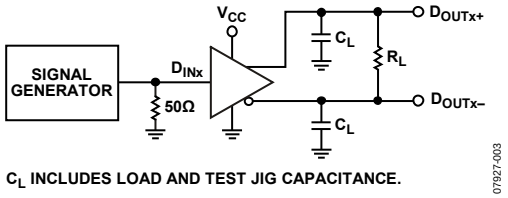

Figure 3. Test Circuit for Driver Propagation Delay, Transition Time, and Maximum Operating Frequency

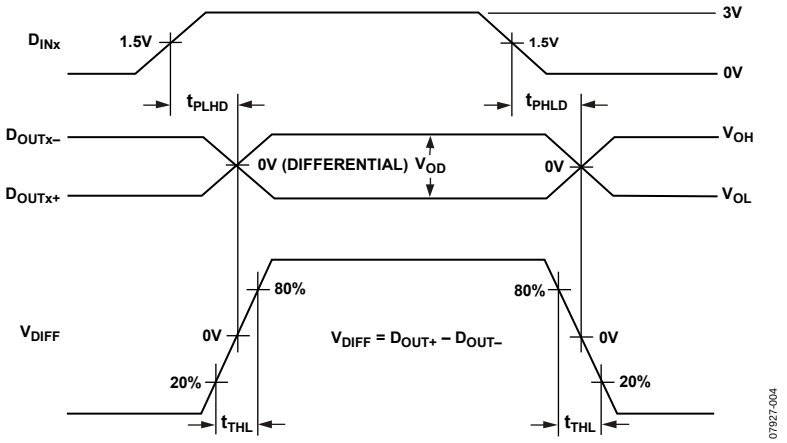

Figure 4. Driver Propagation Delay and Transition Time Waveforms

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All voltages are relative to their respective ground.

Table 3.

Parameter	Rating
V_{CC} to GND	−0.3 V to +4 V
Input Voltage (D_{INx}) to GND	−0.3 V to V_{CC} + 0.3 V
Output Voltage (D_{OUTx+}, D_{OUTx-}) to GND	−0.3 V to V_{CC} + 0.3 V
Short-Circuit Duration (D_{OUTx+}, D_{OUTx-}) to GND	Continuous
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
SOIC Package	
θ_{JA} Thermal Impedance	149.5°C/W
Reflow Soldering Peak Temperature	
Pb-Free	260°C ± 5°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

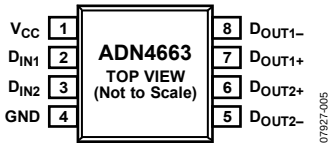

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{CC}	Power Supply Input. The part can be operated from 3.0 V to 3.6 V, and the supply should be decoupled with a 10 µF solid tantalum capacitor in parallel with a 0.1 µF capacitor to GND.
2	D_{IN1}	Driver Channel 1 Logic Input.
3	D_{IN2}	Driver Channel 2 Logic Input.
4	GND	Ground reference point for all circuitry on the part.
5	D_{OUT2-}	Channel 2 Inverting Output Current Driver. When D_{IN2} is high, current flows into D_{OUT2-}. When D_{IN2} is low, current flows out of D_{OUT2-}.
6	D_{OUT2+}	Channel 2 Noninverting Output Current Driver. When D_{IN2} is high, current flows out of D_{OUT2+}. When D_{IN2} is low, current flows into D_{OUT2+}.
7	D_{OUT1+}	Channel 1 Noninverting Output Current Driver. When D_{IN1} is high, current flows out of D_{OUT1+}. When D_{IN1} is low, current flows into D_{OUT1+}.
8	D_{OUT1-}	Channel 1 Inverting Output Current Driver. When D_{IN1} is high, current flows into D_{OUT1-}. When D_{IN1} is low, current flows out of D_{OUT1-}.

TYPICAL PERFORMANCE CHARACTERISTICS

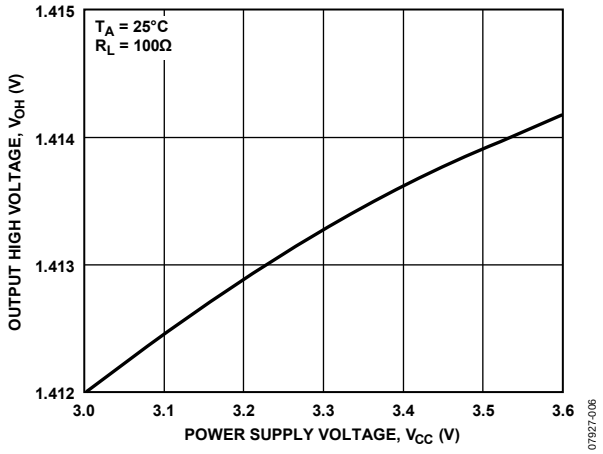

Figure 6. Output High Voltage vs. Power Supply Voltage

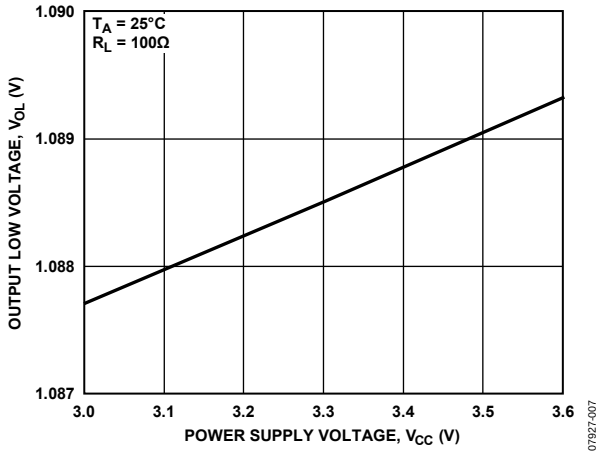

Figure 7. Output Low Voltage vs. Power Supply Voltage

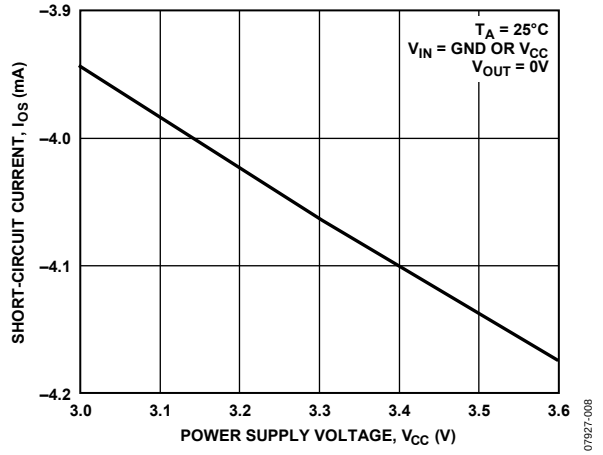

Figure 8. Output Short-Circuit Current vs. Power Supply Voltage

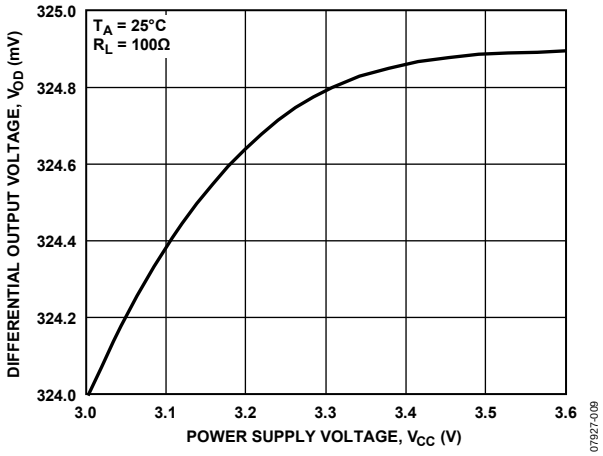

Figure 9. Differential Output Voltage vs. Power Supply Voltage

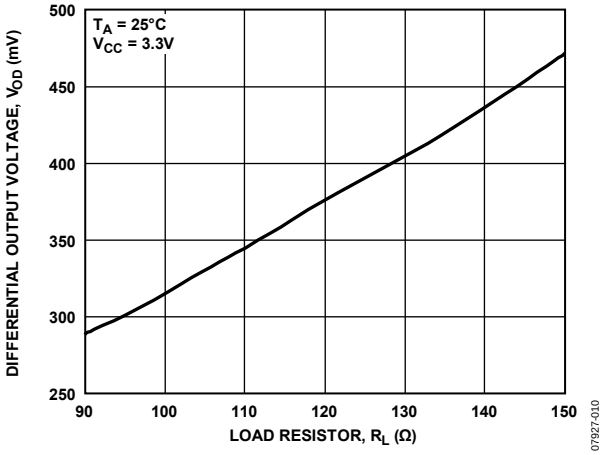

Figure 10. Differential Output Voltage vs. Load Resistor

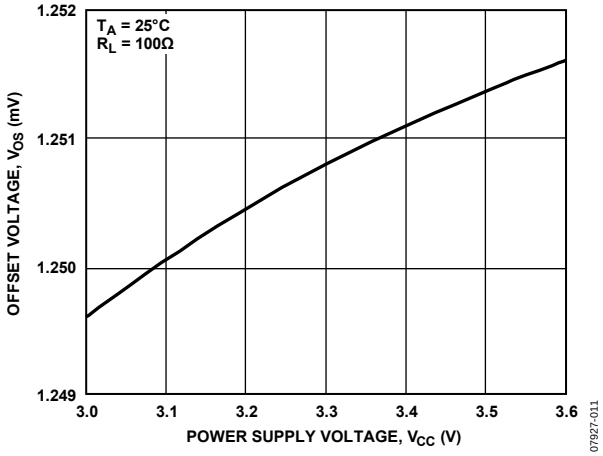

Figure 11. Offset Voltage vs. Power Supply Voltage

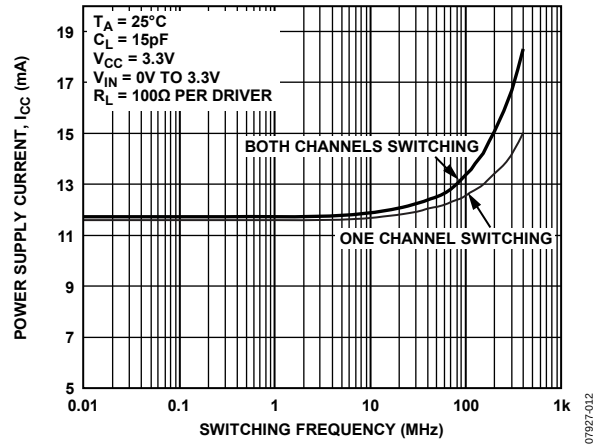

Figure 12. Power Supply Current vs. Switching Frequency

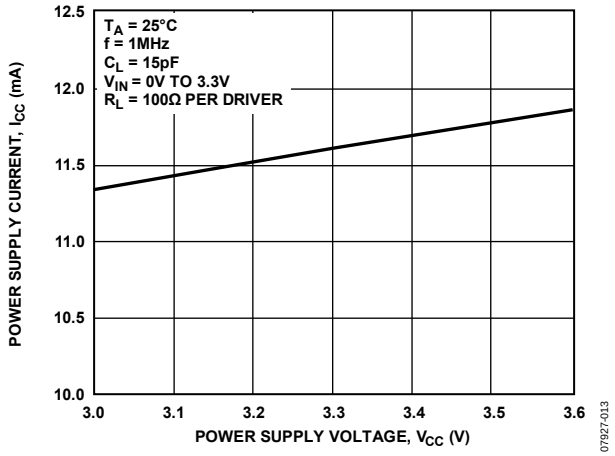

Figure 13. Power Supply Current vs. Power Supply Voltage

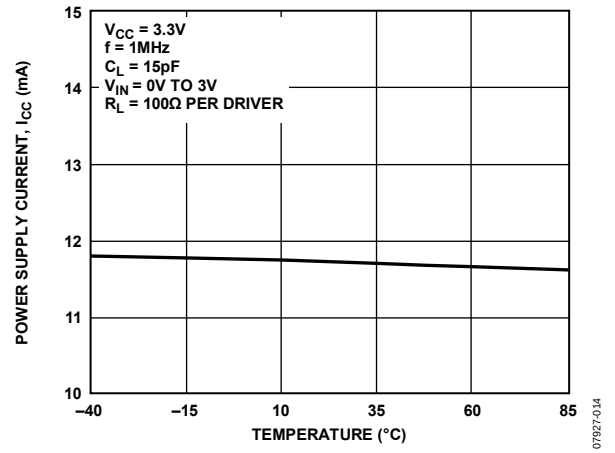

Figure 14. Power Supply Current vs. Ambient Temperature

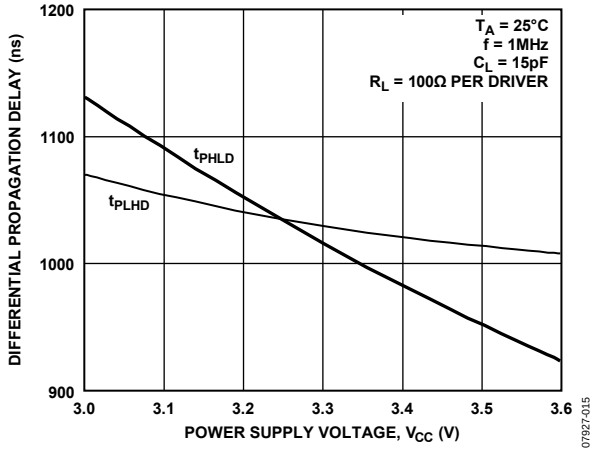

Figure 15. Differential Propagation Delay vs. Power Supply Voltage

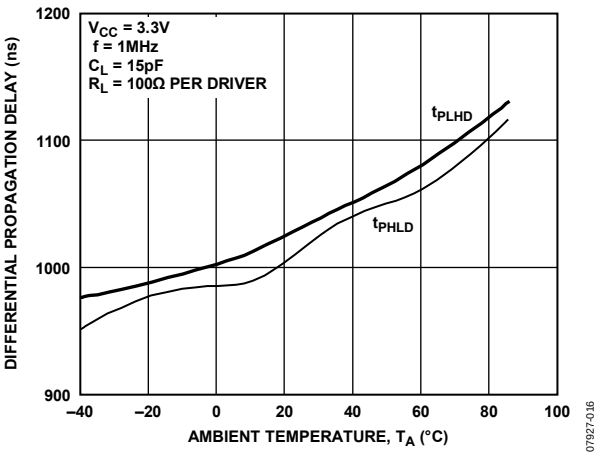

Figure 16. Differential Propagation Delay vs. Ambient Temperature

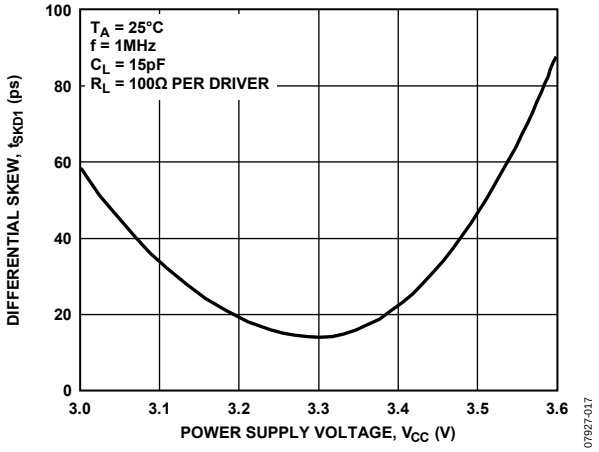

Figure 17. Differential Skew vs. Power Supply Voltage

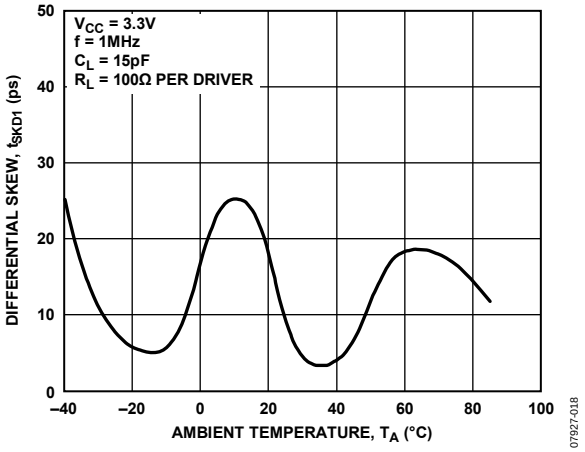

Figure 18. Differential Skew vs. Ambient Temperature

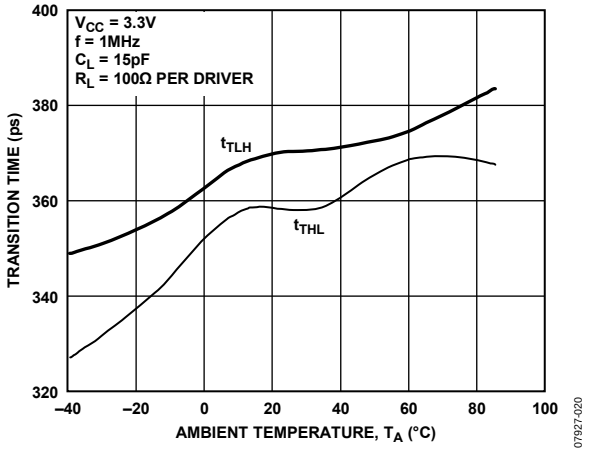

Figure 20. Transition Time vs. Ambient Temperature

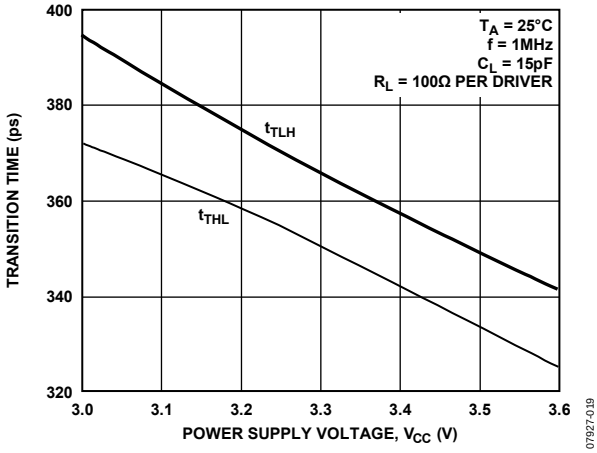

Figure 19. Transition Time vs. Power Supply Voltage

THEORY OF OPERATION

The ADN4663 is a dual line driver for low voltage differential signaling. It takes a single-ended 3 V logic signal and converts it to a differential current output. The data can then be transmitted for considerable distances, over media such as a twisted-pair cable or PCB backplane, to an LVDS receiver, where it develops a voltage across a terminating resistor, R_T. This resistor is chosen to match the characteristic impedance of the medium, typically around 100 Ω. The differential voltage is detected by the receiver and converted back into a single-ended logic signal.

When D_{INx} is high (Logic 1), current flows out of the D_{OUTx+} pin (current source) through R_T and back into the D_{OUTx-} pin (current sink). At the receiver, this current develops a positive differential voltage across R_T (with respect to the inverting input) and results in a Logic 1 at the receiver output. When D_{INx} is low, D_{OUTx+} sinks current and D_{OUTx-} sources current; a negative differential voltage across R_T results in a Logic 0 at the receiver output.

The output drive current is between ±2.5 mA and ±4.5 mA (typically ±3.55 mA), developing between ±250 mV and ±450 mV across a 100 Ω termination resistor. The received voltage is centered around the receiver offset of 1.2 V. Therefore, the noninverting receiver input is typically (1.2 V + [355 mV/2]) = 1.377 V, and the inverting receiver input is (1.2 V − [355 mV/2]) = 1.023 V for Logic 1. For Logic 0, the inverting and noninverting output voltages are reversed. Note that because the differential voltage reverses polarity, the peak-to-peak voltage swing across R_T is twice the differential voltage.

Current mode drivers offer considerable advantages over voltage mode drivers such as RS-422 drivers. The operating current remains fairly constant with increased switching frequency, whereas that of voltage mode drivers increase exponentially in most cases. This is caused by the overlap as internal gates switch between high and low, which causes currents to flow from the device power supply to ground.

A current mode device simply reverses a constant current between its two outputs, with no significant overlap currents.

This is similar to emitter-coupled logic (ECL) and positive emitter-coupled logic (PECL), but without the high quiescent current of ECL and PECL.

APPLICATIONS INFORMATION

Figure 21 shows a typical application for point-to-point data transmission using the ADN4663 as the driver and a LVDS receiver.

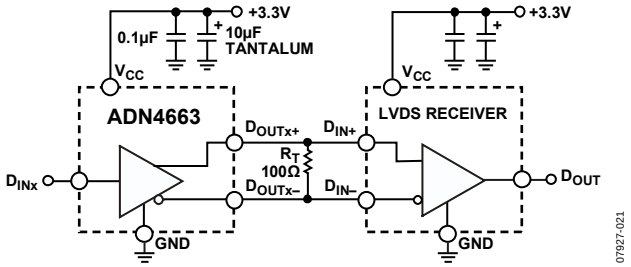

Figure 21. Typical Application Circuit