3 V LVDS Quad CMOS Differential Line Receiver

ADN4668

FEATURES

- ±15 kV ESD protection on receiver input pins
- 400 Mbps (200 MHz) switching rates
- Flow-through pin configuration simplifies PCB layout
- 150 ps channel-to-channel skew (typical)
- 100 ps differential skew (typical)
- 2.7 ns maximum propagation delay
- 3.3 V power supply
- High impedance outputs on power-down
- Low power design (3 mW quiescent typical)
- Interoperable with existing 5 V LVDS drivers
- Accepts small swing (310 mV typical) differential input signal levels
- Supports open, short, and terminated input fail-safe
- 0 V to −100 mV threshold region
- Conforms to TIA/EIA-644 LVDS standard
- Industrial operating temperature range of −40°C to +85°C
- Available in 16-lead surface-mount SOIC and 16-lead low profile TSSOP package

FUNCTIONAL BLOCK DIAGRAM

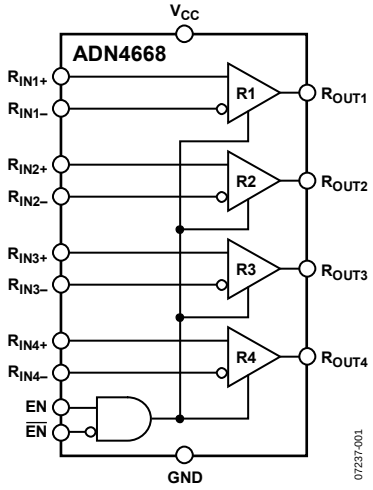

Figure 1.

APPLICATIONS

- Point-to-point data transmission
- Multidrop buses
- Clock distribution networks
- Backplane receivers

GENERAL DESCRIPTION

The ADN4668 is a quad-channel CMOS, low voltage differential signaling (LVDS) line receiver offering data rates of over 400 Mbps (200 MHz) and ultralow power consumption. It features a flow-through pin configuration for easy PCB layout and separation of input and output signals.

The device accepts low voltage (310 mV typical) differential input signals and converts them to a single-ended, 3 V TTL/CMOS logic level.

The ADN4668 also offers active-high and active-low enable/disable inputs (EN and $\overline{\text{EN}}$) that control all four receivers. They disable the receivers and switch the outputs to a high impedance state.

This high impedance state allows the outputs of one or more ADN4668s to be multiplexed together and reduces the quiescent power consumption to 3 mW typical.

The ADN4668 and its companion driver, the ADN4667, offer a new solution to high speed, point-to-point data transmission and a low power alternative to emitter-coupled logic (ECL) or positive emitter-coupled logic (PECL).

Rev. A

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REVISION HISTORY

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3/08—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.0 V to 3.6 V, C_L = 15 pF to GND, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1, 2]

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions/Comments
LVDS INPUTS (R_{INx+}, R_{INx-})					
Differential Input High Threshold, V_{TH} at R_{INx+}, R_{INx-}[3]		−35	0	mV	V_{CM} = 1.2 V, 0.05 V, 2.95 V
Differential Input Low Threshold, V_{TL} at R_{INx+}, R_{INx-}[3]	−100	−35		mV	V_{CM} = 1.2 V, 0.05 V, 2.95 V
Common-Mode Voltage Range, V_{CMR} at R_{INx+}, R_{INx-}[4]	0.1		2.3	V	V_{ID} = 200 mV p-p
Input Current, I_{IN} at R_{INx+}, R_{INx-}	−10	±5	+10	µA	V_{IN} = 2.8 V, V_{CC} = 3.6 V or 0 V
	−10	±1	+10	µA	V_{IN} = 0 V, V_{CC} = 3.6 V or 0 V
	−20	±1	+20	µA	V_{IN} = 3.6 V, V_{CC} = 0 V
LOGIC INPUTS					
Input High Voltage, V_{IH}	2.0		V_{CC}	V	
Input Low Voltage, V_{IL}	GND		0.8	V	
Input Current, I_{IN}	−10	±5	+10	µA	V_{IN} = 0 V or V_{CC}, other input = V_{CC} or GND
Input Clamp Voltage, V_{CL}	−1.5	−0.8		V	I_{CL} = −18 mA
OUTPUTS (R_{OUTx})					
Output High Voltage, V_{OH}	2.7	3.3		V	I_{OH} = −0.4 mA, V_{ID} = 200 mV
	2.7	3.3		V	I_{OH} = −0.4 mA, input terminated
	2.7	3.3		V	I_{OH} = −0.4 mA, input shorted
Output Low Voltage, V_{OL}		0.05	0.25	V	I_{OL} = 2 mA, V_{ID} = −200 mV
Output Short-Circuit Current, I_{OS}[5]	−15	−47	−100	V	Enabled, V_{OUT} = 0 V
Output Off State Current, I_{OZ}	−10	±1	+10	µA	Disabled, V_{OUT} = 0 V or V_{CC}
POWER SUPPLY					
No Load Supply, Current Receivers Enabled, I_{CC}		12	15	mA	EN = V_{CC}, inputs open
No Load Supply, Current Receivers Disabled, I_{CCZ}		1	5	mA	EN = GND, inputs open
ESD PROTECTION					
R_{INx+}, R_{INx-} Pins		±15		kV	Human body model
All Pins Except R_{INx+}, R_{INx-}		±3.5		kV	Human body model

[1] Current-into-device pins are defined as positive. Current-out-of-device pins are defined as negative. All voltages are referenced to ground, unless otherwise specified.
[2] All typicals are given for V_{CC} = 3.3 V and T_A = 25°C.
[3] V_{CC} is always higher than the R_{INx+} and R_{INx-} voltage. R_{INx-} and R_{INx+} have a voltage range of −0.2 V to V_{CC} − V_{ID}/2. However, to be compliant with ac specifications, the common voltage range is 0.1 V to 2.3 V.
[4] V_{CMR} is reduced for larger V_{ID}. For example, if V_{ID} = 400 mV, V_{CMR} is 0.2 V to 2.2 V. The fail-safe condition with inputs shorted is not supported over the common-mode range of 0 V to 2.4 V but is supported only with inputs shorted and no external common-mode voltage applied. V_{ID} up to V_{CC} − 0 V can be applied to the R_{INx+}/R_{INx-} inputs with the common-mode voltage set to V_{CC}/2. Propagation delay and differential pulse skew decrease when V_{ID} is increased from 200 mV to 400 mV. Skew specifications apply for 200 mV ≤ V_{ID} ≤ 800 mV over the common-mode range.
[5] Output short-circuit current (I_{OS}) is specified as magnitude only; a minus sign indicates direction only. Only one output should be shorted at a time; do not exceed the maximum junction temperature specification.

AC CHARACTERISTICS

V_{DD} = 3.0 V to 3.6 V, C_L = 15 pF to GND, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1, 2, 3, 4]

Table 2.

Parameter[5]	Min	Typ	Max	Unit	Conditions/Comments[6]
Differential Propagation Delay, High-to-Low, t_{PHLD}	1.2	2.0	2.7	ns	C_L = 15 pF,[7] V_{ID} = 200 mV, see Figure 2 and Figure 3
Differential Propagation Delay, Low-to-High, t_{PLHD}	1.2	1.9	2.7	ns	C_L = 15 pF,[7] V_{ID} = 200 mV, see Figure 2 and Figure 3
Differential Pulse Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$, t_{SKD1}[8]	0	0.1	0.4	ns	C_L = 15 pF,[7] V_{ID} = 200 mV, see Figure 2 and Figure 3
Differential Channel-to-Channel Skew, Same Device, t_{SKD2}[3]	0	0.15	0.5	ns	C_L = 15 pF,[7] V_{ID} = 200 mV, see Figure 2 and Figure 3
Differential Part-to-Part Skew, t_{SKD3}[4]			1.0	ns	C_L = 15 pF,[7] V_{ID} = 200 mV, see Figure 2 and Figure 3
Differential Part-to-Part Skew, t_{SKD4}[9]			1.5	ns	C_L = 15 pF,[7] V_{ID} = 200 mV, see Figure 2 and Figure 3
Rise Time, t_{TLH}		0.5	1.0	ns	C_L = 15 pF,[7] V_{ID} = 200 mV, see Figure 2 and Figure 3
Fall Time, t_{THL}		0.35	1.0	ns	C_L = 15 pF,[7] V_{ID} = 200 mV, see Figure 2 and Figure 3
Disable Time, High-to-Z, t_{PHZ}		8	14	ns	R_L = 2 kΩ, C_L = 15 pF,[7] see Figure 4 and Figure 5
Disable Time, Low-to-Z, t_{PLZ}		8	14	ns	R_L = 2 kΩ, C_L = 15 pF,[7] see Figure 4 and Figure 5
Enable Time, Z-to-High, t_{PZH}		9	14	ns	R_L = 2 kΩ, C_L = 15 pF,[7] see Figure 4 and Figure 5
Enable Time, Z-to-Low, t_{PZL}		9	14	ns	R_L = 2 kΩ, C_L = 15 pF,[7] see Figure 4 and Figure 5
Maximum Operating Frequency, f_{MAX}[10]	200	250		MHz	All channels switching

[1] All typicals are given for V_{CC} = 3.3 V and T_A = 25°C.
[2] Generator waveform for all tests, unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, and t_R and t_F (0% to 100%) ≤ 3 ns for R_{INx+}/R_{INx-}.
[3] Channel-to-channel skew, t_{SKD2}, is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.
[4] Part-to-part skew, t_{SKD3}, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
[5] AC parameters are guaranteed by design and characterization.
[6] Current-into-device pins are defined as positive. Current-out-of-device pins are defined as negative. All voltages are referenced to ground, unless otherwise specified.
[7] C_L includes probe and jig capacitance.
[8] t_{SKD1} is the magnitude difference in the differential propagation delay time between the positive-going edge and the negative-going edge of the same channel.
[9] Part-to-part skew, t_{SKD4}, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over the recommended operating temperature and voltage ranges and across process distribution. t_{SKD4} is defined as |maximum − minimum| differential propagation delay.
[10] f_{MAX} generator input conditions: f = 200 MHz, $t_R = t_F$ < 1 ns (0% to 100%), 50% duty cycle, differential (1.05 V p-p to 1.35 V p-p). Output criteria: 60%/40% duty cycle, V_{OL} (maximum = 0.4 V), V_{OH} (minimum = 2.7 V), C_L = 15 pF (stray plus probes).

TEST CIRCUITS AND WAVEFORMS

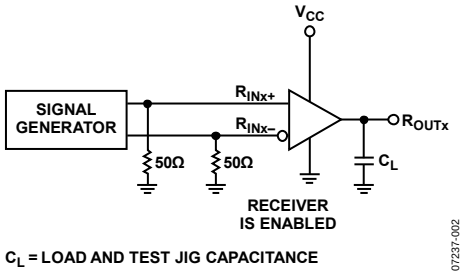


Figure 2. Test Circuit for Receiver Propagation Delay and Transition Time

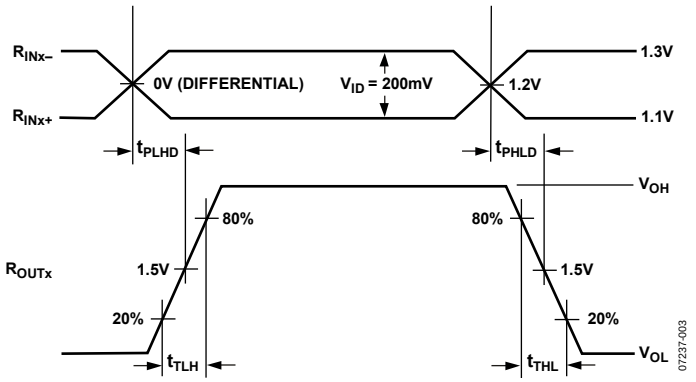
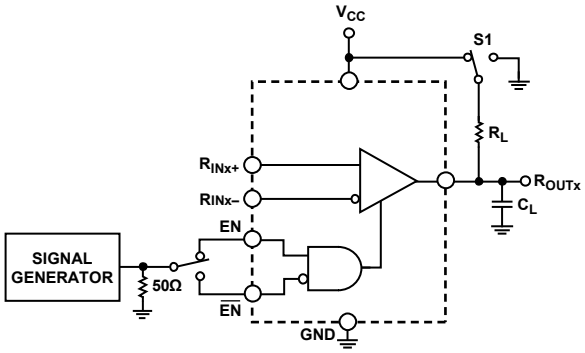


Figure 3. Receiver Propagation Delay and Transition Time Waveforms



NOTES
1. C_L INCLUDES LOAD AND TEST JIG CAPACITANCE.
2. S1 CONNECTED TO V_{CC} FOR t_{PZL} AND t_{PLZ} MEASUREMENTS.
3. S1 CONNECTED TO GND FOR t_{PZH} AND t_{PHZ} MEASUREMENTS.

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Figure 4. Test Circuit for Receiver Enable/Disable Delay

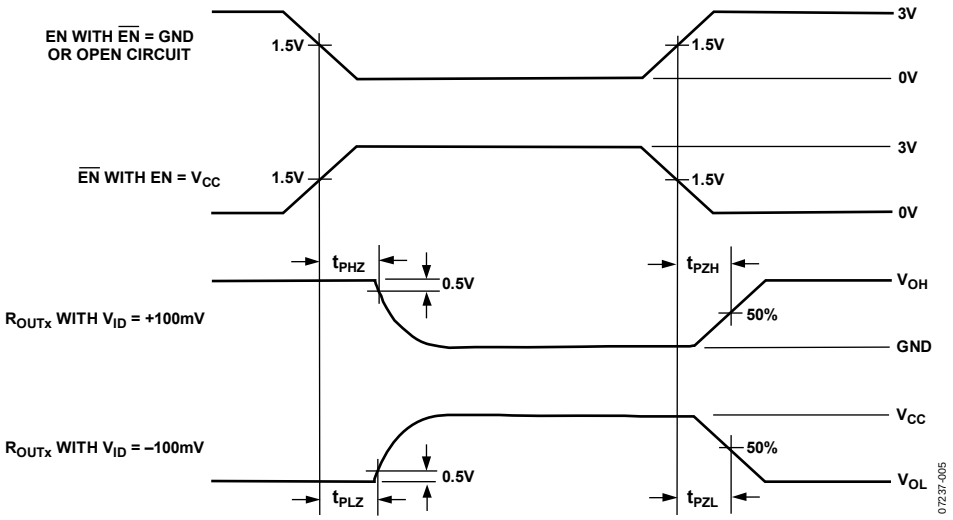

Figure 5. Receiver Enable/Disable Delay Waveforms

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC} to GND	−0.3 V to +4 V
Input Voltage (R_{INx+}, R_{INx-}) to GND	−0.3 V to V_{CC} + 0.3 V
Enable Input Voltage (EN, $\overline{EN}$) to GND	−0.3 V to V_{CC} + 0.3 V
Output Voltage (R_{OUTx}) to GND	−0.3 V to V_{CC} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\,MAX}$)	150°C
Power Dissipation	$(T_{J\,MAX} - T_A)/\theta_{JA}$
Thermal Impedance, θ_{JA}	
TSSOP Package	150.4°C/W
SOIC Package	125°C/W ± 5°C
Reflow Soldering Peak Temperature	
Pb-Free	260°C ± 5°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

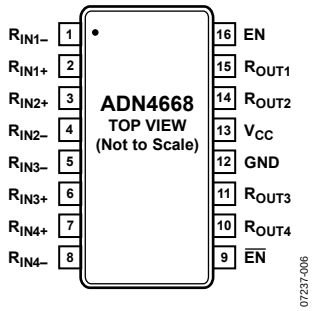

Figure 6. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_{IN1-}	Receiver Channel 1 Inverting Input. When this input is more negative than R_{IN1+}, R_{OUT1} is high. When this input is more positive than R_{IN1+}, R_{OUT1} is low.
2	R_{IN1+}	Receiver Channel 1 Noninverting Input. When this input is more positive than R_{IN1-}, R_{OUT1} is high. When this input is more negative than R_{IN1-}, R_{OUT1} is low.
3	R_{IN2+}	Receiver Channel 2 Noninverting Input. When this input is more positive than R_{IN2-}, R_{OUT2} is high. When this input is more negative than R_{IN2-}, R_{OUT2} is low.
4	R_{IN2-}	Receiver Channel 2 Inverting Input. When this input is more negative than R_{IN2+}, R_{OUT2} is high. When this input is more positive than R_{IN2+}, R_{OUT2} is low.
5	R_{IN3-}	Receiver Channel 3 Inverting Input. When this input is more negative than R_{IN3+}, R_{OUT3} is high. When this input is more positive than R_{IN3+}, R_{OUT3} is low.
6	R_{IN3+}	Receiver Channel 3 Noninverting Input. When this input is more positive than R_{IN3-}, R_{OUT3} is high. When this input is more negative than R_{IN3-}, R_{OUT3} is low.
7	R_{IN4+}	Receiver Channel 4 Noninverting Input. When this input is more positive than R_{IN4-}, R_{OUT4} is high. When this input is more negative than R_{IN4-}, R_{OUT4} is low.
8	R_{IN4-}	Receiver Channel 4 Inverting Input. When this input is more negative than R_{IN4+}, R_{OUT4} is high. When this input is more positive than R_{IN4+}, R_{OUT4} is low.
9	$\overline{EN}$	Active-Low Enable and Power-Down Input with Pull-Down (3 V TTL/CMOS). When EN is held high, $\overline{EN}$ enables the receiver outputs when $\overline{EN}$ is low or open circuit and puts the receiver outputs into a high impedance state and powers down the device when $\overline{EN}$ is high.
10	R_{OUT4}	Receiver Channel 4 Output (3 V TTL/CMOS). If the differential input voltage between R_{IN4+} and R_{IN4-} is positive, this output is high. If the differential input voltage is negative, this output is low.
11	R_{OUT3}	Receiver Channel 3 Output (3 V TTL/CMOS). If the differential input voltage between R_{IN3+} and R_{IN3-} is positive, this output is high. If the differential input voltage is negative, this output is low.
12	GND	Ground Reference Point for All Circuitry on the Part.
13	V_{CC}	Power Supply Input. These parts can be operated from 3.0 V to 3.6 V.
14	R_{OUT2}	Receiver Channel 2 Output (3 V TTL/CMOS). If the differential input voltage between R_{IN2+} and R_{IN2-} is positive, this output is high. If the differential input voltage is negative, this output is low.
15	R_{OUT1}	Receiver Channel 1 Output (3 V TTL/CMOS). If the differential input voltage between R_{IN1+} and R_{IN1-} is positive, this output is high. If the differential input voltage is negative, this output is low.
16	EN	Active-High Enable and Power-Down Input (3 V TTL/CMOS). When $\overline{EN}$ is held low or open circuit, EN enables the receiver outputs when EN is high and puts the receiver outputs into a high impedance state and powers down the device when EN is low.

TYPICAL PERFORMANCE CHARACTERISTICS

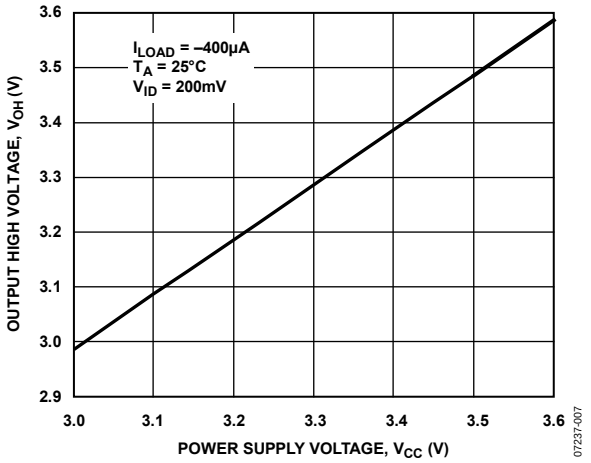

Figure 7. Output High Voltage, V_{OH} vs. Power Supply Voltage, V_{CC}

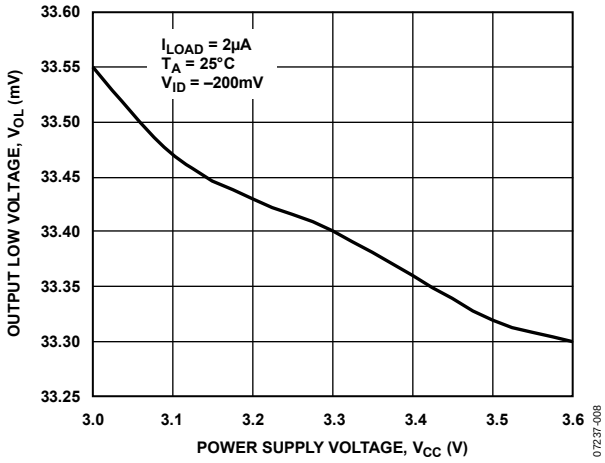

Figure 8. Output Low Voltage, V_{OL} vs. Power Supply Voltage, V_{CC}

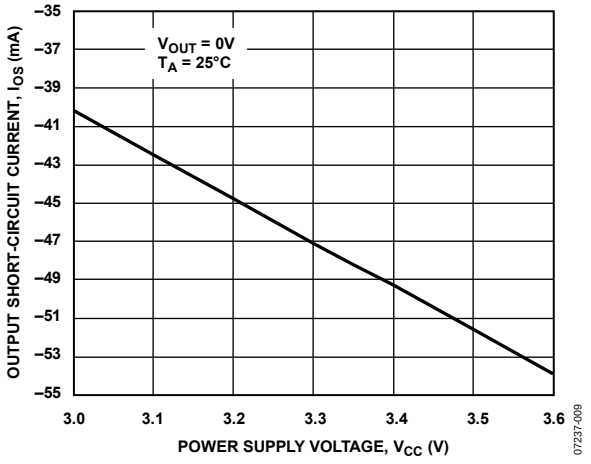

Figure 9. Output Short-Circuit Current, I_{OS} vs. Power Supply Voltage, V_{CC}

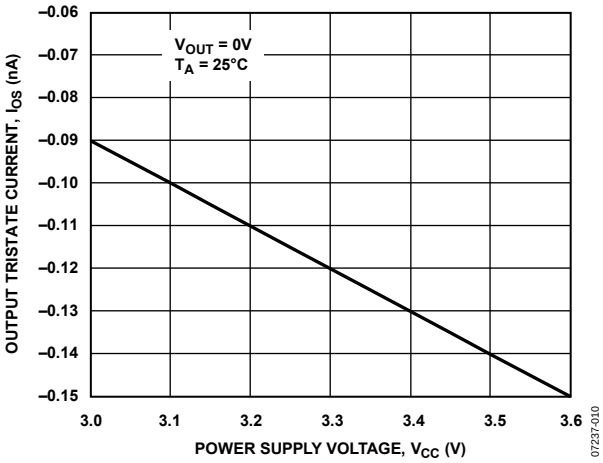

Figure 10. Output Tristate Current, I_{OS} vs. Power Supply Voltage, V_{CC}

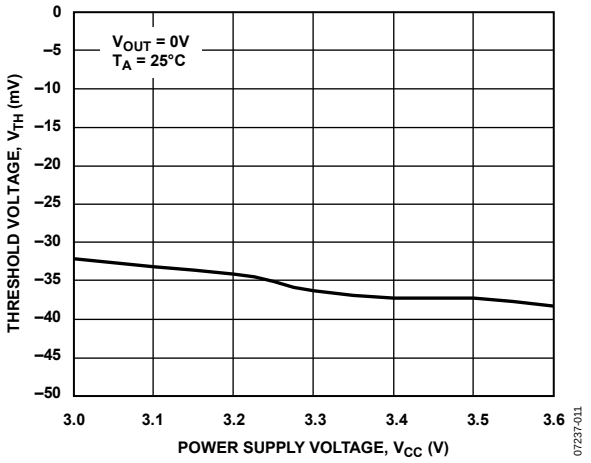

Figure 11. Threshold Voltage, V_{TH} vs. Power Supply Voltage, V_{CC}

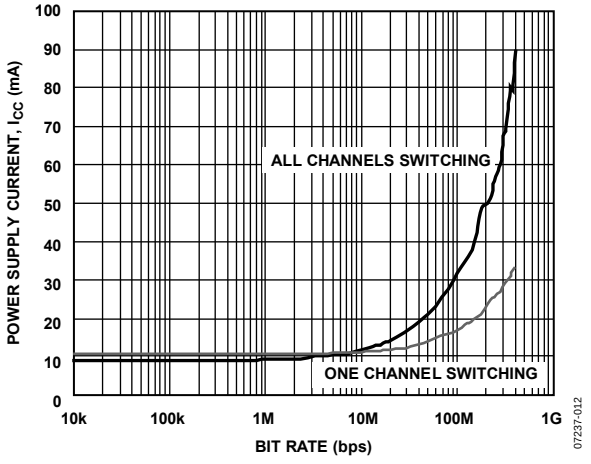

Figure 12. Power Supply Current, I_{CC} vs. Bit Rate

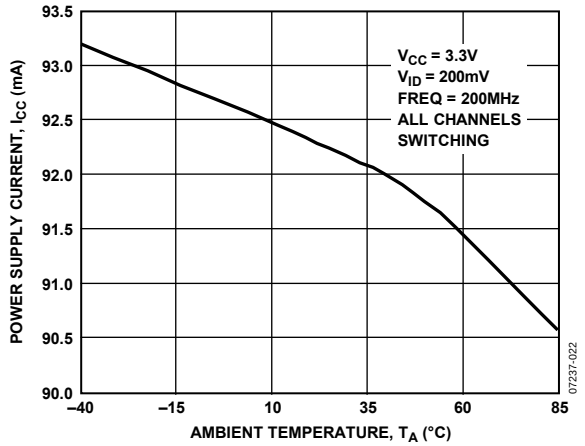

Figure 13. Power Supply Current, I_{CC} vs. Ambient Temperature, T_A

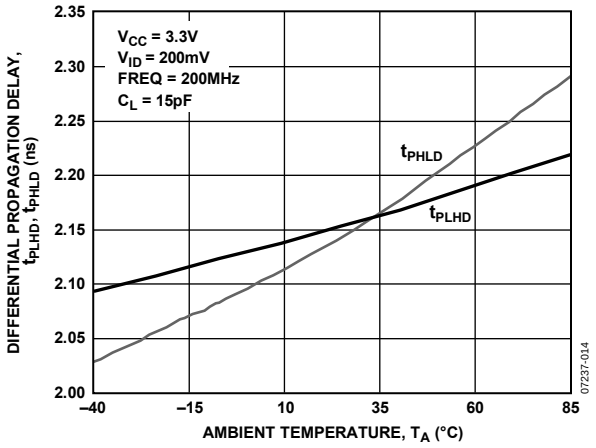

Figure 14. Differential Propagation Delay, t_{PLHD}, t_{PHLD} vs. Ambient Temperature, T_A

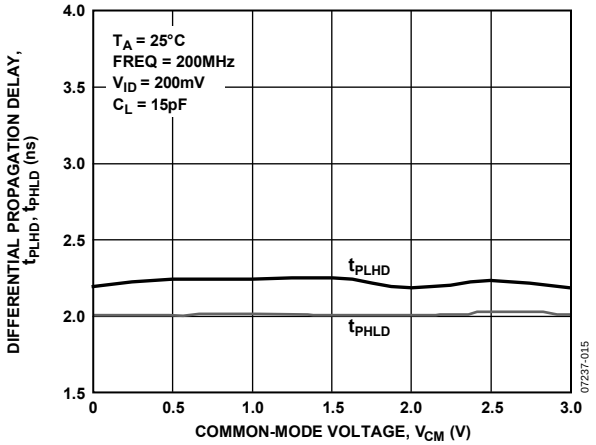

Figure 15. Differential Propagation Delay, t_{PLHD}, t_{PHLD} vs. Common-Mode Voltage, V_{CM}

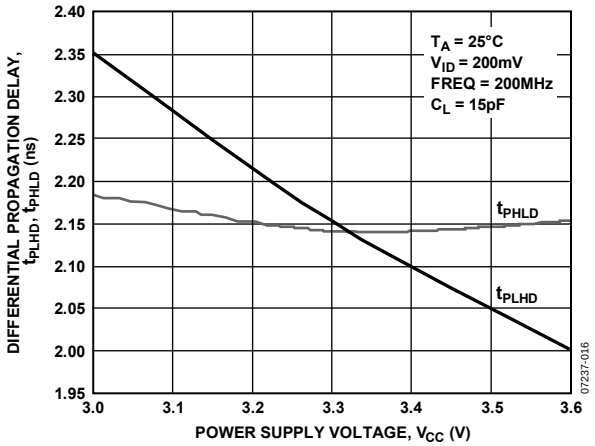

Figure 16. Differential Propagation Delay, t_{PLHD}, t_{PHLD} vs. Power Supply Voltage, V_{CC}

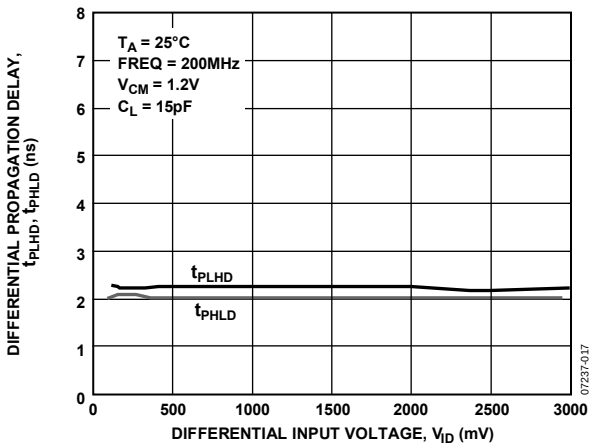

Figure 17. Differential Propagation Delay, t_{PLHD}, t_{PHLD} vs. Differential Input Voltage, V_{ID}

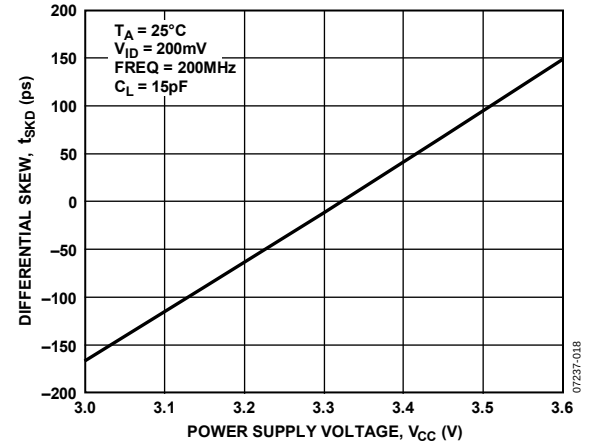

Figure 18. Differential Skew, t_{SKD} vs. Power Supply Voltage, V_{CC}

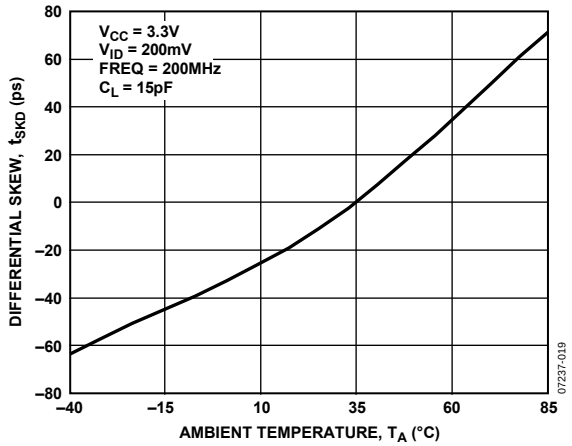

Figure 19. Differential Skew, t_{SKD} vs. Ambient Temperature, T_A

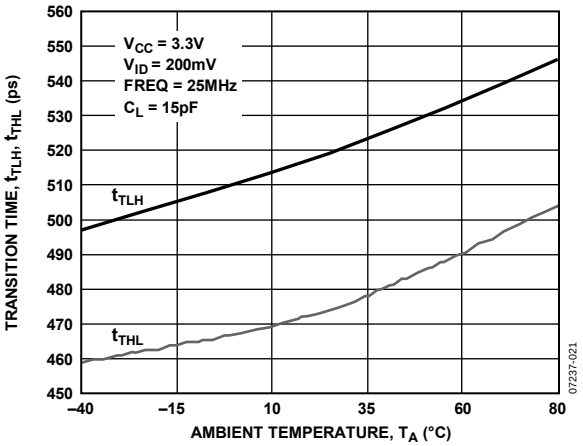

Figure 21. Transition Time, t_{TLH}, t_{THL} vs. Ambient Temperature, T_A

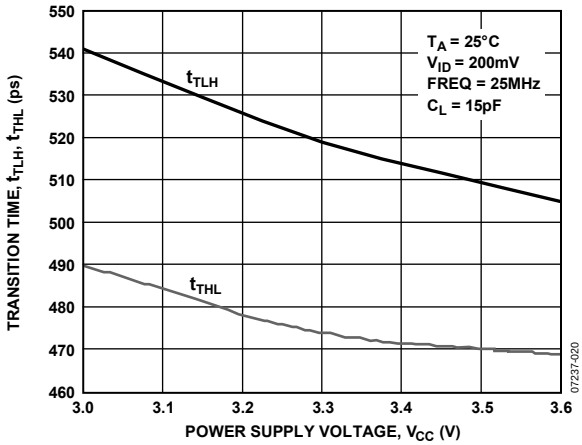

Figure 20. Transition Time, t_{TLH}, t_{THL} vs. Power Supply Voltage, V_{CC}

THEORY OF OPERATION

The ADN4668 is a quad-channel line receiver for low voltage differential signaling. It takes a differential input signal of 310 mV typical and converts it into a single-ended 3 V TTL/CMOS logic signal.

A differential current input signal, received via a transmission medium such as a twisted pair cable, develops a voltage across a terminating resistor, R_T. This resistor is chosen to match the characteristic impedance of the medium, typically around 100 Ω. The differential voltage is detected by the receiver and converted back into a single-ended logic signal.

When the noninverting receiver input, R_{INx+}, is positive with respect to the inverting input, R_{INx-} (current flows through R_T from R_{INx+} to R_{INx-}), R_{OUTx} is high. When the noninverting receiver input, R_{IN+}, is negative with respect to the inverting input, R_{INx-} (current flows through R_T from R_{INx-} to R_{INx+}), R_{OUTx} is low.

Using the ADN4667 as a driver, the received differential current is between ±2.5 mA and ±4.5 mA (±3.1 mA typical), developing between ±250 mV and ±450 mV across a 100 Ω termination resistor. The received voltage is centered on the receiver offset of 1.2 V. The noninverting receiver input is typically (1.2 V + [310 mV/2]) = 1.355 V, and the inverting receiver input is (1.2 V − [310 mV/2]) = 1.045 V for Logic 1. For Logic 0, the inverting and noninverting input voltages are reversed. Note that because the differential voltage reverses polarity, the peak-to-peak voltage swing across R_T is twice the differential voltage.

Current-mode signaling offers considerable advantages over voltage-mode signaling, such as the RS-422. The operating current remains fairly constant with increased switching frequency, whereas the operating current of voltage-mode drivers increases exponentially in most cases. This increase is caused by the overlap as internal gates switch between high and low, causing currents to flow from V_{CC} to ground. A current-mode device reverses a constant current between its two outputs, with no significant overlap currents.

This is similar to emitter-coupled logic (ECL) and positive emitter-coupled logic (PECL), but without the high quiescent current of ECL and PECL.

ENABLE INPUTS

The ADN4668 has active-high and active-low enable inputs that put all the logic outputs into a high impedance state when disabled, reducing device current consumption from 9 mA typical to 1 mA typical. See Table 5 for a truth table of the enable inputs.

Table 5. Enable Inputs Truth Table

EN	$\overline{EN}$	R_{INx+}	R_{INx-}	R_{OUTx}
High	Low or Open	1.045 V	1.355 V	0
High	Low or Open	1.355 V	1.045 V	1
Any other combination of EN and $\overline{EN}$		X	X	High-Z

APPLICATIONS INFORMATION

Figure 22 shows a typical application for point-to-point data transmission using the ADN4667 as the driver and the ADN4668 as the receiver.

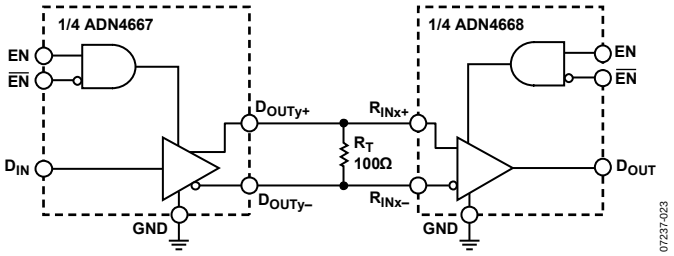

Figure 22. Typical Application Circuit