Data Sheet

ADN4693E-1

3.3 V, 200 Mbps, Full-Duplex, High Speed M-LVDS Transceiver

FEATURES

- Full-duplex M-LVDS transceiver (driver and receiver pair)
- Switching rate: 200 Mbps (100 MHz)
- Type 1 receiver with input hysteresis of 25 mV
- Compatible with the TIA/EIA-899 standard for M-LVDS
- Glitch free power-up/power-down on M-LVDS bus
- Controlled transition times on driver output
- Common-mode range: −1 V to +3.4 V, allowing communication with 2 V of ground noise
- Driver outputs high-Z when disabled or powered off
- Enhanced ESD protection on bus pins
  - ≥±15 kV HBM, air discharge
  - ≥±8 kV HBM, contact discharge
  - ≥±10 kV IEC 61000-4-2, air discharge
  - ≥±8 kV IEC 61000-4-2, contact discharge
- Operating junction temperature range: −40°C to +120°C
- 16-lead, 4 mm × 4 mm LFCSP

APPLICATIONS

- Backplane and cable multipoint data transmission
- Multipoint clock distribution
- Low power, high speed alternative to shorter RS-485 links
- Networking and wireless base station infrastructure
- Grid infrastructure and relay protection systems

FUNCTIONAL BLOCK DIAGRAM

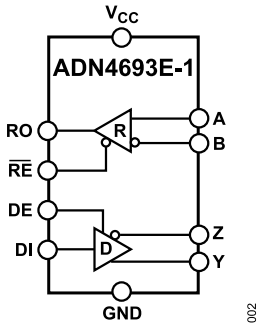

Figure 1.

GENERAL DESCRIPTION

The ADN4693E-1 is a multipoint, low voltage differential signaling (M-LVDS) transceiver (driver and receiver pair) that can operate at up to 200 Mbps (100 MHz) nonreturn to zero (NRZ). The receiver detects the bus state with a differential input of as little as ±50 mV over the common-mode voltage range of the device. Electrostatic discharge (ESD) protection of up to ±15 kV is implemented on the bus pins. The ADN4693E-1 is designed to the TIA/EIA-899 standard for use in M-LVDS networks and complements TIA/EIA-644 LVDS devices with additional multipoint capabilities.

The ADN4693E-1 features a Type 1 receiver with 25 mV of hysteresis so that slow-changing signals or loss of input does not lead to output oscillations.

This full-duplex device is available in a compact 16-lead, 4 mm × 4 mm lead frame chip scale package (LFCSP). The ADN4693E-1 is specified over the −40°C to +120°C junction temperature range.

Rev. 0

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REVISION HISTORY

3/2022—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V, load resistance (R_L) = 50 Ω, and T_J = −40ºC to +120ºC, unless otherwise noted. All typical values are at T_A = 25 ºC and V_{CC} = 3.3 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Differential Outputs						
Differential Output Voltage Magnitude	$\|V_{OD}\|$	450	580	680	mV	See Figure 20
$\Delta\|V_{OD}\|$ for Complementary Output States	$\Delta\|V_{OD}\|$	−50	0	+50	mV	See Figure 20
Common-Mode Output Voltage (Steady State)	$V_{OS(SS)}$	0.8		1.2	V	See Figure 21 and Figure 24
$\Delta V_{OS(SS)}$ for Complementary Output States	$\Delta V_{OS(SS)}$	−50	0	+50	mV	See Figure 21 and Figure 24
Peak-to-Peak V_{OS}[1]	$V_{OS(PP)}$			150	mV	See Figure 21 and Figure 24
Maximum Steady State Open Circuit Output Voltage	$V_{Y(O)}$ or $V_{Z(O)}$	0		2.4	V	See Figure 22
Voltage Overshoot[1]						
Low to High	V_{PH}			1.2 V_{SS}	V	See Figure 25 and Figure 28
High to Low	V_{PL}	−0.2 V_{SS}			V	See Figure 25 and Figure 28
Output Current						
Short Circuit	$\|I_{OS}\|$			24	mA	See Figure 23
High Impedance State	I_{OZ}	−15		+10	µA	–1.4 V ≤ (V_Y or V_Z) ≤ 3.8 V, other output = 1.2 V
Power Off	$I_{O(OFF)}$	−10		+10	µA	–1.4 V ≤ (V_Y or V_Z) ≤ 3.8 V, other output = 1.2 V, 0 V ≤ V_{CC} ≤ 1.5 V
Output Capacitance	C_Y or C_Z		12.8	14	pF	V_I = 0.4 sin(30e^{6}πt) V[1, 2], DE = 0 V
Differential Output Capacitance	C_{YZ}		8		pF	V_{AB} = 0.4 sin(30e^{6}πt) V[1], DE = 0 V
Output Capacitance Balance (C_Y/C_Z)	$C_{Y/Z}$	0.98		1.04		DE = 0 V[1]
Logic Inputs (DI, DE)						
Input Voltage						
High	V_{IH}	2		V_{CC}	V	
Low	V_{IL}	GND		0.8	V	
Input High Current	I_{IH}	0		10	µA	V_{IH} = 2 V
Input Low Current	I_{IL}	0		10	µA	V_{IL} = 0.8 V
Input Capacitance	C_{IN}		3		pF	V_I = 0.2 sin(30e^{6}πt) V[1]
RECEIVER						
Differential Inputs						
Differential Input Threshold Voltage						See Table 2 and Figure 37
Type 1 Receiver	V_{TH}	−50		+50	mV	V_{CM} = 0 V to 3.4 V
	V_{TH}	−70		+70	mV	V_{CM} = −1 V to +3.4 V
Input Hysteresis						
Type 1 Receiver	V_{HYS}		25		mV	V_{CM} = −1 V to +3.4 V
Differential Input Voltage Magnitude	$\|V_{ID}\|$	0.05		V_{CC}	V	
Input Capacitance	C_A or C_B		3	4	pF	V_I = 0.4 sin(30e^{6}πt)[1, 2]
Differential Input Capacitance	C_{AB}		3		pF	V_{AB} = 0.4 sin(30e^{6}πt)[1]
Input Capacitance Balance (C_A/C_B)[1]	$C_{A/B}$	0.91		1.01		
Logic Output RO						
Output Voltage						
High	V_{OH}	2.4			V	Output high current (I_{OH}) = –8 mA
Low	V_{OL}			0.4	V	Output low current (I_{OL}) = 8 mA
High Impedance Output Current	I_{OZ}	−10		+15	µA	Output voltage (V_O) = 0 V or 3.6 V

SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic Input $\overline{RE}$						
Input Voltage						
High	V_{IH}	2		V_{CC}	V	
Low	V_{IL}	GND		0.8	V	
Input High Current	I_{IH}	−10		0	µA	V_{IH} = 2 V
Input Low Current	I_{IL}	−10		0	µA	V_{IL} = 0.8 V
Input Current (A, B)						
Receiver Input A	I_A	0		32	µA	V_B = 1.2 V, V_A = 3.8 V
		−20		+20	µA	V_B = 1.2 V, V_A = 0 V or 2.4 V
		−32		0	µA	V_B = 1.2 V, V_A = −1.4 V
Receiver Input B	I_B	0		32	µA	V_A = 1.2 V, V_B = 3.8 V
		−20		+20	µA	V_A = 1.2 V, V_B = 0 V or 2.4 V
		−32		0	µA	V_A = 1.2 V, V_B = −1.4 V
Differential Balance	I_{AB}	−4		+4	µA	$V_A = V_B$, 1.4 V ≤ V_A ≤ 3.8 V
Power-Off Input Current						0 V ≤ V_{CC} ≤ 1.5 V
Receiver Input A	$I_{A(OFF)}$	0		32	µA	V_B = 1.2 V, V_A = 3.8 V
		−20		+20	µA	V_B = 1.2 V, V_A = 0 V or 2.4 V
		−32		0	µA	V_B = 1.2 V, V_A = −1.4 V
Receiver Input B	$I_{B(OFF)}$	0		32	µA	V_A = 1.2 V, V_B = 3.8 V
		−20		+20	µA	V_A = 1.2 V, V_B = 0 V or 2.4 V
		−32		0	µA	V_A = 1.2 V, V_B = −1.4 V
Differential Balance	$I_{AB(OFF)}$	−4		+4	µA	$V_A = V_B$, 1.4 V ≤ V_A ≤ 3.8 V
POWER SUPPLY						
Supply Current	I_{CC}					
Only Driver Enabled			13	22	mA	DE, $\overline{RE}$ = V_{CC}, R_L = 50 Ω
Both Driver and Receiver Disabled			1	4	mA	DE = 0 V, = V_{CC}, R_L = no load
Both Driver and Receiver Enabled			16	24	mA	DE = V_{CC}, $\overline{RE}$ = 0 V, R_L = 50 Ω
Only Receiver Enabled			4	13	mA	DE, $\overline{RE}$ = 0 V, R_L = 50 Ω

[1] These specifications are guaranteed by design and characterization.

[2] HP4194A impedance analyzer (or equivalent).

RECEIVER INPUT THRESHOLD TEST VOLTAGES

$\overline{RE}$ = 0 V.

Table 2. Test Voltages for Type 1 Receiver

Applied Voltages		Input Voltage, Differential	Input Voltage, Common Mode	Receiver Output
V_A (V)	V_B (V)	V_{ID} (V)	V_{IC} (V)	RO (V)
+2.4	0	+2.4	+1.2	High
0	+2.4	−2.4	+1.2	Low
+0.05	0	+0.05	+0.025	High
+0	+0.05	−0.05	+0.025	Low
+3.4	+3.35	+0.05	+3.375	High
+3.35	+3.4	−0.05	+3.375	Low
−0.93	−1	+0.07	−0.965	High
−1	−0.93	−0.07	−0.965	Low

SPECIFICATIONS

TIMING SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V and T_J = −40°C to +120°C, unless otherwise noted. All typical values are given for V_{CC} = 3.3 V and T_A = 25°C.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate[1]		200			Mbps	
Propagation Delay[1]	t_{PLH}, t_{PHL}	1.5	1.8	2.3	ns	See Figure 25 and Figure 28
Differential Output Rise and Fall Time[1]	t_R, t_F	1.1	1.2	1.4	ns	See Figure 25 and Figure 28
Pulse Skew $\lvert t_{PHL} - t_{PLH} \rvert$[1]	t_{SK}		0	100	ps	See Figure 25 and Figure 28
Part-to-Part Skew[1,2]	$t_{SK(PP)}$			300	ps	See Figure 25 and Figure 28
Period Jitter, RMS (1 Standard Deviation)[1]	$t_{J(PER)}$			3.5	ps	62.5 MHz clock input[3] (see Figure 27)
			2	3.5	ps	100 MHz clock input[3] (see Figure 27)
Peak-to-Peak Jitter[1,4]	$t_{J(PP)}$		90	210	ps	200 Mbps 2^{15} − 1 PRBS input[5] (see Figure 30)
				190	ps	200 Mbps 8b10 input[5] (see Figure 30)
				180	ps	125 Mbps 8b10 input[5] (see Figure 30)
Disable Time[1]						
From High Level	t_{PHZ}			7	ns	See Figure 26 and Figure 29
From Low Level	t_{PLZ}			7	ns	See Figure 26 and Figure 29
Enable Time[1]						
To High Level	t_{PZH}			7	ns	See Figure 26 and Figure 29
To Low Level	t_{PZL}			7	ns	See Figure 26 and Figure 29
RECEIVER						
Propagation Delay[1]	t_{RPLH}, t_{RPHL}	3	3.5	4.6	ns	C_L = 15 pF (see Figure 31 and Figure 34)
Rise and Fall Time[1]	t_R, t_F	0.8		2.6	ns	C_L = 15 pF (see Figure 31 and Figure 34)
Pulse Skew $\lvert t_{RPHL} - t_{RPLH} \rvert$[1]	t_{SK}			660	ps	C_L = 15 pF (see Figure 31 and Figure 34)
Part-to-Part Skew[1,2]	$t_{SK(PP)}$			800	ps	C_L = 15 pF (see Figure 31 and Figure 34)
Period Jitter, RMS (1 Standard Deviation)[1]				7.5	ps	62.5 MHz clock input[6] (see Figure 33 and Figure 27)
	$t_{J(PER)}$		2.5	6	ps	100 MHz clock input[6] (see Figure 33)
Peak-to-Peak Jitter[1,4]	$t_{J(PP)}$		300	720	ps	200 Mbps 2^{15} − 1 PRBS input[7] (see Figure 36)
				700	ps	200 Mbps 8b10 input[7] (see Figure 36 and Figure 30)
				575	ps	125 Mbps 8b10 input[7] (see Figure 36 and Figure 30)
Disable Time[1]						
From High Level	t_{RPHZ}			10	ns	See Figure 32 and Figure 35
From Low Level	t_{RPLZ}			10	ns	See Figure 32 and Figure 35
Enable Time[1]						
To High Level	t_{RPZH}			15	ns	See Figure 32 and Figure 35
To Low Level	t_{RPZL}			15	ns	See Figure 32 and Figure 35

[1] Timing specifications are guaranteed by design and characterization. Jitter values do not include stimulus jitter.

[2] $t_{SK(PP)}$ is defined as the difference between the propagation delays of two devices between any specified terminals. This specification applies to devices at the same V_{CC} and temperature, and with identical packages and test circuits.

[3] t_R = t_F = 0.5 ns (10% to 90%), measured over 30,000 samples.

[4] Peak-to-peak jitter specifications include jitter due to pulse skew (t_{SK}).

[5] t_R = t_F = 0.5 ns (10% to 90%), measured over 100,000 samples.

[6] $|V_{ID}|$ = 400 mV, V_{IC} = 1.1 V, t_R = t_F = 0.5 ns (10% to 90%), measured over 30,000 samples.

[7] $|V_{ID}|$ = 400 mV, V_{IC} = 1.1 V, t_R = t_F = 0.5 ns (10% to 90%), measured over 100,000 samples.

ABSOLUTE MAXIMUM RATINGS

$T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Rating
V_{CC}	−0.5 V to +4 V
Digital Input Voltage (DE, $\overline{RE}$, DI)	−0.5 V to +4 V
Receiver Input (A, B) Voltage	−4 V to +6 V
Receiver Output Voltage (RO)	−0.3 V to +4 V
Driver Output (Y, Z) Voltage	−1.8 V to +4 V
Operating Junction Temperature Range	−40°C to +120°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

The junction temperature (T_J) refers to the temperature of the silicon die within the package of the device when the device is powered. The ADN4693E-1 parameters are specified over an operating junction temperature range of −40°C to +120°C.

Monitoring the ambient temperature (T_A) with the power dissipation (P_D) and an accurate thermal model ensures that T_J is within the specified temperature limits.

Use T_J and P_D to calculate T_A, as follows

$$T_A = T_J - P_D \times \theta_{JA}$$

where θ_{JA} is the junction to ambient thermal resistance of the package.

M-LVDS transceivers are designed for use in high speed clock and data distribution applications. In applications where the M-LVDS transmitter outputs are held in a dc state for the lifetime of the device, the operating junction temperature must be controlled to ≤105°C.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operation environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction-to-case-bottom thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-16-17[1, 2]	50.6	4.6	°C/W

[1] Thermal impedance measured values are based on still air measurements on a four-layer PCB.

[2] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with nine thermal vias. See JEDEC JESD51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2

ESD Ratings for ADN4693E-1

Table 6. ADN4693E-1, 16-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	≥±4,000 (contact discharge)	3A[1]
	≥±8,000 (contact discharge)	3B[2]
	≥±15,000 (air discharge)	3B[2]
FICDM	≥±1,250	C3[1]
IEC	≥±8,000 (contact discharge)	Level 4[2]
	≥±10,000 (air discharge)	Level 3[2]

[1] This class is for all pins.

[2] This class is for the A, B, Y, and Z pins only.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

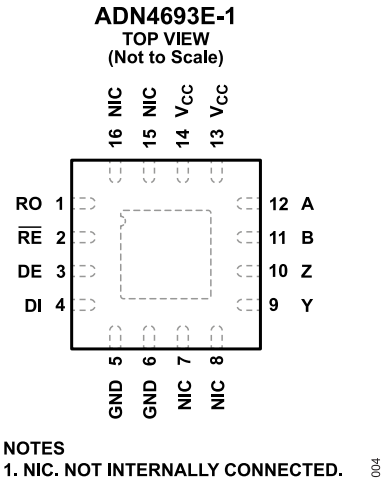


Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output. Type 1 receiver, when enabled: If A − B ≥ 50 mV, then RO = logic high. If A − B ≤ −50 mV, then RO = logic low. Receiver output is undefined outside these conditions.
2	$\overline{RE}$	Receiver Output Enable. A logic low on this pin enables the receiver output, RO. A logic high on this pin places RO in a high impedance state.
3	DE	Driver Output Enable. A logic high on this pin enables the driver differential outputs. A logic low on this pin places the driver differential outputs in a high impedance state.
4	DI	Full duplex, when enabled: A logic low on DI forces Y low and Z high, whereas a logic high on DI forces Y high and Z low.
5, 6	GND	Ground.
7, 8, 15, 16	NIC	Not Internally Connected.
9	Y	Noninverting Driver Output Y.
10	Z	Inverting Driver Output Z.
11	B	Inverting Receiver Input B.
12	A	Noninverting Receiver Input A.
13, 14	V_{CC}	Power Supply (3.3 V ± 0.3 V).

TYPICAL PERFORMANCE CHARACTERISTICS

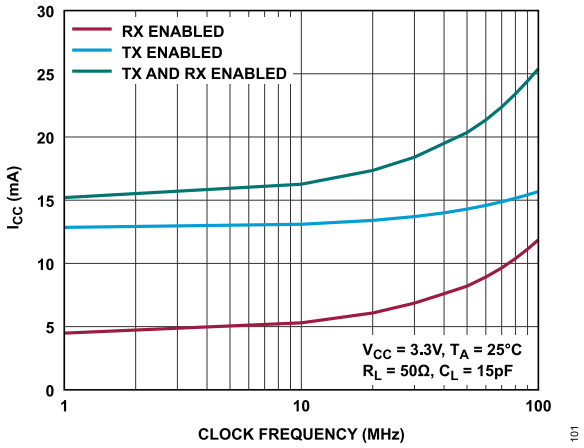


Figure 3. Power Supply Current (I_{CC}) vs. Clock Frequency

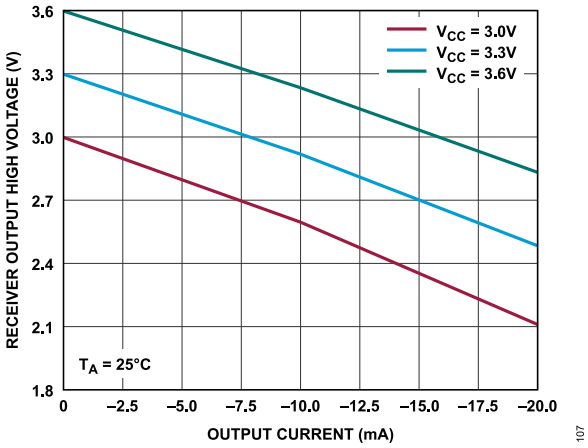


Figure 6. Receiver Output High Voltage vs. Output Current

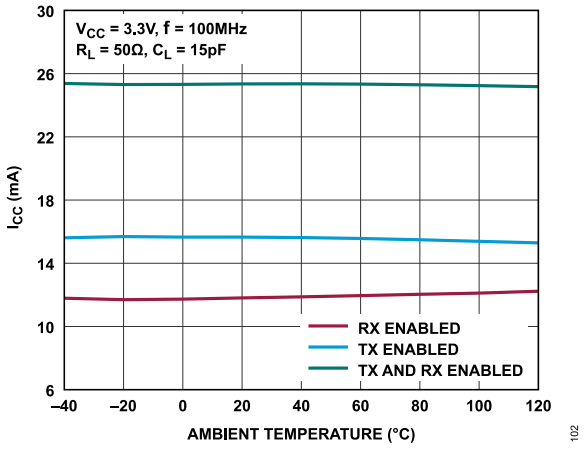


Figure 4. I_{CC} vs. Ambient Temperature (Clock Input)

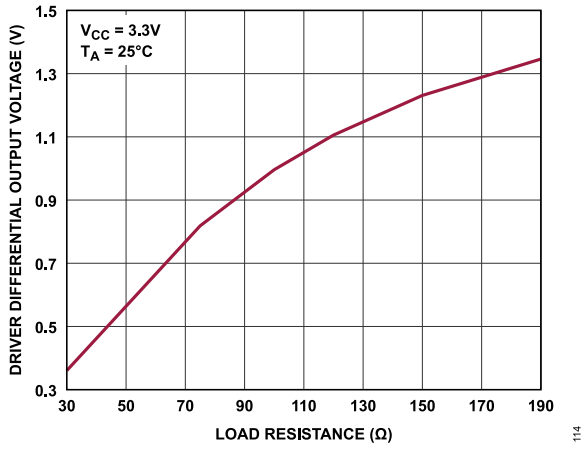


Figure 7. Driver Differential Output Voltage vs. Load Resistance

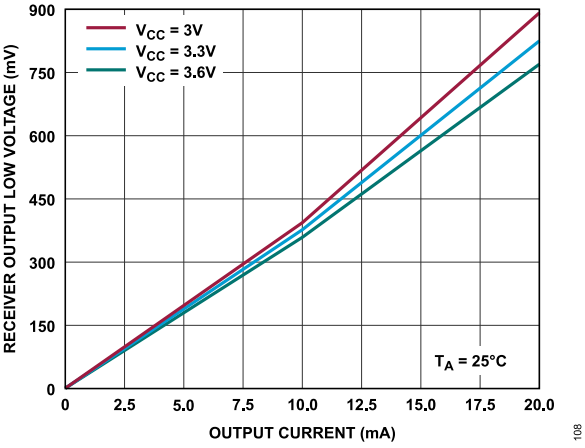


Figure 5. Receiver Output Low Voltage vs. Output Current

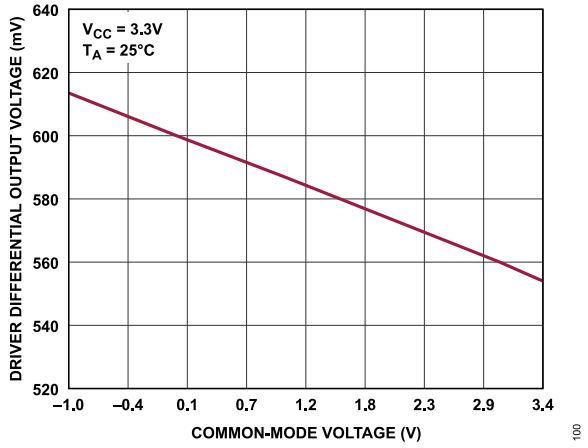


Figure 8. Driver Differential Output Voltage vs. Common-Mode Voltage (See Figure 21)

TYPICAL PERFORMANCE CHARACTERISTICS

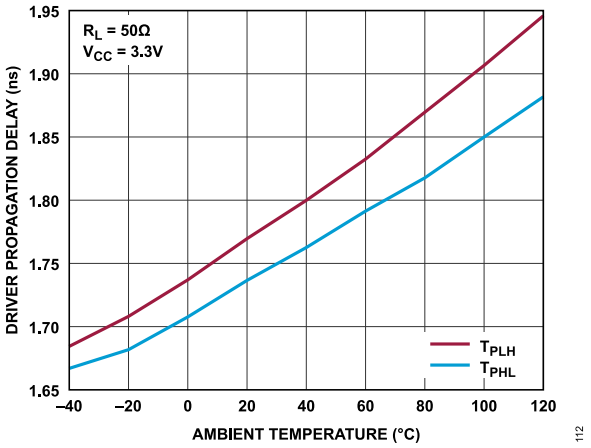


Figure 9. Driver Propagation Delay vs. Ambient Temperature (Clock Frequency = 100 MHz)

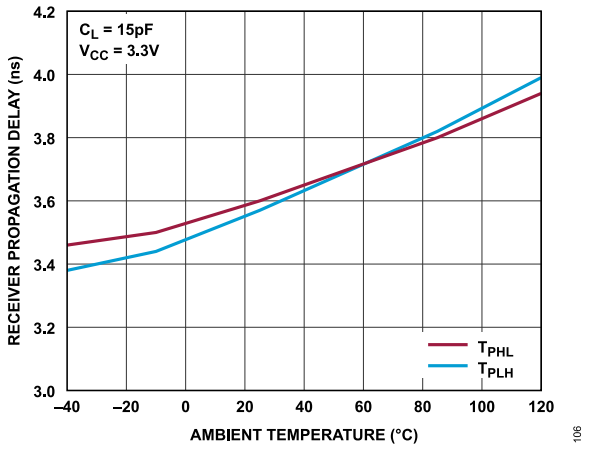


Figure 10. Receiver Propagation Delay vs. Ambient Temperature (Clock Frequency = 100 MHz, V_{ID} = 300 mV, V_{IC} = 1.1 V)

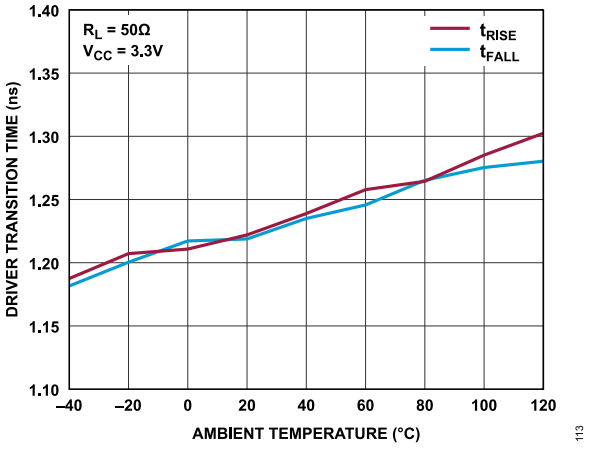


Figure 11. Driver Transition Time vs. Ambient Temperature

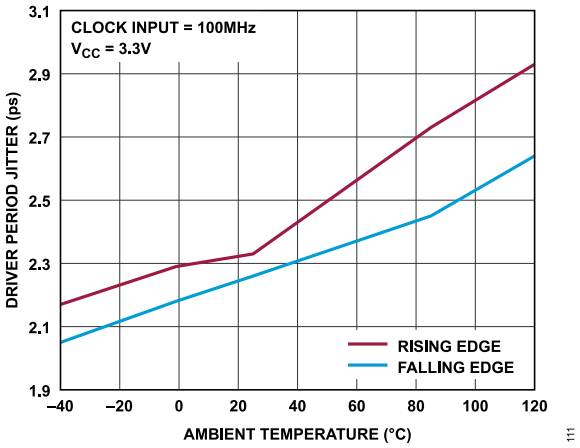


Figure 12. Driver Period Jitter vs. Ambient Temperature

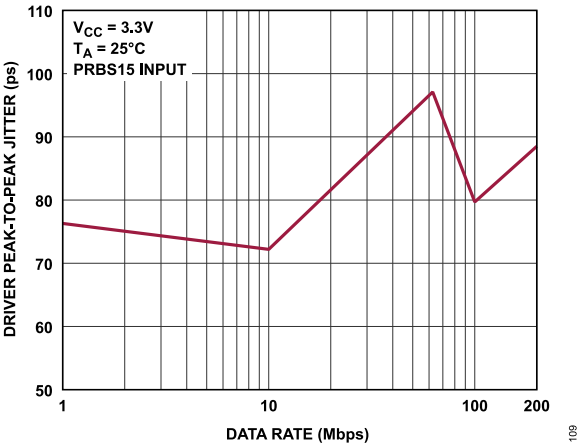


Figure 13. Driver Peak-to-Peak Jitter vs. Data Rate

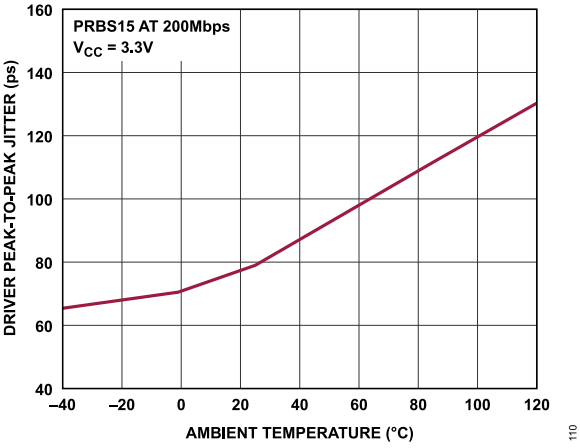


Figure 14. Driver Peak-to-Peak Jitter vs. Ambient Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

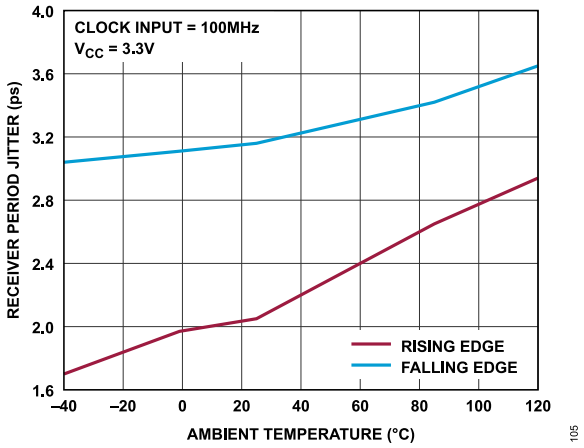


Figure 15. Receiver Period Jitter vs. Ambient Temperature (V_{ID} = 400 mV, V_{IC} = 1.1 V)

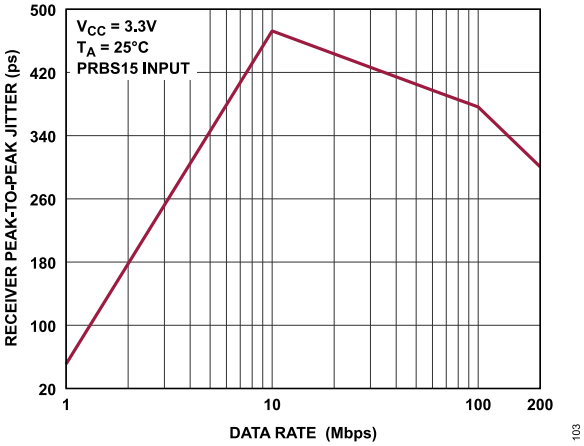


Figure 16. Receiver Peak-to-Peak Jitter vs. Data Rate (V_{ID} = 400 mV, V_{IC} = 1.1 V)

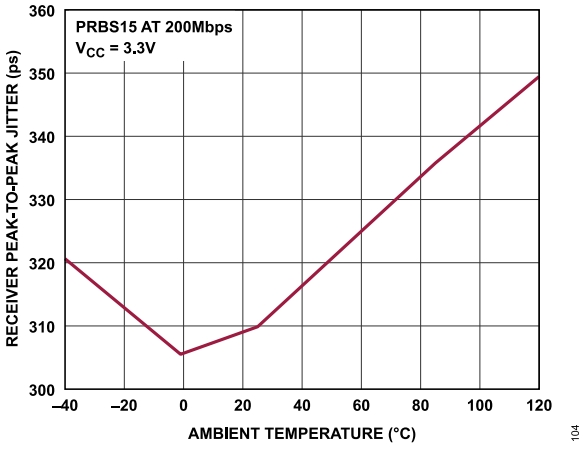


Figure 17. Receiver Peak-to-Peak Jitter vs. Ambient Temperature (V_{ID} = 400 mV, V_{IC} = 1.1 V)

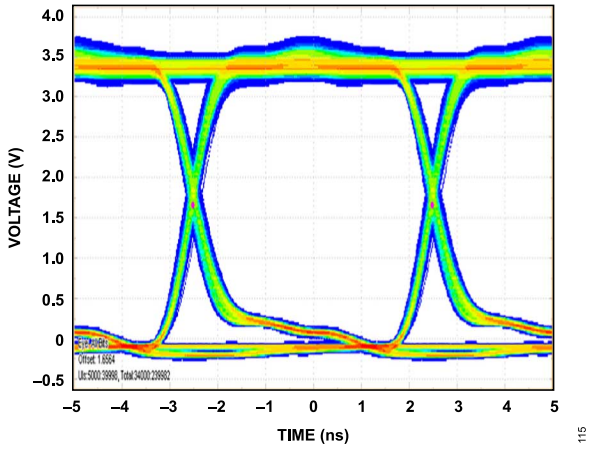


Figure 18. ADN4693E-1 Driver Output Eye Pattern (V_{CC} = 3.3 V, T_A = 25°C, Data Rate = 200 Mbps, PRBS 2^{15} − 1 Input, R_L = 50 Ω)

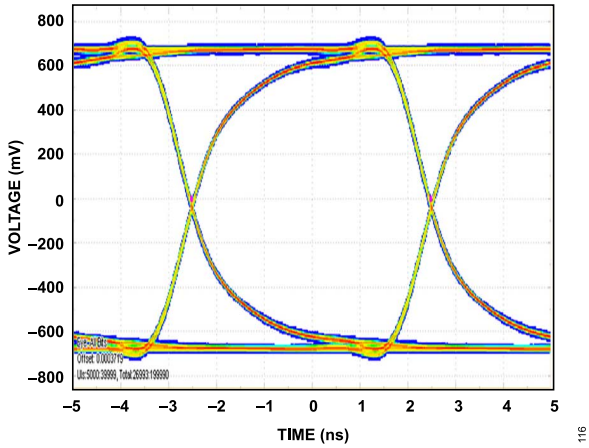
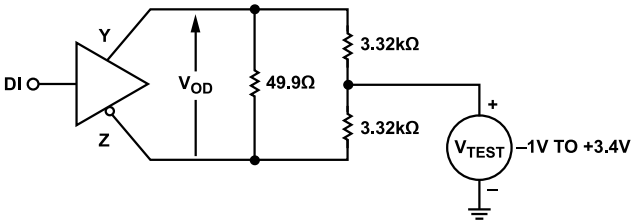


Figure 19. ADN4693E-1 Receiver Output Eye Pattern (V_{CC} = 3.3 V, T_A = 25°C, Data Rate = 200 Mbps, PRBS 2^{15} − 1 Input, C_L = 15 pF)

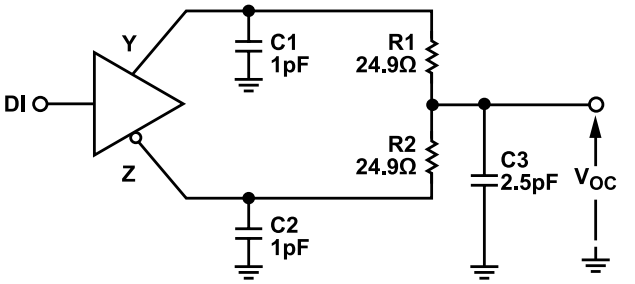
TEST CIRCUITS AND SWITCHING CHARACTERISTICS

DRIVER VOLTAGE AND CURRENT MEASUREMENTS



NOTES
1. 1% TOLERANCE FOR ALL RESISTORS.

Figure 20. Driver Voltage Measurement over Common-Mode Range (V_{TEST} Is the Test Voltage)



NOTES
1. C1, C2, AND C3 ARE 20% AND INCLUDE PROBE/STRAY CAPACITANCE.

Figure 21. Driver Common-Mode Output Voltage Measurement

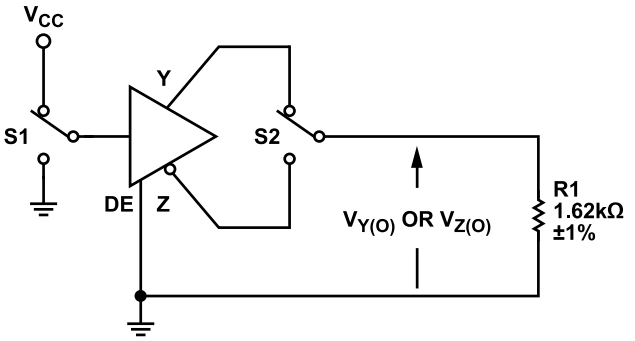


Figure 22. Maximum Steady State Output Voltage Measurement (S1 Is Switch 1, S2 Is Switch 2)

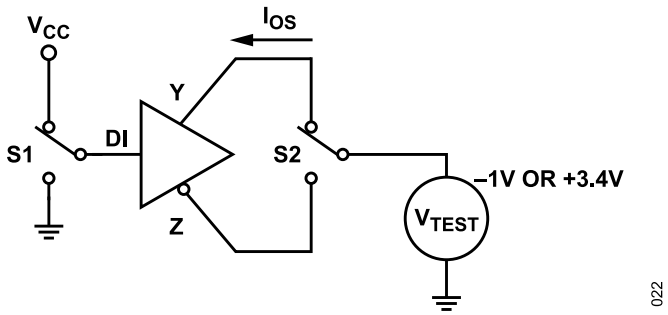
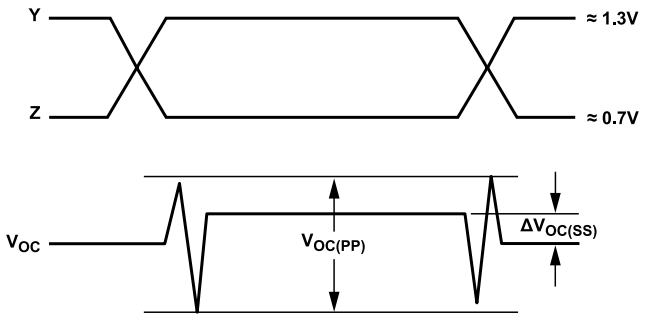


Figure 23. Driver Short Circuit

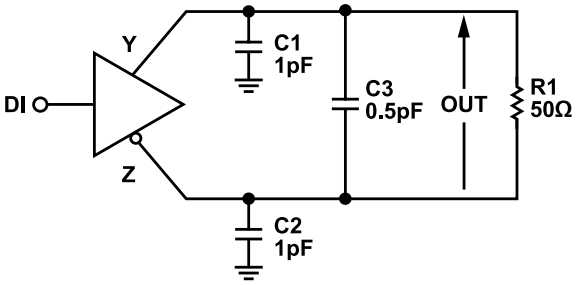


NOTES
1. INPUT PULSE GENERATOR: 100MHz.

Figure 24. Driver Common-Mode Output Voltage (Steady State)

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

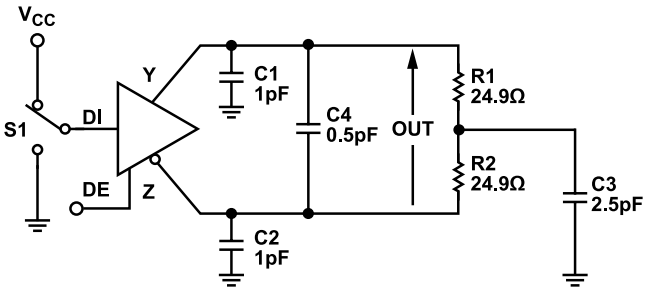
DRIVER TIMING MEASUREMENTS



NOTES
1. C1, C2, AND C3 ARE 20% AND INCLUDE PROBE/STRAY CAPACITANCE.

024

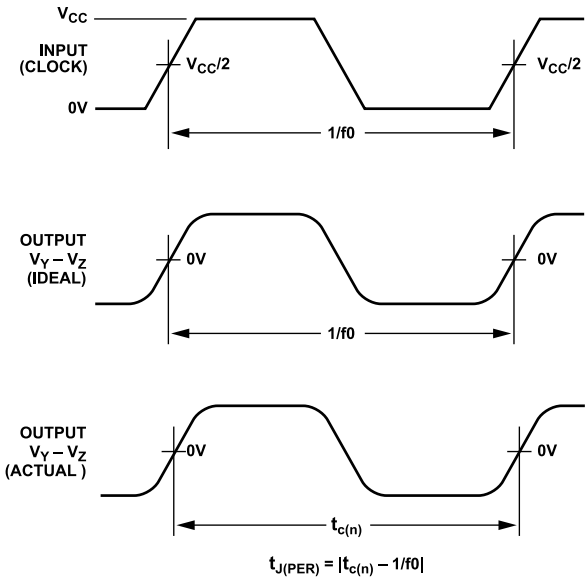
Figure 25. Driver Timing Measurement Circuit



NOTES
1. C1, C2, C3, AND C4 ARE 20% AND INCLUDE PROBE/STRAY CAPACITANCE.

025

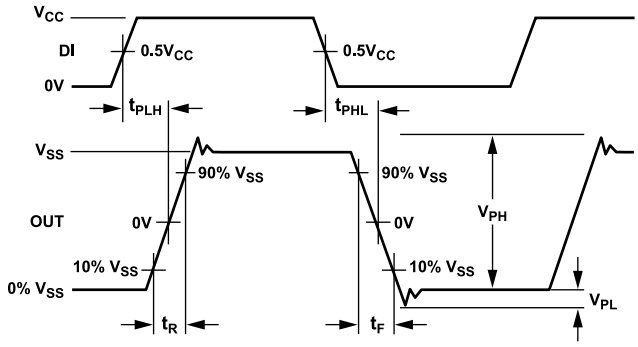
Figure 26. Driver Enable and Disable Time Circuit



NOTES
1. INPUT PULSE GENERATOR: TEK AWG5208 STIMULUS SYSTEM; 50% ± 1% DUTY CYCLE.
2. MEASURED USING TEK DPO7254 WITH DPOJET SOFTWARE.

026

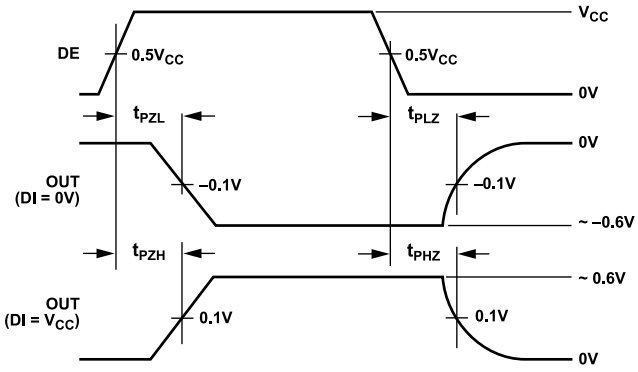
Figure 27. Driver Period Jitter Characteristics



NOTES
1. INPUT PULSE GENERATOR: 100MHz; 50% ± 5% DUTY CYCLE; t_R, t_F ≤ 1ns.
2. MEASURED ON TEST EQUIPMENT WITH –3dB BANDWIDTH ≥ 1GHz.

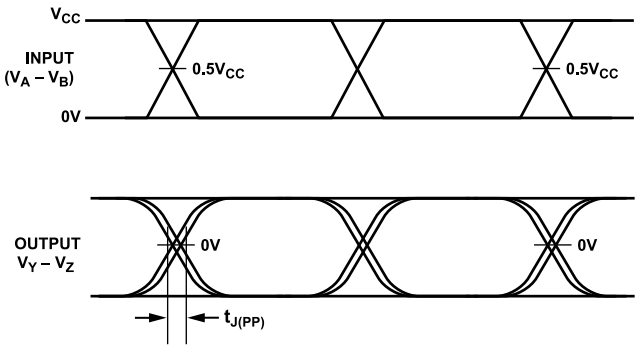
027

Figure 28. Driver Propagation, Rise and Fall Times, and Voltage Overshoot



028

Figure 29. Driver Enable and Disable Times



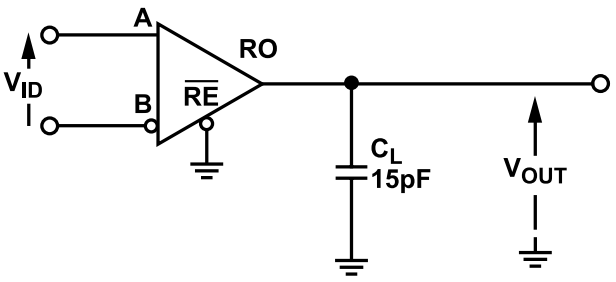
NOTES
1. INPUT PULSE GENERATOR: TEK AWG5208 STIMULUS SYSTEM.
2. MEASURED USING TEK DPO7254 WITH DPOJET SOFTWARE.

029

Figure 30. Driver Peak-to-Peak Jitter Characteristics

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

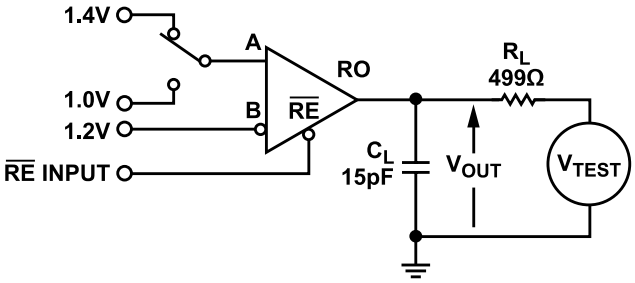
RECEIVER TIMING MEASUREMENTS



NOTES
1. C_L INCLUDES PROBE/STRAY CAPACITANCE.

030

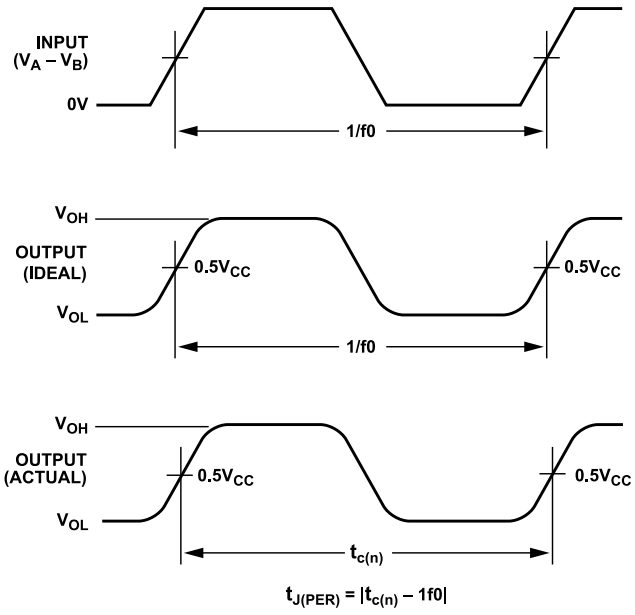
Figure 31. Receiver Timing Measurement Circuit



NOTES
1. C_L INCLUDES PROBE/STRAY CAPACITANCE.

031

Figure 32. Receiver Enable and Disable Time Circuit

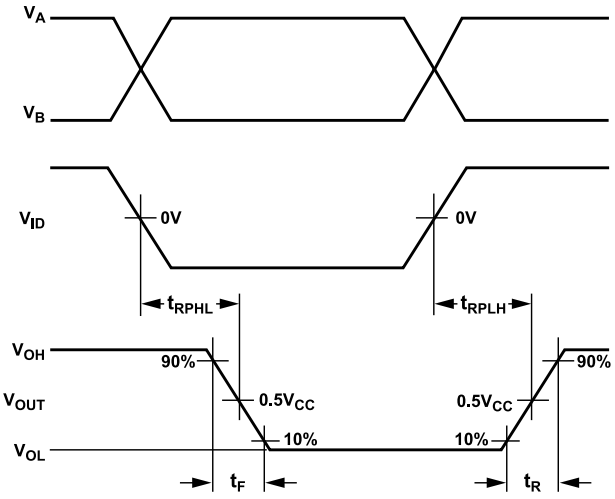


$t_{J(PER)} = |t_{c(n)} - 1f0|$

NOTES
1. INPUT PULSE GENERATOR: KEYSIGHT M8041A JBERT SYSTEM; 50% ± 1% DUTY CYCLE.
2. MEASURED USING TEK DPO7254 WITH DPOJET SOFTWARE.

032

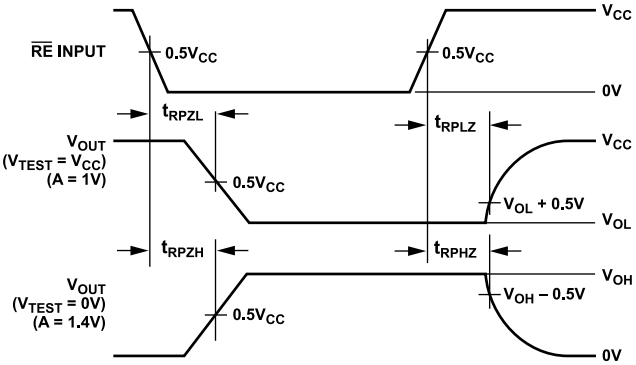
Figure 33. Receiver Period Jitter Characteristics



NOTES
1. INPUT PULSE GENERATOR: 100MHz; 50% ± 5% DUTY CYCLE; t_R, t_F ≤ 1ns.
2. MEASURED ON TEST EQUIPMENT WITH –3dB BANDWIDTH ≥ 500MHz.

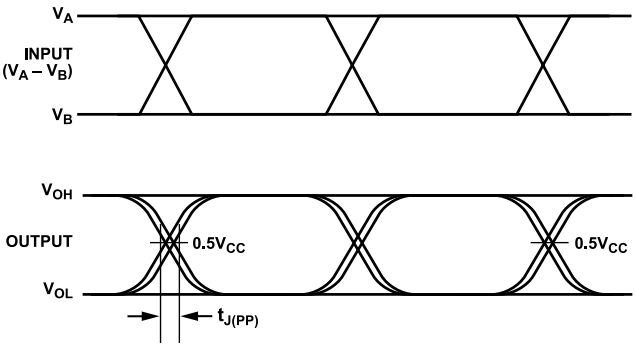
033

Figure 34. Receiver Propagation and Rise and Fall Times



034

Figure 35. Receiver Enable and Disable Times



NOTES
1. INPUT PULSE GENERATOR: TEK AWG5208 STIMULUS SYSTEM
2. MEASURED USING TEK DPO7254 WITH DPOJET SOFTWARE.

035

Figure 36. Receiver Peak-to-Peak Jitter Characteristics

THEORY OF OPERATION

The ADN4693E-1 is a transceiver for transmitting and receiving M-LVDS at high data rates of up to 200 Mbps NRZ. Each device has a differential line driver and a differential line receiver, allowing each device to send and receive data.

M-LVDS expands on the established LVDS method by allowing bi-directional communication between more than two nodes. M-LVDS transceivers feature an increased transmitter output current and a wide receiver common-mode range, allowing reliable multipoint communication over cables or backplanes. Up to 32 nodes can connect on an M-LVDS bus.

FULL-DUPLEX OPERATION

Half-duplex operation allows a transceiver to transmit or receive, but not both at the same time. However, with full-duplex operation, a transceiver can transmit and receive simultaneously. The ADN4693E-1 is a full-duplex device that has dedicated driver output and receiver input pins. Figure 38 shows a typical full-duplex bus topology for M-LVDS.

THREE-STATE BUS CONNECTION

The outputs of the device can be placed in a high impedance state by disabling the driver or the receiver. Placing the driver in a high impedance state allows several driver outputs to connect to a single M-LVDS bus. Note that, on each bus line, only one driver can be enabled at a time, but many receivers can be enabled simultaneously.

The driver can be enabled or disabled using the driver enable pin (DE). The DE pin enables the driver outputs when driven logic high. When driven logic low, the DE pin puts the driver outputs into a high impedance state. Similarly, an active low receiver enable pin ($\overline{RE}$) controls the receiver. Driving the $\overline{RE}$ pin low enables the receiver, whereas driving the $\overline{RE}$ pin high puts the receiver output into a high impedance state. The M-LVDS driver outputs remain in a high impedance state while the transceiver is not powered.

Truth tables for driver and receiver output states under various conditions are shown in Table 8, Table 9, and Table 10.

TRUTH TABLES

Table 8. Truth Table Abbreviation Definitions

Abbreviation	Description
H	High level
L	Low level
X	Don't care
I	Indeterminate
Z	High impedance (off)
NC	Disconnected/no input

Table 9. Transmitting (See Table 8 for Abbreviations)

	Inputs		Outputs	
V_{CC}	DE	DI	Y	Z
On	H	H	H	L
On	H	L or NC	L	H
On	L or NC	X	Z	Z
Off (≤1.5 V)	X	X	Z	Z

Table 10. Receiving (See Table 8 for Abbreviations)

	Inputs		Output
V_{CC}	A − B	$\overline{RE}$	RO
On	≥+50 mV	L	H
On	≤−50 mV	L	L
On	−50 mV < A − B < +50 mV	L	I
On	NC or short circuit	L	I
On	X	H or NC	Z
Off (≤1.5 V)	X	X	I

GLITCH FREE POWER-UP AND POWER-DOWN

To minimize disruption to the bus when adding nodes, the M-LVDS outputs of the device are kept glitch free when the device is powering up or powering down. This feature allows insertion of devices onto a live M-LVDS bus because the bus outputs are not switched on before the device is fully powered. In addition, all outputs are placed in a high impedance state when the device is powered off.

FAULT CONDITIONS

The ADN4693E-1 contains short-circuit current protection that protects the device under fault conditions in the case of short circuits on the bus. This protection limits the current in a fault condition to 24 mA at the transmitter outputs for short-circuit faults between −1 V and +3.4 V. Any network fault must clear to avoid data transmission errors and to ensure reliable operation of the data network and any devices that are connected to the network.

RECEIVER INPUT THRESHOLDS AND FAIL-SAFE

The TIA/EIA-899 standard defines two receiver types, both of which incorporate protection against short circuits.

The Type 1 receivers of the ADN4693E-1 incorporate 25 mV of hysteresis. This ensures that slow changing signals or a loss of input does not result in oscillation of the receiver output. Type 1 receiver thresholds are ±50 mV. Therefore, the state of the receiver output is indeterminate if the differential between A and B is about 0 V. This state occurs if the bus is idle (approximately 0 V on both A and B), with no drivers enabled on the attached nodes.

Type 2 receivers have an open circuit and bus idle fail-safe. The input threshold is offset by 100 mV so a logic low is present on the receiver output when the bus is idle or when the receiver inputs are open.

THEORY OF OPERATION

The different receiver thresholds for the two receiver types are illustrated in Figure 37. See Table 10 for the Type 1 receiver output states of the ADN4693E-1 under various conditions.

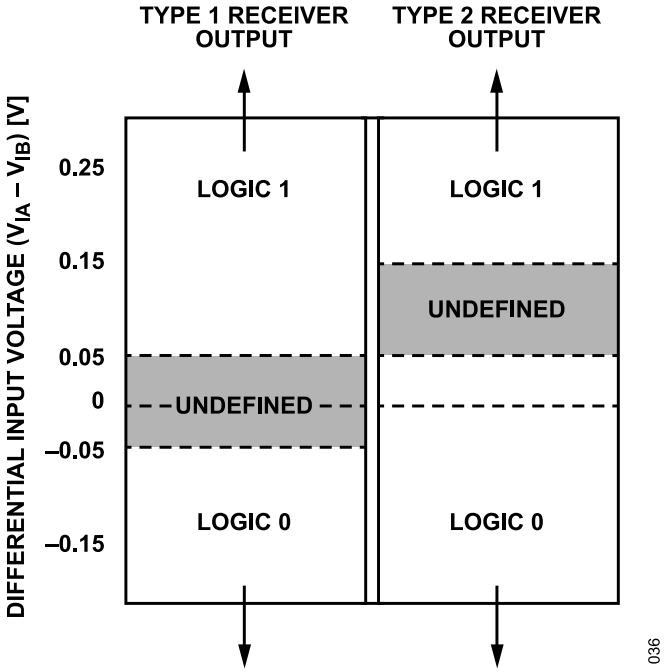


Figure 37. Input Threshold Voltages (V_{IA} Is the Voltage Input on Pin A, and V_{IB} Is the Voltage Input on Pin B)

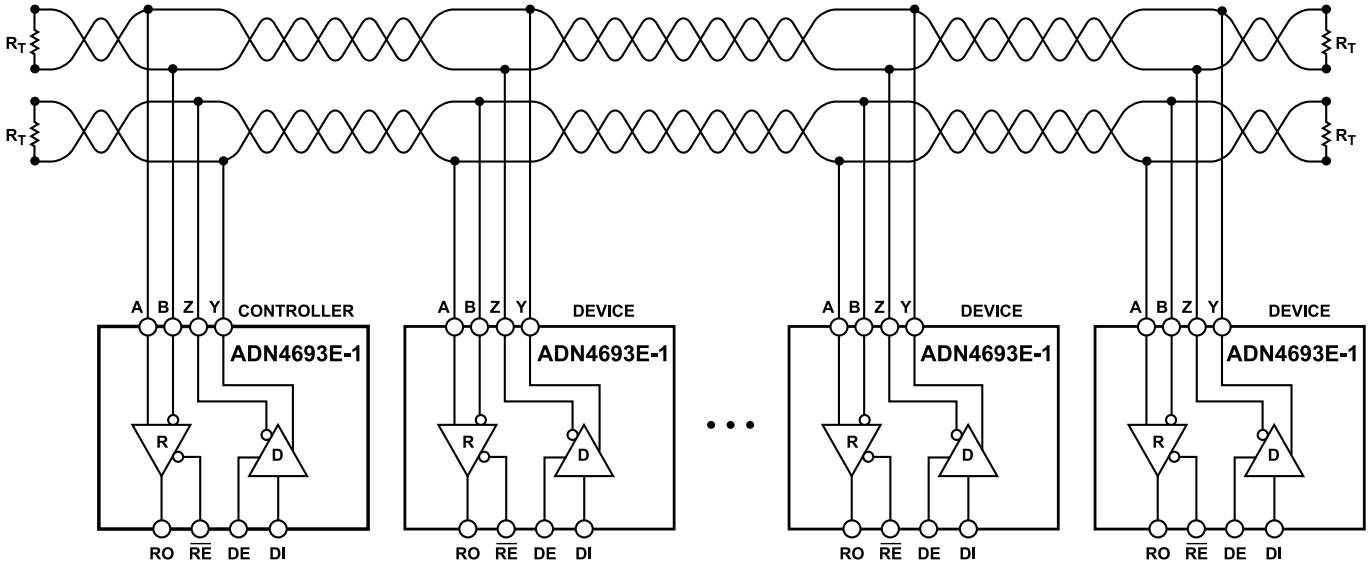
APPLICATIONS INFORMATION

M-LVDS extends the low power, high speed, differential signaling of LVDS to multipoint systems where multiple nodes are connected over short distances in a bus topology network.

With M-LVDS, a transmitting node drives a differential signal across a transmission medium, such as a twisted pair cable or backplane. The transmitted differential signal allows other receiving nodes that are connected along the bus to detect a differential voltage that can then be converted back into a single-ended logic signal by the receiver.

The communication line is typically terminated at both ends by resistors (R_T), the value of which is chosen to match the characteristic impedance of the medium (typically 100 Ω). In loaded backplanes, a termination resistor of less than 100 Ω may be appropriate.

For half-duplex multipoint applications, only one driver can be enabled at any time. Full-duplex nodes allow a controller/device topology, as shown in Figure 38. In this configuration, a controller node can concurrently send and receive data to and from device nodes. At any time, only one device node can have a driver enabled to concurrently transmit data back to the controller node.



NOTES
1. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE COMMUNICATION MEDIUM.

Figure 38. ADN4693E-1 Typical Full-Duplex M-LVDS Controller/Device Network (Type 1 Receivers)