5.5 V, 5 A/6 A, High Efficiency, Step-Down DC-to-DC Regulators with Output Tracking

Data Sheet **ADP2165/ADP2166**

FEATURES

- **Continuous output current**
  - **ADP2165: 5 A**
  - **ADP2166: 6 A**
- **Integrated MOSFET**
  - **High-side on resistance: 19 mΩ**
  - **Low-side on resistance: 15 mΩ**
- **Reference voltage: 0.6 V ± 1% over temperature range**
- **Input voltage range: 2.7 V to 5.5 V**
- **Current mode architecture**
- **Switching frequency**
  - **Fixed frequency: 620 kHz or 1.2 MHz**
  - **Adjustable frequency: 250 kHz to 1.4 MHz**
- **Synchronizes to external clock: 250 kHz to 1.4 MHz**
- **Selectable synchronize phase shift: in phase or out of phase**
- **External compensation**
- **Programmable soft start**
- **Startup into a precharged output**
- **Voltage tracking input**
- **Power-good output and precision enable input**
- **Accurate current limit**
- **Available in 24-lead, 4 mm × 4 mm LFCSP package**
- **Supported by ADIsimPower™ design tool**

APPLICATIONS

- **Point of load regulation**
- **Communications and networking**
- **High end consumer**
- **Industrial, instrumentation, and healthcare**

GENERAL DESCRIPTION

The ADP2165/ADP2166 are high efficiency, current mode control, step-down dc-to-dc regulators with an integrated 19 mΩ high-side FET and a 15 mΩ synchronous rectified FET. The ADP2165/ADP2166 combine a small size, 4 mm × 4 mm LFCSP package with an accurate current limit, resulting in a smaller inductor size and a high power density, point of load solution.

Key features include precision enable, power-good monitor, and output voltage tracking to facilitate robust sequencing. The switching frequency can be programmed from 250 kHz to 1.4 MHz, or it can be fixed at 620 kHz or 1.2 MHz. The synchronization function allows the switching frequency to synchronize to an external clock, minimizing the electromagnetic interference (EMI) of the system.

TYPICAL APPLICATION CIRCUIT

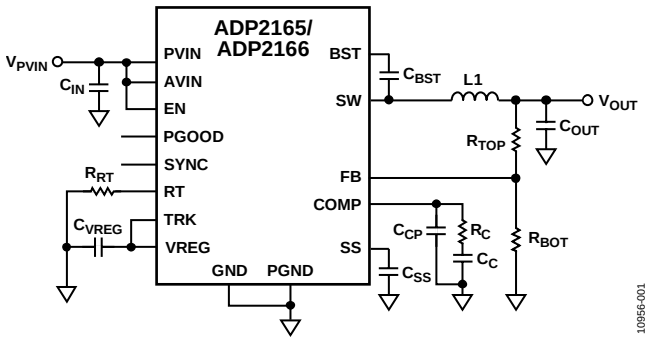

Figure 1.

The ADP2165/ADP2166 are designed to be extremely flexible with the addition of a minimal amount of external components to program soft start and control loop compensation.

The ADP2165/ADP2166 are supplied from an input voltage of 2.7 V to 5.5 V. Output voltage options include 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, or 1.0 V fixed outputs and adjustable options capable of supporting an output voltage range from 0.6 V to 90% of the input voltage. Protection features include undervoltage lockout (UVLO), overvoltage protection (OVP), overcurrent protection (OCP), and thermal shutdown (TSD) for robust performance.

The ADP2165/ADP2166 operate over the −40°C to +125°C junction temperature range and are available in a 24-lead LFCSP package.

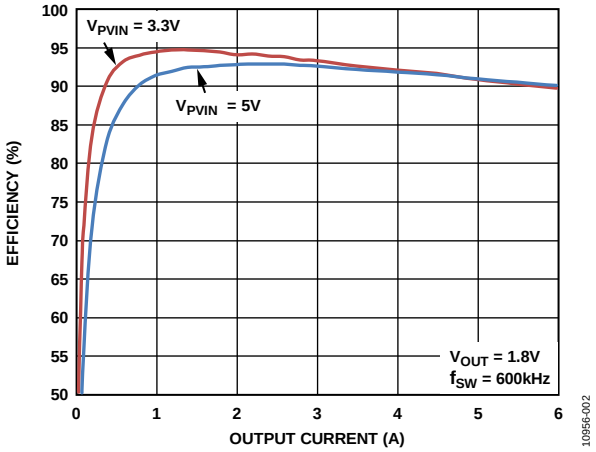

Figure 2. Efficiency vs. Output Current

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REVISION HISTORY

8/2017—Rev. A to Rev. B

Changed LFCSP_WQ to LFCSP ... Throughout
Updated Outline Dimensions ... 23
Changes to Ordering Guide ... 23

9/2016—Rev. 0 to Rev. A

Change to Compensation Components Section ... 18
Change to Table 8 ... 19

8/2014—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

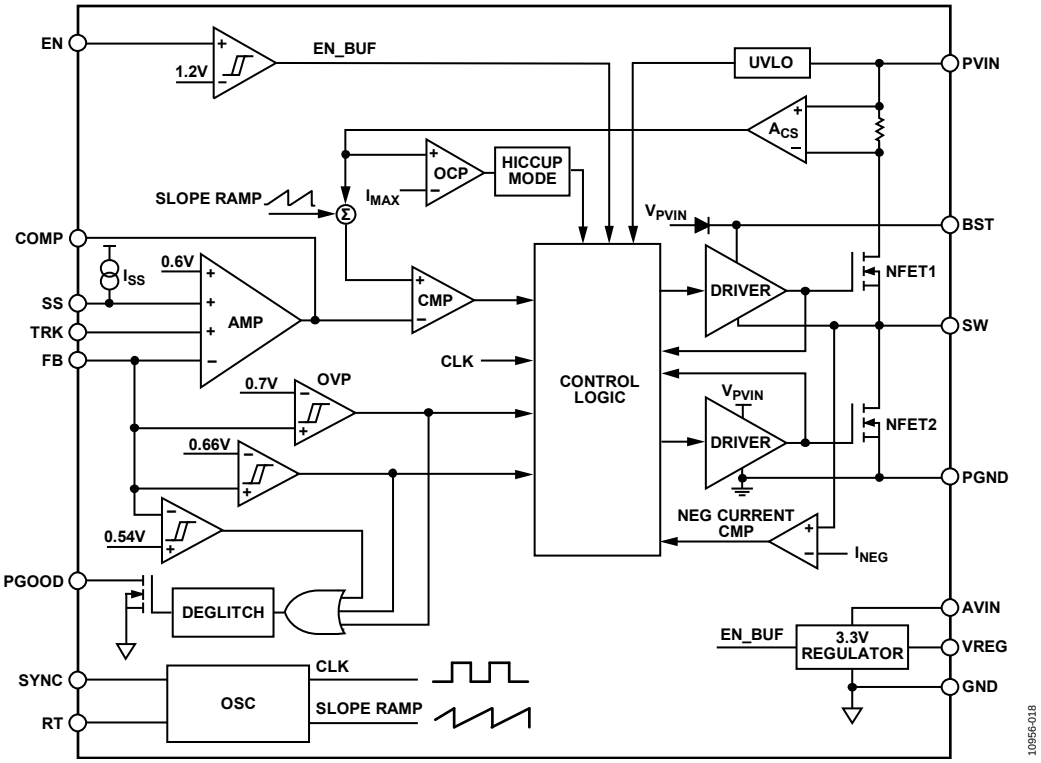

Figure 3. ADP2165/ADP2166 Functional Block Diagram

SPECIFICATIONS

V_{PVIN} = V_{AVIN} = 5 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
PVIN AND AVIN						
V_{PVIN} Voltage Range	V_{PVIN}		2.7		5.5	V
V_{AVIN} Voltage Range	V_{AVIN}		2.7		5.5	V
Quiescent Current	I_Q	No switching, f_{SW} = 600 kHz		2	10	mA
Shutdown Current	I_{SHDN}	EN = 0 V		25	150	µA
V_{AVIN} Undervoltage Lockout Threshold	UVLO	V_{AVIN} rising		2.6	2.7	V
		V_{AVIN} falling	2.35	2.5		V
FB						
FB Regulation Voltage	V_{FB}	V_{PVIN} = 2.7 V to 5.5 V	0.594	0.6	0.606	V
Fixed Output Version	V_{OUT}		−1		+1	%
FB Bias Current	I_{FB}			0.01	0.1	µA
ERROR AMPLIFIER (EA)						
Transconductance	g_m		430	500	570	µS
EA Source Current	I_{SOURCE}			75		µA
EA Sink Current	I_{SINK}			85		µA
INTERNAL REGULATOR (VREG)						
VREG Voltage			3.1	3.3	3.5	V
Dropout Voltage		I_{VREG} = 10 mA		140		mV
Regulator Current Limit				50		mA
SW						
High-Side On Resistance[1]		$V_{BST} - V_{SW}$ = 5 V		19	29	mΩ
		$V_{BST} - V_{SW}$ = 3.3 V		22	34	mΩ
Low-Side On Resistance[1]		V_{PVIN} = 5 V		15	23	mΩ
		V_{PVIN} = 3.3 V		16	26	mΩ
High-Side Peak Current Limit		ADP2165	6.5	8	9.5	A
		ADP2166	7.5	9	10.5	A
Low-Side Negative Current Limit				2.4		A
SW Minimum Off Time[2]	t_{OFF_MIN}			100		ns
SW Minimum On Time[2]	t_{ON_MIN}			100		ns
OSCILLATOR (RT)						
Switching Frequency	f_{SW}	RT pin floating	525	620	715	kHz
		RT pin connected to VREG	1.08	1.2	1.32	MHz
		R_{RT} = 95.3 kΩ	500	590	680	kHz
Switching Frequency Range			250		1400	kHz
SYNC						
Synchronization Range			250		1400	kHz
SYNC Minimum Pulse Width			100			ns
SYNC Minimum Off Time			100			ns
SYNC Input High Voltage			1.3			V
SYNC Input Low Voltage					0.4	V
SOFT START (SS)						
SS Pull-Up Current	I_{SS}		2.7	3.5	4.3	µA
TRK						
TRK Input Voltage Range			0		600	mV
TRK-to-FB Offset Voltage		TRK = 300 mV to 500 mV	−9		+9	mV
TRK Input Bias Current					100	nA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
PGOOD						
Power-Good Range		FB rising threshold	107	111	115	%
		FB rising hysteresis		3		%
		FB falling threshold	87	90.5	94.5	%
		FB falling hysteresis		3		%
Power-Good Deglitch Time		From FB to PGOOD		16		Clock cycles
PGOOD Leakage Current		V_{PGOOD} = 5 V		0.1	1	µA
PGOOD Output Low Voltage		I_{PGOOD} = 1 mA		27	45	mV
EN						
EN Threshold			1.12	1.2	1.28	V
EN Hysteresis				100		mV
EN Pull-Down Resistor				1		MΩ
THERMAL						
Thermal Shutdown Threshold				150		°C
Thermal Shutdown Hysteresis				25		°C

[1] Pin-to-pin measurement.
[2] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
PVIN, AVIN, EN, PGOOD, FB	−0.3 V to +6 V
SW	−1 V to +6 V
BST	SW + 6 V
SS, COMP, TRK, VREG, SYNC, RT	−0.3 V to +6 V
PGND to GND	−0.3 V to +0.3 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board (4-layer, JEDEC standard board) for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
24-Lead LFCSP	38.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

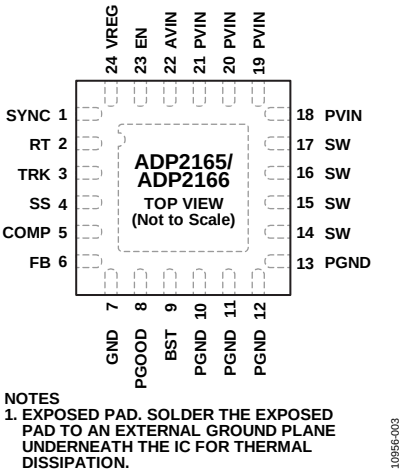

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SYNC	Synchronization Input. Connect this pin to an external clock between 250 kHz and 1.4 MHz to synchronize the switching frequency to the external clock. RT can be used to program the phase shift when synchronizing the external clock.
2	RT	Frequency Setting. Connect a resistor between the RT and GND pins to program the switching frequency between 250 kHz to 1.4 MHz. When the RT pin is floating, the frequency is set to 620 kHz, and when the RT pin is connected to VREG, the frequency is set to 1.2 MHz.
3	TRK	Tracking Input. This pin can be used for tracking and sequencing. If the tracking function is not used, connect TRK to VREG.
4	SS	Soft Start Control. Connect a capacitor from the SS pin to the GND pin to program the soft start time.
5	COMP	Error Amplifier Output. Connect a compensation network from the COMP pin to the GND pin.
6	FB	Feedback Voltage Sense Input. Connect to a resistor divider from V_{OUT}.
7	GND	Analog Ground. Connect to the ground plane.
8	PGOOD	Power-Good Output (Open-Drain). A pull-up resistor of 100 kΩ is recommended.
9	BST	Supply Rail for the High-Side MOSFET Gate Drive. Place a 0.1 µF capacitor between the SW pin and the BST pin.
10, 11, 12, 13	PGND	Power Ground. Connect this pin to the ground plane and to the output return side of the output capacitor.
14, 15, 16, 17	SW	Switching Node.
18, 19, 20, 21	PVIN	Power Input. Connect this pin to the input power source and connect a bypass capacitor between this pin and ground.
22	AVIN	Bias Voltage Input Pin. Connect a bypass capacitor between this pin and GND and a small (10 Ω) resistor between this pin and PVIN.
23	EN	Precision Enable Input Pin. An external resistor divider can be used to set the turn-on threshold. To enable the device automatically, connect the EN pin to PVIN. This pin has a 1 MΩ pull-down resistor to GND.
24	VREG	Internal Bias Regulator Output. It supplies the regulated voltage to the internal circuitry. Bypass the VREG pin to the GND pin with a high quality, low ESR 1 µF ceramic capacitor.
	EPAD	Exposed Pad. Solder the exposed pad to an external ground plane underneath the IC for thermal dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{PVIN} = V_{AVIN} = 5 V, V_{OUT} = 1.2 V, L = 1 µH, C_{IN} = 47 µF, C_{OUT} = 100 µF, f_{SW} = 600 kHz, unless otherwise noted.

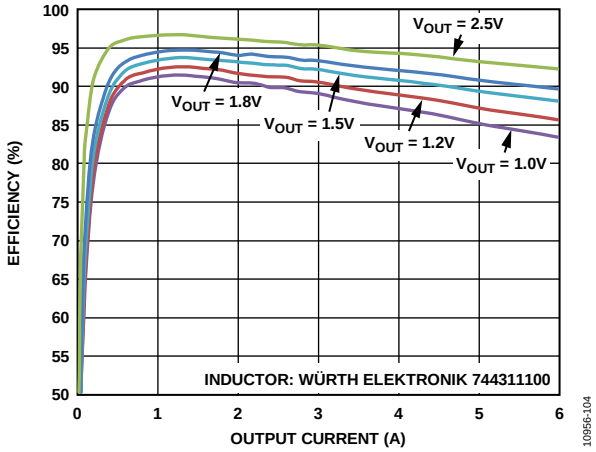

Figure 5. Efficiency (f_{SW} = 600 kHz, V_{PVIN} = 3.3 V) vs. Output Current

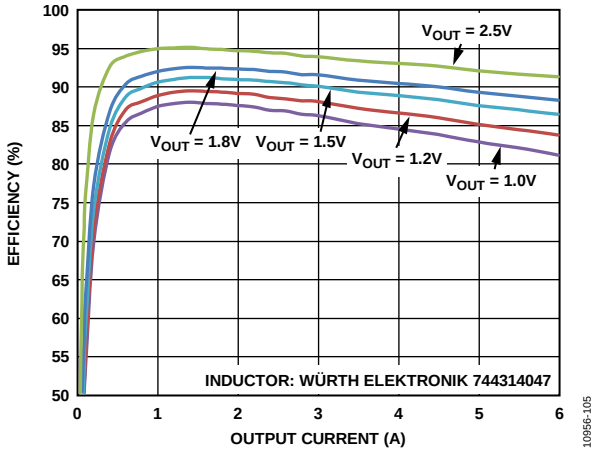

Figure 6. Efficiency (f_{SW} = 1.2 MHz, V_{PVIN} = 3.3 V) vs. Output Current

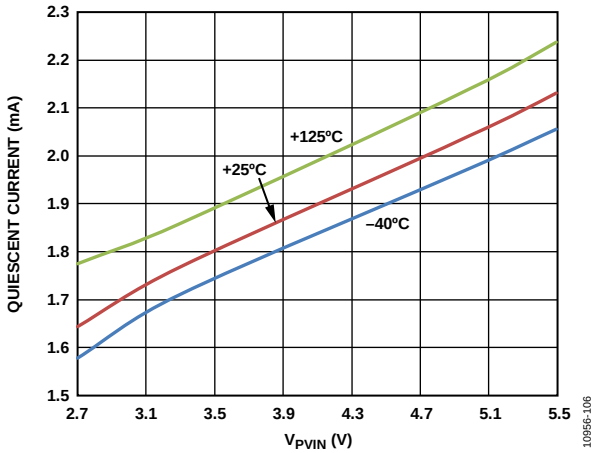

Figure 7. Quiescent Current vs. V_{PVIN} (No Switching)

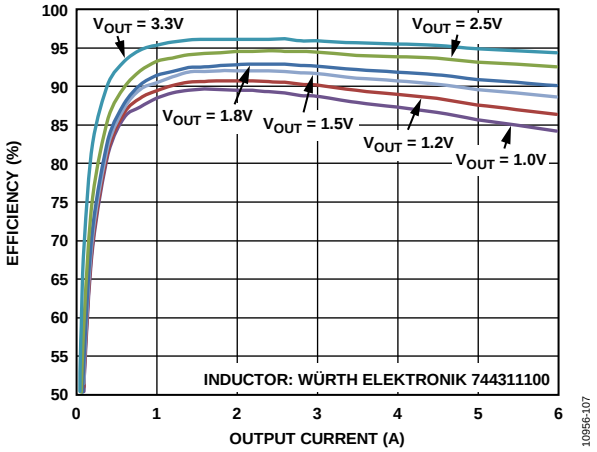

Figure 8. Efficiency (f_{SW} = 600 kHz, V_{PVIN} = 5 V) vs. Output Current

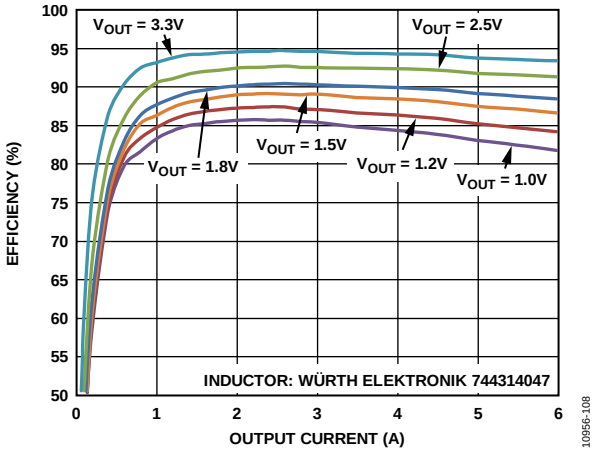

Figure 9. Efficiency (f_{SW} = 1.2 MHz, V_{PVIN} = 5 V) vs. Output Current

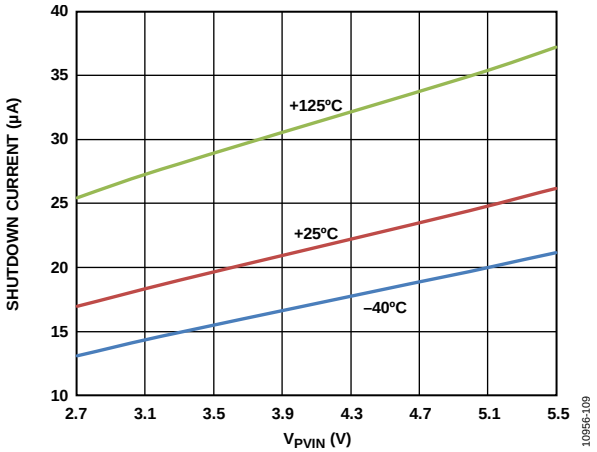

Figure 10. Shutdown Current vs. V_{PVIN}

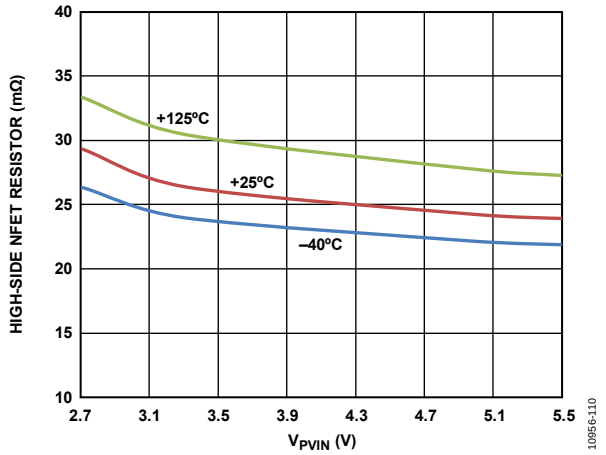

Figure 11. High-Side NFET Resistor vs. V_{PVIN} (Pin-to-Pin Measurements)

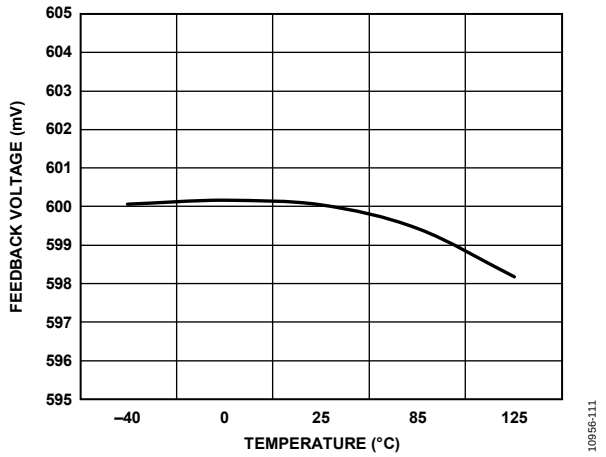

Figure 12. Feedback Voltage vs. Temperature, V_{PVIN} = 5 V

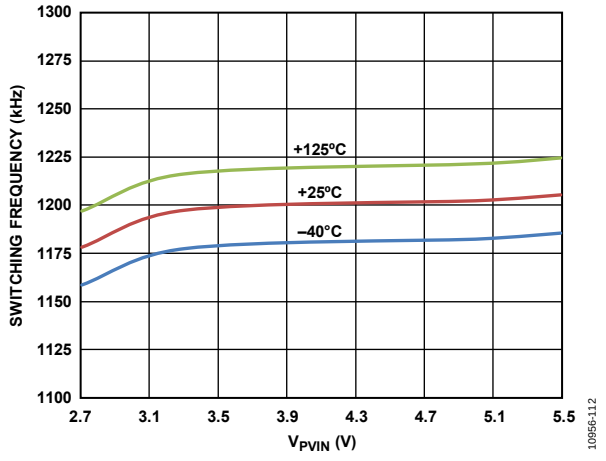

Figure 13. Switching Frequency vs. V_{PVIN} at 1.2 MHz (RT = VREG)

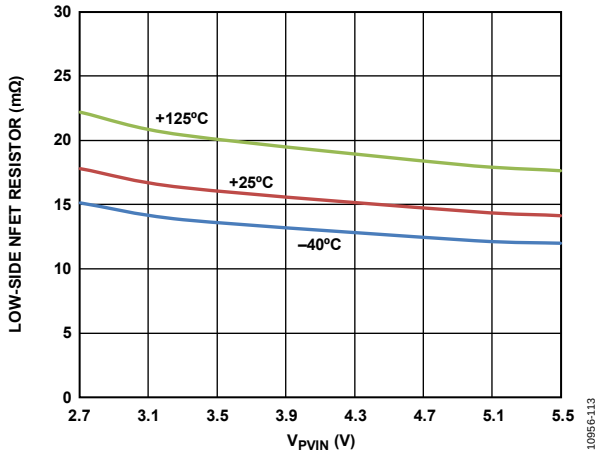

Figure 14. Low-Side NFET Resistor vs. V_{PVIN} (Pin-to-Pin Measurements)

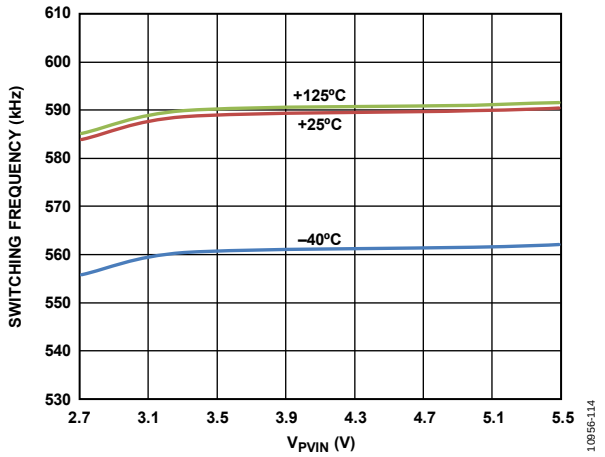

Figure 15. Switching Frequency vs. V_{PVIN} (R_{RT} = 95.3 kΩ)

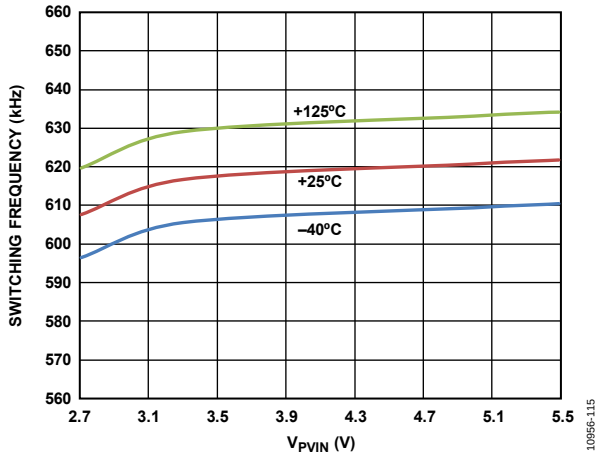

Figure 16. Switching Frequency vs. V_{PVIN} at 620 kHz (RT Floating)

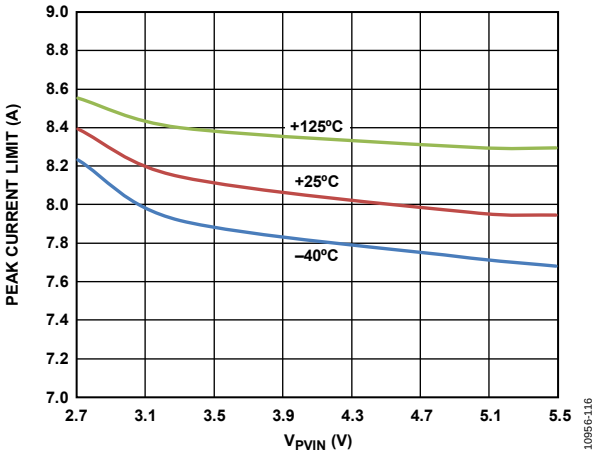

Figure 17. ADP2165 Peak Current Limit vs. V_{PVIN}

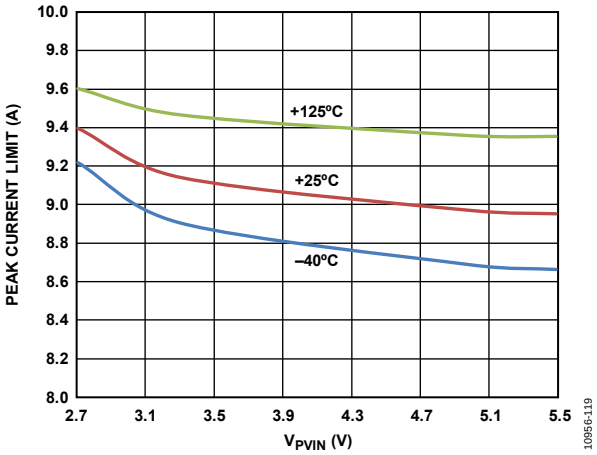

Figure 20. ADP2166 Peak Current Limit vs. V_{PVIN}

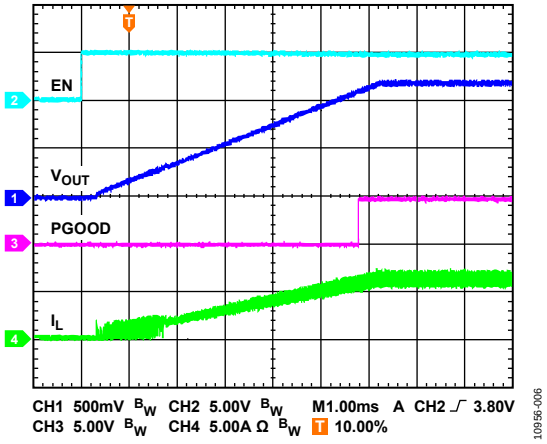

Figure 18. Soft Start with Full Load (600 kHz, V_{PVIN} = 5 V)

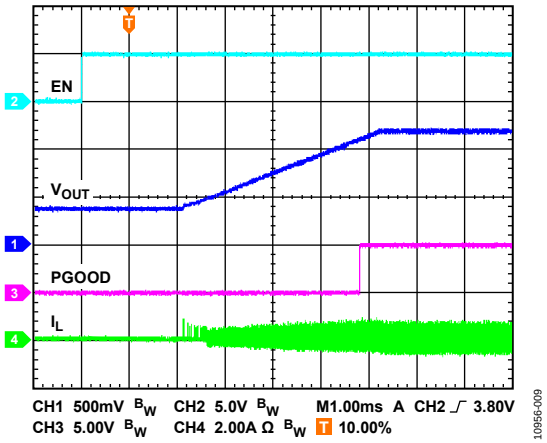

Figure 21. Soft Start with Precharge (600 kHz, V_{PVIN} = 5 V)

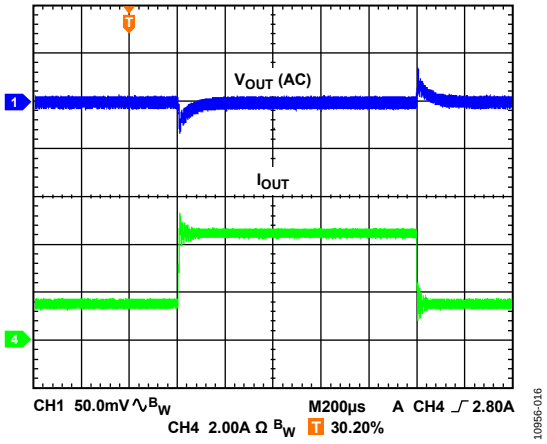

Figure 19. Load Transient (600 kHz, 1.5 A to 4.5 A Load Step)

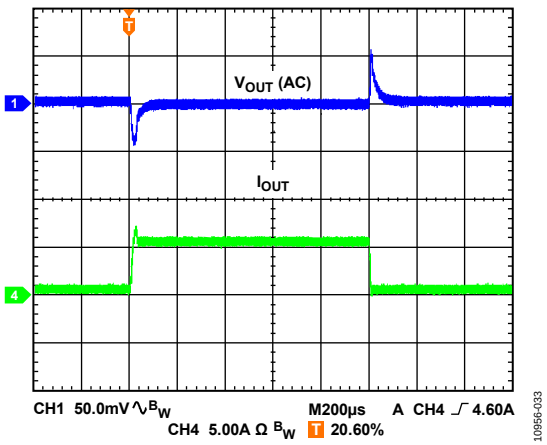

Figure 22. Load Transient (1.2 MHz, 0.5 A to 5.5 A Load Step)

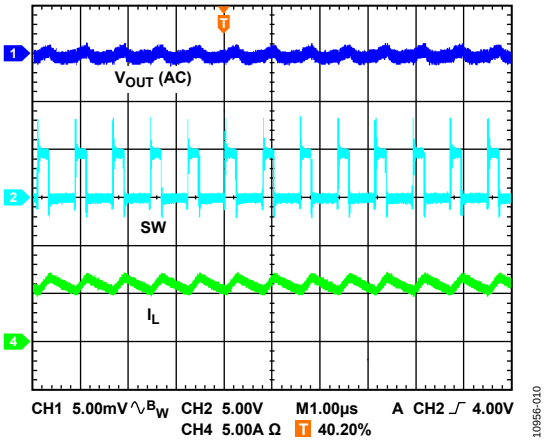

Figure 23. Steady Waveform

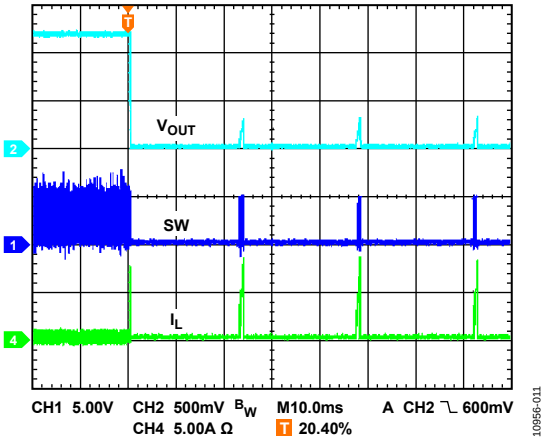

Figure 24. Output Short

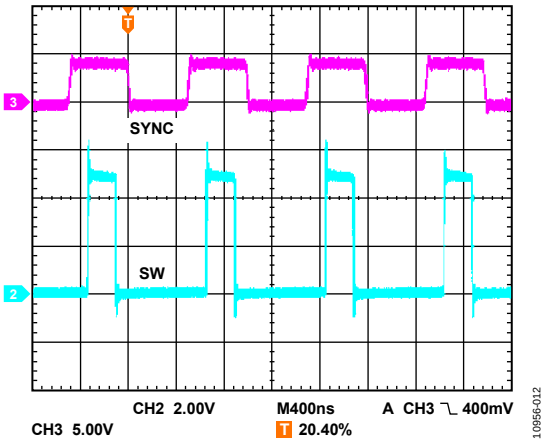

Figure 25. Synchronized to 1 MHz in Phase

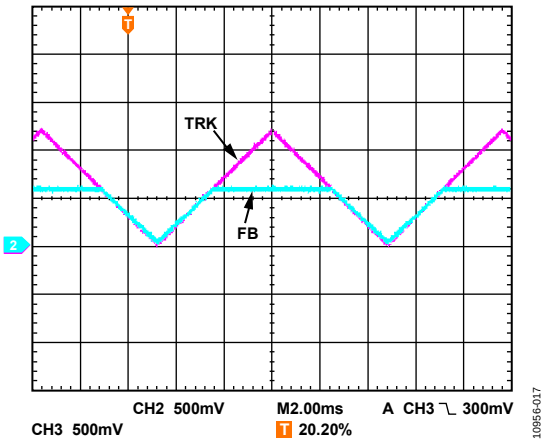

Figure 26. Tracing Function

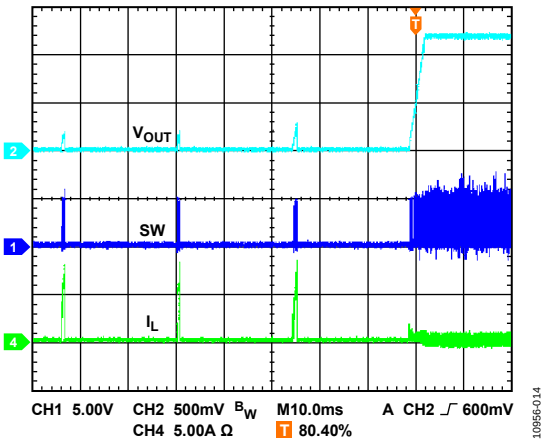

Figure 27. Output Short Recovery

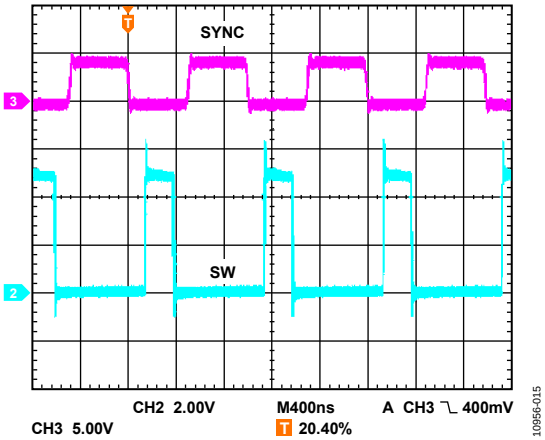

Figure 28. Synchronized to 1 MHz 180° Out of Phase

THEORY OF OPERATION

The ADP2165/ADP2166 are step-down, dc-to-dc regulators. They use a current mode architecture with an integrated high-side and low-side switch. They target high performance applications that require high efficiency and design simplicity.

The ADP2165/ADP2166 can operate with an input voltage from 2.7 V to 5.5 V and regulate the output voltage down to 0.6 V. Additional features for flexible design include programmable switching frequency, programmable soft start, external compensation, and enable and power-good pins. The ADP2165/ADP2166 are also available with preset output voltage options of 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, and 1.0 V.

CONTROL SCHEME

The ADP2165/ADP2166 use a fixed frequency, current mode PWM control architecture for good line and load transient performance. In fixed frequency PWM mode, adjust the duty cycle of the integrated MOSFET to regulate the output voltage that has a low output ripple voltage.

PWM MODE

At the start of each oscillator cycle, the high-side NFET (N-channel MOSFET) switch turns on and transmits a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current level set by the voltage on the COMP pin. The high-side NFET then turns off, and the low-side NFET synchronous rectifier then turns on. This puts a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle.

ENABLE/SHUTDOWN

The EN input pin has a precision analog threshold of 1.2 V (typical) with 100 mV of hysteresis. When the enable voltage exceeds 1.2 V, the regulator turns on, and when it falls below 1.1 V (typical), the regulator turns off. To force the devices to automatically start when input power is applied, connect the EN pin to the PVIN pin.

When the ADP2165/ADP2166 are shut down, the soft start capacitor discharges. When the devices are reenabled, a new soft start cycle begins.

If the EN pin is not externally connected, an internal pull-down resistor (1 MΩ) prevents an accidental enable.

INTERNAL REGULATOR (VREG)

The internal regulator provides a stable supply for the internal control circuits. It is recommended to place a 1 µF ceramic capacitor between the VREG and GND pins. The internal regulator also includes a current-limit circuit to protect the circuit if the maximum external load is added.

The AVIN pin provides the power supply for the internal regulator. When device is enabled, the internal regulator is active.

BOOTSTRAP CIRCUITRY

The ADP2165/ADP2166 integrate the boot regulator to provide the gate drive voltage for the high-side NFET. A capacitor between the BST and SW pins is charged from the PVIN pin while the low-side NFET is on.

Placing an X7R or X5R 0.1 µF ceramic capacitor between the BST and SW pins is recommended.

OSCILLATOR AND SYNCHRONIZATION

The switching frequency of the ADP2165/ADP2166 can be set by connecting a resistor between the RT pin and the GND pin. Use the following equation to set the switching frequency:

$$R_{RT}\,(\text{k}\Omega) = 60{,}000/[f_{SW}\,(\text{kHz}) + 10] - 5$$

A 191 kΩ resistor sets the frequency to 300 kHz, and a 93.1 kΩ resistor sets frequency to 600 kHz. Figure 29 shows the typical relationship between R_{RT} and f_{SW}.

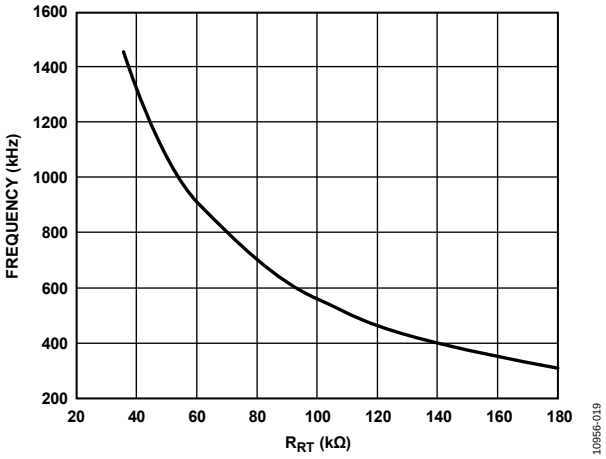

Figure 29. Frequency (f_{SW}) vs. RT Resistor

To synchronize the ADP2165/ADP2166, drive an external clock at the SYNC pin. The frequency of the external clock can be in the 250 kHz to 1.4 MHz range.

During the synchronization, the RT pin can be used to program the phase shift. When the RT pin is connected to the VREG pin, the rising edge of the SW pin is 180° out of phase with the external clock. If the RT pin is floating, the rising edge of the SW pin is in phase with the external clock.

SOFT START

The SS pin is used to program the soft start time. By connecting a capacitor between the SS and GND pins, the internal current then charges this capacitor and establishes the soft start ramp-up. The soft start time can be calculated by the following equation:

$$t_{SS} = \frac{0.6V \times C_{SS}}{I_{SS}}$$

where:
C_{SS} is the soft start capacitance.
I_{SS} is the soft start pull-up current (3.5 µA).

If the output voltage is precharged prior to startup, the ADP2165/ADP2166 prevent reverse inductor current that discharges the output capacitor until the soft start voltage exceeds the voltage on the FB pin.

When the channel is disabled or a current fault happens, the soft start capacitor discharges.

TRACKING

The ADP2165/ADP2166 have a tracking input feature, TRK, that allows the output voltage to track another voltage (master voltage). It is especially useful in core and I/O voltage tracking for field programmable gate arrays (FPGAs), digital signal processors (DSPs), and application specific integrated circuits (ASICs).

The internal error amplifier includes three positive inputs: the internal reference voltage, the soft start voltage, and the TRK voltage. The error amplifier regulates the FB voltage to the lowest of the three voltages. To track a master voltage, tie the TRK pin to a resistor divider from the master voltage.

If the TRK function is not used, connect the TRK pin to the VREG.

POWER-GOOD (PGOOD)

The PGOOD pin is an active high, open-drain output that requires a pull-up resistor. A logic high on the PGOOD pin indicates that the voltage on the FB pin (and, therefore, the output voltage) is within ±10% of the desired value. In addition, there is a 16-cycle waiting period after the FB pin is detected as being within the ±10% range. A logic low on the PGOOD pin indicates that the voltage on the FB pin is not within ±10% of the desired value. Similarly, there is a 16-cycle delay to deassert PGOOD.

PEAK CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTION

The ADP2165/ADP2166 have a peak current-limit protection circuit to prevent current runaway. When the inductor peak current reaches the current-limit value, the high-side NFET turns off, and the low-side NFET turns on until the next cycle, while the overcurrent counter increments. If the overcurrent counter count exceeds 10, the device enters hiccup mode, and the high-side NFET and low-side NFET both turn off. The devices remain in this mode for seven times the soft start time and then attempt to restart from the soft start. If the current-limit fault clears, the devices resume normal operation. Otherwise, they reenter hiccup mode after counting 10 current-limit violations.

OVERVOLTAGE PROTECTION

The ADP2165/ADP2166 provide an overvoltage protection feature that protects the system from an output short to a higher voltage supply or from a strong unload transient. If the feedback voltage increases to 0.7 V, the internal high-side NFET turns off and the low-side NFET turns on until the current through the low-side NFET reaches the negative current limit. Thereafter, both the high-side and low-side NFET are held in the off state until the voltage at FB decreases to 0.63 V, and the devices resume normal operation.

UNDERVOLTAGE LOCKOUT

Undervoltage lockout circuitry is integrated in the ADP2165/ADP2166. If AVIN drops below 2.5 V, the devices turn off. When the AVIN voltage rises above 2.6 V, the soft start period initiates, and the devices are enabled.

THERMAL SHUTDOWN

In the event that the junction temperatures of the ADP2165/ADP2166 rise above 150°C, the thermal shutdown circuit turns the regulator off. Extreme junction temperatures can be the result of high current operation, poor circuit board design, and/or high ambient temperature. A 25°C hysteresis is included so that when thermal shutdown occurs, the ADP2165/ADP2166 do not return to operation until the on-chip temperature drops below 125°C. When coming out of thermal shutdown, soft start initiates.

APPLICATIONS INFORMATION

ADIsimPOWER DESIGN TOOL

The ADP2165/ADP2166 are supported by the ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized to a specific design goal. The tools allow the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. The ADIsimPower tool can be found at www.analog.com/ADIsimPower, and the user can request an unpopulated board through the tool.

INPUT CAPACITOR SELECTION

The input capacitor reduces the input voltage ripple caused by the switch current on the PVIN pin. Place the input capacitor as close as possible to the PVIN pin. A ceramic capacitor in the 10 µF to 47 µF range is recommended. The loop that is composed of this input capacitor, the high-side NFET, and the low-side NFET must be kept as small as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. The rms current rating of the input capacitor must be larger than the value calculated by the following equation:

$$I_{C_{IN\_RMS}} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

OUTPUT VOLTAGE SETTING

The output voltage of the ADP2165/ADP2166 is set by an external resistive divider. The resistor values are calculated using the following equation:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

To limit the output voltage accuracy degradation due to FB bias current (0.1 µA maximum) to less than 0.5% (maximum), ensure that $R_{BOT} < 30$ kΩ.

Table 5 lists the recommended resistor divider for various output voltages.

Table 5. Resistor Divider for Various Output Voltages

V_{OUT} (V)	R_{TOP} ± 1% (kΩ)	R_{BOT} ± 1% (kΩ)
1.0	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	47.5	15
3.3	10	2.21

VOLTAGE CONVERSION LIMITATIONS

The minimum output voltage for a given input voltage and switching frequency is constrained by the minimum on time. The minimum on time of the ADP2165/ADP2166 is typically 100 ns. The minimum output voltage at a given input voltage and frequency can be calculated using the following equation:

$$V_{OUT\_MIN} = V_{PVIN} \times t_{ON\_MIN} \times f_{SW} - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MIN} \times t_{ON\_MIN} \times f_{SW} - (R_{DSON\_LS} + R_L) \times I_{OUT\_MIN} \quad (1)$$

where:
V_{OUT_MIN} is the minimum output voltage.
t_{ON_MIN} is the minimum on time.
I_{OUT_MIN} is the minimum output current.
f_{SW} is the switching frequency.
R_{DSON_HS} is the high-side MOSFET on resistance.
R_{DSON_LS} is the low-side MOSFET on resistance.
R_L is the series resistance of the output inductor.

The maximum output voltage for a given input voltage and switching frequency is constrained by the minimum off time and the maximum duty cycle. The minimum off time is typically 100 ns, and the maximum duty cycle of the ADP2165/ADP2166 is typically 90%.

The maximum output voltage, limited by the minimum off time at a given input voltage and frequency, can be calculated using the following equation:

$$V_{OUT\_MAX} = V_{PVIN} \times (1 - t_{OFF\_MIN} \times f_{SW}) - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MAX} \times (1 - t_{OFF\_MIN} \times f_{SW}) - (R_{DSON\_LS} + R_L) \times I_{OUT\_MAX} \quad (2)$$

where:
V_{OUT_MAX} is the maximum output voltage.
t_{OFF_MIN} is the minimum off time.
I_{OUT_MAX} is the maximum output current.

The maximum output voltage, limited by the maximum duty cycle at a given input voltage, can be calculated using the following equation:

$$V_{OUT\_MAX} = D_{MAX} \times V_{PVIN} \quad (3)$$

where D_{MAX} is the maximum duty cycle.

As Equation 1 to Equation 3 show, reducing the switching frequency alleviates the minimum on time and minimum off time limitation.

INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage, output voltage, and inductor ripple current. Using a small inductor leads to a faster transient response; however, it degrades efficiency due to a larger inductor ripple current. Conversely, using a large inductor value leads to a smaller ripple current and better efficiency; however, it results in a slower transient response.

As a guideline, the inductor ripple current, ΔI_L, is typically set to one-third of the maximum load current. The inductor value is calculated using the following equation:

$$L = \frac{(V_{PVIN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:
V_{PVIN} is the input voltage.
V_{OUT} is the output voltage.
ΔI_L is the inductor ripple current.
f_{SW} is the switching frequency.
D is the duty cycle, $D = V_{OUT}/V_{PVIN}$.

The ADP2165/ADP2166 use adaptive slope compensation in the current loop to prevent subharmonic oscillations when the duty cycle is larger than 50%. The internal slope compensation limits the minimum inductor value.

For a duty cycle that is larger than 50%, the minimum inductor value is determined by using the following equation:

$$L\ (Minimum) = \frac{V_{OUT} \times (1 - D)}{4 \times f_{SW}}$$

The peak inductor current is calculated by using the following equation:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a quick saturation characteristic, the saturation current rating of the inductor must be higher than the current limit threshold of the switch. This prevents the inductor from reaching saturation.

The rms current of the inductor is calculated from the following equation:

$$I_{RMS} = \sqrt{{I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low EMI. Table 6 lists some recommended inductors.

Table 6. Recommended Inductors

Vendor	Part No.	L (µH)	I_{SAT} (A)	I_{RMS} (A)	DCR (mΩ)
Würth Elektronik	744311022	0.22	32	21	1.10
	744314047	0.47	20	18	1.35
	744314076	0.76	15	15.5	2.25
	744311100	1.0	19	15	4.6
	744311150	1.5	14	11	6.6
	7443340220	2.2	12.5	16.5	4.4
	7443340330	3.3	8.5	14	6.5
Coilcraft	XAL7020-271ME	0.27	30	21	2.9
	XAL7020-331ME	0.33	28	20	4.0
	XAL7020-471ME	0.47	24.3	17	4.75
	XAL7020-681ME	0.68	22.3	13	7.9
	XAL7020-102ME	1.0	16.4	11	9.8
	XAL7030-152ME	1.5	23.5	15	7.6
	XAL7030-222ME	2.2	18	12.9	13.7

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects the output ripple voltage load step transient and the loop stability of the regulator.

For example, during a load step transient where the load is suddenly increased, the output capacitor supplies the load until the control loop can ramp up the inductor current. The delay caused by the control loop causes the output to undershoot. The output capacitance that is required to satisfy the voltage droop requirement can be calculated by using the following equation:

$$C_{OUT\_UV} = \frac{K_{UV} \times {\Delta I_{STEP}}^2 \times L}{2 \times (V_{PVIN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where:
K_{UV} is a factor, with a typical setting of $K_{UV} = 2$.
ΔI_{STEP} is the load step.
ΔV_{OUT_UV} is the allowable undershoot on the output voltage.

Another example occurs when a load is suddenly removed from the output, and the energy stored in the inductor rushes into the output capacitor, causing the output to overshoot.

The output capacitance that is required to meet the overshoot requirement can be calculated using the following equation:

$$C_{OUT\_OV} = \frac{K_{OV} \times {\Delta I_{STEP}}^2 \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^2 - {V_{OUT}}^2}$$

where:
K_{OV} is a factor, with a typical setting of $K_{OV} = 2$.
ΔV_{OUT_OV} is the allowable overshoot on the output voltage.

The ESR and the value of the capacitance determine the output ripple. Use the following equation to select a capacitor that can meet the output ripple requirements:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

where:
ΔV_{OUT_RIPPLE} is the allowable output ripple voltage.
R_{ESR} is the equivalent series resistance of the output capacitor in ohms (Ω).

Select the largest output capacitance given by C_{OUT_UV}, C_{OUT_OV}, and C_{OUT_RIPPLE} to meet both the load transient and the output ripple performance.

The selected output capacitor voltage rating must be greater than the output voltage. The rms current rating of the output capacitor must be larger than the value calculated by

$$I_{C_{OUT\_RMS}} = \frac{\Delta I_L}{\sqrt{12}}$$

COMPENSATION DESIGN

For peak current mode control, the power stage can be simplified as a voltage controlled current source supplying current to the output capacitor and load resistor. It is composed of one domain pole and a zero that is contributed by the output capacitor ESR. The control to output transfer function is based on the following:

$$G_{VD}(S) = \frac{V_{OUT}(s)}{V_{COMP}(s)} = A_{VI} \times R \times \frac{1 + \frac{s}{2 \times \pi \times f_Z}}{1 + \frac{s}{2 \times \pi \times f_P}}$$

$$f_Z = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

$$f_P = \frac{1}{2 \times \pi \times (R + R_{ESR}) \times C_{OUT}}$$

where:
A_{VI} = 10 A/V.
R is the load resistance.
C_{OUT} is the output capacitance.
R_{ESR} is the equivalent series resistance of the output capacitor.

The ADP2165/ADP2166 use a transconductance amplifier for the error amplifier, which compensates for the system loop. Figure 30 shows the simplified, peak current mode control, small signal circuit.

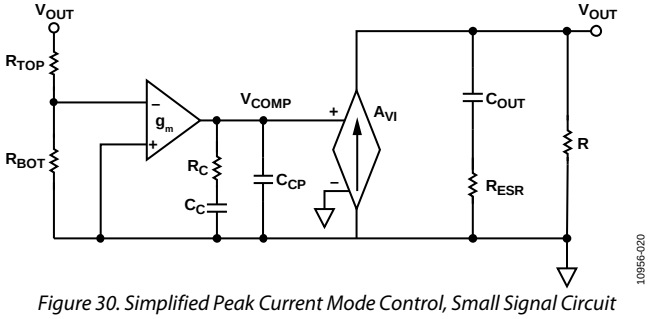

Figure 30. Simplified Peak Current Mode Control, Small Signal Circuit

The compensation components, R_C and C_C, contribute a zero, and the optional C_{CP} and R_C contribute an optional pole.

The loop gain transfer equation is as follows:

$$T_V(S) = \frac{R_{BOT}}{R_{BOT} + R_{TOP}} \times \frac{-g_m}{C_C + C_{CP}} \times \frac{1 + R_C \times C_C \times s}{s \times (1 + \frac{R_C \times C_C \times C_{CP}}{C_C + C_{CP}} \times s)} \times G_{VD}(s)$$

The following design guideline shows how to select the R_C, C_C, and C_{CP} compensation components for the ceramic output capacitor applications:

1. Determine the cross frequency, f_C. Generally, f_C is between $f_{SW}/12$ and $f_{SW}/6$.
2. Calculate R_C by using the following equation:

$$R_C = \frac{2 \times \pi \times V_{OUT} \times C_{OUT} \times f_C}{0.6\,\text{V} \times g_m \times A_{VI}}$$

3. Place the compensation zero at the domain pole, f_P; then determine C_C by using the following equation:

$$C_C = \frac{(R + R_{ESR}) \times C_{OUT}}{R_C}$$

4. C_{CP} is optional. It can be used to cancel the zero caused by the ESR of the output capacitor.

$$C_{CP} = \frac{R_{ESR} \times C_{OUT}}{R_C}$$

The fixed output version IC must consider the feedforward capacitance of feedback resistor (R_{TOP}) to calculate C_{CP}. The total internal feedback resistance is 1 MΩ.

First, place the compensation pole at the minimum value between the domain pole, f_P, and $\sqrt{f_{FB_P} \times f_{FB_Z}}$.

$$f_{FB_P} = \frac{1}{2\pi \times C_F \times (1/R_{TOP} + 1/R_{BOT})}$$

$$f_{FB_Z} = \frac{1}{2\pi \times R_{TOP} \times C_F}$$

Then, determine C_{CP} by

$$C_{CP} = \frac{C_C \times min\left(f_P, \sqrt{f_{FB_P} \times f_{FB_Z}}\right)}{R_C \times C_C - C_C \times min\left(f_P, \sqrt{f_{FB_P} \times f_{FB_Z}}\right)}$$

where C_F = 8.14 pF.

DESIGN EXAMPLE

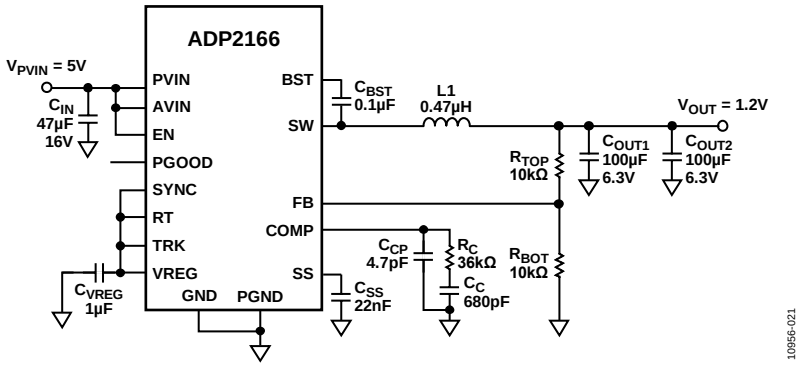

Figure 31. Schematic for Design Example

This section describes the procedures for selecting the external components based on the example specifications listed in Table 7. See Figure 31 for the schematic of this design example.

Table 7. Step-Down DC-to-DC Regulator Requirements

Parameter	Specification
Input Voltage	V_{PVIN} = 5.0 V ± 10%
Output Voltage	V_{OUT} = 1.2 V
Output Current	I_{OUT} = 6 A
Output Voltage Ripple	ΔV_{OUT_RIPPLE} = 12 mV
Load Transient	±5%, 1 A to 5 A, 2 A/µs
Switching Frequency	f_{SW} = 1.2 MHz

OUTPUT VOLTAGE SETTING

Choose a 10 kΩ resistor as the top feedback resistor (R_{TOP}) and calculate the bottom feedback resistor (R_{BOT}) by using the following equation:

$$R_{BOT} = R_{TOP} \times \left(\frac{0.6}{V_{OUT} - 0.6} \right)$$

To set the output voltage to 1.2 V, the resistor values are as follows: R_{TOP} = 10 kΩ and R_{BOT} = 10 kΩ.

FREQUENCY SETTING

To use the fixed 1.2 MHz switching frequency, connect the RT pin to the VREG pin.

INDUCTOR SELECTION

The peak-to-peak inductor ripple current, ΔI_L, is set to 30% of the maximum output current. Use the following equation to estimate the inductor value:

$$L = \frac{(V_{PVIN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:
V_{PVIN} = 5 V.
V_{OUT} = 1.2 V.
D = 0.24.
ΔI_L = 1.8 A.
f_{SW} = 1.2 MHz.

This calculation results in L = 0.422 µH. Choose the standard inductor value of 0.47 µH.

The peak-to-peak inductor ripple current can be calculated by using the following equation:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}}$$

This calculation results in ΔI_L = 1.617 A.

Use the following equation to calculate the peak inductor current:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

This calculation results in I_{PEAK} = 6.809 A.

Use the following equation to calculate the rms current flowing through the inductor:

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}$$

This calculation results in I_{RMS} = 6.018 A.

Based on the calculated current value, select an inductor with a minimum rms current rating of 6.03 A and a minimum saturation current rating of 6.9 A.

However, to protect the inductor from reaching its saturation point under the current-limit condition, use an inductor that is rated for at least a 9 A saturation current for reliable operation.

Based on the requirements described previously, select a 0.47 µH inductor, such as the 744314047 from Würth, which has a 1.35 mΩ DCR and a 20 A saturation current.

OUTPUT CAPACITOR SELECTION

The output capacitor is required to meet both the output voltage ripple and load transient response requirements.

To meet the output voltage ripple requirement, use the following equation to calculate the ESR and capacitance value of the output capacitor:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_S \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

This calculation results in C_{OUT_RIPPLE} = 14 µF and R_{ESR} = 7.4 mΩ.

To meet the ±5% overshoot and undershoot transient requirements, use the following equations to calculate the capacitance:

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}{}^2 \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^2 - V_{OUT}{}^2}$$

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}{}^2 \times L}{2 \times (V_{PVIN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where:
$K_{OV} = K_{UV} = 2$, the coefficients for estimation purposes.
ΔI_{STEP} = 4 A, the load transient step.
ΔV_{OUT_OV} = 5% × V_{OUT}, the overshoot voltage.
ΔV_{OUT_UV} = 5% × V_{OUT}, the undershoot voltage.

This calculation results in C_{OUT_OV} = 100 µF and C_{OUT_UV} = 33 µF.

According to the calculation, the output capacitance must be greater than 100 µF, and the ESR of the output capacitor must be smaller than 7.4 mΩ. It is recommended that one 100 µF, X5R, 6.3 V ceramic capacitor and one 47 µF, X5R, 6.3 V ceramic capacitor be used, such as the GRM32ER60J107ME20 and GRM32ER60J476ME20 from Murata, with an ESR of 2 mΩ.

COMPENSATION COMPONENTS

For better load transient and stability performance, set the cross frequency, f_C, to f_{SW}/10. In this case, f_{SW} is running at 1200 kHz; therefore, the f_C is set to 120 kHz.

The 100 µF and 47 µF ceramic output capacitors have a derated value of 62 µF and 32 µF.

$$R_C = \frac{2 \times \pi \times 1.2\,\text{V} \times 94\,\mu\text{F} \times 120\,\text{kHz}}{0.6\,\text{V} \times 500\,\mu\text{s} \times 10\,\text{A/V}} = 28.35\ \text{k}\Omega$$

$$C_C = \frac{(0.2\ \Omega + 0.002\ \Omega) \times 94\ \mu\text{F}}{28.35\ \text{k}\Omega} = 669.8\ \text{pF}$$

$$C_{CP} = \frac{0.002\ \Omega \times 94\ \mu\text{F}}{28.35\ \text{k}\Omega} = 6.63\ \text{pF}$$

Choose standard components as follows: R_C = 27 kΩ, C_C = 680 pF, and C_{CP} = 4.7 pF.

SOFT START TIME PROGRAM

The soft start feature allows the output voltage to ramp up in a controlled manner, eliminating output voltage overshoot during soft start and limiting the inrush current. Set the soft start time to 4 ms.

$$C_{SS} = \frac{t_{SS\_EXT} \times I_{SS\_UP}}{0.6} = \frac{4\ \text{ms} \times 3.5\,\mu\text{A}}{0.6\,\text{V}} = 23.3\ \text{nF}$$

Choose a standard component value as follows: C_{SS} = 22 nF.

INPUT CAPACITOR SELECTION

A minimum 22 µF ceramic capacitor must be placed near the PVIN pin. In this application, it is recommended that one 47 µF, X5R, 16 V ceramic capacitor be used.

RECOMMENDED EXTERNAL COMPONENTS

Table 8. Recommended External Components for Typical Applications with 6 A Output Current

f_{SW} (kHz)	V_{PVIN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)[1]	R_{TOP} (kΩ)	R_{BOT} (kΩ)	R_C (kΩ)	C_C (pF)	C_{CP} (pF)
300	3.3	1	1.5	680 + 330	10	15	52.9	3300	134
	3.3	1.2	1.5	680 + 47	10	10	44.7	3300	111
	3.3	1.5	2.2	680	15	10	53.4	3300	89
	3.3	1.8	2.2	470 + 100	20	10	50.1	3300	85
	3.3	2.5	1.5	470 + 47	47.5	15	65.7	3300	61
	5	1	1.5	680 + 330	10	15	52.9	3300	668
	5	1.2	2.2	680 + 470	10	10	72.3	3300	64
	5	1.5	2.2	680	15	10	53.4	3300	89
	5	1.8	2.2	470	20	10	44.3	3300	85
	5	2.5	3.3	330 + 47	47.5	15	47.4	3300	267
	5	3.3	2.2	3 × 100	10	2.21	32.1	3300	12
600	3.3	1	0.6	330 + 47	10	15	45.5	1600	279
	3.3	1.2	0.82	330 + 47	10	10	54.6	1500	232
	3.3	1.5	0.82	2 × 100 + 47	15	10	29.4	1300	11
	3.3	1.8	0.82	2 × 100	20	10	28.0	1300	9
	3.3	2.5	0.6	2 × 100	47.5	15	39.0	1300	6
	5	1	0.82	470 + 100	10	15	66.9	1300	64
	5	1.2	0.82	330 + 47	10	10	54.6	1500	232
	5	1.5	1	330	15	10	62.2	1500	186
	5	1.8	1	2 × 100	20	10	28.0	1300	9
	5	2.5	1.5	100 + 47	47.5	15	39.0	1300	6
	5	3.3	1	100	10	2.21	25.7	1300	5
1200	3.3	1	0.33	2 × 100	10	15	31.2	680	8
	3.3	1.2	0.47	2 × 100	10	10	37.4	680	7
	3.3	1.5	0.47	100 + 47	15	10	35.4	680	5
	3.3	1.8	0.47	100	20	10	28.0	680	4
	3.3	2.5	0.33	100	47.5	15	39.0	680	3
	5	1	0.47	330	10	15	82.9	680	139
	5	1.2	0.47	2 × 100	10	10	37.4	680	7
	5	1.5	0.47	100 + 47	15	10	35.4	680	5
	5	1.8	0.6	100	20	10	28.0	680	4
	5	2.5	0.6	100	47.5	15	19.6	680	3
	5	3.3	0.6	100	10	2.21	51.4	680	2

[1] 680 µF: 2.5 V, KEMET T520D687M2R5ATE010; 470 µF: 2.5 V, KEMET T520D477M2R5ATE006; 330 µF: 2.5 V, KEMET T520D337M2R5ATE006; 220 µF: 2.5 V, KEMET T520D227M2R5ATE007; 330 µF: 4 V, KEMET T520D337M004ATE006; 100 µF: 6.3 V, X5R, Murata GRM32ER60J107ME20; 47 µF: 6.3 V, X5R, Murata GRM32ER60J476ME20. V_{OUT} is higher than 1.5 V, and C_{OUT} must use a 4 V tantalum capacitor.

PRINTED CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good circuit board layout is essential for obtaining the best performance from the ADP2165/ADP2166. Poor printed circuit board (PCB) layout degrades the output regulation as well as the electromagnetic interface (EMI) and electromagnetic compatibility (EMC) performance. Figure 32 shows a PCB layout example. For optimum layout, use the following guidelines:

- Use separate analog ground and power ground planes. Connect the ground reference of sensitive analog circuitry, such as output voltage divider components, to analog ground. In addition, connect the ground reference of power components, such as input and output capacitors, to power ground. Connect both ground planes to the exposed pad of the ADP2165/ADP2166.
  Place the input capacitor, inductor, and output capacitor as close to the IC as possible and use short traces.
- Ensure that the high current loop traces are as short and as wide as possible. Make the high current path from the input capacitor through the inductor, the output capacitor, and the power ground plane back to the input capacitor as short as possible. To accomplish this, ensure that the input and output capacitors share a common power ground plane.
- Connect the exposed pad of the ADP2165/ADP2166 to a large copper plane to maximize its power dissipation capability for better thermal dissipation.

Place the feedback resistor divider network as close as possible to the FB pin to prevent noise pickup. Try to minimize the length of the trace that connects the top of the feedback resistor divider to the output while keeping the trace away from the high current traces and the switching node to avoid noise pickup. To further reduce noise pickup, place an analog ground plane on either side of the FB trace and ensure that the trace is as short as possible to reduce parasitic capacitance pickup.

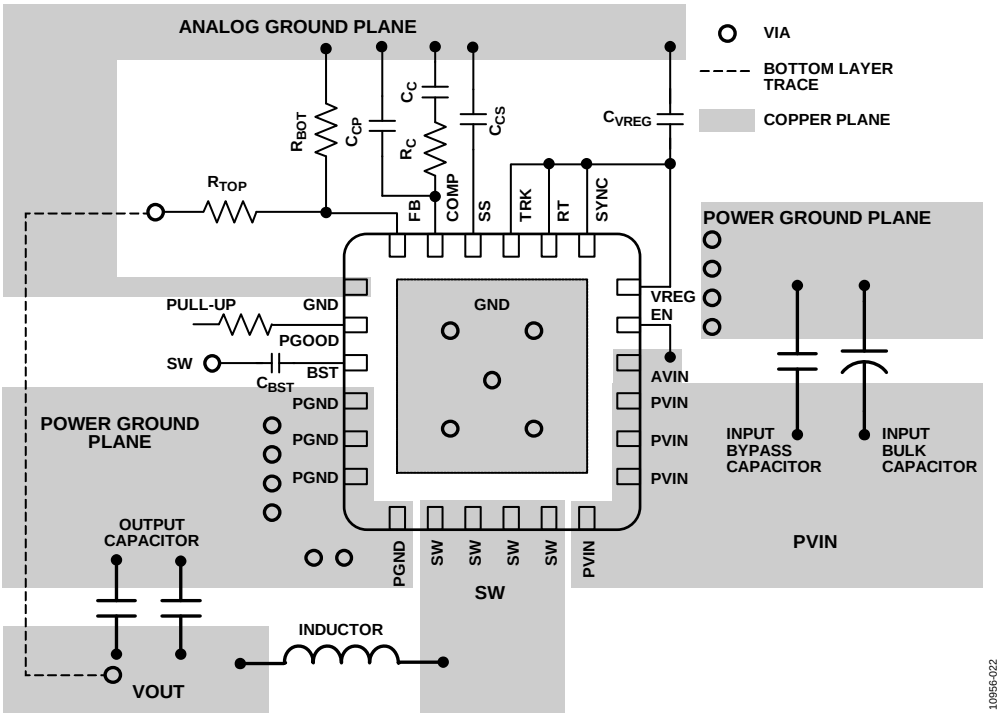

Figure 32. Recommended PCB Layout

REFERENCE DESIGNS

See Figure 33 through Figure 36 for the detailed reference designs.

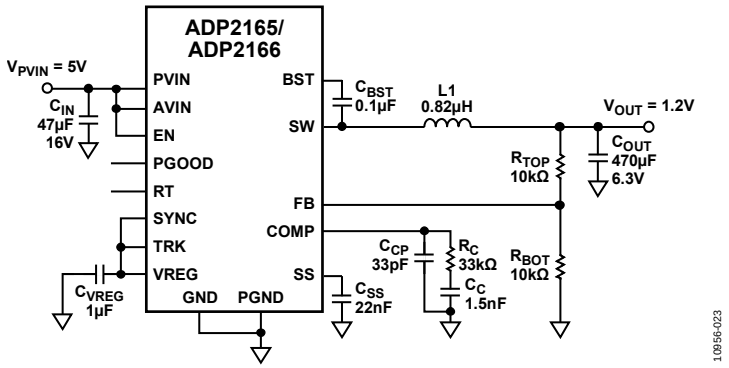

Figure 33. 1.2 V, 5 A/6 A, 620 kHz by Floating the RT Pin Step-Down Regulator Application

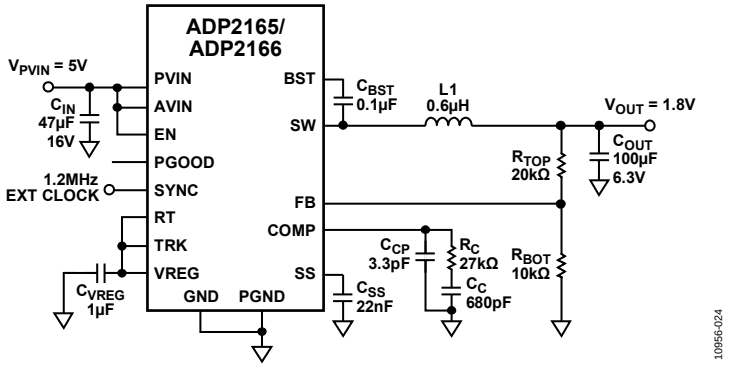

Figure 34. 1.8 V, 5 A/6 A Step-Down Regulator Application, Synchronized to 1.2 MHz, 180° Out of Phase with the External Clock

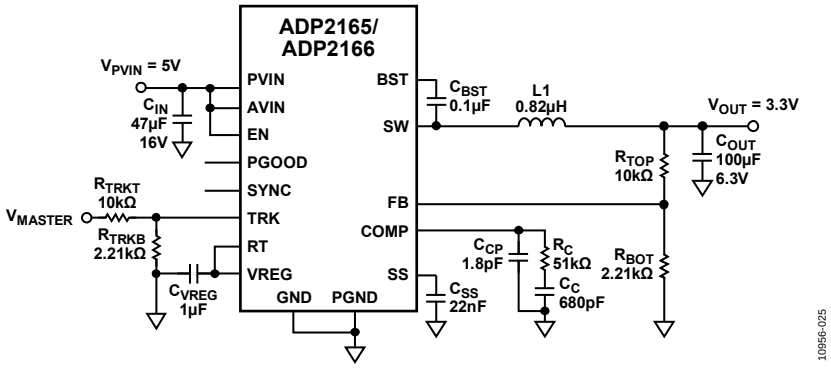

Figure 35. 3.3 V, 5 A/6 A, 1.2 MHz Step-Down Regulator Application, Tracking Mode

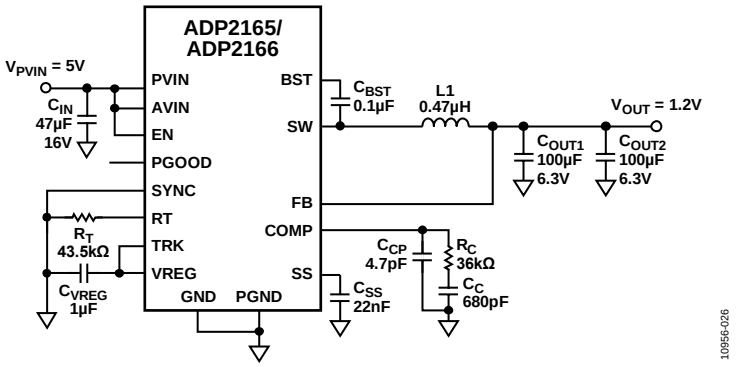

Figure 36. Fixed Output 1.2 V, 5 A/6 A, 1.2 MHz Step-Down Regulator Application