20 V, 500 mA, Low Noise LDO Regulator with Soft Start

Data Sheet **ADP7105**

FEATURES

Input voltage range: 3.3 V to 20 V
Maximum output current: 500 mA
Low noise: 15 µV rms for fixed output versions
PSRR performance of 60 dB at 10 kHz, V_{OUT} = 3.3 V
Reverse current protection
Low dropout voltage: 350 mV at 500 mA
Initial accuracy: ±0.8%
Accuracy over line, load, and temperature
- **−2% to +1%, T_J = −40°C to +125°C**
- **−1.25% to +1%, T_J = 0°C to +85°C**

Low quiescent current: 900 µA at V_{IN} = 10 V, I_{OUT} = 500 mA
Low shutdown current: <50 µA at V_{IN} = 12 V, stable with small 1 µF ceramic output capacitor
3 fixed output voltage options: 1.8, 3.3 V and 5 V
Adjustable output from 1.22 V to 19 V
Programmable soft start for inrush current control
Foldback current-limit and thermal overload protection
User programmable precision UVLO/enable
Power-good indicator
8-lead LFCSP and 8-lead SOIC packages

APPLICATIONS

Regulation of noise sensitive applications: ADC and DAC circuits, precision amplifiers, high frequency oscillators, clocks, and PLLs
Communications and infrastructure
Medical and healthcare
Industrial and instrumentation

TYPICAL APPLICATION CIRCUITS

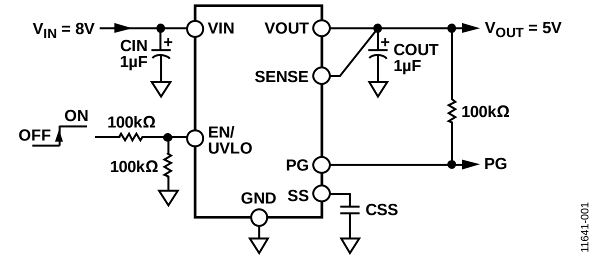

Figure 1. ADP7105 with Fixed Output Voltage, 5 V

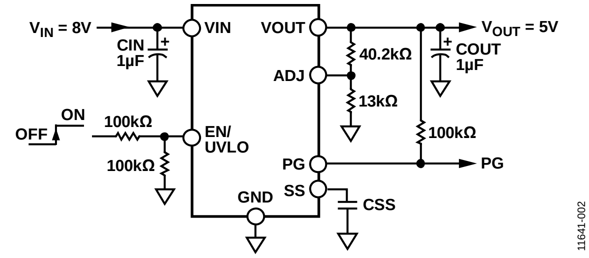

Figure 2. ADP7105 with Adjustable Output Voltage, 5 V

GENERAL DESCRIPTION

The ADP7105 is a CMOS, low dropout (LDO) linear regulator that operates from 3.3 V to 20 V and provides up to 500 mA of output current. This high input voltage LDO is ideal for regulation of high performance analog and mixed-signal circuits operating from 1.22 V to 19 V rails. Using an advanced proprietary architecture, the ADP7105 provides high power supply rejection and low noise, and achieves excellent line and load transient response with only a small 1 µF ceramic output capacitor.

The ADP7105 is available in three fixed output voltage options and an adjustable version that allows output voltages ranging from 1.22 V to 19 V via an external feedback divider. The ADP7105 allows an external soft start capacitor to be connected to program the startup.

Note that throughout this data sheet, the sense function (SENSE) of the SENSE/ADJ pin applies to fixed output voltage models only, whereas the adjust input function (ADJ) applies to adjustable output voltage models only. For example, Figure 1 shows the sense function, and Figure 2 shows the adjust input function.

The ADP7105 output noise voltage is 15 µV rms and is independent of the output voltage. A digital power-good output allows power system monitors to check the health of the output voltage. A user programmable precision undervoltage lockout function facilitates sequencing of multiple power supplies.

The ADP7105 is available in 8-lead, 3 mm × 3 mm LFCSP and 8-lead SOIC packages. The LFCSP offers a very compact solution and provides excellent thermal performance for applications that require up to 500 mA of output current in a small, low profile footprint.

Rev. C **Document Feedback**

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REVISION HISTORY

1/2020—Rev. B to Rev. C

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10/2015—Rev. A to Rev. B

Changes to Figure 60 and Figure 61 ... 17

5/2014—Rev. 0 to Rev. A

Change to UVLO Threshold Rising Parameter, Table 1 ... 4

7/2013—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} + 1 V) or 3.3 V (whichever is greater), EN = V_{IN}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}		3.3		20	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 100 µA, V_{IN} = 10 V		400		µA
		I_{OUT} = 100 µA, V_{IN} = 10 V, T_J = −40°C to +125°C			900	µA
		I_{OUT} = 10 mA, V_{IN} = 10 V		450		µA
		I_{OUT} = 10 mA, V_{IN} = 10 V, T_J = −40°C to +125°C			1050	µA
		I_{OUT} = 300 mA, V_{IN} = 10 V		750		µA
		I_{OUT} = 300 mA, V_{IN} = 10 V, T_J = −40°C to +125°C			1400	µA
		I_{OUT} = 500 mA, V_{IN} = 10 V		900		µA
		I_{OUT} = 500 mA, V_{IN} = 10 V, T_J = −40°C to +125°C			1600	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND, V_{IN} = 12 V		40	50	µA
		EN = GND, V_{IN} = 12 V, T_J = −40°C to +125°C			75	µA
INPUT REVERSE CURRENT	$I_{REV-INPUT}$	EN = GND, V_{IN} = 0 V, V_{OUT} = 20 V		0.3		µA
		EN = GND, V_{IN} = 0 V, V_{OUT} = 20 V, T_J = −40°C to +125°C			5	µA
OUTPUT VOLTAGE ACCURACY						
Fixed Output Voltage Accuracy	V_{OUT}	I_{OUT} = 10 mA	−0.8		+0.8	%
		1 mA < I_{OUT} < 500 mA, V_{IN} = (V_{OUT} + 1 V) to 20 V, T_J = −40°C to +125°C	−2		+1	%
		1 mA < I_{OUT} < 500 mA, V_{IN} = (V_{OUT} + 1 V) to 20 V, T_J = 0°C to +85°C	−1.25		+1	%
Adjustable Output Voltage Accuracy	V_{ADJ}	I_{OUT} = 10 mA	1.21	1.22	1.23	V
		1 mA < I_{OUT} < 500 mA, V_{IN} = (V_{OUT} + 1 V) to 20 V, T_J = −40°C to +125°C	1.196		1.232	V
		1 mA < I_{OUT} < 500 mA, V_{IN} = (V_{OUT} + 1 V) to 20 V, T_J = 0°C to +85°C	1.204		1.232	V
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 1 V) to 20 V, T_J = −40°C to +125°C	−0.015		+0.015	%/V
LOAD REGULATION[1]	$\Delta V_{OUT}/\Delta I_{OUT}$	1 mA < I_{OUT} < 500 mA		0.2		%/A
		1 mA < I_{OUT} < 500 mA, T_J = −40°C to +125°C			0.75	%/A
ADJ INPUT BIAS CURRENT[2]	ADJ_{I-BIAS}	1 mA < I_{OUT} < 500 mA, V_{IN} = (V_{OUT} + 1 V) to 20 V, ADJ connected to VOUT		10		nA
SENSE INPUT BIAS CURRENT[2]	$SENSE_{I-BIAS}$	1 mA < I_{OUT} < 500 mA, V_{IN} = (V_{OUT} + 1 V) to 20 V, SENSE connected to VOUT, V_{OUT} = 1.5 V		1		µA
DROPOUT VOLTAGE[3]	$V_{DROPOUT}$	I_{OUT} = 10 mA		20		mV
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			40	mV
		I_{OUT} = 150 mA		100		mV
		I_{OUT} = 150 mA, T_J = −40°C to +125°C			175	mV
		I_{OUT} = 300 mA		200		mV
		I_{OUT} = 300 mA, T_J = −40°C to +125°C			325	mV
		I_{OUT} = 500 mA		350		mV
		I_{OUT} = 500 mA, T_J = −40°C to +125°C			550	mV
START-UP TIME[4]	$t_{START-UP}$	C_{SS} = 0 nF, I_{OUT} = 10 mA		625		µs
		C_{SS} = 10 nF, I_{OUT} = 10 mA		11.5		ms
CURRENT-LIMIT THRESHOLD[5]	I_{LIMIT}		625	775	1000	mA
PG OUTPUT LOGIC LEVEL						
PG Output Logic High	PG_{HIGH}	I_{OH} < 1 µA	1.0			V
PG Output Logic Low	PG_{LOW}	I_{OL} < 2 mA			0.4	V
PG OUTPUT THRESHOLD						
Output Voltage Falling	PG_{FALL}			−9.2		%
Output Voltage Rising	PG_{RISE}			−6.5		%

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
SOFT START SOURCE CURRENT	$SS_{I-SOURCE}$	SS = GND		1		µA
PROGRAMMABLE EN/UVLO						
UVLO Threshold Rising	$UVLO_{RISE}$	3.3 V ≤ V_{IN} ≤ 20 V, T_J = −40°C to +125°C	1.18	1.22	1.28	V
UVLO Threshold Falling	$UVLO_{FALL}$	3.3 V ≤ V_{IN} ≤ 20 V, T_J = −40°C to +125°C, 10 kΩ in series with the enable input pin		1.13		V
UVLO Hysteresis Current	$UVLO_{HYS}$	V_{EN} > 1.25 V, T_J = −40°C to +125°C	7.5	9.8	12	µA
Enable Pull-Down Current	I_{EN-IN}	EN = V_{IN}		500		nA
Start Threshold	V_{START}	T_J = −40°C to +125°C			3.2	V
Shutdown Threshold	$V_{SHUTDOWN}$	T_J = −40°C to +125°C	2.45			V
Hysteresis				250		mV
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{IN} = 5.5 V, V_{OUT} = 1.8 V		15		µV rms
		10 Hz to 100 kHz, V_{IN} = 6.3 V, V_{OUT} = 3.3 V		15		µV rms
		10 Hz to 100 kHz, V_{IN} = 8 V, V_{OUT} = 5 V		15		µV rms
		10 Hz to 100 kHz, V_{IN} = 12 V, V_{OUT} = 9 V		15		µV rms
		10 Hz to 100 kHz, V_{IN} = 5.5 V, V_{OUT} = 1.5 V, adjustable mode		18		µV rms
		10 Hz to 100 kHz, V_{IN} = 12 V, V_{OUT} = 5 V, adjustable mode		30		µV rms
		10 Hz to 100 kHz, V_{IN} = 20 V, V_{OUT} = 15 V, adjustable mode		65		µV rms
POWER SUPPLY REJECTION RATIO	PSRR	100 kHz, V_{IN} = 4.3 V, V_{OUT} = 3.3 V		50		dB
		100 kHz, V_{IN} = 6 V, V_{OUT} = 5 V		50		dB
		10 kHz, V_{IN} = 4.3 V, V_{OUT} = 3.3 V		60		dB
		10 kHz, V_{IN} = 6 V, V_{OUT} = 5 V		60		dB
		100 kHz, V_{IN} = 3.3 V, V_{OUT} = 1.8 V, adjustable mode		50		dB
		100 kHz, V_{IN} = 6 V, V_{OUT} = 5 V, adjustable mode		60		dB
		100 kHz, V_{IN} = 16 V, V_{OUT} = 15 V, adjustable mode		60		dB
		10 kHz, V_{IN} = 3.3 V, V_{OUT} = 1.8 V, adjustable mode		60		dB
		10 kHz, V_{IN} = 6 V, V_{OUT} = 5 V, adjustable mode		80		dB
		10 kHz, V_{IN} = 16 V, V_{OUT} = 15 V, adjustable mode		80		dB

[1] Based on an endpoint calculation using 1 mA and 500 mA loads. See Figure 6 for typical load regulation performance for loads less than 1 mA.
[2] The adjust input function (ADJ) of the SENSE/ADJ pin applies to adjustable output voltage models only; whereas the sense function (SENSE) applies to fixed output voltage models only.
[3] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This specification applies only for output voltages greater than 3.0 V.
[4] Start-up time is defined as the time between the rising edge of EN to VOUT being at 90% of its nominal value.
[5] Current-limit threshold is defined as the current at which the output voltage falls to 90% of the specified typical value. For example, the current limit for a 5.0 V output voltage is defined as the current that causes the output voltage to fall to 90% of 5.0 V, or 4.5 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Minimum Input and Output Capacitance[1]	C_{MIN}	T_A = −40°C to +125°C	0.7			µF
Capacitor ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		0.2	Ω

[1] Ensure that the minimum input and output capacitance is greater than 0.7 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO regulator.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	−0.3 V to +22 V
VOUT to GND	−0.3 V to +20 V
EN/UVLO to GND	−0.3 V to VIN
PG to GND	−0.3 V to VIN
SENSE/ADJ to GND	−0.3 V to VOUT
SS to GND	−0.3 V to +3.6 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP7105 can be damaged when the junction temperature (T_J) limit is exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor printed circuit board (PCB) thermal resistance, the maximum ambient temperature may need to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. circuit board. See JEDEC JESD51-7 and JESD51-9 for detailed information on the board construction. For additional information, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*, available at www.analog.com.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. The package Ψ_{JB} is based on modeling and calculation using a 4-layer board. JEDEC JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than through a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. θ_{JC} is a parameter for surface-mount packages with top mounted heat sinks. θ_{JC} is presented here for reference only.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Ψ_{JB}	Unit
8-Lead LFCSP	40.1	27.1	17.2	°C/W
8-Lead SOIC	48.5	58.4	31.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

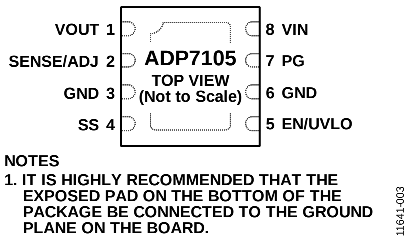

Figure 3. Pin Configuration, LFCSP Package

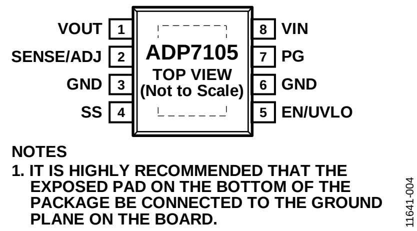

Figure 4. Pin Configuration, Narrow-Body SOIC Package

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 1 µF or greater capacitor.
2	SENSE/ADJ	Sense (SENSE). SENSE measures the actual output voltage at the load and feeds it to the error amplifier. Connect SENSE as close as possible to the load to minimize the effect of IR drop between the regulator output and the load. This function applies to fixed voltage models only. Adjust Input (ADJ). An external resistor divider sets the output voltage. This function applies to adjustable voltage models only.
3	GND	Ground.
4	SS	Soft Start. A capacitor connected to this pin determines the soft start time.
5	EN/UVLO	Enable Input (EN). Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN. Programmable Undervoltage Lockout (UVLO). When the programmable UVLO function is used, the upper and lower thresholds are determined by the programming resistors.
6	GND	Ground.
7	PG	Power Good. This open-drain output requires an external pull-up resistor to VIN or VOUT. If the part is in shutdown mode, current-limit mode, or thermal shutdown, or if V_{OUT} falls below 90% of the nominal output voltage, PG immediately transitions low. If the power-good function is not used, the pin can be left open or connected to ground.
8	VIN	Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor.
	EPAD	Exposed Pad. The exposed pad on the bottom of the package enhances thermal performance and is electrically connected to GND inside the package. It is highly recommended that the exposed pad be connected to the ground plane on the board.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 7.5 V, V_{OUT} = 5 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

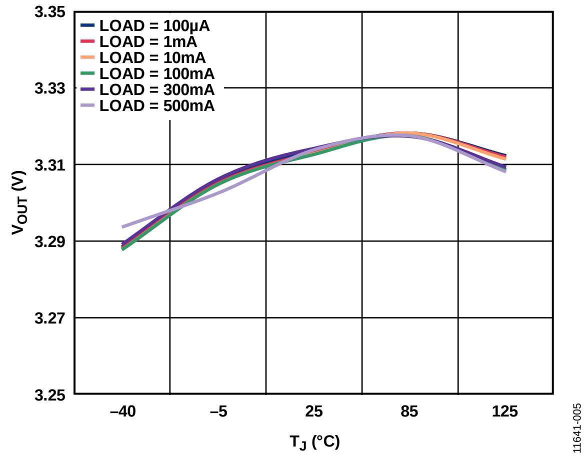

Figure 5. Output Voltage vs. Junction Temperature, V_{OUT} = 3.3 V

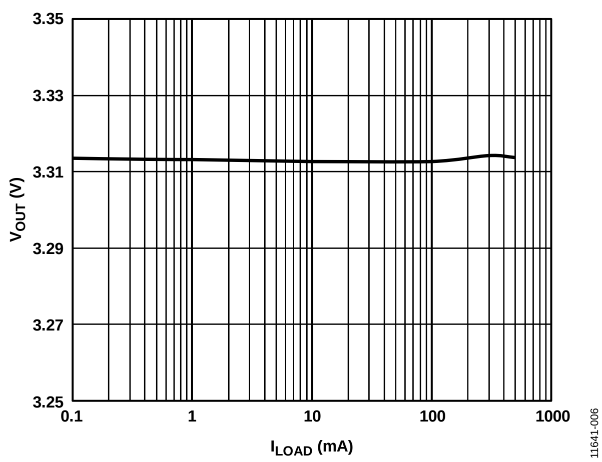

Figure 6. Output Voltage vs. Load Current, V_{OUT} = 3.3 V

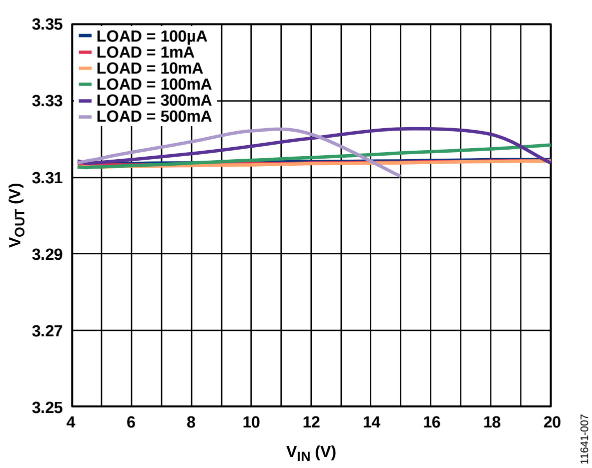

Figure 7. Output Voltage vs. Input Voltage, V_{OUT} = 3.3 V

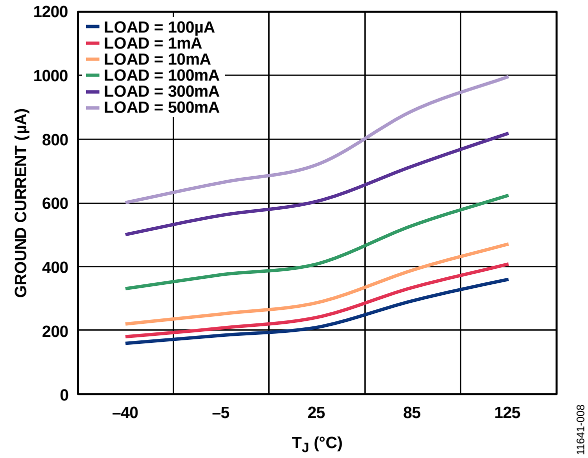

Figure 8. Ground Current vs. Junction Temperature, V_{OUT} = 3.3 V

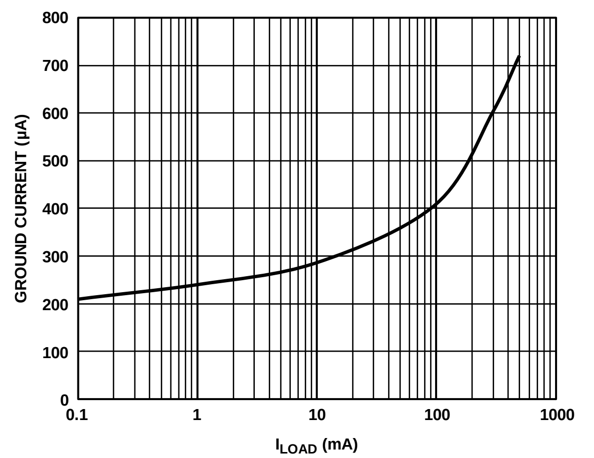

Figure 9. Ground Current vs. Load Current, V_{OUT} = 3.3 V

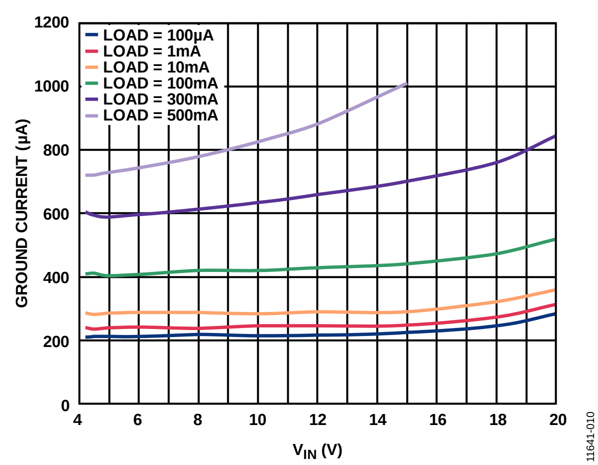

Figure 10. Ground Current vs. Input Voltage, V_{OUT} = 3.3 V

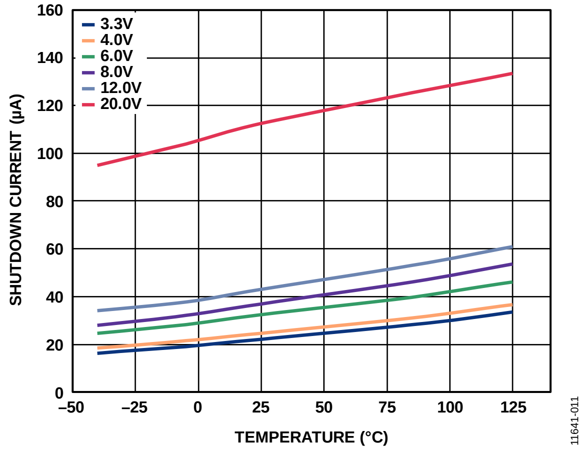

Figure 11. Shutdown Current vs. Temperature at Various Input Voltages

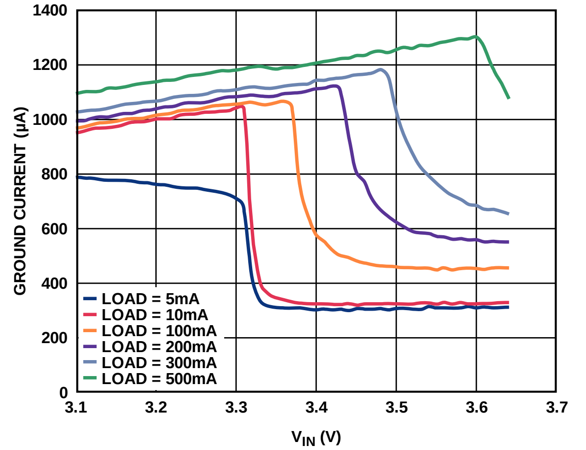

Figure 14. Ground Current vs. Input Voltage (in Dropout), $V_{OUT} = 3.3$ V

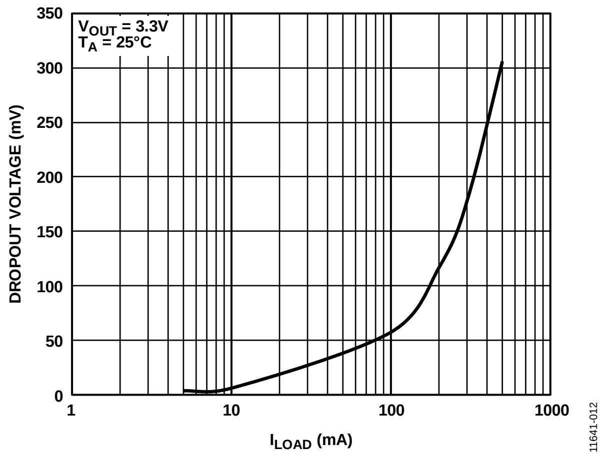

Figure 12. Dropout Voltage vs. Load Current, $V_{OUT} = 3.3$ V

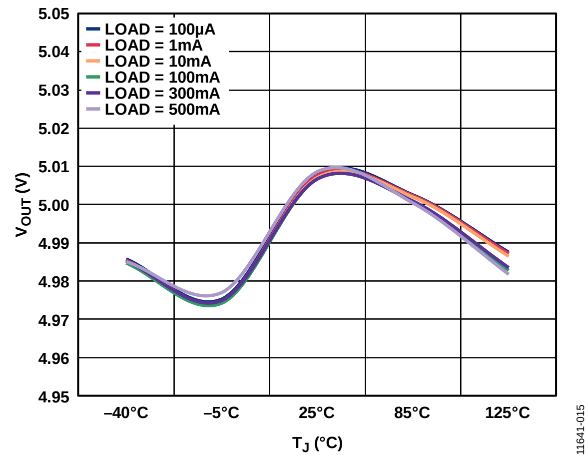

Figure 15. Output Voltage vs. Junction Temperature, $V_{OUT} = 5$ V

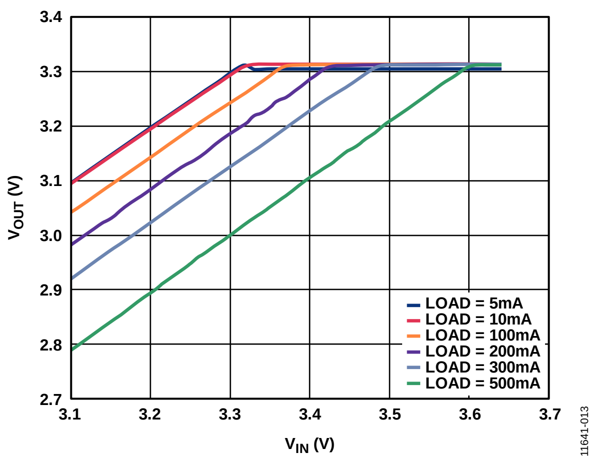

Figure 13. Output Voltage vs. Input Voltage (in Dropout), $V_{OUT} = 3.3$ V

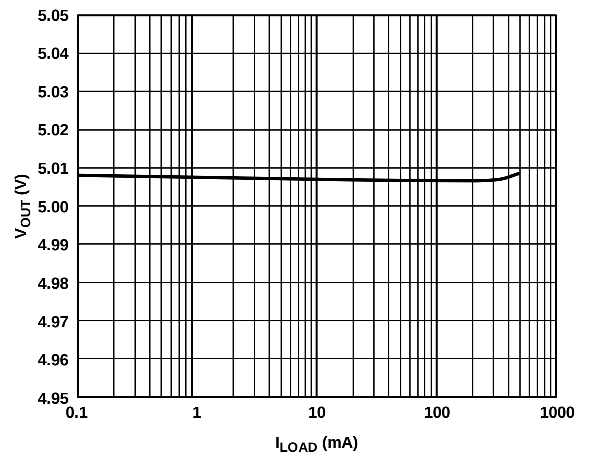

Figure 16. Output Voltage vs. Load Current, $V_{OUT} = 5$ V

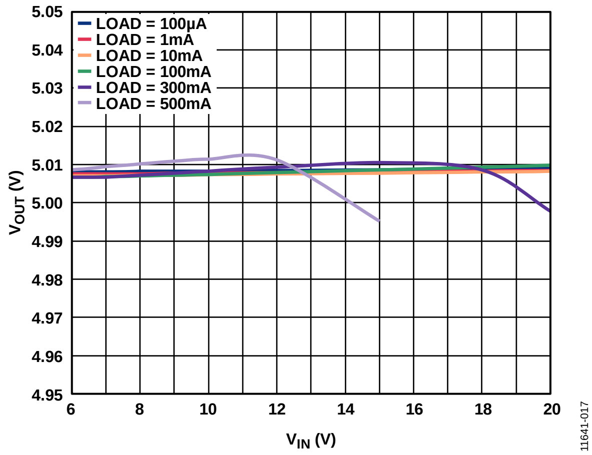

Figure 17. Output Voltage vs. Input Voltage, V_{OUT} = 5 V

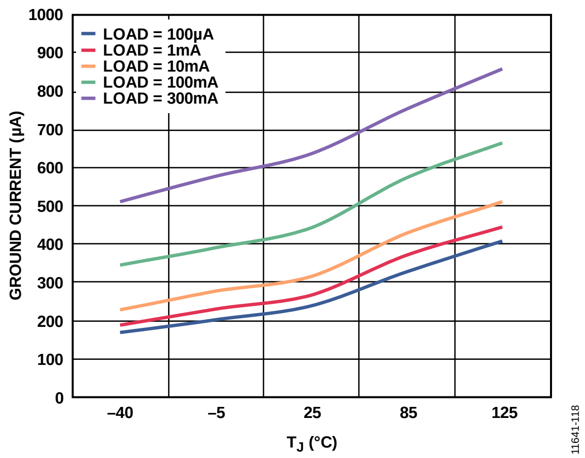

Figure 18. Ground Current vs. Junction Temperature, V_{OUT} = 5 V

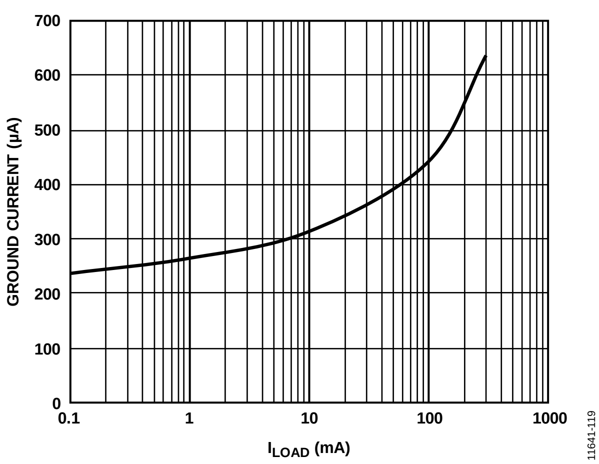

Figure 19. Ground Current vs. Load Current, V_{OUT} = 5 V

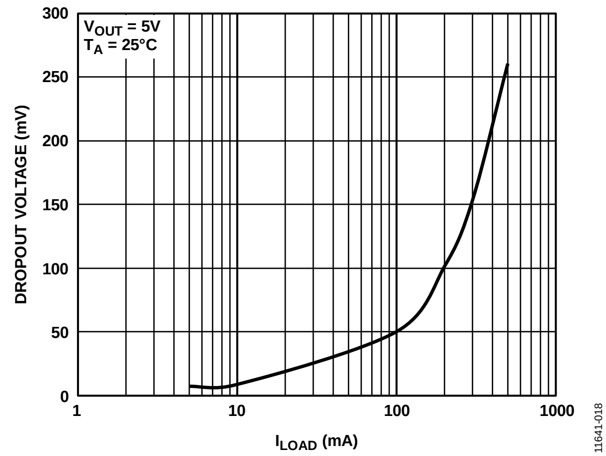

Figure 20. Dropout Voltage vs. Load Current, V_{OUT} = 5 V

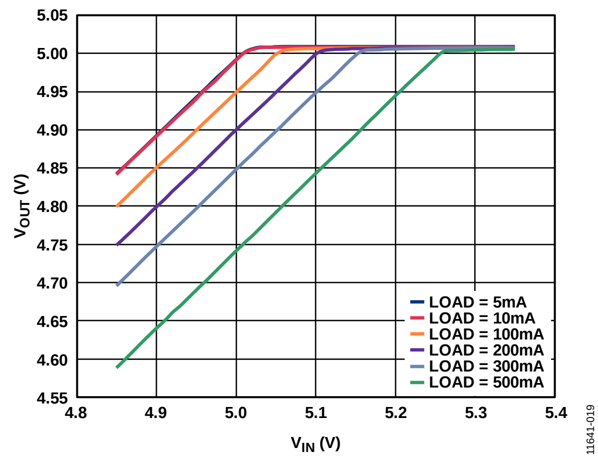

Figure 21. Output Voltage vs. Input Voltage (in Dropout), V_{OUT} = 5 V

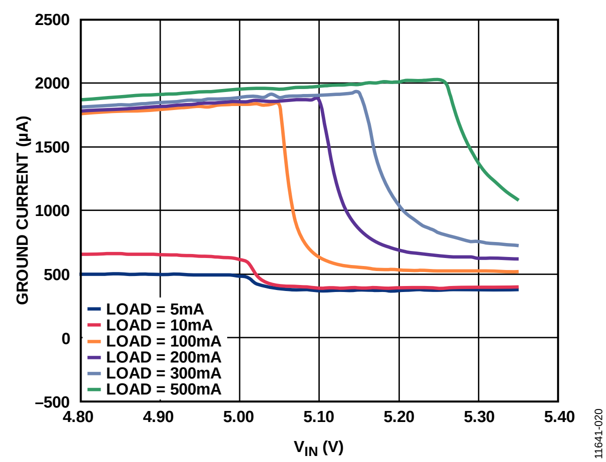

Figure 22. Ground Current vs. Input Voltage (in Dropout), V_{OUT} = 5 V

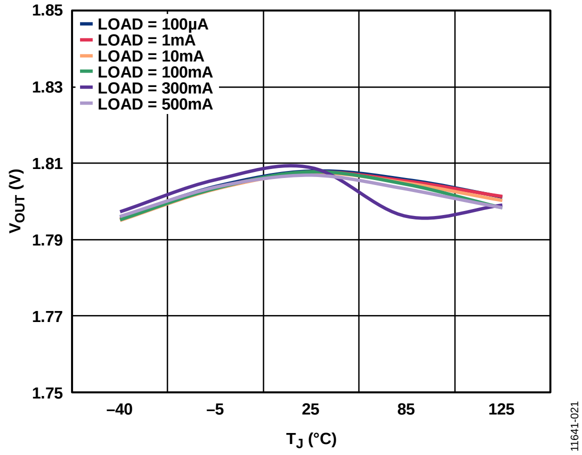

Figure 23. Output Voltage vs. Junction Temperature, $V_{OUT} = 1.8$ V

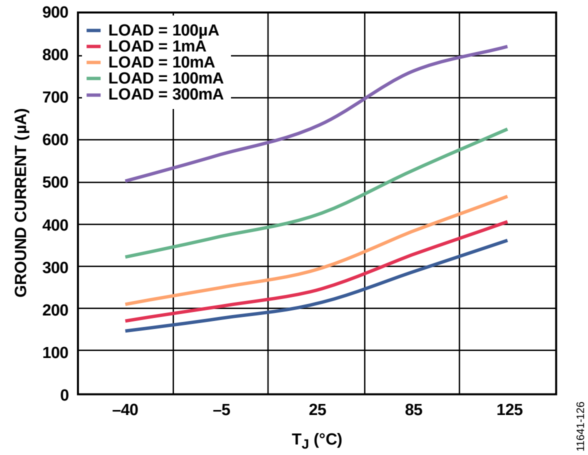

Figure 26. Ground Current vs. Junction Temperature, $V_{OUT} = 1.8$ V

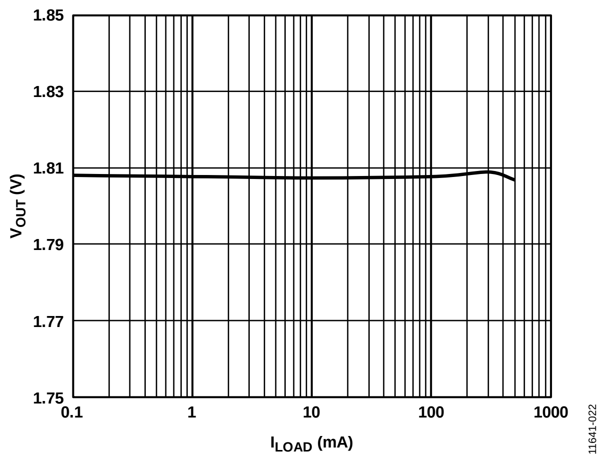

Figure 24. Output Voltage vs. Load Current, $V_{OUT} = 1.8$ V

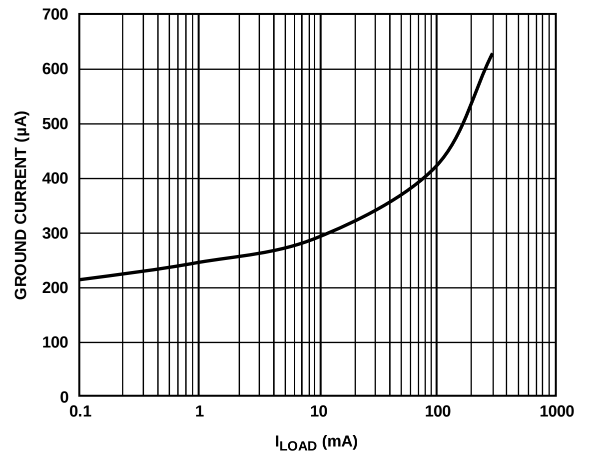

Figure 27. Ground Current vs. Load Current, $V_{OUT} = 1.8$ V

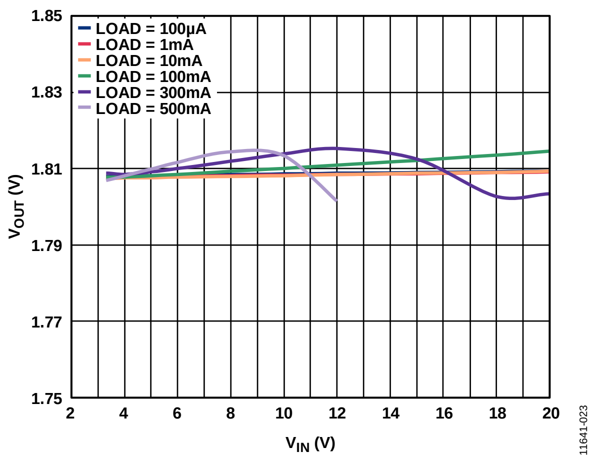

Figure 25. Output Voltage vs. Input Voltage, $V_{OUT} = 1.8$ V

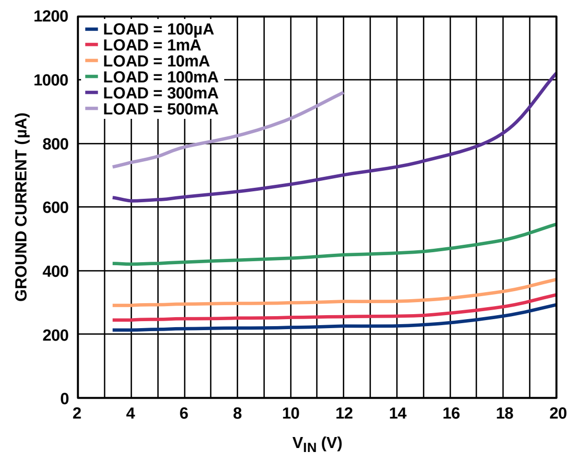

Figure 28. Ground Current vs. Input Voltage, $V_{OUT} = 1.8$ V

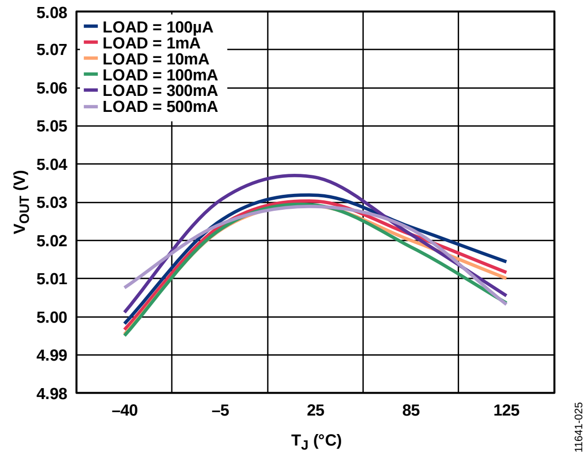

Figure 29. Output Voltage vs. Junction Temperature, V_{OUT} = 5 V, Adjustable

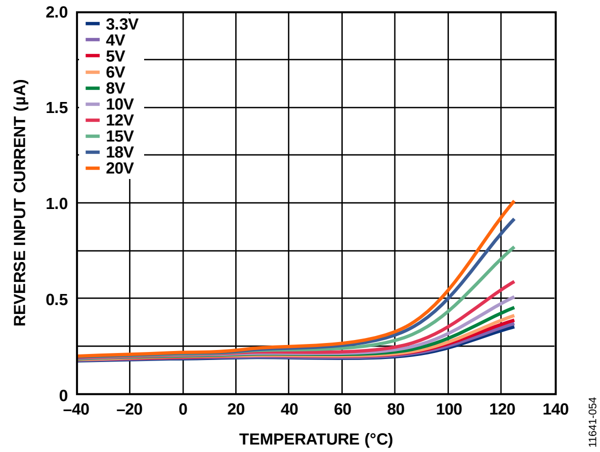

Figure 32. Reverse Input Current vs. Temperature, V_{IN} = 0 V, Different Voltages on V_{OUT}

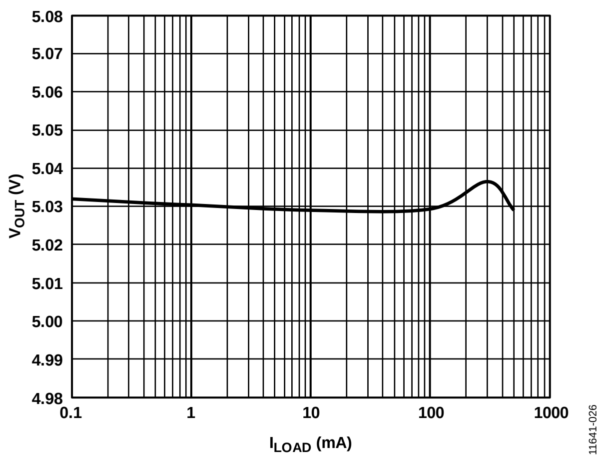

Figure 30. Output Voltage vs. Load Current, V_{OUT} = 5 V, Adjustable

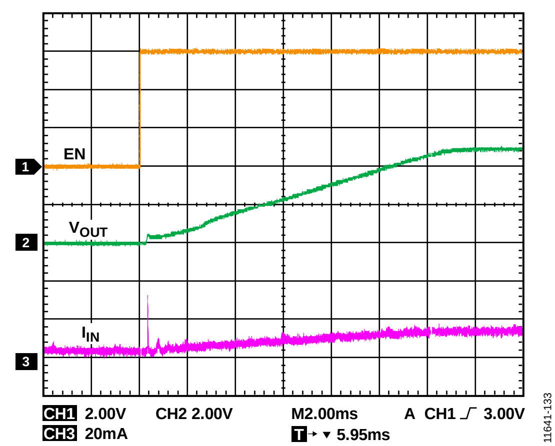

Figure 33. Start-Up Time, V_{EN} and V_{IN} = 6 V, C_{IN} and C_{OUT} = 1 µF, C_{SS} = 10 nF, I_{OUT} = 10 mA, V_{OUT} = 5 V

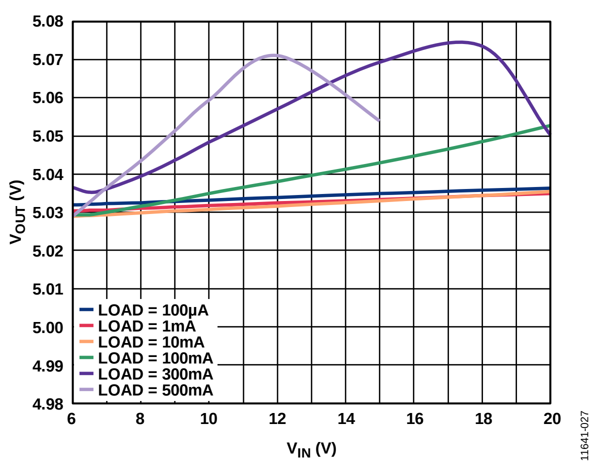

Figure 31. Output Voltage vs. Input Voltage, V_{OUT} = 5 V, Adjustable

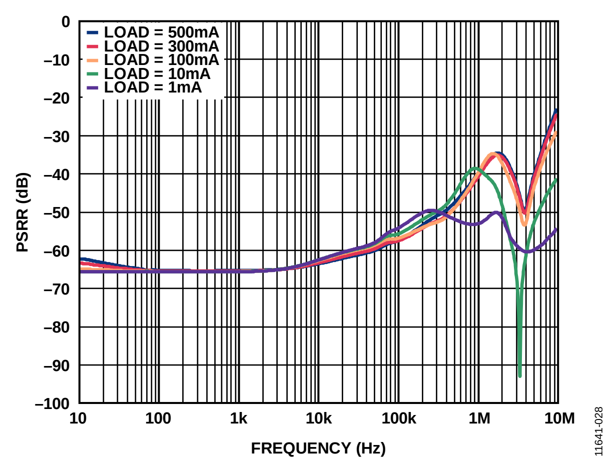

Figure 34. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 1.8 V, V_{IN} = 3.3 V

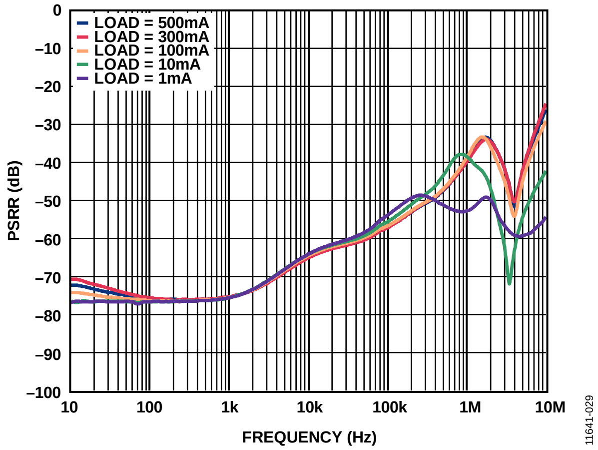

Figure 35. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 3.3 V, V_{IN} = 4.8 V

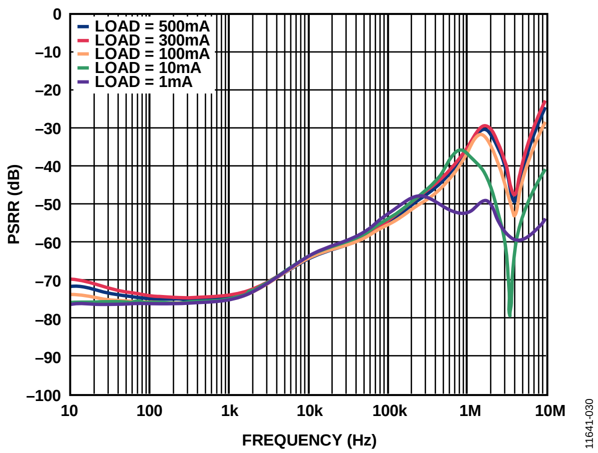

Figure 36. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 3.3 V, V_{IN} = 4.3 V

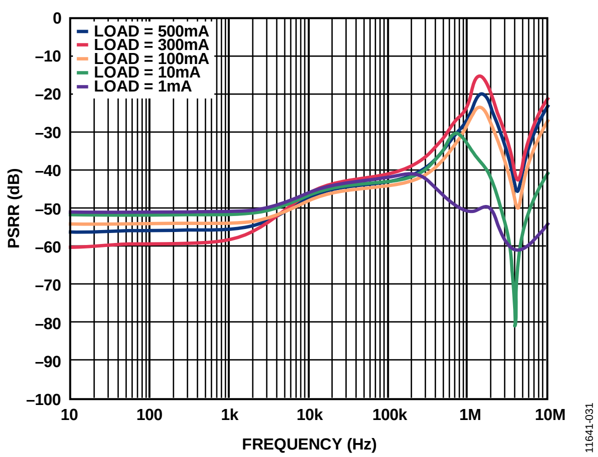

Figure 37. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 3.3 V, V_{IN} = 3.8 V

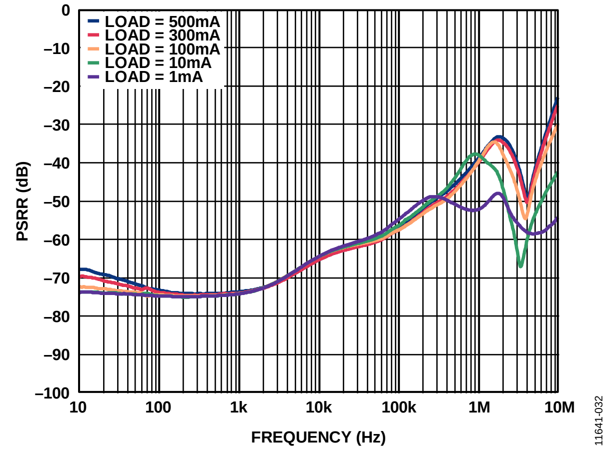

Figure 38. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 5 V, V_{IN} = 6.5 V

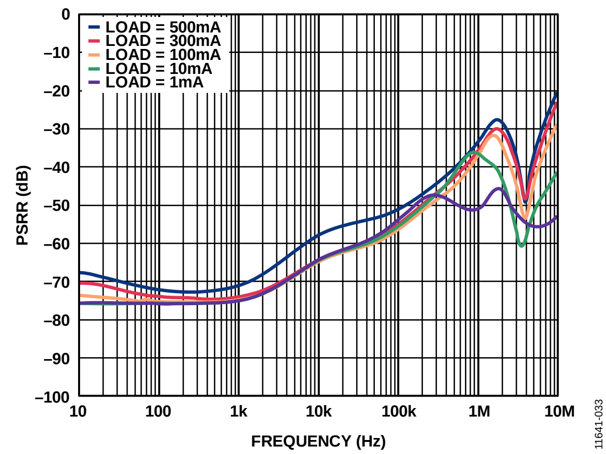

Figure 39. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 5 V, V_{IN} = 6 V

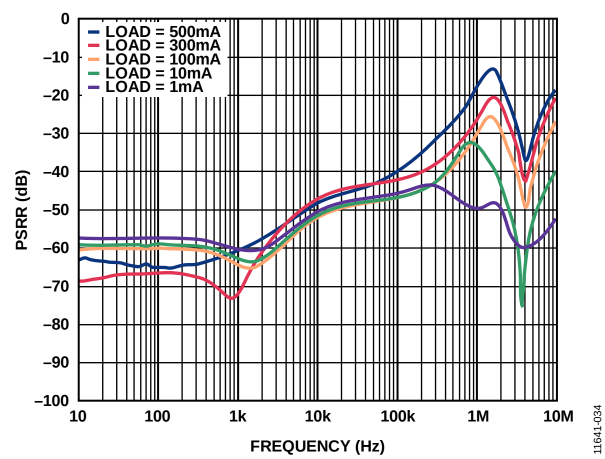

Figure 40. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 5 V, V_{IN} = 5.5 V

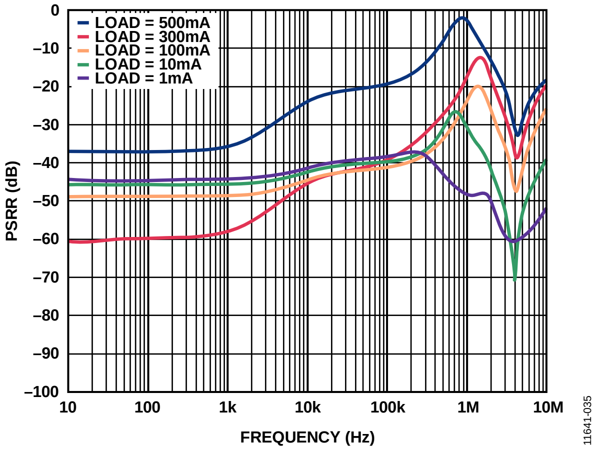

Figure 41. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 5 V, V_{IN} = 5.3 V

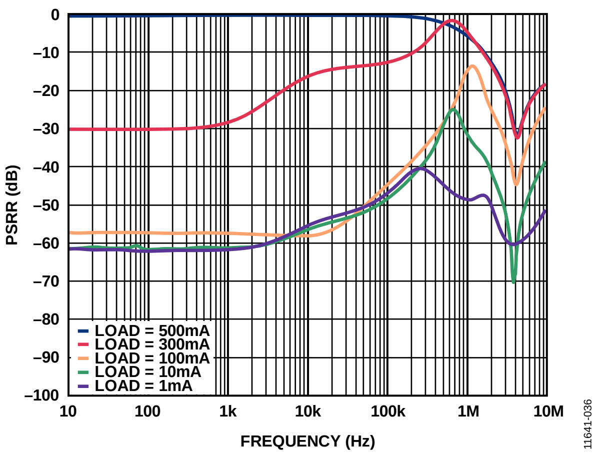

Figure 42. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 5 V, V_{IN} = 5.2 V

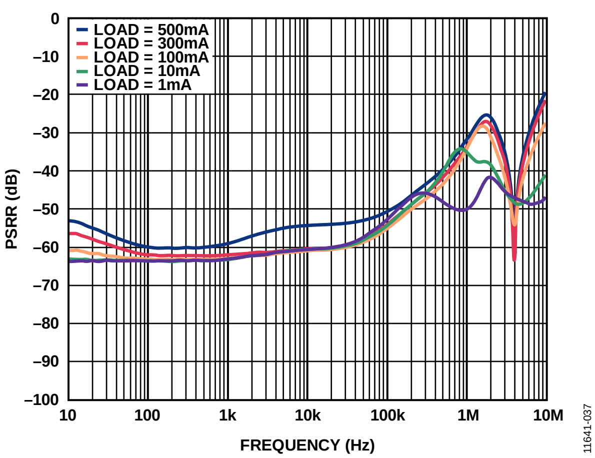

Figure 43. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 5 V, V_{IN} = 6 V, Adjustable

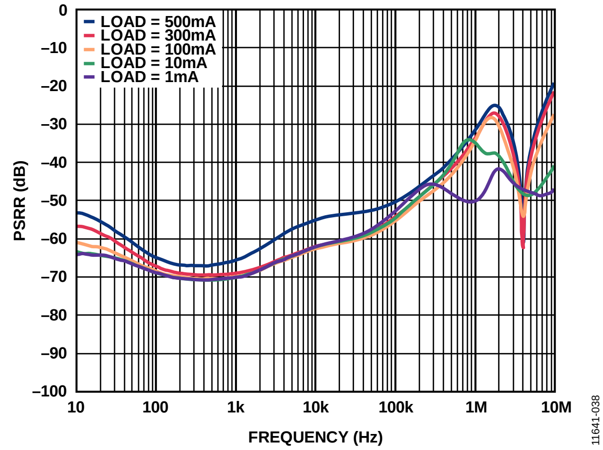

Figure 44. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 5 V, V_{IN} = 6 V, Adjustable with Noise Reduction Circuit

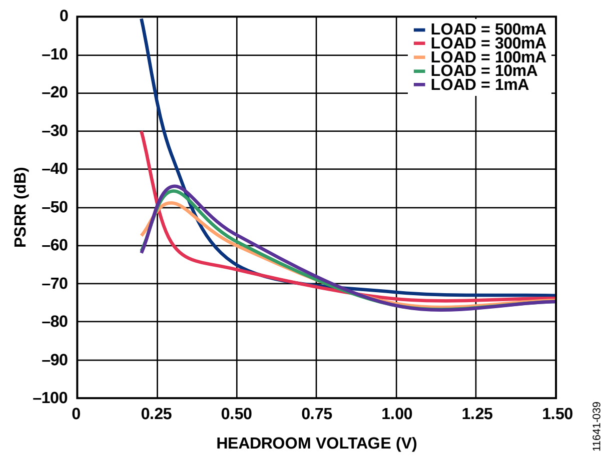

Figure 45. Power Supply Rejection Ratio vs. Headroom Voltage, 100 Hz, V_{OUT} = 5 V

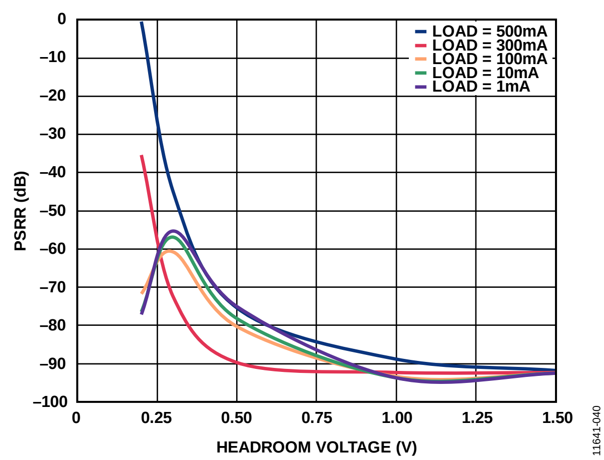

Figure 46. Power Supply Rejection Ratio vs. Headroom Voltage, 1 kHz, V_{OUT} = 5 V

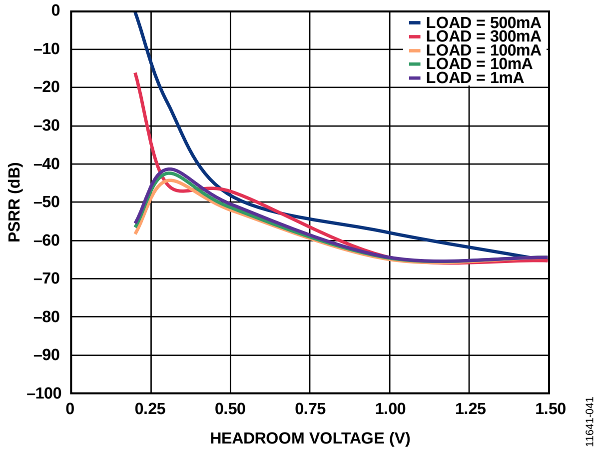

Figure 47. Power Supply Rejection Ratio vs. Headroom Voltage, 10 kHz, $V_{OUT} = 5$ V

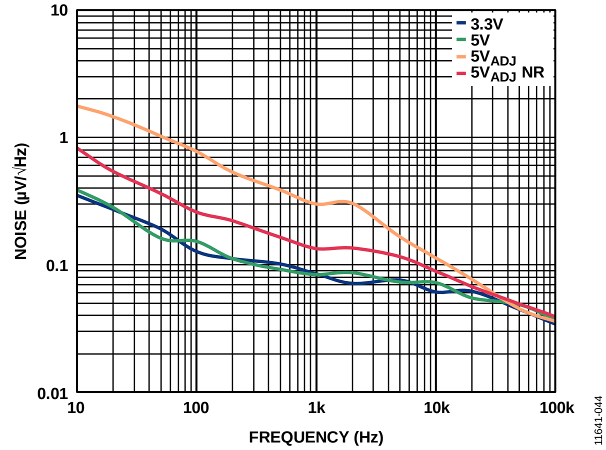

Figure 50. Output Noise Spectral Density, $I_{LOAD} = 10$ mA, $C_{OUT} = 1$ µF

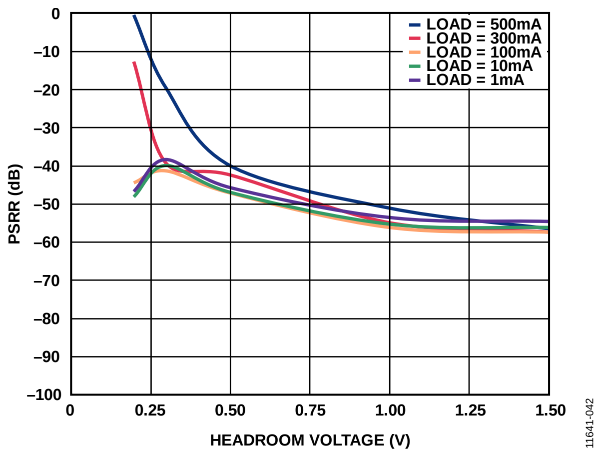

Figure 48. Power Supply Rejection Ratio vs. Headroom Voltage, 100 kHz, $V_{OUT} = 5$ V

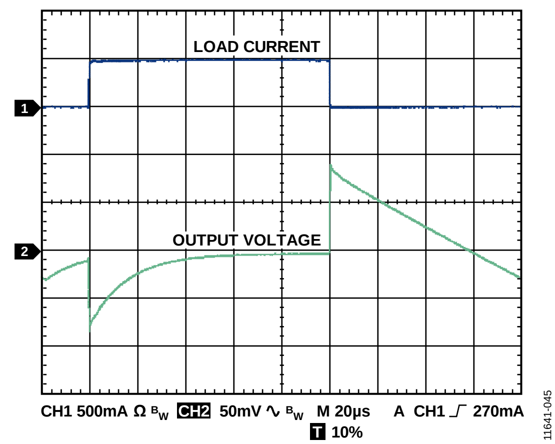

Figure 51. Load Transient Response, $C_{IN} = C_{OUT} = 1$ µF, $I_{LOAD} = 1$ mA to 500 mA, $V_{OUT} = 1.8$ V, $V_{IN} = 5$ V

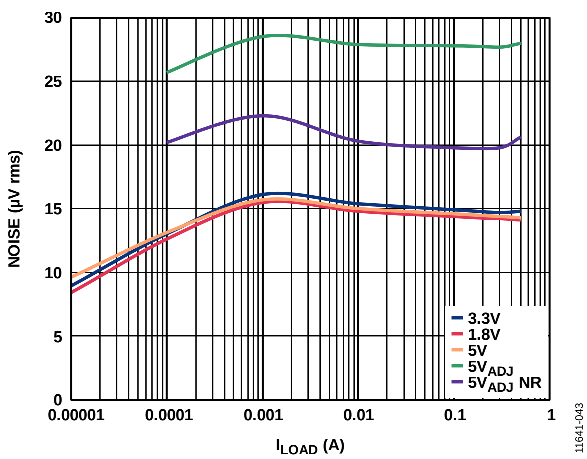

Figure 49. Output Noise vs. Load Current and Output Voltage, $C_{OUT} = 1$ µF

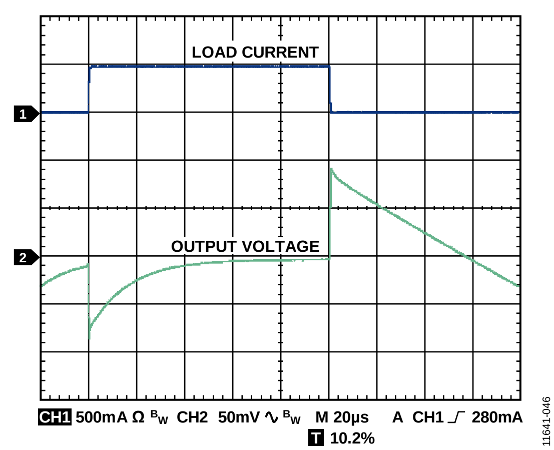

Figure 52. Load Transient Response, $C_{IN} = C_{OUT} = 1$ µF, $I_{LOAD} = 1$ mA to 500 mA, $V_{OUT} = 3.3$ V, $V_{IN} = 5$ V

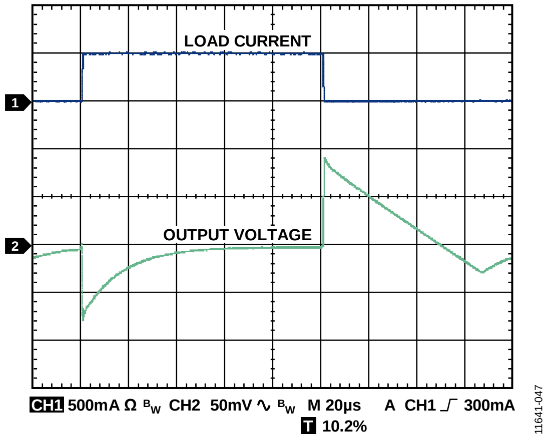

Figure 53. Load Transient Response, $C_{IN} = C_{OUT} = 1\ \mu F$, $I_{LOAD} = 1\ mA$ to 500 mA, $V_{OUT} = 5\ V$, $V_{IN} = 7\ V$

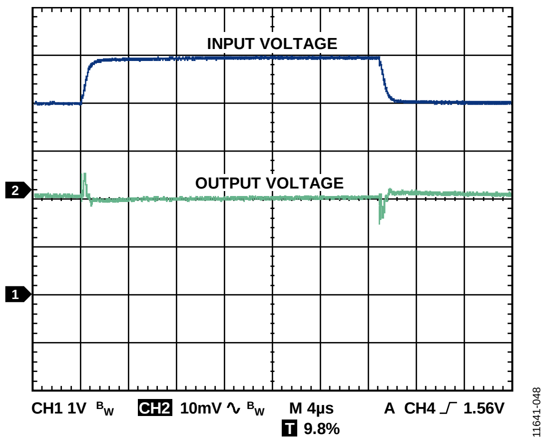

Figure 54. Line Transient Response, $C_{IN} = C_{OUT} = 1\ \mu F$, $I_{LOAD} = 500\ mA$, $V_{OUT} = 1.8\ V$

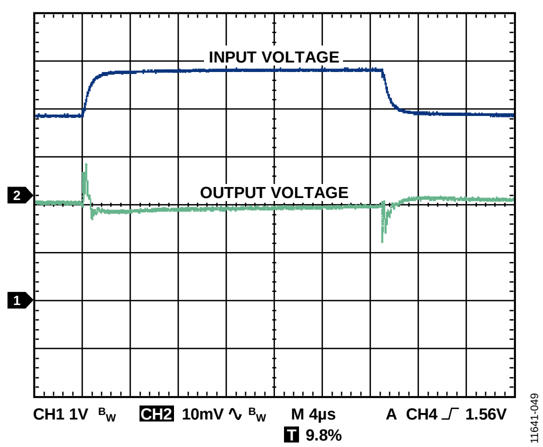

Figure 55. Line Transient Response, $C_{IN} = C_{OUT} = 1\ \mu F$, $I_{LOAD} = 500\ mA$, $V_{OUT} = 3.3\ V$

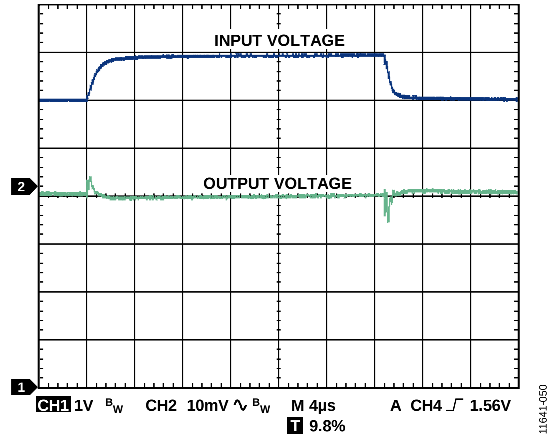

Figure 56. Line Transient Response, $C_{IN} = C_{OUT} = 1\ \mu F$, $I_{LOAD} = 500\ mA$, $V_{OUT} = 5\ V$

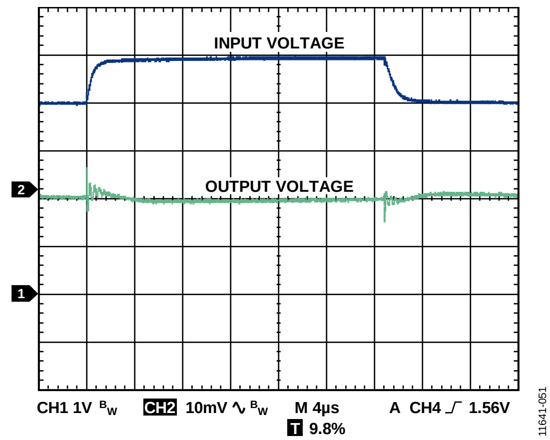

Figure 57. Line Transient Response, $C_{IN} = C_{OUT} = 1\ \mu F$, $I_{LOAD} = 1\ mA$, $V_{OUT} = 1.8\ V$

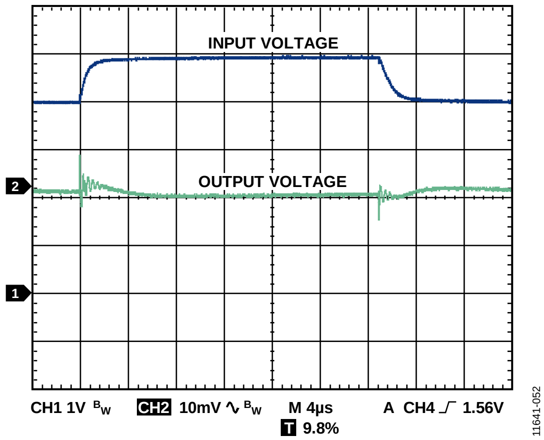

Figure 58. Line Transient Response, $C_{IN} = C_{OUT} = 1\ \mu F$, $I_{LOAD} = 1\ mA$, $V_{OUT} = 3.3\ V$

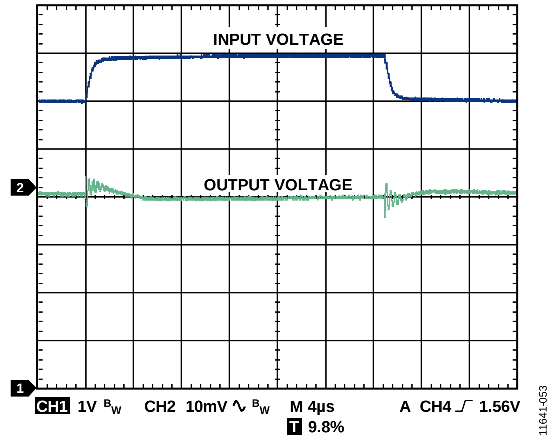

Figure 59. Line Transient Response, $C_{IN} = C_{OUT} = 1\ \mu F$, $I_{LOAD} = 1\ mA$, $V_{OUT} = 5\ V$

THEORY OF OPERATION

The ADP7105 is a low quiescent current, LDO linear regulator that operates from 3.3 V to 20 V and provides up to 500 mA of output current. The ADP7105 draws a low 900 µA of quiescent current (typical) at full load, making it ideal for battery-operated portable equipment. Typical shutdown current consumption is 40 µA at room temperature.

Optimized for use with small 1 µF ceramic capacitors, the ADP7105 provides excellent transient performance.

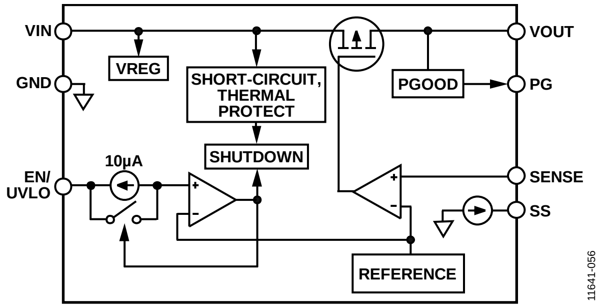

Figure 60. Fixed Output Voltage Internal Block Diagram

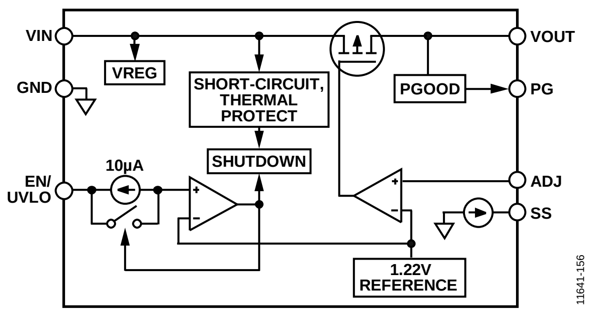

Figure 61. Adjustable Output Voltage Internal Block Diagram

Internally, the ADP7105 consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The ADP7105 is available in three fixed output voltage options, 1.8 V, 3.3 V, and 5 V, and in an adjustable version with an output voltage that can be set from 1.22 V to 19 V by an external voltage divider. The output voltage can be set according to the following equation:

$$V_{OUT} = 1.22\ \text{V}(1 + R1/R2)$$

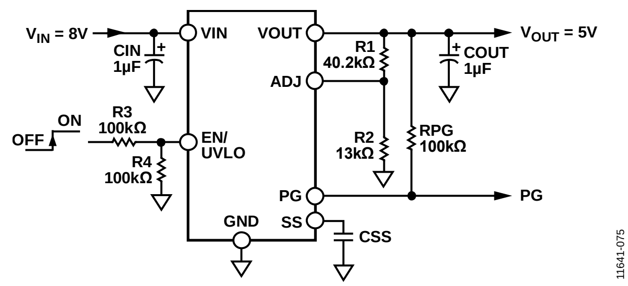

Figure 62. Typical Adjustable Output Voltage Application Schematic

Ensure that the value of R2 is less than 200 kΩ to minimize errors in the output voltage caused by the ADJ input current. For example, when R1 and R2 each equal 200 kΩ, the output voltage is 2.46 V. The output voltage error introduced by the ADJ input current is 2 mV or 0.08%, assuming a typical ADJ input current of 10 nA at 25°C.

The ADP7105 uses the EN/UVLO pin to enable and disable the VOUT pin under normal operating conditions. When EN/UVLO is high, VOUT turns on; when EN/UVLO is low, VOUT turns off. For automatic startup, EN/UVLO can be tied to VIN.

The ADP7105 incorporates reverse current protection circuitry that prevents current flow backwards through the pass element when the output voltage is greater than the input voltage. A comparator senses the difference between the input and output voltages. When the difference between the input voltage and output voltage exceeds 55 mV, the body of the PFET is switched to V_{OUT} and turned off or opened. In other words, the gate is connected to VOUT.

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP7105 is designed for operation with small, space-saving ceramic capacitors but functions with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 1 μF capacitance with an ESR of 1 Ω or less is recommended to ensure the stability of the ADP7105. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP7105 to large changes in load current. Figure 63 shows the transient responses for an output capacitance value of 1 μF.

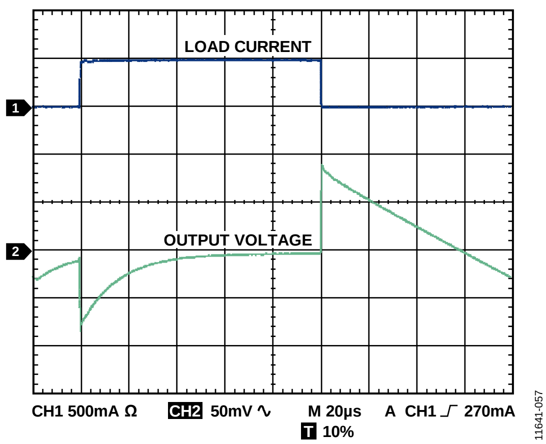

Figure 63. Output Transient Response, V_{OUT} = 1.8 V, C_{OUT} = 1 μF

Input Bypass Capacitor

Connecting a 1 μF capacitor from VIN to GND reduces the circuit sensitivity to PCB layout, especially when long input traces or high source impedance is encountered. If greater than 1 μF of output capacitance is required, increase the input capacitor to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP7105, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V to 25 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 64 shows the capacitance vs. voltage bias characteristic of an 0402, 1 μF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is ~±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

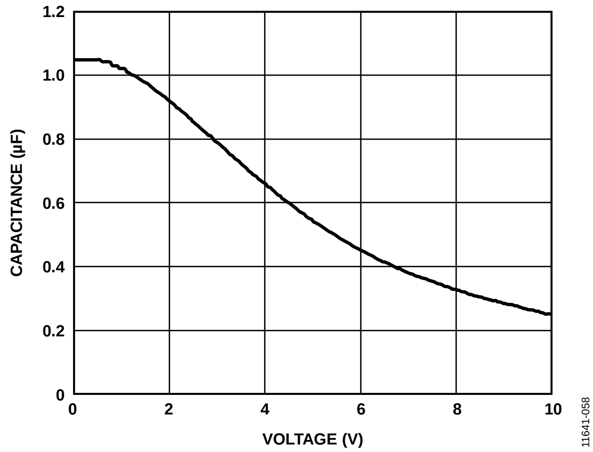

Figure 64. Capacitance vs. Voltage Bias Characteristic

Use Equation 1 to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 0.94 μF at 1.8 V, as shown in Figure 64.

Substituting these values in Equation 1 yields

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO regulator overtemperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP7105, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

PROGRAMMABLE UNDERVOLTAGE LOCKOUT (UVLO)

The ADP7105 uses the EN/UVLO pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 65, when a rising voltage on EN/UVLO crosses the upper threshold, VOUT turns on. When a falling voltage on EN/UVLO crosses the lower threshold, VOUT turns off. The hysteresis of the EN/UVLO threshold is determined by the Thevenin equivalent resistance in series with the EN/UVLO pin.

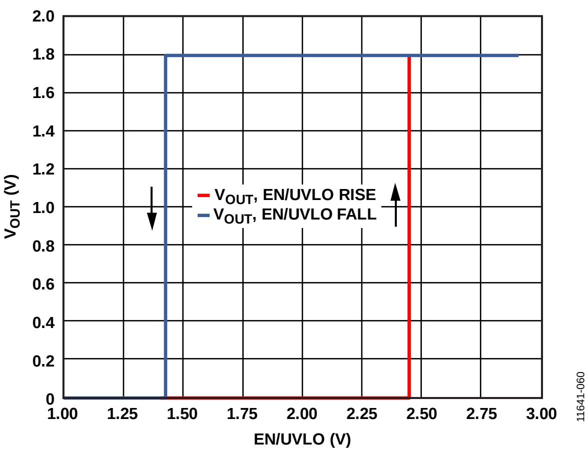

Figure 65. Typical VOUT Response to EN/UVLO Pin Operation

The upper and lower thresholds are user programmable and can be set using two resistors. When the EN/UVLO pin voltage is below 1.23 V, the LDO is disabled. When the EN/UVLO pin voltage transitions above 1.23 V, the LDO is enabled and 10 μA hysteresis current is sourced out of the pin, raising the voltage and thus providing threshold hysteresis. Typically, two external resistors program the minimum operational voltage for the LDO. The resistance values, R1 and R2, can be determined from the following:

$$R1 = V_{HYS}/10\ \mu A$$

$$R2 = 1.23\ V \times R1/(V_{IN} - 1.23\ V)$$

where:

V_{HYS} is the desired EN/UVLO hysteresis level.
V_{IN} is the desired turn-on voltage.

Hysteresis can also be achieved by connecting a resistor in series with the EN/UVLO pin. For the example shown in Figure 66, the enable threshold is 2.46 V with a hysteresis of 1 V.

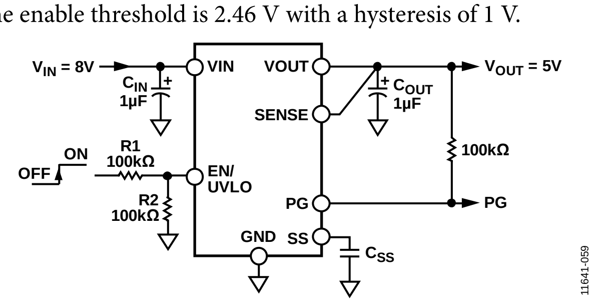

Figure 66. Typical EN/UVLO Pin Voltage Divider

Figure 65 shows the typical hysteresis of the EN/UVLO pin. This prevents on/off oscillations that can occur due to noise on the EN/UVLO pin as it passes through the threshold points.

SOFT START FUNCTION

For applications that require a controlled startup, the ADP7105 provides a programmable soft start function. Programmable soft start is useful for reducing inrush current upon startup and for providing voltage sequencing. To implement soft start, connect a small ceramic capacitor from SS to GND. Upon startup, a 1 μA current source charges this capacitor. The ADP7105 start-up output voltage is limited by the voltage at SS, providing a smooth ramp-up to the nominal output voltage. The soft start time is calculated by

$$t_{SS} = V_{REF} \times (C_{SS}/I_{SS})$$

where:

t_{SS} is the soft start delay.
V_{REF} is the 1.22 V reference voltage.
C_{SS} is the soft start capacitance between SS and GND.
I_{SS} is the current sourced from SS (1 μA).

When the ADP7105 is disabled (by driving EN low), the soft start capacitor is discharged to GND through an internal 5 kΩ resistor.

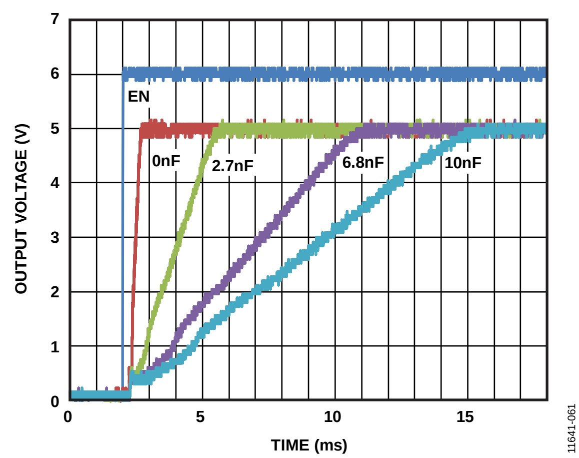

Figure 67. Typical Start-Up Behavior

POWER-GOOD FEATURE

The ADP7105 provides a power-good pin (PG) to indicate the status of the output. This open-drain output requires an external pull-up resistor to VIN or VOUT. If the part is in shutdown mode, current-limit mode, or thermal shutdown, or if V_{OUT} falls below 90% of the nominal output voltage, the power-good pin (PG) immediately transitions low. During soft start, the rising threshold of the power-good signal is 93.5% of the nominal output voltage.

The open-drain output is held low when the ADP7105 has sufficient input voltage to turn on the internal PG transistor. The PG transistor is terminated via a pull-up resistor to VOUT or VIN.

Power-good accuracy is 93.5% of the nominal regulator output voltage when this voltage is rising, with a 90.8% trip point when this voltage is falling. Regulator input voltage brownouts or glitches trigger power no good signals if V_{OUT} falls below 90.8% of the nominal output voltage.

A normal power-down causes the power-good signal to go low when V_{OUT} falls below 90.8%.

Figure 68 and Figure 69 show the typical power-good rising and falling thresholds over temperature.

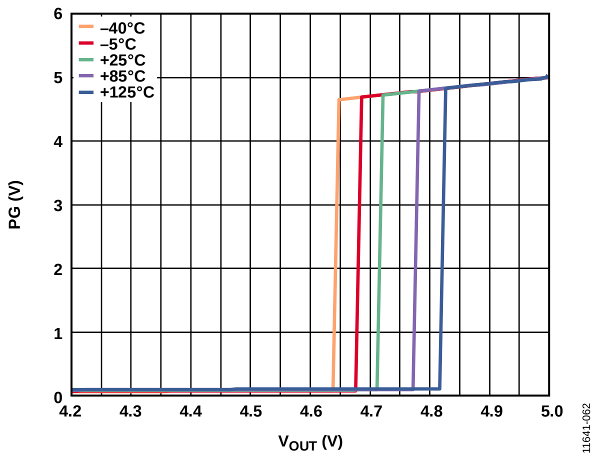

Figure 68. Typical Power-Good Threshold vs. Output Voltage and Temperature, V_{OUT} Rising

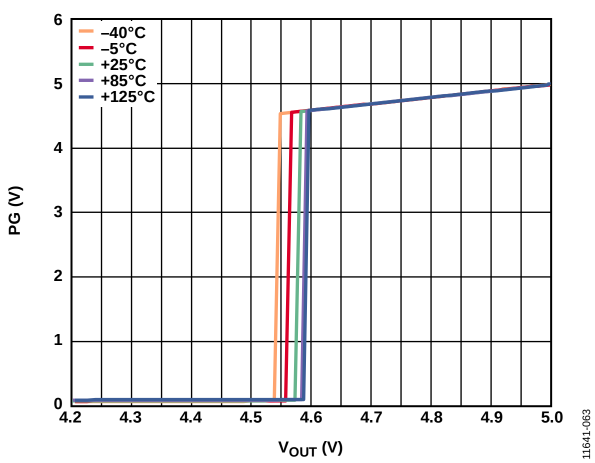

Figure 69. Typical Power-Good Threshold vs. Output Voltage and Temperature, V_{OUT} Falling

NOISE REDUCTION OF THE ADJUSTABLE ADP7105

The ultralow output noise of the fixed output ADP7105 is achieved by keeping the LDO error amplifier in unity gain and setting the reference voltage equal to the output voltage. This architecture does not apply to the adjustable output voltage LDO regulator. The adjustable output ADP7105 uses the more conventional architecture where the reference voltage is fixed and the error amplifier gain is a function of the output voltage. The disadvantage of the conventional LDO architecture is that the output voltage noise is proportional to the output voltage.

The adjustable LDO circuit can be modified slightly to reduce the output voltage noise to levels close to that of the fixed output ADP7105. The circuit shown in Figure 70 adds two additional components to the output voltage setting resistor divider. C_{NR} and R_{NR} are added in parallel with R_{FB1} to reduce the ac gain of the error amplifier. R_{NR} is chosen to be equal to R_{FB2}. This limits the ac gain of the error amplifier to approximately 6 dB. The actual gain is the parallel combination of R_{NR} and R_{FB1} divided by R_{FB2}. This ensures that the error amplifier always operates at greater than unity gain.

C_{NR} is chosen by setting the reactance of C_{NR} equal to $R_{FB1} - R_{NR}$ at a frequency between 50 Hz and 100 Hz. This capacitor value sets the frequency so that the ac gain of the error amplifier is 3 dB less than its dc gain.

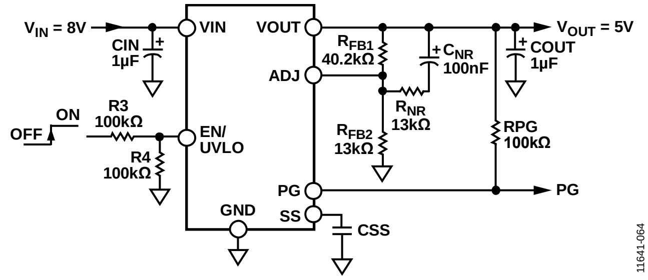

Figure 70. Noise Reduction Modification to Adjustable LDO Regulator

The noise of the adjustable LDO regulator can be found by using the following formula, assuming the noise of a fixed output LDO is approximately 15 µV:

$$15\,\mu\text{V} \times \sqrt{1 + \left(\left(\frac{1}{1/13\,\text{k}\Omega + 1/40.2\,\text{k}\Omega}\right)/13\,\text{k}\Omega\right)}$$

Based on the component values shown in Figure 70, the ADP7105 has the following characteristics:

- DC gain of 4.09 (12.2 dB)
- 3 dB roll-off frequency of 59 Hz
- High frequency ac gain of 1.76 (4.89 dB)
- Noise reduction factor of 1.33 (2.59 dB)
- RMS noise of the ADP7105 adjustable LDO without noise reduction of 27.8 µV rms
- RMS noise of the ADP7105 adjustable LDO with noise reduction (assuming 15 µV rms for fixed voltage option) of 19.95 µV rms

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP7105 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP7105 is designed to limit the current when the output load reaches 775 mA (typical). When the output load exceeds 775 mA, the output voltage is reduced to maintain a constant current limit. As the output voltage drops, the current is folded back to approximately 50 mA to minimize heat generation inside the LDO regulator.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and/or high power dissipation) when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature falls below 135°C, the output is turned on again, and output current is restored to its operating value.

Consider the case where a hard short from VOUT to ground occurs. At first, the ADP7105 limits the current so that only 775 mA is conducted into the short. If self heating of the junction is great enough to cause its temperature to rise above 150°C, thermal shutdown is activated, turning off the output and reducing the output current to zero. As the junction temperature cools and falls below 135°C, the output turns on and conducts 775 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 775 mA and 0 mA that continues as long as the short remains at the output.

Current-limit and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that the junction temperature does not exceed 125°C.

THERMAL CONSIDERATIONS

In applications with a low input-to-output voltage differential, the ADP7105 does not dissipate much heat. However, in applications with high ambient temperature and/or high input voltage, the heat dissipated in the package may become significant enough that it causes the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 150°C, the regulator enters thermal shutdown. It recovers only after the junction temperature decreases below 135°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADP7105 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} value is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pins to the PCB.

Table 6 shows typical θ_{JA} values for the 8-lead SOIC and 8-lead LFCSP packages for various PCB copper sizes. Table 7 shows the typical Ψ_{JB} values for the 8-lead SOIC and 8-lead LFCSP with PCB area.

Table 6. Typical θ_{JA} Values

	θ_{JA} (°C/W)	
Copper Size (mm²)	**LFCSP**	**SOIC**
25[1]	165.1	167.8
100	125.8	111
500	68.1	65.9
1000	56.4	56.1
6400	42.1	45.8

[1] Device soldered to minimum size pin traces.

Table 7. Typical Ψ_{JB} Values with PCB Area

Model	Ψ_{JB} (°C/W)
8-Lead LFCSP[1]	15.1
8-Lead SOIC	31.3

[1] Note that the Ψ_{JB} value for the LFCSP package accounts for PCB area, which is being used as a heat sink via the exposed pad, whereas the value in Table 4 is per the JEDEC standard.

The junction temperature of the ADP7105 is calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
θ_{JA} *is* the junction-to-ambient thermal resistance.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (3)$$

where:
V_{IN} and V_{OUT} are the input and output voltages, respectively.
I_{LOAD} is the load current.
I_{GND} is the ground current.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input-to-output voltage differential, and continuous load current, a minimum copper size requirement for the PCB exists to ensure that the junction temperature does not rise above 125°C. Figure 71 to Figure 76 show junction temperature calculations for different ambient temperatures, power dissipation, and areas of PCB copper.

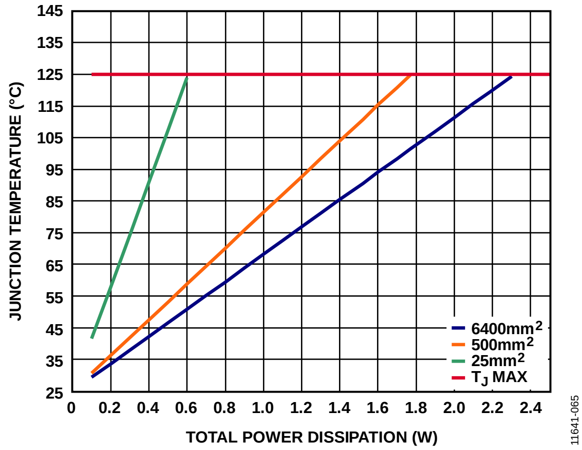

Figure 71. LFCSP, T_A = 25°C

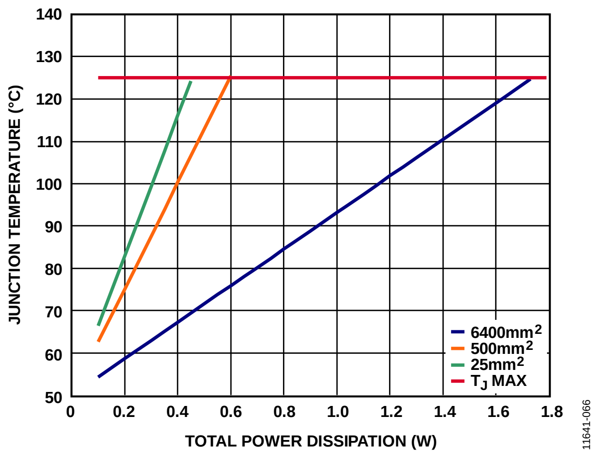

Figure 72. LFCSP, T_A = 50°C

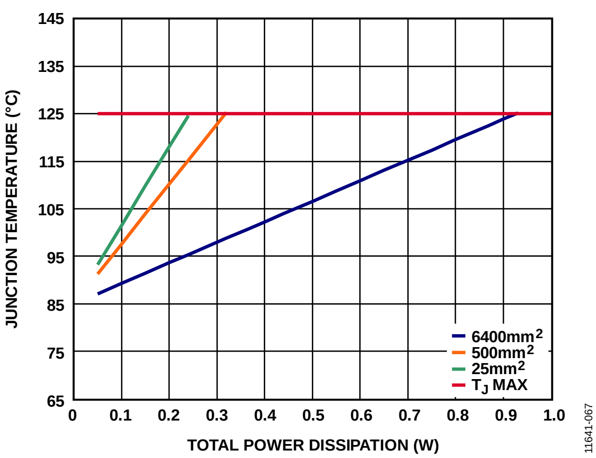

Figure 73. LFCSP, T_A = 85°C

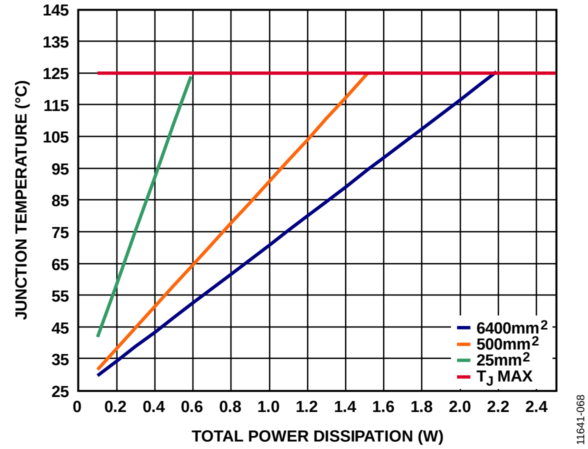

Figure 74. SOIC, T_A = 25°C

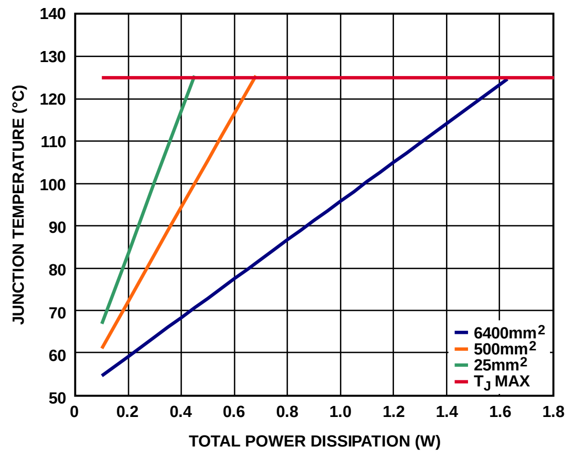

Figure 75. SOIC, T_A = 50°C

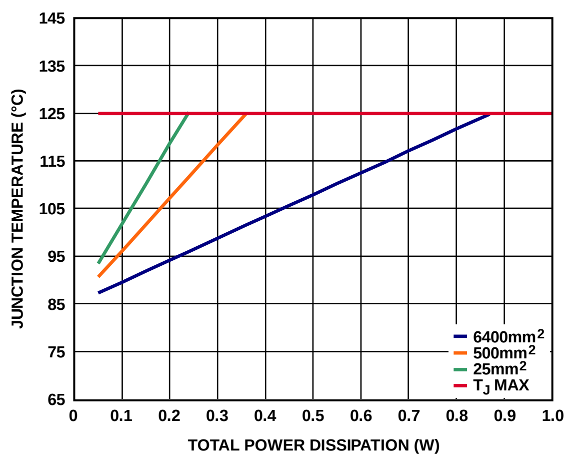

Figure 76. SOIC, T_A = 85°C

In the case where the board temperature is known, use the Ψ_{JB} thermal characterization parameter to estimate the junction temperature rise (see Figure 77 and Figure 78). Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

The typical value of Ψ_{JB} is 15.1°C/W for the 8-lead LFCSP package and 31.3°C/W for the 8-lead SOIC package (see Table 7).

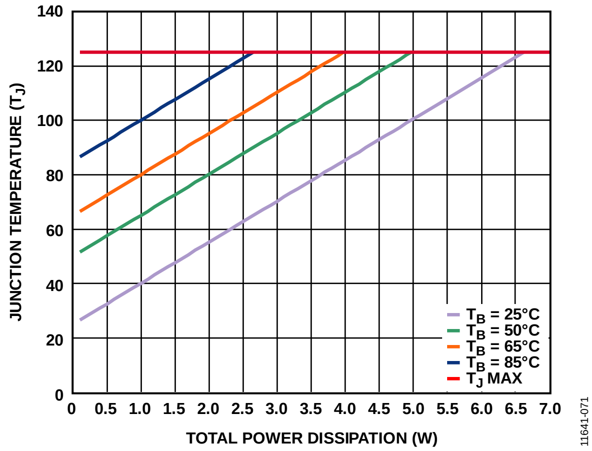

Figure 77. LFCSP

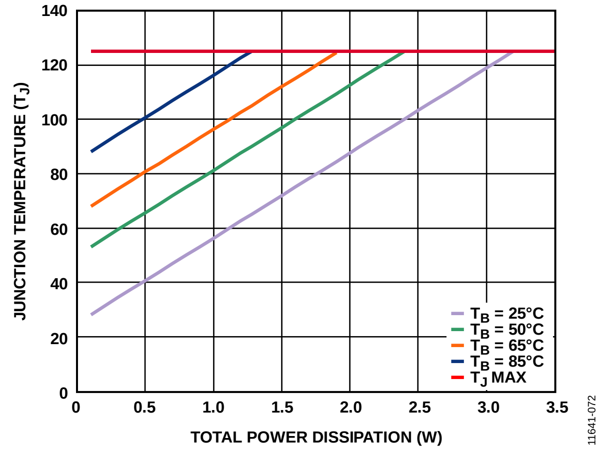

Figure 78. SOIC

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP7105. However, as shown in Table 6, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Use of 0805 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where space is limited.

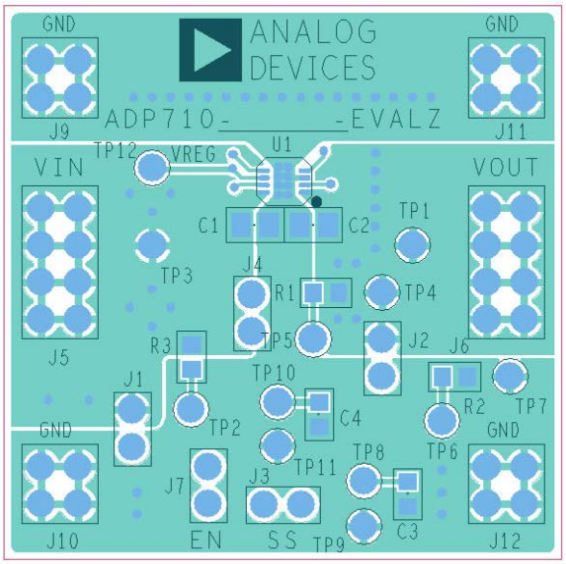

Figure 79. Example LFCSP PCB Layout

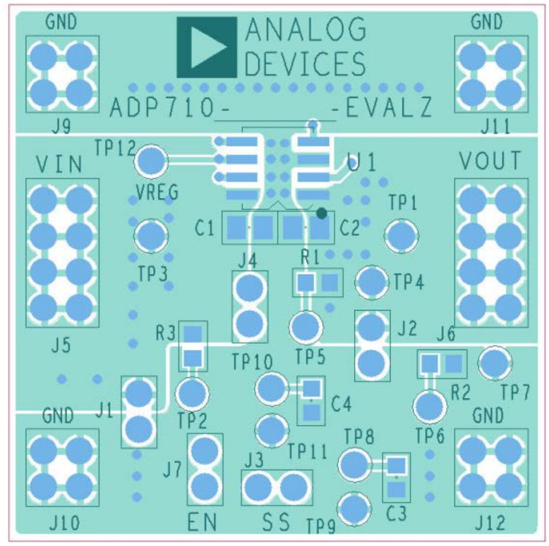

Figure 80. Example SOIC PCB Layout

OUTLINE DIMENSIONS

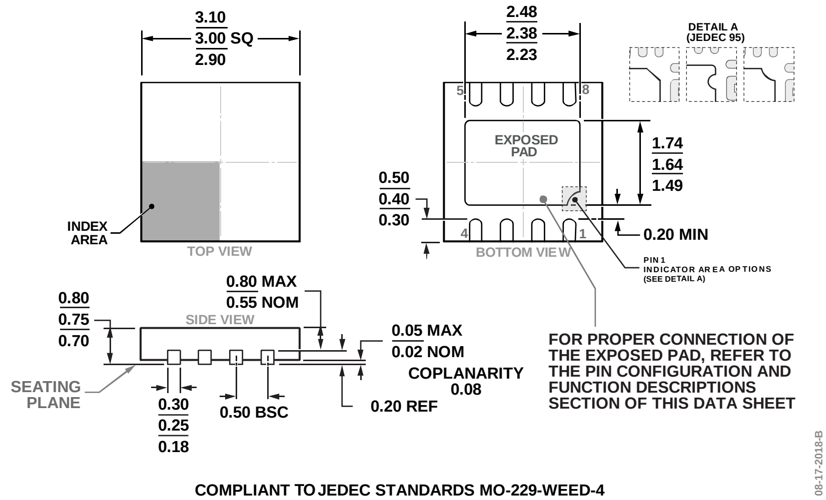

Figure 81. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-5)
Dimensions shown in millimeters

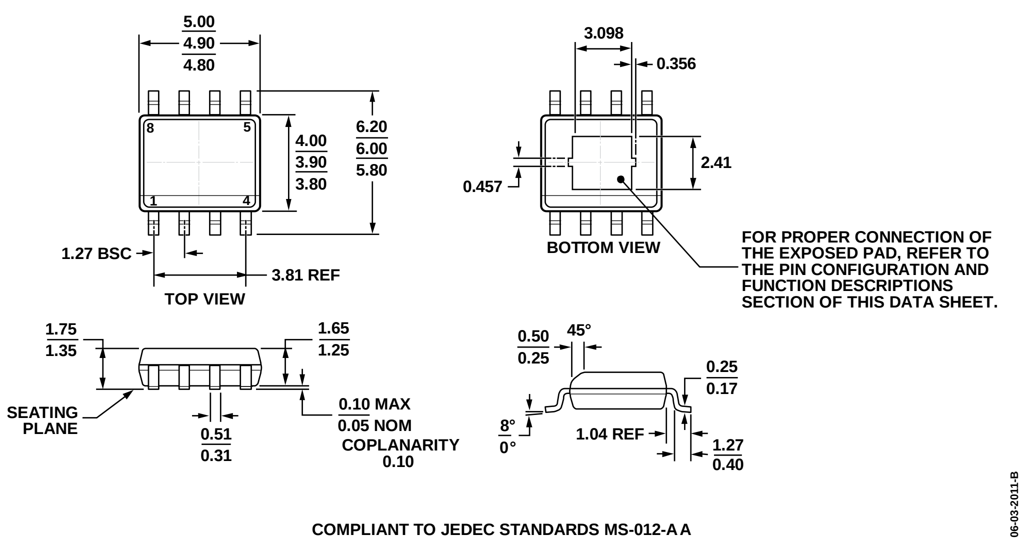

Figure 82. 8-Lead Standard Small Outline Package, with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-2)
Dimensions shown in millimeters