Photometric Front Ends

Data Sheet

ADPD1080/ADPD1081

FEATURES

- Multifunction photometric front end
- Fully integrated AFE, ADC, LED drivers, and timing core
- Enables ambient light rejection capability without the need for photodiode optical filters
- Three 370 mA LED peak current drivers
- Flexible, multiple, short LED pulses per optical sample
- 20-bit burst accumulator enabling 20 bits per sample period
- On-board sample to sample accumulator, enabling up to 27 bits per data read
- Low power operation
- SPI, I^2C interface, and 1.8 V analog/digital core
- Flexible sampling frequency ranging from 0.122 Hz to 2700 Hz
- FIFO data operation
- Qualified for automotive applications

APPLICATIONS

- Wearable health and fitness monitors
- Clinical measurements, for example, SpO_2
- Industrial monitoring
- Background light measurements

GENERAL DESCRIPTION

The ADPD1080/ADPD1081 are highly efficient, photometric front ends, each with an integrated 14-bit analog-to-digital converter (ADC) and a 20-bit burst accumulator that works with flexible light emitting diode (LED) drivers. The ADPD1080/ADPD1081 stimulate an LED and measures the corresponding optical return signal. The data output and functional configuration occur over a 1.8 V I^2C interface on the ADPD1080 or a serial port interface (SPI) on the ADPD1081. The control circuitry includes flexible LED signaling and synchronous detection.

The analog front end (AFE) features rejection of signal offset and corruption due to modulated interference commonly caused by ambient light without the need for optical filters or dc cancellation circuitry that requires external control.

Couple the ADPD1080/ADPD1081 with a low capacitance photodiode of <100 pF for optimal performance. The ADPD1080/ADPD1081 can be used with any LED. The ADPD1080 is available in a 16-ball, 2.46 mm × 1.4 mm WLCSP and a 28-lead, 4 mm × 4 mm LFCSP. The SPI only version, ADPD1081, is available in a 17-ball, 2.46 mm × 1.4 mm WLCSP.

Rev. C

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10/2018—Rev. A to Rev. B

Changed T_A = Full Operating Temperature Range to T_A = 25°C ..... Throughout
Changes to Features Section 1
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Deleted Input Capacitance Parameter, Table 4 8
Changes to Digital Specifications Section 10
Changes to Timing Specifications Section 11
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Added Improving SNR Using Integrator Chopping Section, Figure 46, and Table 25; Renumbered Sequentially 40
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Added Automotive Products Section 74

7/2018—Rev. 0 to Rev. A

Added ADPD1081 ..... Universal
Added 28-Lead LFCSP (CP-28-5), ADPD1080 ..... Universal
Added 17-Ball WLCSP (CB-17-1), ADPD1081 ..... Universal
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Added Figure 2; Renumbered Sequentially 5
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Added SPI Timing Specifications Section, Table 7; Renumbered Sequentially, SPI Timing Diagram Section, and Figure 4 12
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1/2018—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAMS

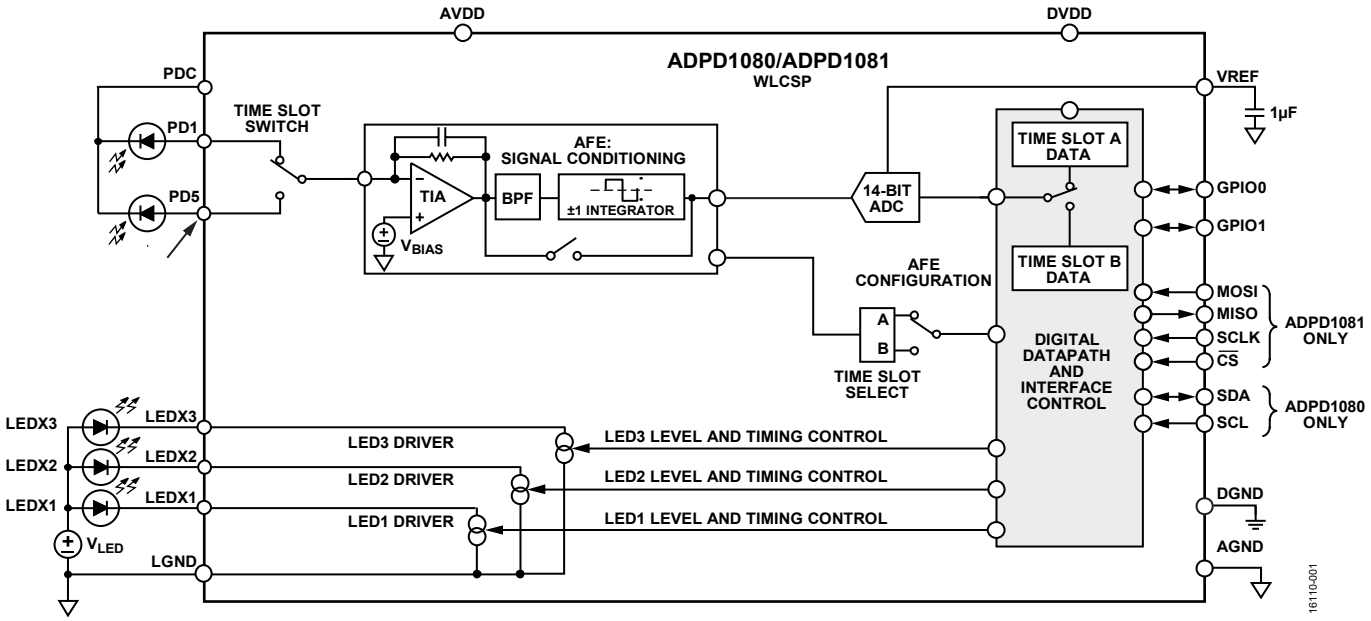

Figure 1. Block Diagram for ADPD1080/ADPD1081 WLCSP (Chip Scale Package) Versions

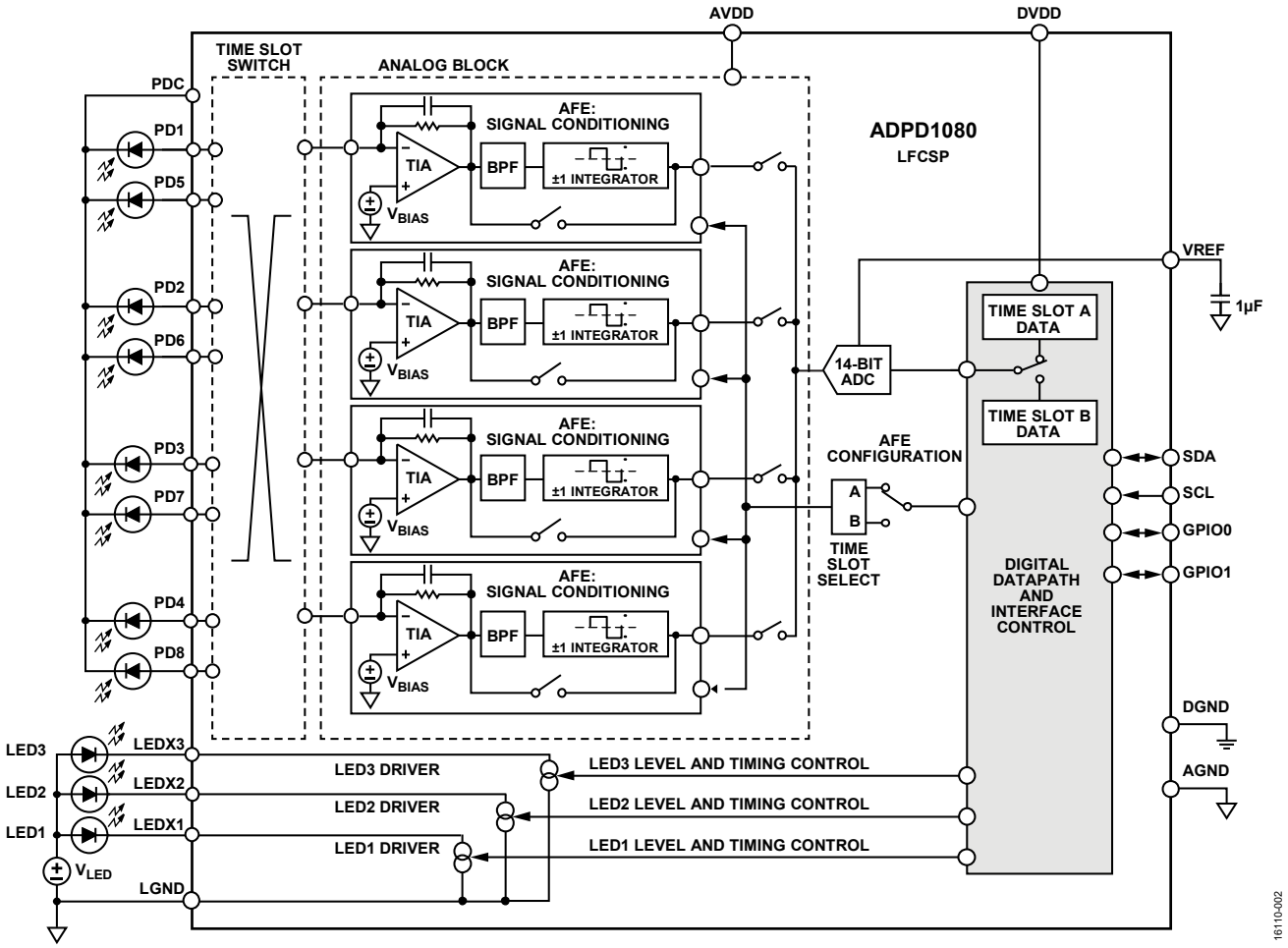

Figure 2. Block Diagram for ADPD1080 LFCSP Version

SPECIFICATIONS

TEMPERATURE AND POWER SPECIFICATIONS

Operating Conditions

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE					
Operating Range		−40		+85	°C
ADPD1080WBCPZR7	Automotive grade only	−40		+105	°C
Storage Range		−65		+150	°C
POWER SUPPLY VOLTAGE					
V_{DD}	Applied at the AVDD, DVDD, and VDD pins	1.7	1.8	1.9	V

Current Consumption

AVDD = DVDD = 1.8 V, ambient temperature (T_A) = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY (V_{DD}) CURRENT						
V_{DD} Supply Current[1]		SLOTx_LED_OFFSET = 25 µs; LED_PERIOD =13 µs; LED peak current = 25 mA, single-channel mode				
1 Pulse		100 Hz data rate; Time Slot A only		53		µA
		100 Hz data rate; Time Slot B only		41		µA
		100 Hz data rate; both Time Slot A and Time Slot B		76		µA
10 Pulses		100 Hz data rate; Time Slot A only		107		µA
		100 Hz data rate; Time Slot B only		95		µA
		100 Hz data rate; both Time Slot A and Time Slot B		184		µA
Peak V_{DD} Supply Current (1.8 V)	IV_{DD_PEAK}					
4-Channel Operation				9.3		mA
1-Channel Operation				4.5		mA
Standby Mode Current	$IV_{DD\_STANDBY}$			0.3		µA
SYSTEM POWER DISSIPATION[2]		Continuous, single channel, photoplethysmography (PPG) measurement				
Average Power		V_{LED} = 4.0 V, V_{DD} = 1.8 V, signal-to-noise ratio (SNR) = 75 dB, 25 Hz output data rate, 70% full-scale input signal				
		Current transfer ratio (CTR) = 20 nA/mA		258		µW
		CTR = 100 nA/mA		75		µW
POWER SUPPLY REJECTION RATIO (PSRR)		DC PSRR at 75% full-scale input		24		dB

[1] V_{DD} is the voltage applied at the AVDD and DVDD pins.
[2] System power dissipation is the total average power dissipation, including the AFE V_{DD} supply plus the V_{LED} power supply to the LEDs.

PERFORMANCE SPECIFICATIONS

AVDD = DVDD = 1.8 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DATA ACQUISITION					
Resolution	Single pulse		14		Bits
Sample	64 to 255 pulses		20		Bits
Data Read	64 to 255 pulses and sample average = 128		27		Bits
LED DRIVER					
LED Current Slew Rate[1]	T_A = 25°C; I_{LED} = 70 mA				
Rising	Slew rate control setting = 0		240		mA/µs
	Slew rate control setting = 7		1400		mA/µs
Falling	Slew rate control setting = 0, 1, or 2		3200		mA/µs
	Slew rate control setting = 6 or 7		4500		mA/µs
LED Peak Current	LED pulse enabled			370	mA
Driver Compliance Voltage	Voltage above ground required for LED driver operation		0.6		V
LED PERIOD	AFE width = 4 µs[2]		19		µs
	AFE width = 3 µs		17		µs
Sampling Frequency[3]	Time Slot A or Time Slot B; normal mode; 1 pulse; SLOTA_LED_OFFSET = 23 µs; SLOTA_PERIOD = 19 µs	0.122		2000	Hz
	Both time slots; normal mode; 1 pulse; SLOTA_LED_OFFSET = 23 µs; SLOTA_PERIOD = 19 µs	0.122		1600	Hz
	Time Slot A or Time Slot B; normal mode; 8 pulses; SLOTA_LED_OFFSET = 23 µs; SLOTA_PERIOD = 19 µs	0.122		1600	Hz
	Both time slots; normal mode; 8 pulses; SLOTA_LED_OFFSET = 23 µs; SLOTA_PERIOD = 19 µs	0.122		1000	Hz
CATHODE PIN (PDC) VOLTAGE					
During All Sampling Periods	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 1[4]		1.8		V
	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 0		1.3		V
During Time Slot A Sampling	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x0[4]		1.8		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x1		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x2		1.55		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x3[5]		0		V
During Time Slot B Sampling	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x0[4]		1.8		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x1		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x2		1.55		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x3[5]		0		V
During Sleep Periods	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 1		1.8		V
	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 0		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[13:12] = 0x0		1.8		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[13:12] = 0x1		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[13:12] = 0x2		1.55		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[13:12] = 0x3		0		V
PHOTODIODE INPUT PINS/ANODE VOLTAGE					
During All Sampling Periods			1.3		V
During Sleep Periods			Cathode voltage		V

[1] LED inductance is negligible for these values. The effective slew rate slows with increased inductance.
[2] Minimum LED period = (2 × AFE width) + 5 µs.
[3] The maximum values in this specification are the internal ADC sampling rates in normal mode using the internal 32 kHz state machine clock. The I²C read rates in some configurations may limit the output data rate.
[4] This mode can induce additional noise and is not recommended unless necessary. The 1.8 V setting uses V_{DD}, which contains greater amounts of differential voltage noise with respect to the anode voltage.
[5] This setting is not recommended for photodiodes because it causes a 1.3 V forward-bias of the photodiode.

ANALOG SPECIFICATIONS

AVDD = DVDD = 1.8 V, T_A = 25°C, unless otherwise noted. Compensation of the AFE offset is explained in the AFE Operation section.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PULSED SIGNAL CONVERSIONS, 3 µs WIDE LED PULSE[1]	4 µs wide AFE integration; normal operation, Register 0x43 and Register 0x45 = 0xADA5				
ADC Resolution[2]	Transimpedance amplifier (TIA) feedback resistor				
	25 kΩ		3.27		nA/LSB
	50 kΩ		1.64		nA/LSB
	100 kΩ		0.82		nA/LSB
	200 kΩ		0.41		nA/LSB
ADC Saturation Level	TIA feedback resistor				
	25 kΩ		26.8		µA
	50 kΩ		13.4		µA
	100 kΩ		6.7		µA
	200 kΩ		3.35		µA
Ambient Signal Headroom on Pulsed Signal	TIA feedback resistor				
	25 kΩ		23.6		µA
	50 kΩ		11.8		µA
	100 kΩ		5.9		µA
	200 kΩ		2.95		µA
PULSED SIGNAL CONVERSIONS, 2 µs WIDE LED PULSE[1]	3 µs wide AFE integration; normal operation, Register 0x43 and Register 0x45 = 0xADA5				
ADC Resolution[2]	TIA feedback resistor				
	25 kΩ		4.62		nA/LSB
	50 kΩ		2.31		nA/LSB
	100 kΩ		1.15		nA/LSB
	200 kΩ		0.58		nA/LSB
ADC Saturation Level	TIA feedback resistor				
	25 kΩ		37.84		µA
	50 kΩ		18.92		µA
	100 kΩ		9.46		µA
	200 kΩ		4.73		µA
Ambient Signal Headroom on Pulsed Signal	TIA feedback resistor				
	25 kΩ		12.56		µA
	50 kΩ		6.28		µA
	100 kΩ		3.14		µA
	200 kΩ		1.57		µA
FULL SIGNAL CONVERSIONS[3]					
TIA Saturation Level of Pulsed Signal and Ambient Level	TIA feedback resistor				
	25 kΩ		50.4		µA
	50 kΩ		25.2		µA
	100 kΩ		12.6		µA
	200 kΩ		6.3		µA
TIA Linear Range	TIA feedback resistor				
	25 kΩ		42.8		µA
	50 kΩ		21.4		µA
	100 kΩ		10.7		µA
	200 kΩ		5.4		µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSTEM PERFORMANCE					
Total Output Noise Floor	Normal mode; per pulse; per channel; no LED; photodiode capacitance (C_{PD}) = 70 pF				
	25 kΩ; referred to ADC input		1.0		LSB rms
	25 kΩ; referred to peak input signal for 2 µs LED pulse		4.6		nA rms
	25 kΩ; referred to peak input signal for 3 µs LED pulse		3.3		nA rms
	25 kΩ; saturation SNR per pulse per channel[4]		78.3		dB
	50 kΩ; referred to ADC input		1.2		LSB rms
	50 kΩ; referred to peak input signal for 2 µs LED pulse		2.8		nA rms
	50 kΩ; referred to peak input signal for 3 µs LED pulse		2.0		nA rms
	50 kΩ; saturation SNR per pulse per channel[4]		76.6		dB
	100 kΩ; referred to ADC input		1.5		LSB rms
	100 kΩ; referred to peak input signal for 2 µs LED pulse		1.7		nA rms
	100 kΩ; referred to peak input signal for 3 µs LED pulse		1.2		nA rms
	100 kΩ; saturation SNR per pulse per channel[4]		74.9		dB
	200 kΩ; referred to ADC input		2.2		LSB rms
	200 kΩ; referred to peak input signal for 2 µs LED pulse		1.3		nA rms
	200 kΩ; referred to peak input signal for 3 µs LED pulse		0.9		nA rms
	200 kΩ; saturation SNR per pulse per channel[4]		71.2		dB

[1] This saturation level applies to the ADC only and, therefore, includes only the pulsed signal. Any nonpulsatile signal is removed prior to the ADC stage.
[2] ADC resolution is listed per pulse when the AFE offset is correctly compensated per the AFE Operation section. If using multiple pulses, divide by the number of pulses.
[3] This saturation level applies to the full signal path and, therefore, includes both the ambient signal and the pulsed signal. The linear dynamic range of the TIA is 85% of the TIA saturation levels shown.
[4] The noise term of the saturation SNR value refers to the receiver noise only and does not include photon shot noise or any noise on the LED signal itself.

DIGITAL SPECIFICATIONS

DVDD = 1.7 V to 1.9 V, T_A = -40°C to 105°C, unless otherwise noted.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS (GPIOx, SCL[1], SDA[1], SCLK[2], MOSI[2], $\overline{CS}$[2])						
Input Voltage Level						
High	V_{IH}	SCL[1], SDA[1]	0.7 × DVDD		3.6	V
		GPIOx, SCLK[2], MOSI[2], $\overline{CS}$[2]	0.7 × DVDD		DVDD	V
Low	V_{IL}				0.3 × DVDD	V
Input Current Level						
High	I_{IH}		−10		+10	µA
Low	I_{IL}		−10		+10	µA
Input Capacitance	C_{IN}			10		pF
LOGIC OUTPUTS						
Output Voltage Level		GPIOx, MISO[2]				
High	V_{OH}	2 mA high level output current	DVDD − 0.5			V
Low	V_{OL}	2 mA low level output current			0.5	V
Output Voltage Level		SDA[1]				
Low	V_{OL1}	2 mA low level output current			0.2 × DVDD	V
Output Current Level		SDA[1]				
Low	I_{OL}	V_{OL1} = 0.6 V	6			mA

[1] This pin is only available as part of the I²C interface on the ADPD1080.
[2] This pin is only available as part of the SPI port on the ADPD1081.

TIMING SPECIFICATIONS

DVDD = 1.7 V to 1.9 V, T_A = −40°C to +105°C, unless otherwise noted.

I²C Timing Specifications

Table 6.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
I²C PORT		I²C port on ADPD1080 only.				
SCL						
Frequency				1	0.4	Mbps
Minimum Pulse Width						
High	t_1		370			ns
Low	t_2		530			ns
Start Condition						
Hold Time	t_3		260			ns
Setup Time	t_4		260			ns
SDA Setup Time	t_5		50			ns
SDA Hold Time	t_9		0			ns
SCL and SDA						
Rise Time	t_6				1000	ns
Fall Time	t_7				300	ns
Stop Condition						
Setup Time	t_8		260			ns

I²C Timing Diagram

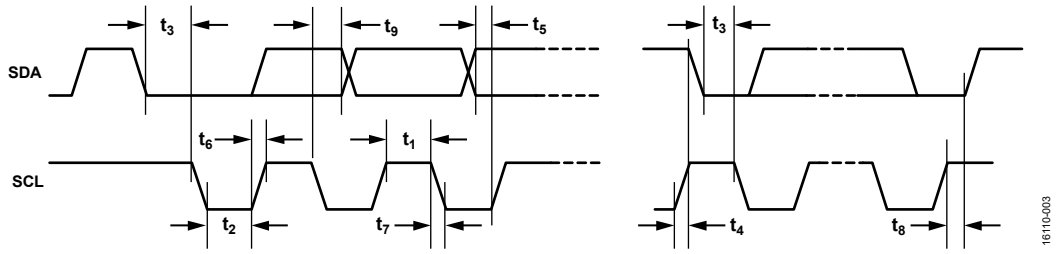

Figure 3. I²C Timing Diagram

SPI Timing Specifications

DVDD = 1.7 V to 1.9 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 7.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SPI PORT		SPI Port available on ADPD1081 only				
SCLK						
Frequency	f_{SCLK}				10	MHz
Minimum Pulse Width						
High	$t_{SCLKPWH}$		20			ns
Low	$t_{SCLKPWL}$		20			ns
$\overline{CS}$						
Setup Time	$t_{\overline{CSS}}$	$\overline{CS}$ setup to SCLK rising edge	10			ns
Hold Time	$t_{\overline{CSH}}$	$\overline{CS}$ hold from SCLK rising edge	10			ns
Pulse Width High	$t_{\overline{CSPWH}}$	$\overline{CS}$ pulse width high	10			ns
MOSI						
Setup Time	t_{MOSIS}	MOSI setup to SCLK rising edge	10			ns
Hold Time	t_{MOSIH}	MOSI hold from SCLK rising edge	10			ns
MISO Output Delay	t_{MISOD}	MISO valid output delay from SCLK falling edge			21	ns

SPI Timing Diagram

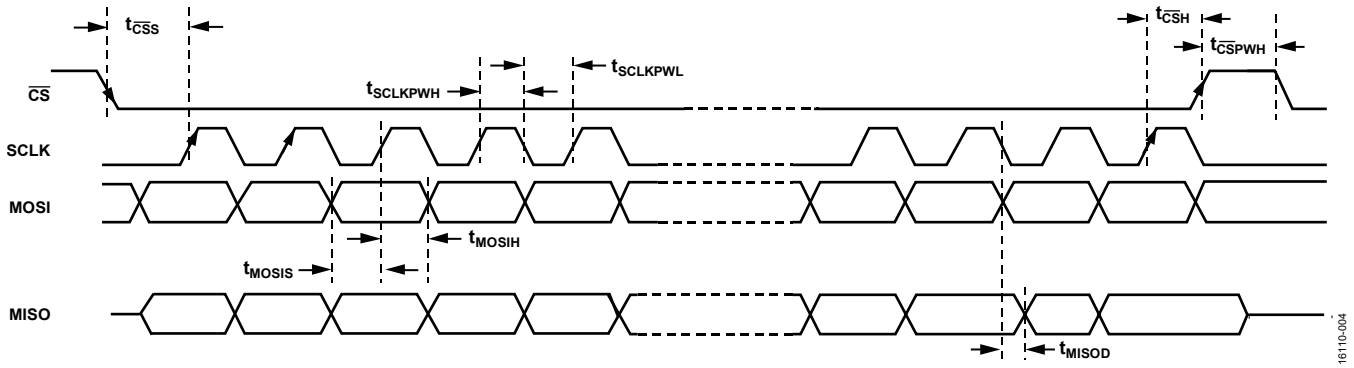

Figure 4. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 8. ADPD1080 Absolute Maximum Rating

Parameter	Rating
AVDD to AGND	−0.3 V to +2.2 V
DVDD to AGND (LFCSP Only)	−0.3 V to +2.2 V
GPIOx to AGND (LFCSP Only)	−0.3 V to +2.2 V
DVDD to DGND (WLCSP Only)	−0.3 V to +2.2 V
GPIOx to DGND (WLCSP Only)	−0.3 V to +2.2 V
LEDXx to LGND	−0.3 V to +3.6 V
SCL, SDA to DGND	−0.3 V to +3.9 V
Junction Temperature	150°C
Electrostatic Discharge (ESD)	
Human Body Model (HBM)	1500 V
Charged Device Model (CDM)	500 V
Machine Model (MM)	100 V

Table 9. ADPD1081 Absolute Maximum Rating

Parameter	Rating
VDD to AGND	−0.3 V to +2.2 V
VDD to DGND	−0.3 V to +2.2 V
GPIOx, MOSI, MISO, SCLK, $\overline{CS}$ to DGND	−0.3 V to +2.2 V
LEDXx to LGND	−0.3 V to +3.6 V
Junction Temperature	150°C
Electrostatic Discharge (ESD)	
Human Body Model (HBM)	1500 V
Charged Device Model (CDM)	500 V
Machine Model (MM)	100 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance value, and θ_{JC} is the junction to case thermal resistance value.

Table 10. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
CP-28-5 (28-Lead LFCSP)	54.9	5.3	°C/W
CB-16-18 (16-Ball WLCSP)	60	0.5	°C/W
CB-17-1 (17-Ball WLCSP)	60	0.5	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P board and 2 thermal vias. See JEDEC JESD-51.

RECOMMENDED SOLDERING PROFILE

Figure 5 and Table 11 provide details about the recommended soldering profile.

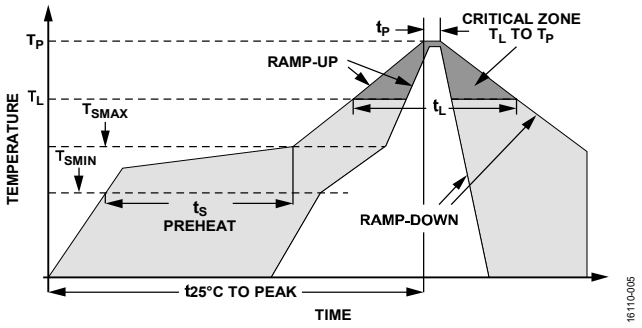

Figure 5. Recommended Soldering Profile

Table 11. Recommended Soldering Profile

Profile Feature	Condition (Pb-Free)
Average Ramp Rate (T_L to T_P)	3°C/sec max
Preheat	
Minimum Temperature (T_{SMIN})	150°C
Maximum Temperature (T_{SMAX})	200°C
Time (T_{SMIN} to T_{SMAX}) (t_S)	60 sec to 180 sec
T_{SMAX} to T_L Ramp-Up Rate	3°C/sec maximum
Time Maintained Above Liquidous Temperature	
Liquidous Temperature (T_L)	217°C
Time (t_L)	60 sec to 150 sec
Peak Temperature (T_P)	+260 (+0/−5)°C
Time Within 5°C of Actual Peak Temperature (t_P)	<30 sec
Ramp-Down Rate	6°C/sec maximum
Time from 25°C to Peak Temperature	8 minutes maximum

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

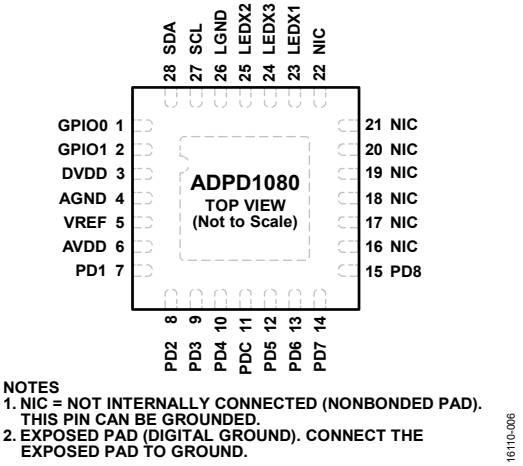

Figure 6. 28-Lead LFCSP Pin Configuration (ADPD1080)

Table 12. 28-Lead LFCSP Pin Function Descriptions (ADPD1080)

Pin No.	Mnemonic	Type[1]	Description
1	GPIO0	DIO	General-Purpose Input/Output 0. This pin is used for interrupts and various clocking options.
2	GPIO1	DIO	General-Purpose Input/Output 1. This pin is used for interrupts and various clocking options.
3	DVDD	S	1.8 V Digital Supply.
4	AGND	S	Analog Ground.
5	VREF	REF	Internally Generated ADC Voltage Reference. Buffer this pin with a 1 µF capacitor to AGND.
6	AVDD	S	1.8 V Analog Supply.
7	PD1	AI	Photodiode Current Input (Anode) 1. If not in use, leave this pin floating.
8	PD2	AI	Photodiode Current Input (Anode) 2. If not in use, leave this pin floating.
9	PD3	AI	Photodiode Current Input (Anode) 3. If not in use, leave this pin floating.
10	PD4	AI	Photodiode Current Input (Anode) 4. If not in use, leave this pin floating.
11	PDC	AO	Photodiode Common Cathode Bias.
12	PD5	AI	Photodiode Current Input (Anode) 5. If not in use, leave this pin floating.
13	PD6	AI	Photodiode Current Input (Anode) 6. If not in use, leave this pin floating.
14	PD7	AI	Photodiode Current Input (Anode) 7. If not in use, leave this pin floating.
15	PD8	AI	Photodiode Current Input (Anode) 8. If not in use, leave this pin floating.
16 to 22	NIC	R	Not Internally Connected (Nonbonded Pad). This pin can be grounded.
23	LEDX1	AO	LED Driver 1 Current Sink. If not in use, leave this pin floating.
24	LEDX3	AO	LED Driver 3 Current Sink. If not in use, leave this pin floating.
25	LEDX2	AO	LED Driver 2 Current Sink. If not in use, leave this pin floating.
26	LGND	S	LED Driver Ground.
27	SCL	DI	I^2C Clock Input.
28	SDA	DIO	I^2C Data Input/Output.
	EPAD (DGND)	S	Exposed Pad (Digital Ground). Connect the exposed pad to ground.

[1] DIO means digital input/output, S means supply, REF means voltage reference, AI means analog input, AO means analog output, R means reserved, and DI means digital input.

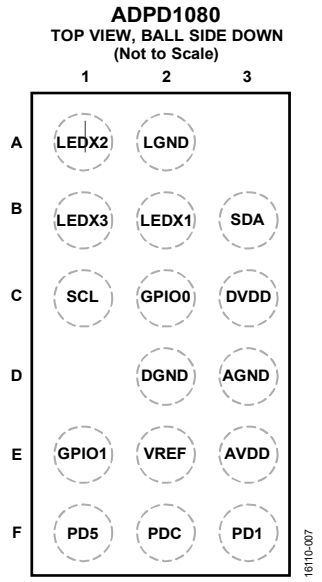

Figure 7. 16-Ball WLCSP Pin Configuration (ADPD1080)

Table 13. 16-Ball WLCSP Pin Function Descriptions (ADPD1080)

Pin No.	Mnemonic	Type[1]	Description
A1	LEDX2	AO	LED2 Driver Current Sink. If not in use, leave this pin floating.
A2	LGND	S	LED Driver Ground.
B1	LEDX3	AO	LED3 Driver Current Sink. If not in use, leave this pin floating.
B2	LEDX1	AO	LED1 Driver Current Sink. If not in use, leave this pin floating.
B3	SDA	DIO	I^2C Data Input/Output.
C1	SCL	DI	I^2C Clock Input.
C2	GPIO0	DIO	General-Purpose Input/Output 0. This pin is used for interrupts and various clocking options.
C3	DVDD	S	1.8 V Digital Supply.
D2	DGND	S	Digital Ground.
D3	AGND	S	Analog Ground.
E1	GPIO1	DIO	General-Purpose Input/Output 1. This pin is used for interrupts and various clocking options.
E2	VREF	REF	Internally Generated ADC Voltage Reference. Buffer this pin with a 1 µF capacitor to AGND.
E3	AVDD	S	1.8 V Analog Supply.
F1	PD5	AI	PD5 Photodiode Current Input. If not in use, leave this pin floating.
F2	PDC	AO	Photodiode Common Cathode Bias.
F3	PD1	AI	PD1 Photodiode Current Input. If not in use, leave this pin floating.

[1] AO means analog output, S means supply, DIO means digital input/output, DI means digital input, REF means voltage reference, AI means analog input, and AO means analog output.

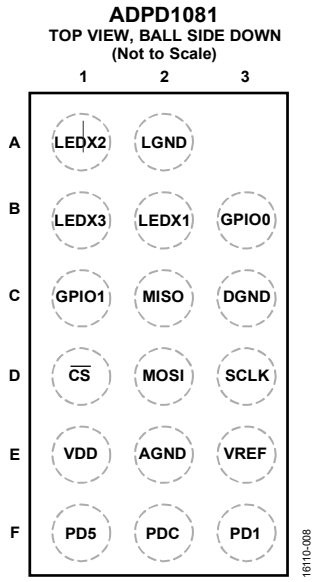

Figure 8. 17-Ball WLCSP Pin Configuration (ADPD1081)

Table 14. 17-Ball WLCSP Pin Function Descriptions (ADPD1081)

Pin No.	Mnemonic	Type[1]	Description
A1	LEDX2	AO	LED2 Driver Current Sink. If not in use, leave this pin floating.
A2	LGND	S	LED Driver Ground.
B1	LEDX3	AO	LED3 Driver Current Sink. If not in use, leave this pin floating.
B2	LEDX1	AO	LED1 Driver Current Sink. If not in use, leave this pin floating.
B3	GPIO0	DIO	General-Purpose Input/Output 0. This pin is used for interrupts and various clocking options.
C1	GPIO1	DIO	General-Purpose Input/Output 1. This pin is used for interrupts and various clocking options.
C2	MISO	DO	Master Input, Slave Output.
C3	DGND	S	Digital Ground.
D1	$\overline{CS}$	DI	SPI Chip Select. Active low.
D2	MOSI	DI	Master Output, Slave Input.
D3	SCLK	DI	SPI Clock Input.
E1	VDD	S	1.8 V Power Supply.
E2	AGND	S	Analog Ground.
E3	VREF	REF	Internally Generated ADC Voltage Reference. Buffer this pin with a 1 µF capacitor to AGND.
F1	PD5	AI	PD5 Photodiode Current Input. If not in use, leave this pin floating.
F2	PDC	AO	Photodiode Common Cathode Bias.
F3	PD1	AI	PD1 Photodiode Current Input. If not in use, leave this pin floating.

[1] AO means analog output, S means supply, DIO means digital input/output, DO means digital output, DI means digital input, REF means voltage reference, and AI means analog input.

TYPICAL PERFORMANCE CHARACTERISTICS

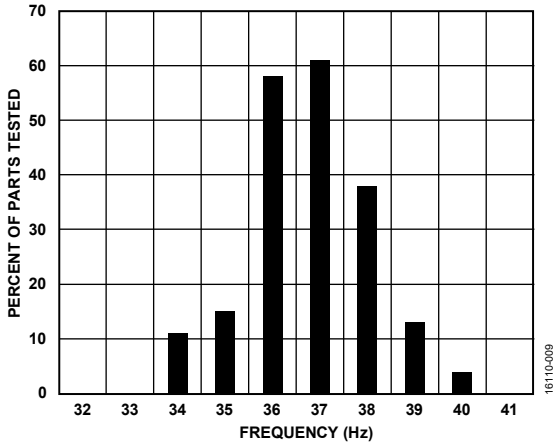

Figure 9. 32 kHz Clock Frequency Distribution
(Default Settings, Before User Calibration: Register 0x4B = 0x2612)

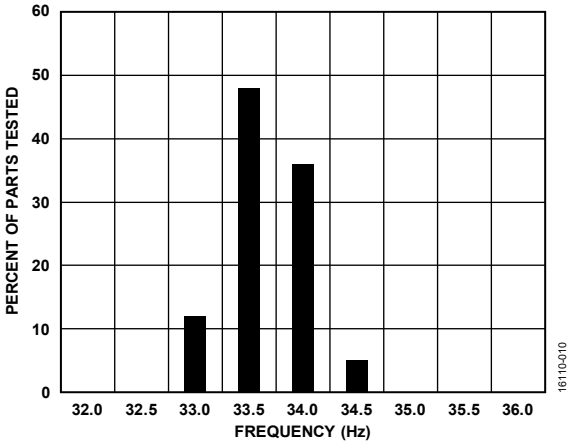

Figure 10. 32 MHz Clock Frequency Distribution
(Default Settings, Before User Calibration: Register 0x4D = 0x0098)

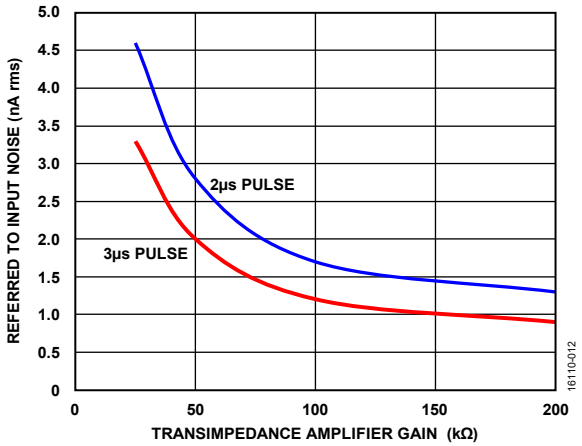

Figure 11. Referred to Input Noise vs. Transimpedance Amplifier Gain at C_{PD} = 70 pF

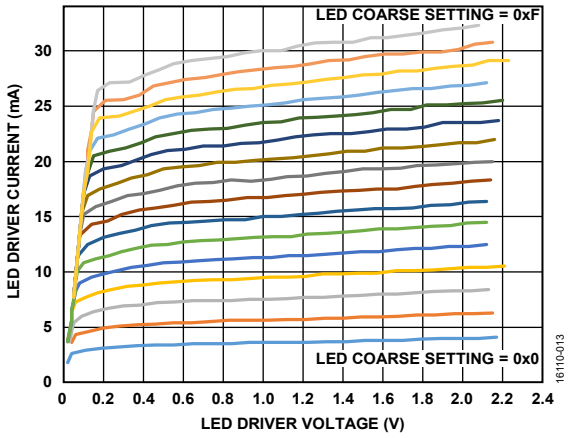

Figure 12. LED Driver Current vs. LED Driver Voltage at 10% Drive Strength, Fine Setting at Default

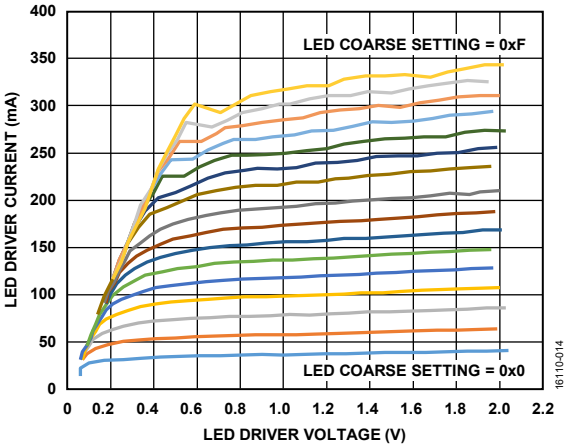

Figure 13. LED Driver Current vs. LED Driver Voltage at 100% Drive Strength, Fine Setting at Default

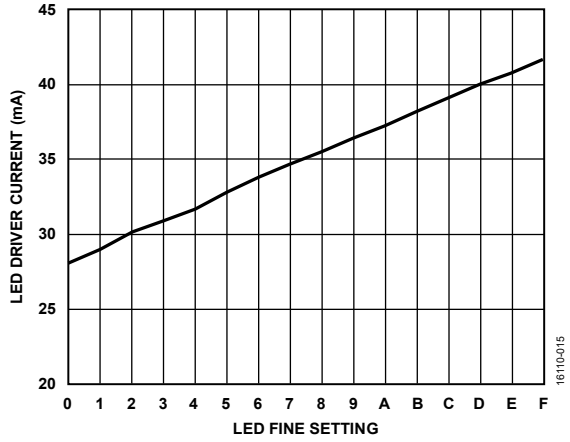

Figure 14. LED Driver Current vs. LED Fine Setting (Coarse Setting = 0x0)

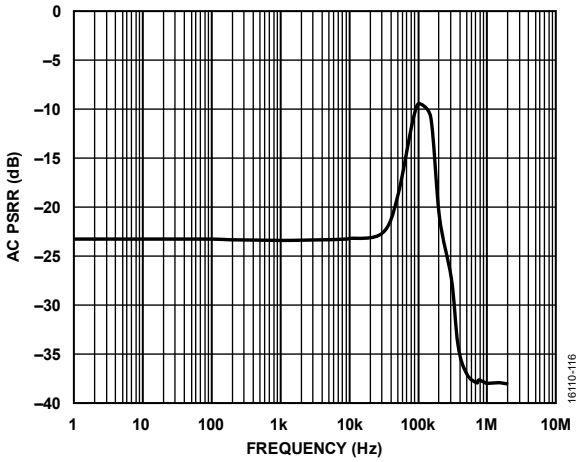

Figure 16. AC PSRR vs. Frequency for 75% Full-Scale Input Signal

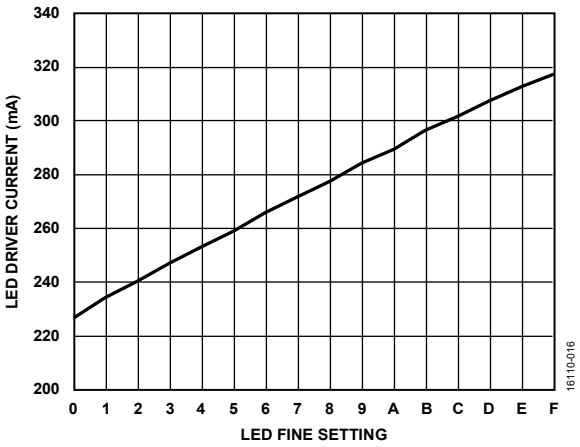

Figure 15. LED Driver Current vs. LED Fine Setting (Coarse Setting = 0xF)

THEORY OF OPERATION

INTRODUCTION

The ADPD1080/ADPD1081 operate as a complete optical transceiver stimulating up to three LEDs and measuring the return signal on up to two separate current inputs. The core consists of a photometric front end coupled with an ADC, digital block, and three independent LED drivers. The core circuitry stimulates the LEDs and measures the return in the analog block through one to eight photodiode inputs, storing the results in discrete data locations. The two inputs can drive four simultaneous input channels. Data can be read directly by a register or through a first in, first out (FIFO) method. This highly integrated system includes an analog signal processing block, digital signal processing block, an I^2C communication interface on the ADPD1080 or an SPI port on the ADPD1081, and programmable pulsed LED current sources.

The LED driver is a current sink and is agnostic to the LED supply voltage and the LED type. The photodiode (PDx) inputs can accommodate any photodiode with an input capacitance of less than 100 pF. The ADPD1080/ADPD1081 produces a high SNR for relatively low LED power while greatly reducing the effect of ambient light on the measured signal.

DUAL TIME SLOT OPERATION

The ADPD1080/ADPD1081 operate in two independent time slots, Time Slot A and Time Slot B, that operate sequentially. The entire signal path from LED stimulation to data capture and processing executes during each time slot. Each time slot has a separate datapath that uses independent settings for the LED driver, AFE setup, and the resulting data. Time Slot A and Time Slot B operate in sequence for every sampling period, as shown in Figure 17.

The timing parameters for Time Slot A and Time Slot B are defined as follows:

$$t_A\ (\mu s) = SLOTA\_LED\_OFFSET + n_A \times SLOTA\_PERIOD$$

where n_A is the number of pulses for Time Slot A (Register 0x31, Bits[15:8]).

$$t_B\ (\mu s) = SLOTB\_LED\_OFFSET + n_B \times SLOTB\_PERIOD$$

where n_B is the number of pulses for Time Slot B (Register 0x36, Bits[15:8]).

Calculate the LED period using the following equation:

$$LED\_PERIOD,\ minimum = 2 \times SLOTx\_AFE\_WIDTH + 11$$

t_1 and t_2 are fixed and based on the computation time for each slot. If a slot is not in use, these times do not add to the total active time. Table 15 defines the values for these LED and sampling time parameters.

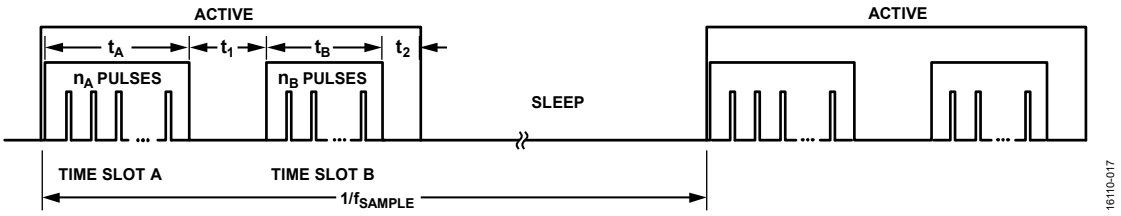

Figure 17. Time Slot Timing Diagram (f_{SAMPLE} is the sampling frequency (Register 0x12, Bits[15:0]).)

Table 15. LED Timing and Sample Timing Parameters

Parameter	Register	Bits	Test Conditions/Comments	Min	Typ	Max	Unit
SLOTA_LED_OFFSET[1]	0x30	[7:0]	Delay from power-up to LEDA rising edge	23		63	µs
SLOTB_LED_OFFSET[1]	0x35	[7:0]	Delay from power-up to LEDB rising edge	23		63	µs
SLOTA_PERIOD[2]	0x31	[7:0]	Time between LED pulses in Time Slot A; SLOTx_AFE_WIDTH = 4 µs	19		63	µs
SLOTB_PERIOD[2]	0x36	[7:0]	Time between LED pulses in Time Slot B; SLOTx_AFE_WIDTH = 4 µs	19		63	µs
t_1	N/A	N/A	Compute time for Time Slot A		68		µs
t_2	N/A	N/A	Compute time for Time Slot B		20		µs
t_{SLEEP}	N/A	N/A	Sleep time between sample periods	222			µs

[1] Setting the SLOTx_LED_OFFSET less than the specified minimum value can cause failure of ambient light rejection for large photodiodes.
[2] Setting the SLOTx_LED_PERIOD less than the specified minimum value can cause invalid data captures.

TIME SLOT SWITCH

ADPD1080 LFCSP Input Configurations

Up to eight photodiodes (PD1 to PD8) can be connected to the ADPD1080 for the LFCSP. The photodiode anodes are connected to the PD1 to PD8 input pins; the photodiode cathodes are connected to the cathode pin, PDC. The anodes are assigned in seven different configurations depending on the settings of Register 0x14 (see Figure 18 through Figure 24).

Figure 18 through Figure 24 show multiple configurations that can be used. The configuration selected depends on the requirements of the application. Depending on the dynamic range requirements of the application, 1-, 2-, or 4-channel modes can be selected. There are also several modes where input pins can be multiplexed together in cases where photodiode currents must be summed.

See Table 16 for the time slot switch settings. It is important to leave any unused inputs floating for proper operation of the devices. The photodiode inputs are current inputs and as such, these pins are considered voltage outputs. Tying these inputs to a voltage saturates the analog block.

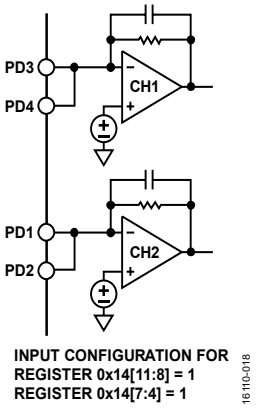

Figure 18. PD1 to PD4 Connections with Register 0x14, Bits[11:8] and Bits[7:4] = 1 for the LFCSP

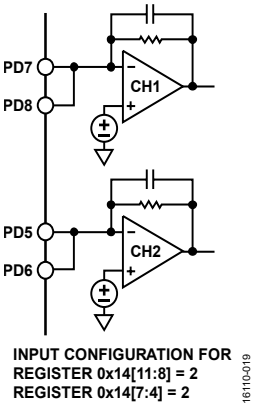

Figure 19. PD5 to PD8 Connections with Register 0x14, Bits[11:8] and Bits[7:4] = 2 for the LFCSP

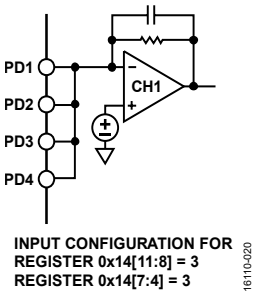

Figure 20. PD1 to PD4 Connections with Register 0x14, Bits[11:8] and Bits[7:4] = 3 for the LFCSP

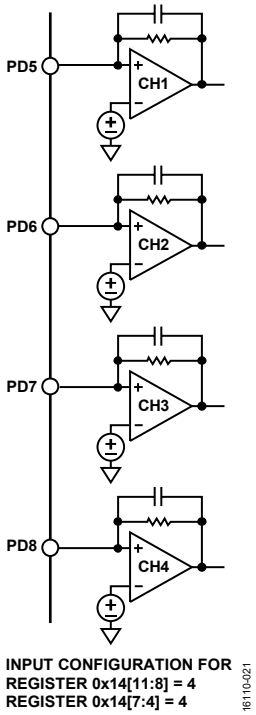

Figure 21. PD5 to PD8 Connections with Register 0x14, Bits[11:8] and Bits[7:4] = 4 for the LFCSP

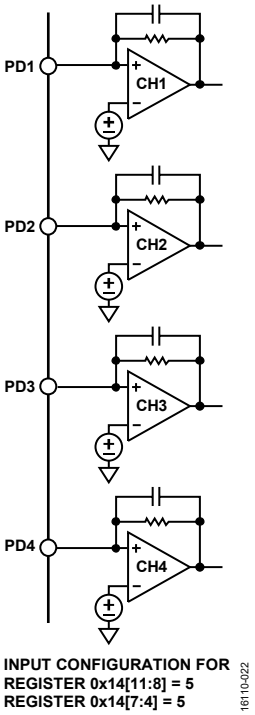

Figure 22. PD1 to PD4 Connections with Register 0x14, Bits[11:8] and Bits[7:4] = 5 for the LFCSP

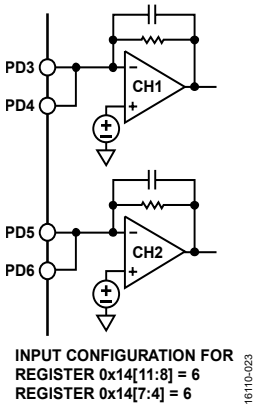

Figure 23. PD3 to PD6 Connections with Register 0x14, Bits[11:8] and Bits[7:4] = 6 for the LFCSP

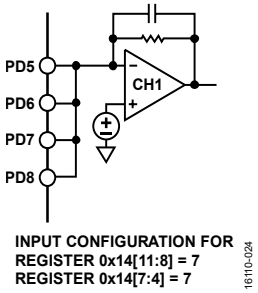

Figure 24. PD5 to PD8 Connection with Register 0x14, Bits[11:8] and Bits[7:4] = 4 for the LFCSP

Table 16. Time Slot Switch (Register 0x14), ADPD1080 LFCSP

Register, Bits, and Time Slot	Setting	Channel			
		1	2	3	4
Register 0x14, Bits[11:8] for Time Slot B and Bits[7:4] for Time Slot A	0	No connect	No connect	No connect	No connect
	1	PD3, PD4	PD1, PD2	No connect	No connect
	2	PD7, PD8	PD5, PD6	No connect	No connect
	3	PD1 to PD4	No connect	No connect	No connect
	4	PD5	PD6	PD7	PD8
	5	PD1	PD2	PD3	PD4
	6	PD3, PD4	PD5, PD6	No connect	No connect
	7	PD5 to PD8	No connect	No connect	No connect

WLCSP Input Configurations

Up to two photodiodes can be connected to the PD1 and PD5 input pins of the ADPD1080 and ADPD1081 WLCSP models. The photodiode anodes are connected to the PD1 and PD5 input pins; the photodiode cathodes are connected to the cathode pin, PDC. The anodes are assigned in the configurations shown in Figure 25 and Figure 26 based on the bit settings of Register 0x14.

See Table 17 for the time slot switch settings. It is important to leave any unused inputs floating for proper operation of the devices. The photodiode inputs are current inputs and, as such, these pins are also considered voltage outputs. Tying these inputs to a voltage saturates the analog block.

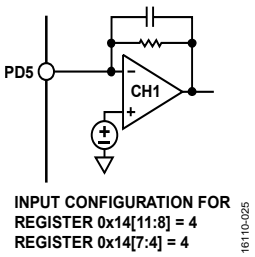

Figure 25. PD5 Connection with Register 0x14, Bits[11:8] and Bits[7:4] = 4 for the WLCSP

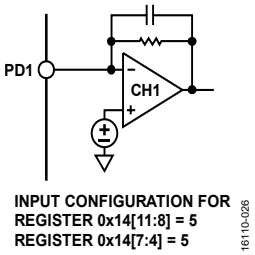

Figure 26. PD1 Connection with Register 0x14, Bits[11:8] and Bits[7:4] = 5 for the WLCSP

Table 17. Time Slot Switch (Register 0x14), ADPD1080/ADPD1081 WLCSP

		Channel			
Register, Bits, and Time Slot	**Setting**	**1**	**2**	**3**	**4**
Register 0x14, Bits[11:8] for Time Slot B and Bits[7:4] for Time Slot A	4	PD5	No connect	No connect	No connect
	5	PD1	No connect	No connect	No connect

ADJUSTABLE SAMPLING FREQUENCY

Register 0x12 controls the sampling frequency setting of the ADPD1080/ADPD1081 and Register 0x4B, Bits[5:0] further tunes this clock for greater accuracy. An internal 32 kHz sample rate clock that also drives the transition of the internal state machine governs the sampling frequency. The maximum sampling frequencies for some sample conditions are listed in Table 3. The maximum sample frequency for all conditions is determined by the following equation:

$$f_{SAMPLE, MAX} = 1/(t_A + t_1 + t_B + t_2 + t_{SLEEP, MIN})$$

where $t_{SLEEP, MIN}$ is the minimum sleep time required between samples. See Table 15.

If a given time slot is not in use, elements from that time slot do not factor into the calculation. For example, if Time Slot A is not in use, t_A and t_1 do not add to the sampling period and the new maximum sampling frequency is calculated as follows:

$$f_{SAMPLE, MAX} = 1/(t_B + t_2 + t_{SLEEP, MIN})$$

See the Dual Time Slot Operation section for the definitions of t_A, t_1, t_B, and t_2. The maximum achievable sampling rate with a single pulse in Time Slot B is ~2.8 kSPS.

External Sync for Sampling

The ADPD1080/ADPD1081 provide an option to use an external sync signal to trigger the sampling periods. This external sample sync signal can be provided either on the GPIO0 pin or the GPIO1 pin. This functionality is controlled by Register 0x4F, Bits[3:2]. When enabled, a rising edge on the selected input specifies when the next sample cycle occurs. When triggered, there is a delay of one to two internal sampling clock (32 kHz) cycles, and then the normal start-up sequence occurs. This sequence is the same when the normal sample timer provides the trigger. To enable the external sync signal feature, use the following procedure:

1. Write 0x1 to Register 0x10 to enter program mode.
2. Write the appropriate value to Register 0x4F, Bits[3:2] to select whether the GPIO0 pin or the GPIO1 pin specifies when the next sample cycle occurs. Also, enable the appropriate input buffer using Register 0x4F, Bit 1, for the GPIO0 pin, or Register 0x4F, Bit 5, for the GPIO1 pin.
3. Write 0x4000 to Register 0x38.
4. Write 0x2 to Register 0x10 to start the sampling operations.
5. Apply the external sync signal on the selected pin at the desired rate; sampling occurs at that rate. As with normal sampling operations, read the data using the FIFO or the data registers.

The maximum frequency constraints also apply in this case.

Providing an External 32 kHz Clock

The ADPD1080/ADPD1081 have an option for the user to provide an external 32 kHz clock to the devices for system synchronization or for situations where a clock with better accuracy than the internal 32 kHz clock is required. The external 32 kHz clock is provided on the GPIO1 pin. To enable the 32 kHz external clock, use the following procedure at startup:

1. Drive the GPIO1 pin to a valid logic level or with the desired 32 kHz clock prior to enabling the GPIO1 pin as an input. Do not leave the pin floating prior to enabling it.
2. Write 01 to Register 0x4F, Bits[6:5] to enable the GPIO1 pin as an input.
3. Write 10 to Register 0x4B, Bits[8:7] to configure the devices to use an external 32 kHz clock. This setting disables the internal 32 kHz clock and enables the external 32 kHz clock.
4. Write 0x1 to Register 0x10 to enter program mode.
5. Write additional control registers in any order while the devices are in program mode to configure the devices as required.
6. Write 0x2 to Register 0x10 to start the normal sampling operation.

STATE MACHINE OPERATION

During each time slot, the ADPD1080/ADPD1081 operate according to a state machine. The state machine operates in the sequence shown in Figure 27.

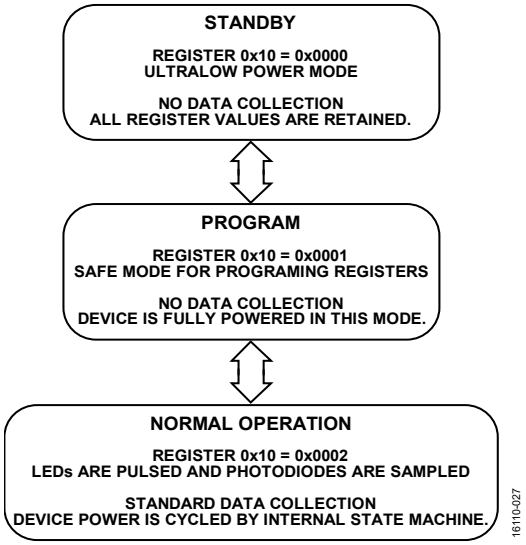

Figure 27. State Machine Operation Flowchart

The ADPD1080/ADPD1081 operate in one of three modes: standby, program, and normal operation.

Standby mode is a power saving mode in which no data collection occurs. All register values are retained in this mode. To place the devices in standby mode, write 0x0 to Register 0x10, Bits[1:0]. The devices power up in standby mode.

Program mode is used for programming registers. Always cycle the ADPD1080/ADPD1081 through program mode when writing registers or changing modes. Because no power cycling occurs in this mode, the devices may consume higher current in program mode than in normal operation. To place the devices in program mode, write 0x1 to Register 0x10, Bits[1:0].

In normal operation, the ADPD1080/ADPD1081 pulse light and collect data. Power consumption in this mode depends on the pulse count and data rate. To place the devices in normal sampling mode, write 0x2 to Register 0x10, Bits[1:0].

NORMAL MODE OPERATION AND DATA FLOW

In normal mode, the ADPD1080/ADPD1081 follow a specific pattern set up by the state machine. This pattern is shown in the corresponding datapath diagram shown in Figure 28. The pattern is as follows:

1. LED pulse and sample. The ADPD1080/ADPD1081 pulse external LEDs. The response of a photodiode or photodiodes to the reflected light is measured by the ADPD1080/ADPD1081. Each data sample is constructed from the sum of n individual pulses, where n is user configurable between 1 and 255.
2. Intersample averaging. If desired, the logic can average n samples, from 2 to 128 in powers of 2, to produce output data. New output data is saved to the output registers every N samples.
3. Data read. The host processor reads the converted results from the data register or the FIFO.
4. Repeat. The sequence has a few different loops that enable different types of averaging while keeping both time slots close in time relative to each other.

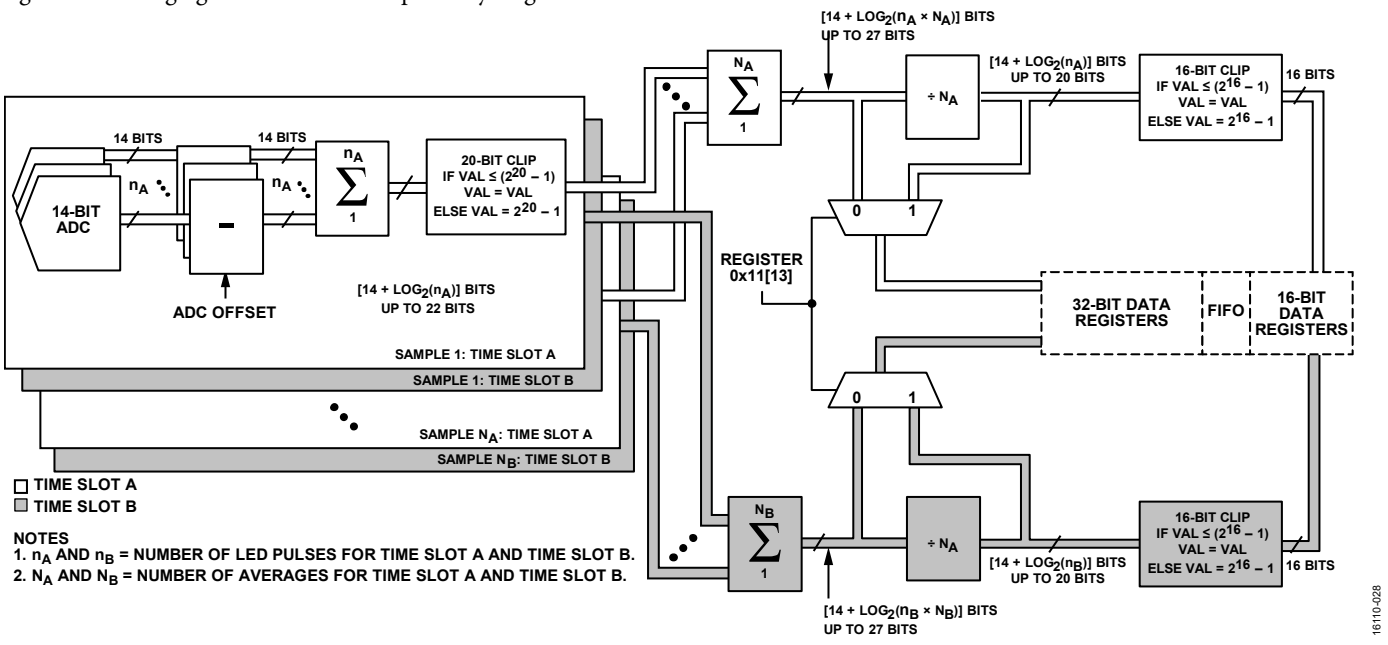

Figure 28. ADPD1080/ADPD1081 Datapath

LED Pulse and Sample

At each sampling period, the selected LED driver drives a series of LED pulses, as shown in Figure 29. The magnitude, duration, and number of pulses are programmable over the I²C interface. Each LED pulse coincides with a sensing period so that the sensed value represents the total charge acquired on the photodiode in response to only the corresponding LED pulse. Charge, such as ambient light, that does not correspond to the LED pulse is rejected.

After each LED pulse, the photodiode output relating the pulsed LED signal is sampled and converted to a digital value by the 14-bit ADC. Each subsequent conversion within a sampling period is summed with the previous result. Up to 255 pulse values from the ADC can be summed in an individual sampling period. There is a 20-bit maximum range for each sampling period.

Averaging

The ADPD1080/ADPD1081 offer sample accumulation and averaging functionality to increase signal resolution.

Within a sampling period, the AFE can sum up to 256 sequential pulses. As shown in Figure 28, samples acquired by the AFE are clipped to 20 bits at the output of the AFE. Additional resolution, up to 27 bits, can be achieved by averaging between sampling periods. This accumulated data of N samples is stored as 27-bit values and can be read out directly by using the 32-bit output registers or the 32-bit FIFO configuration.

When using the averaging feature set up by Register 0x15, subsequent pulses can be averaged by powers of 2. The user can select from 2, 4, 8 … up to 128 samples to be averaged. Pulse data is still acquired by the AFE at the sampling frequency, f_{SAMPLE} (Register 0x12), but new data is written to the registers at the rate of f_{SAMPLE}/N every N^{th} sample. This new data consists of the sum of the previous N samples. The full 32-bit sum is stored in the 32-bit registers. However, before sending this data to the FIFO, a divide by N operation occurs. This divide operation maintains bit depth to prevent clipping on the FIFO.

Use this between sample averaging to lower the noise while maintaining 16-bit resolution. If the pulse count registers are kept to 8 or less, the 16-bit width is never exceeded. Therefore, when using Register 0x15 to average subsequent pulses, many pulses can be accumulated without exceeding the 16-bit word width. This averaging can reduce the number of FIFO reads required by the host processor.

Data Read

The host processor reads output data from the ADPD1080/ADPD1081 via the I²C protocol on the ADPD1080 or the SPI port on the ADPD1081. Data is read from the data registers or from the FIFO. New output data is made available every N samples, where N is the user configured averaging factor. The averaging factors for Time Slot A and Time Slot B are configurable independently of each other. If they are the same, both time slots can be configured to save data to the FIFO. If the two averaging factors are different, only one time slot can save data to the FIFO; data from the other time slot can be read from the output registers.

The data read operations are described in more detail in the Reading Data section.

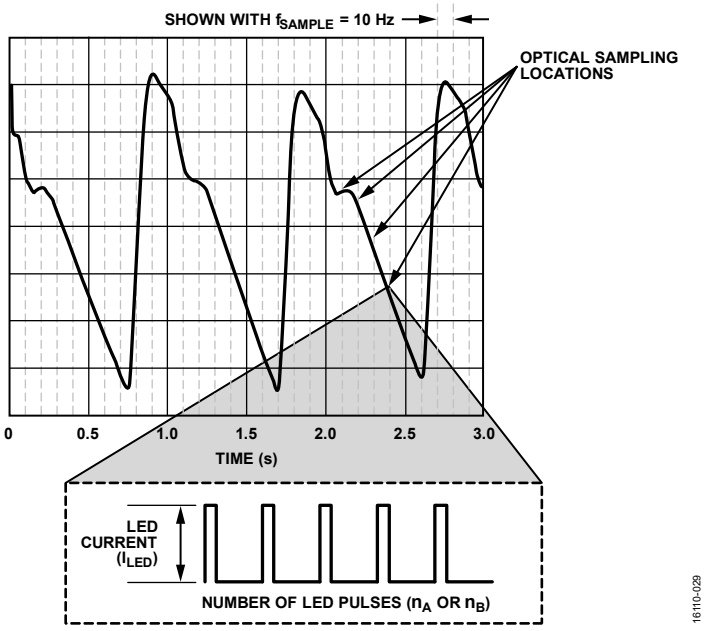

Figure 29. Example of a PPG Signal Sampled at a Data Rate of 10 Hz Using Five Pulses per Sample

AFE OPERATION

The timing within each pulse burst is important for optimizing the operation of the ADPD1080/ADPD1081. Figure 30 shows the timing waveforms for a single time slot as an LED pulse response propagates through the analog block of the AFE. The first graph, shown in green, shows the ideal LED pulsed output. The filtered LED response, shown in blue, shows the output of the analog integrator. The third graph, shown in orange, shows an optimally placed integration window. When programmed to the optimized value, the full signal of the filtered LED response can be integrated. The AFE integration window is then applied to the output of the band-pass filter (BPF) and the result is sent to the ADC and summed for N pulses. If the AFE window is not correctly sized or located, all of the receive signal is not properly reported and system performance is not optimal; therefore, it is important to verify proper AFE position for every new hardware design or the LED width.

AFE INTEGRATION OFFSET ADJUSTMENT

The AFE integration width must be equal or larger than the LED width. As AFE width increases, the output noise increases and the ability to suppress high frequency content from the environment decreases. It is therefore desirable to keep the AFE integration width small. However, if the AFE width is too small, the LED signal is attenuated. With most hardware selections, the AFE width produces the optimal SNR at 1 µs more than the LED width. After setting LED width, LED offset, and AFE width, the ADC offset can then be optimized. The AFE offset must be manually set such that the falling edge of the first segment of the integration window matches the zero crossing of the filtered LED response.

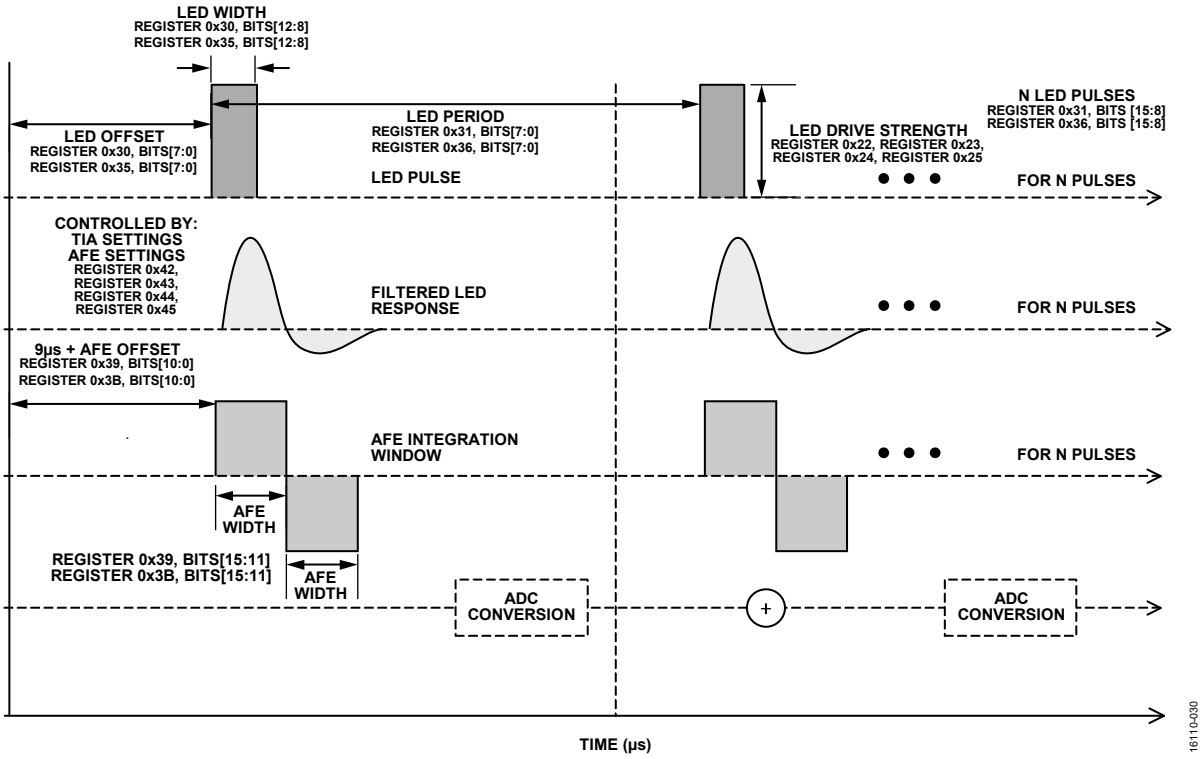

Figure 30. AFE Operation Diagram

AFE Integration Offset Starting Point

The starting point of the AFE integration offset, as expressed in microseconds, is set such that the falling edge of the integration window aligns with the falling edge of the LED.

LED_FALLING_EDGE = SLOTx_LED_OFFSET + SLOTx_LED_WIDTH

and,

AFE_INTEGRATION_FALLING_EDGE = 9 + SLOTx_AFE_OFFSET + SLOTx_AFE_WIDTH

If both falling edges are set equal to each other, solve for SLOTx_AFE_OFFSET to obtain the following equation:

AFE_OFFSET_STARTING_POINT = SLOTx_LED_OFFSET + SLOTx_LED_WIDTH − 9 − SLOTx_AFE_WIDTH

Setting the AFE offset to any point in time earlier than the starting point is equivalent to setting the integration in the future; the AFE cannot integrate the result from an LED pulse that has not yet occurred. As a result, a SLOTx_AFE_OFFSET value less than the AFE_OFFSET_STARTING_POINT value is an erroneous setting. Such a result may indicate that current in the TIA is operating in the reverse direction from intended, where the LED pulse is causing the current to leave the TIA rather than enter it.

Because, for most setups, the SLOTx_AFE_WIDTH is 1 µs wider than the SLOTx_LED_WIDTH, the AFE_OFFSET_STARTING_POINT value is typically 10 µs less than the SLOTx_LED_OFFSET value. Any value less than SLOTx_LED_
OFFSET − 10 is erroneous. The optimal AFE offset is some time after the AFE_OFFSET_STARTING_POINT value. The BPF response, LED response, and photodiode response each add some delay. In general, the component choice, board layout, SLOTx_LED_OFFSET, and SLOTx_LED_WIDTH are the variables that can change the SLOTx_AFE_OFFSET value. After a specific design is set, the SLOTx_AFE_OFFSET value can be locked down and does not need to be optimized further.

Sweeping the AFE Position

The AFE offsets for Time Slot A and Time Slot B are controlled by Bits[10:0] of Register 0x39 and Register 0x3B, respectively. Each LSB represents one cycle of the 32 MHz clock, or 31.25 ns. The register can be thought of as 2^{11-1} of these 31.25 ns steps, or it can be broken into an AFE coarse setting using Bits[10:5] to represent 1 µs steps and Bits[4:0] to represent 31.25 ns steps. Sweeping the AFE position from the starting point to find a local maximum is the recommended way to optimize the AFE offset. The setup for this test is to allow the LED light to fall on the photodiode in a static way. This test is typically done with a reflecting surface at a fixed distance. The AFE position can then be swept to look for changes in the output level. When adjusting the AFE position, it is important to sweep the position using the 31.25 ns steps. Typically, a local maximum is found within 2 µs of the starting point for most systems. Figure 31 shows an example of an AFE sweep, where 0 on the x-axis represents the AFE starting point defined previously. Each data point in Figure 31 corresponds to one 31.25 ns step of the SLOTx_AFE_OFFSET. The optimal location for SLOTx_AFE_OFFSET in this example is 0.687 µs from the AFE starting point.

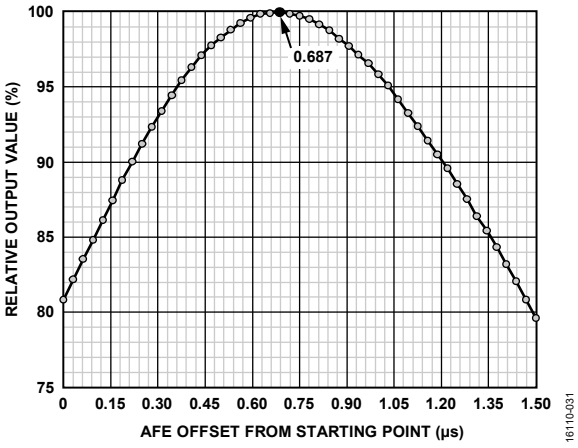

Figure 31. AFE Sweep Example

Table 18 lists some typical LED and AFE values after optimization. In general, it is not recommended to use the SLOTx_AFE_OFFSET numbers in Table 18 without first verifying them against the AFE sweep method. Repeat this method for every new LED width and with every new set of hardware made with the ADPD1080/ ADPD1081. For maximum accuracy, it is recommended that the 32 MHz clock be calibrated prior to sweeping the AFE.

Table 18. AFE Window Settings

LED Register 0x30 or Register 0x35	AFE Register 0x39 or Register 0x3B	Comment
0x0219	0x1A08	2 µs LED pulse, 3 µs AFE width, 25 µs LED delay
0x0319	0x21FE	3 µs LED pulse, 4 µs AFE width, 25 µs LED delay

I²C SERIAL INTERFACE

The ADPD1080 supports an I²C serial interface via the SDA (data) and SCL (clock) pins. All internal registers are accessed through the I²C interface. The ADPD1080 is an I²C only device and does not support an SPI.

The ADPD1080 conforms to the *UM10204 I²C-Bus Specification and User Manual*, Rev. 05—9 October 2012, available from NXP Semiconductors. The I²C interface supports up to 1 Mbps data transfers. Register read and write are supported, as shown in Figure 32. Figure 3 shows the timing diagram for the I²C interface.

Slave Address

The default 7-bit I²C slave address for the device is 0x64, followed by the R/$\overline{W}$ bit. For a write, the default I²C slave address is 0xC8; for a read, the default I²C address is 0xC9. The slave address is configurable by writing to Register 0x09, Bits[7:1]. When multiple ADPD1080 devices are on the same bus lines, the GPIO0 and GPIO1 pins can be used to select specific devices for the address change. Register 0x0D can be used to select a key to enable address changes in specific devices. Use the following procedure to change the slave address when multiple ADPD1080 devices are connected to the same I²C bus lines:

1. Using Register 0x4F, enable the input buffer of the GPIO1 pin, the GPIO0 pin, or both, depending on the key being used.
2. For the device identified as requiring an address change, set the GPIO0 and/or GPIO1 pins high or low to match the key being used.
3. Write the SLAVE_ADDRESS_KEY bits using Register 0x0D, Bits[15:0] to match the desired function. The allowed keys are shown in Table 42.
4. Write to the desired SLAVE_ADDRESS bits using Register 0x09, Bits[7:1]. While writing to Register 0x09, Bits[7:1], write 0xAD to Register 0x09, Bits[15:8] (ADDRESS_WRITE_KEY). Register 0x09 must be written to immediately after writing to Register 0x0D.
5. Repeat Step 1 to Step 4 for all the devices that need SLAVE_ADDRESS changed.
6. Set the GPIO0 and GPIO1 pins as desired for normal operation using the new SLAVE_ADDRESS for each device.

I²C Write and Read Operations

Figure 32 shows the ADPD1080 I²C write and read operations. Single-word and multiword read operations are supported. For a single register read, the host sends a no acknowledge (NACK) after the second data byte is read and a new register address is needed for each access.

For multiword operations, each pair of data bytes is followed by an acknowledge from the host until the last byte of the last word is read. The host indicates the last read word by sending a no acknowledge. When reading from the FIFO_ACCESS (Register 0x60), the data is automatically advanced to the next word in the FIFO, and the space is freed. When reading from other registers, the register address is automatically advanced to the next register, except at Register 0x5F (DATA_ACCESS_CTL) or Register 0x7F (B_PD4_HIGH), where the address does not increment. This auto-incrementing allows lower overhead reading of sequential registers.

All register writes are single word only and require 16 bits (one word) of data.

The software reset, SW_RESET (Register 0x0F, Bit 0), returns an acknowledge. The device then returns to standby mode with all registers in the default state.

Table 19. Definitions of I²C Terminology

Term	Description
SCL	Serial clock.
SDA	Serial address and data.
Master	The master is the device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The slave is the device addressed by a master. The ADPD1080 operates as a slave device.
Start (S)	A high to low transition on the SDA line while SCL is high; all transactions begin with a start condition.
Start (Sr)	Repeated start condition.
Stop (P)	A low to high transition on the SDA line while SCL is high. A stop condition terminates all transactions.
ACK	During the acknowledge or no acknowledge clock pulse, the SDA line is pulled low and remains low.
NACK	During the acknowledge or no acknowledge clock pulse, the SDA line remains high.
Slave Address	After a start (S), a 7-bit slave address is sent, which is followed by a data direction bit (read or write).
Read (R)	A 1 indicates a request for data.
Write (W)	A 0 indicates a transmission.

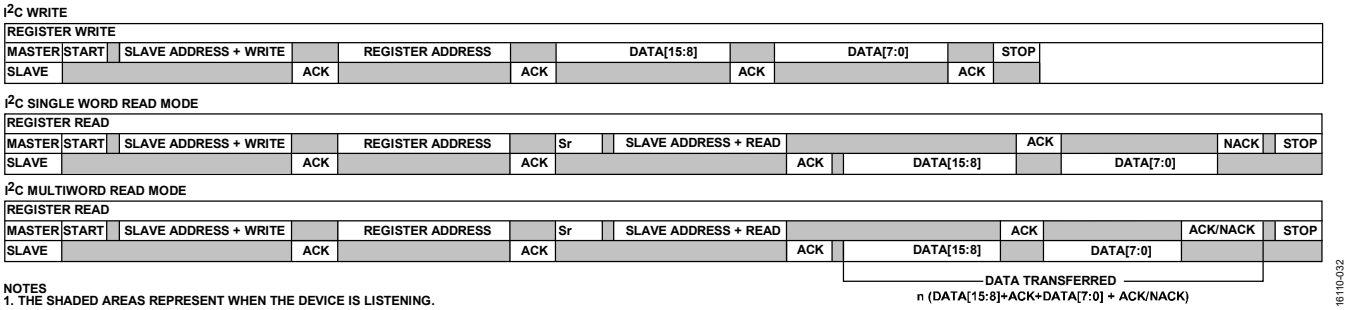

Figure 32. I²C Write and Read Operations

SPI PORT

The ADPD1081 is a SPI only device. It does not support the I²C interface. The SPI port uses a 4-wire interface, consisting of the $\overline{CS}$, MOSI, MISO, and SCLK signals, and it is always a slave port. The $\overline{CS}$ signal goes low at the beginning of a transaction and high at the end of a transaction. The SCLK signal latches MOSI on a low to high transition. The MISO data is shifted out of the device on the falling edge of SCLK and must be clocked into a receiving device, such as a microcontroller, on the SCLK rising edge. The MOSI signal carries the serial input data, and the MISO signal carries the serial output data. The MISO signal remains three state until a read operation is requested, which allows other SPI-compatible peripherals to share the same MISO line. All SPI transactions have the same basic format shown in Table 20. A timing diagram is shown in Figure 4. Write all data MSB first.

Table 20. Generic Control Word Sequence

Byte 0	Byte 1	Byte 2	Subsequent Bytes
Address[6:0], W/$\overline{R}$	Data[15:8]	Data[7:0]	Data[15:8], Data[7:0]

The first byte written in a SPI transaction is a 7-bit address, which is the location of the address being accessed, followed by the W/$\overline{R}$ bit. This bit determines whether the communication is a write (Logic Level 1) or a read (Logic Level 0). This format is shown in Table 21.

Table 21. SPI Address and Write/$\overline{R}$ Byte Format

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
A6	A5	A4	A3	A2	A1	A0	W/$\overline{R}$

Data on the MOSI pin is captured on the rising edge of the clock, and data is propagated on the MISO pin on the falling edge of the clock. The maximum read and write speed for the SPI slave port is 10 MHz. See Figure 4 for the SPI timing diagram, and see Table 7 for the SPI timing specifications.

A sample timing diagram for a multiple word SPI write operation to a register is shown in Figure 33. A sample timing diagram of a single-word SPI read operation is shown in Figure 34. The MISO pin transitions from being three-state to being driven following the reception of a valid $\overline{R}$ bit. In this example, Byte 0 contains the address and the W/$\overline{R}$ bit and subsequent bytes carry the data. A sample timing diagram of a multiple word SPI read operation is shown in Figure 35. In Figure 33 to Figure 35, rising edges on SCLK are indicated with an arrow, signifying that the data lines are sampled on the rising edge.

When performing multiple word reads or writes, the data address is automatically incremented to the next consecutive address for subsequent transactions except for Address 0x5F (DATA_ACCESS_CTL), Address 0x60 (FIFO_ACCESS), and Address 0x7F (B_PD4_HIGH).

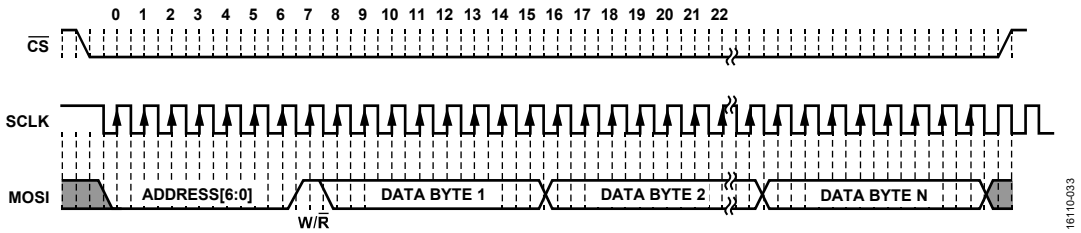

Figure 33. SPI Slave Write Clocking (Burst Write Mode, N Bytes)

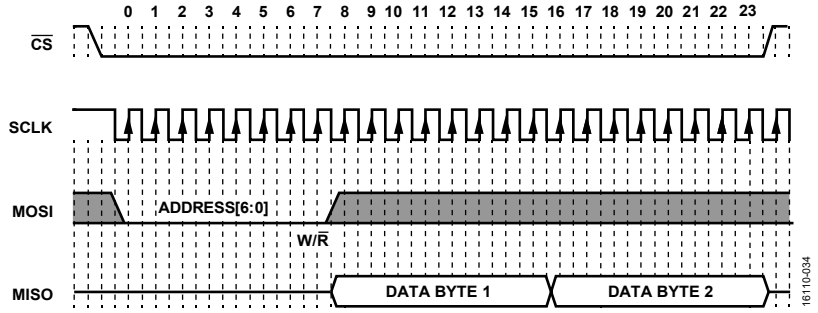

Figure 34. SPI Slave Read Clocking (Single-Word Mode, Two Bytes)

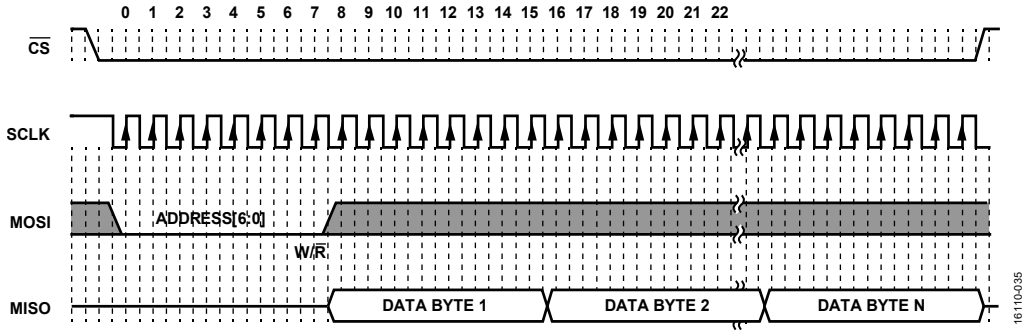

Figure 35. SPI Slave Read Clocking (Burst Read Mode, N Bytes)

APPLICATIONS INFORMATION

TYPICAL CONNECTION DIAGRAM

Figure 36 shows a typical circuit used for wrist-based heart rate measurement with the ADPD1080 WLCSP using a green LED. The 1.8 V I²C communication lines, SCL and SDA, along with the GPIO0 and GPIO1 lines, connect to a system microprocessor or sensor hub. The I²C signals can have pull-up resistors connected to a 1.8 V or a 3.3 V power supply. The GPIO0 and GPIO1 signals are only compatible with a 1.8 V supply and may need a level translator. The circuit shown in Figure 36 is identical for the ADPD1081, except the I²C interface is replaced by an SPI. There are multiple ways to connect photodiodes to the 8-channel ADPD1080 LFCSP, as shown in Table 22 and Figure 39. The photodiode anodes are connected to the PD1 to PD8 input pins and the photodiode cathodes are connected to the cathode pin, PDC.

Provide the 1.8 V supply, V_{DD}, to AVDD and DVDD. The LED supply uses a standard regulator circuit according to the peak current requirements specified in Table 3 and calculated in the LED Driver Pins and LED Supply Voltage section.

For best noise performance, connect AGND, DGND, and LGND together at a large conductive surface, such as a ground plane, a ground pour, or a large ground trace.

The number of photodiodes or LEDs used varies depending on the application as well as the dynamic range and SNR required. For example, when using a single, large photodiode in an application, split the current between multiple inputs to increase the dynamic range. By connecting the anode of the photodiode to multiple channels, the current can split evenly among the number of channels connected, effectively increasing the dynamic range over a single channel configuration. Alternatively, in situations where the photodiode is small or the signal is greatly attenuated, SNR can be maximized by connecting the anode of the photodiode to a single channel. It is important to leave the unused input floating for proper device operation.

Figure 37 and Figure 38 show the recommended connection diagram and printed circuit board (PCB) layout for the 16-ball WLCSP ADPD1080 and 17-ball WLCSP ADPD1081, respectively. The current input pins, PD1 and PD5, have a typical voltage of 1.3 V during the sampling period. During the sleep period, these pins are connected to the cathode pin. The cathode and anode voltages are listed in Table 3.

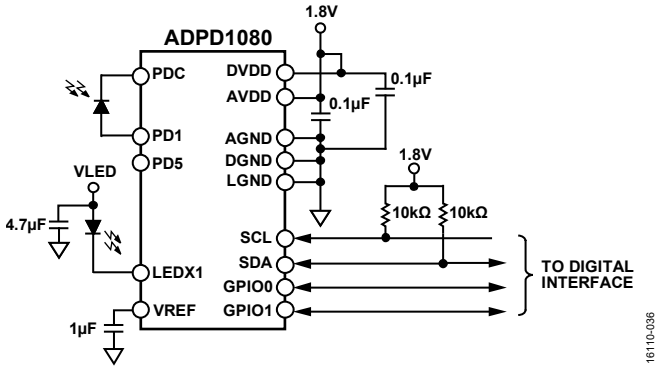

Figure 36. Typical Wrist-Based HRM Measurement

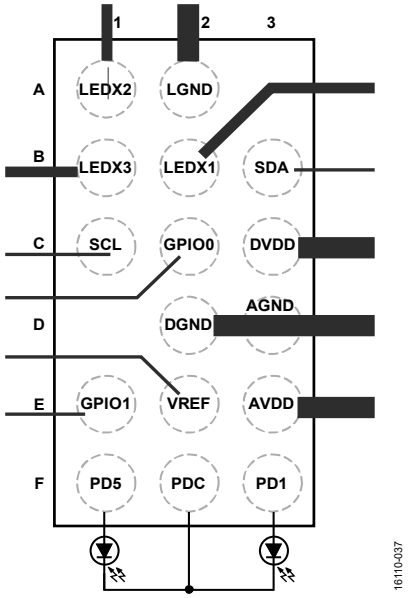

Figure 37. ADPD1080 Connection and PCB Layout Diagram (Top View), 16-Ball WLCSP

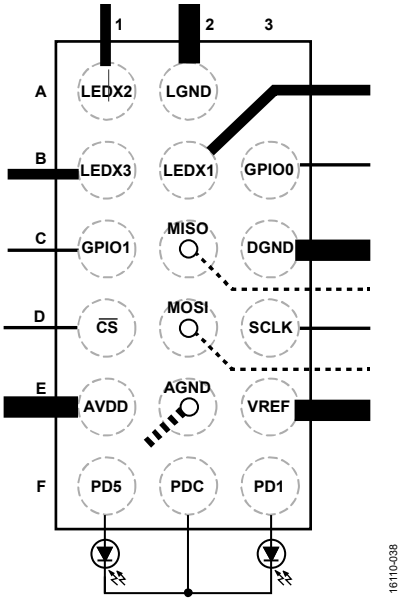

Figure 38. ADPD1081 Connection and PCB Layout Diagram, Dashed Line Traces from Blind Vias (Top View), 16-Ball WLCSP

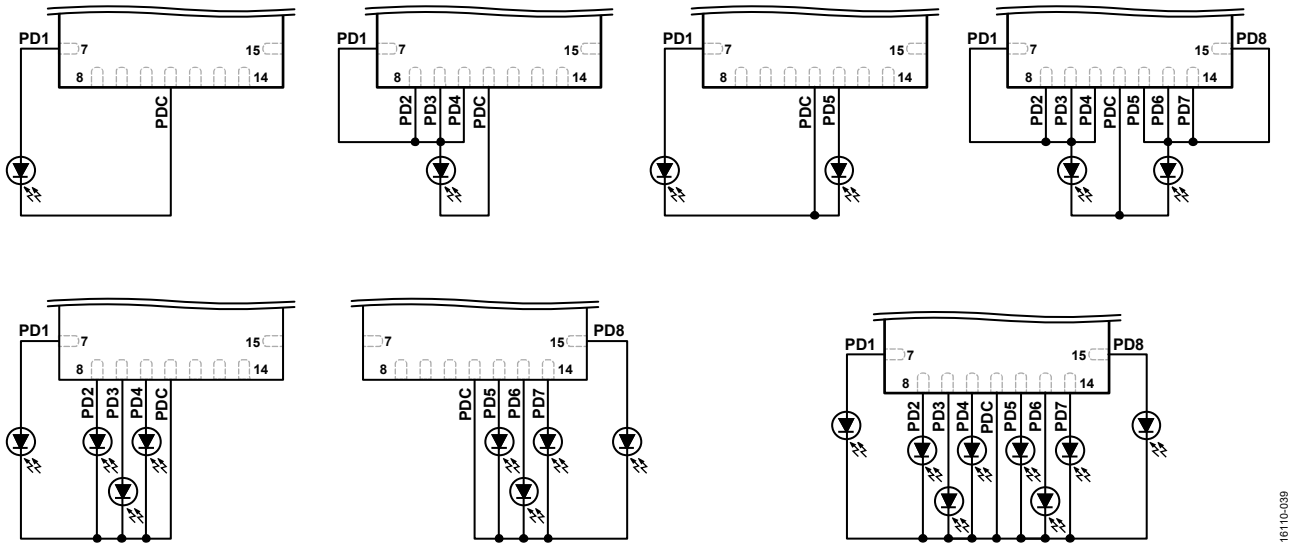

Figure 39. Photodiode Configuration Options for the ADPD1080 LFCSP

Table 22. Typical Photodiode Anode to Input Channel Connections for the ADPD1080 LFCSP[1, 2]

	Input Channel							
Photodiode Anode Configuration	**PD1**	**PD2**	**PD3**	**PD4**	**PD5**	**PD6**	**PD7**	**PD8**
Single Photodiode (PD1)	D1	NC	NC	NC	NC	NC	NC	NC
	NC	NC	NC	NC	D1	NC	NC	NC
	D1	D1	D1	D1	NC	NC	NC	NC
	NC	NC	NC	NC	D1	D1	D1	D1
Two Photodiodes (PD1, PD2)	D1	NC	NC	NC	D2	NC	NC	NC
	D1	D1	D1	D1	D2	D2	D2	D2
Four Photodiodes (PD1 to PD4)	D1	D2	D3	D4	NC	NC	NC	NC
	NC	NC	NC	NC	D1	D2	D3	D4
Eight Photodiodes (PD1 to PD8)	D1	D2	D3	D4	D5	D6	D7	D8

[1] Dx refers to the diode connected to the specified channel.
[2] NC means do not connect. Leave all unused inputs floating.

LED DRIVER PINS AND LED SUPPLY VOLTAGE

The LEDX1, LEDX2, and LEDX3 pins have an absolute maximum voltage rating of 3.6 V. Any voltage exposure over this rating affects the reliability of the device operation and, in certain circumstances, causes the device to cease proper operation. The voltage of the LEDx pins must not be confused with the supply voltages for the LED themselves. V_{LEDx} is the voltage applied to the anode of the external LED, whereas the LEDXx pin is the input of the internal current driver, and the pins are connected to the cathode of the external LED.

LED DRIVER OPERATION

The LED driver for the ADPD1080/ADPD1081 is a current sink. The compliance voltage, measured at the driver pin with respect to ground, required to maintain the programmed LED current level is a function of the current required. Figure 12 shows the typical compliance voltages required at the various LED coarse settings. Figure 40 shows the basic schematic of how the ADPD1080/ADPD1081 connect to an LED through the LED driver. The Determining the Average Current section and the Determining C_{VLED} section define the requirements for the bypass capacitor (C_{VLED}) and the supply voltages of the LEDs (V_{LEDx}).

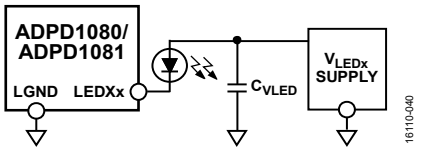

Figure 40. V_{LEDx} Supply Schematic

DETERMINING THE AVERAGE CURRENT

The ADPD1080/ADPD1081 drive an LED in a series of short pulses. Figure 41 shows the typical ADPD1080/ADPD1081 configuration of an LED pulse burst sequence.

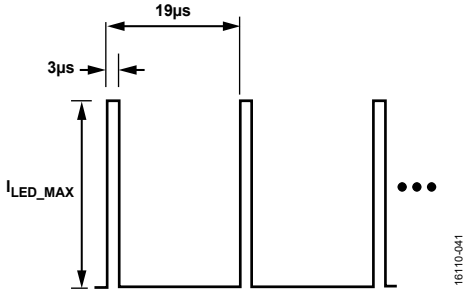

Figure 41. Typical LED Pulse Burst Sequence Configuration

In this example, the LED pulse width, t_{LED_PULSE}, is 3 µs, and the LED pulse period, t_{LED_PERIOD}, is 19 µs. The LED being driven is a pair of green LEDs driven to a 250 mA peak. The goal of C_{VLED} is to buffer the LED between individual pulses. In the worst case scenario, where the pulse train shown in Figure 41 is a continuous sequence of short pulses, the V_{LEDx} supply must supply the average current. Therefore, calculate $I_{LED\_AVERAGE}$ as follows:

$$I_{LED\_AVERAGE} = (t_{LED\_PULSE}/t_{LED\_PERIOD}) \times I_{LED\_MAX} \quad (1)$$

where:

$I_{LED\_AVERAGE}$ is the average current needed from the V_{LEDx} supply during the pulse period, and it is also the V_{LEDx} supply current rating.

I_{LED_MAX} is the peak current setting of the LED.

For the values shown in Equation 1, $I_{LED\_AVERAGE} = 3/19 \times I_{LED\_MAX}$. For typical LED timing, the average V_{LEDx} supply current is 3/19 × 250 mA = 39.4 mA, indicating that the V_{LEDx} supply must support a dc current of 40 mA.

DETERMINING C_{VLED}

To determine the C_{VLED} capacitor value, determine the maximum forward-biased voltage, $V_{FB\_LED\_MAX}$, of the LED in operation. The LED current, I_{LED_MAX}, converts to $V_{FB\_LED\_MAX}$ as shown in Figure 42. In this example, 250 mA of current through two green LEDs in parallel yields $V_{FB\_LED\_MAX}$ = 3.95 V. Any series resistance in the LED path must also be included in this voltage. When designing the LED path, keep in mind that small resistances can add up to large voltage drops due to the LED peak current being large. In addition, these resistances can be unnecessary constraints on the V_{LEDx} supply.

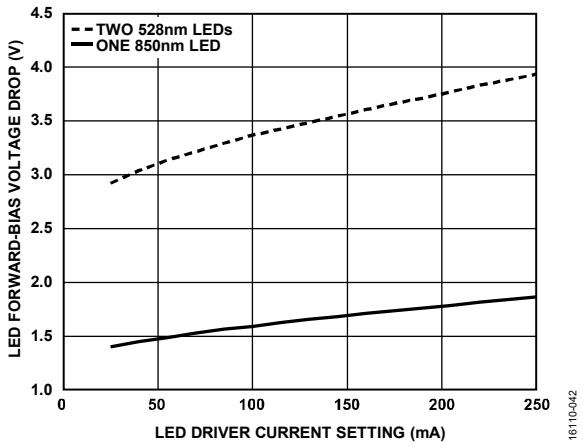

Figure 42. Example of the Average LED Forward-Bias Voltage Drop as a Function of the LED Driver Current Setting

To correctly size the C_{VLED} capacitor, do not deplete it during the pulse of the LED to the point where the voltage on the capacitor is less than the forward bias on the LED. Calculate the minimum value for the VLEDx bypass capacitor by

$$C_{VLED} = \frac{t_{LED\_PULSE} \times I_{LED\_MAX}}{V_{LED\_MIN} - \left(V_{FB\_LED\_MAX} + 0.6\right)} \quad (2)$$

where:

t_{LED_PULSE} is the LED pulse width.

I_{LED_MAX} is the maximum forward-biased current on the LED used in operating the devices.

V_{LED_MIN} is the lowest voltage from the V_{LEDx} supply with no load.

$V_{FB\_LED\_MAX}$ is the maximum forward-biased voltage required on the LED to achieve I_{LED_MAX}.

The numerator of the C_{VLED} equation sets up the total discharge amount in coulombs from the bypass capacitor to satisfy a single programmed LED pulse of the maximum current. The denominator represents the difference between the lowest voltage from the V_{LEDx} supply and the LED required voltage. The LED required voltage is the voltage of the anode of the LED such that the compliance of the LED driver and the forward-biased voltage of the LED operating at the maximum current is satisfied. At a 250 mA drive current, the compliance voltage of the driver is 0.6 V. For a typical ADPD1080 example, assume that the lowest value for the V_{LEDx} supply is 4.75 V and that the peak current is 250 mA for two 528 nm LEDs in parallel. The minimum value for C_{VLED} is then equal to 3.75 µF.

$$C_{VLED} = (3 \times 10^{-6} \times 0.250)/(4.75 - (3.95 + 0.6)) = 3.75\ \mu F \quad (3)$$

As shown in Equation 3, as the minimum supply voltage drops close to the maximum anode voltage, the demands on C_{VLED} become more stringent, forcing the capacitor value higher. It is important to insert the correct values into Equation 1, Equation 2, and Equation 3. For example, using an average value for V_{LED_MIN} instead of the worst case value for V_{LED_MIN} can cause a serious design deficiency, resulting in a C_{VLED} value that is too small and that causes insufficient optical power in the application.

Therefore, adding a sufficient margin on C_{VLED} is strongly recommended. Add additional margin to C_{VLED} to account for derating of the capacitor value over voltage, bias, temperature, and other factors over the life of the component.

LED INDUCTANCE CONSIDERATIONS

The LED drivers (LEDXx) on the ADPD1080/ADPD1081 have configurable slew rate settings (Register 0x22, Bits[6:4], Register 0x23, Bits[6:4], and Register 0x24, Bits[6:4]). These slew rates are defined in Table 3. Even at the lowest setting, carefully consider board design and layout. If a large series inductor, such as a long PCB trace, is placed between the LED cathode and one of the LEDXx pins, voltage spikes from the switched inductor can cause violations of absolute maximum and minimum voltages on the LEDXx pins during the slew portion of the LED pulse.

To verify that there are no voltage spikes on the LEDXx pins due to parasitic inductance, use an oscilloscope on the LEDXx pins to monitor the voltage during normal operation. Any positive spike >3.6 V may damage the devices.

In addition, a negative spike less than −0.3 V may also damage the devices.

RECOMMENDED START-UP SEQUENCE

At power-up, the device is in standby mode (Register 0x10 = 0x0000), as shown in Figure 27. The ADPD1080/ADPD1081 do not require a particular power-up sequence.

From standby mode, to begin measurement, initiate the ADPD1080/ADPD1081 as follows:

1. Set the CLK32K_EN bit (Register 0x4B, Bit 7) to start the sample clock (32 kHz clock). This clock controls the state machine. If this clock is off, the state machine is not able to transition as defined by Register 0x10.
2. Write 0x1 to Register 0x10 to force the device into program mode. Step 1 and Step 2 can be swapped, but the actual state transition does not occur until both steps occur.
3. Write additional control registers in any order while the device is in program mode to configure the devices as required.
4. Write 0x2 to Register 0x10 to start normal sampling operation.

To terminate normal operation, follow this sequence to place the ADPD1080/ADPD1081 in standby mode:

1. Write 0x1 to Register 0x10 to force the devices into program mode.
2. Write to the registers in any order while the devices are in program mode.
3. Write 0x00FF to Register 0x00 to clear all interrupts. If desired, clear the FIFO as well by writing 0x80FF to Register 0x00.
4. Write 0x0 to Register 0x10 to force the devices into standby mode.
   Optionally, stop the 32 kHz clock by resetting the CLK32K_EN bit (Register 0x4B, Bit 7). Register 0x4B, Bit 7 = 0 is the only write that must be written when the device is in standby mode (Register 0x10 = 0x0). If 0 is written to this bit while in program mode or normal mode, the devices become unable to transition into any other mode, including standby mode, even if they are subsequently written to do so. As a result, the power consumption in what appears to be standby mode is greatly elevated. For this reason, and due to the low current draw of the 32 kHz clock while in operation, it is recommended from an ease of use perspective to keep the 32 kHz clock running after it is turned on.

READING DATA

The ADPD1080/ADPD1081 provide multiple methods for accessing the sample data. Each time slot can be independently configured to provide data access using the FIFO or the data registers. Interrupt signaling is also available to simplify timely data access. The FIFO is available to loosen the system timing requirements for data accesses.

Reading Data Using the FIFO

The ADPD1080/ADPD1081 include a 128-byte FIFO memory buffer that can store data from either or both time slots. Register 0x11 selects the kind of data from each time slot to be written to the FIFO. Note that both time slots can use the FIFO, but only if their output data rate is the same.

$$Output\ Data\ Rate = f_{SAMPLE}/N_X$$

where:
f_{SAMPLE} is the sampling frequency.
N_X is the averaging factor for each time slot (N_A for Time Slot A and N_B for Time Slot B). In other words, $N_A = N_B$ must be true to store data from both time slots in the FIFO.

Data packets are written to the FIFO at the output data rate. A data packet for the FIFO consists of a complete sample for each enabled time slot. Data for each photodiode channel can be stored as either 16 or 32 bits. Each time slot can store 2, 4, 8, or 16 bytes of data per sample, depending on the mode and data format. To ensure that data packets are intact, new data is only written to the FIFO if there is sufficient space for a complete packet. Any new data that arrives when there is not enough space is lost. The FIFO continues to store data when sufficient space exists. Always read FIFO data in complete packets to ensure that data packets remain intact.

The number of bytes currently stored in the FIFO is available in Register 0x00, Bits[15:8]. A dedicated FIFO interrupt is also available and automatically generates when a specified amount of data is written to the FIFO.

Interrupt-Based Method

To read data from the FIFO using an interrupt-based method, use the following procedure:

1. In program mode, set the configuration of the time slots as desired for operation.
2. Write to Register 0x11 with the desired data format for each time slot.
3. Set FIFO_THRESH in Register 0x06, Bits[13:8] to the interrupt threshold. A recommended value for this is the number of 16-bit words in a data packet minus 1, which causes an interrupt to generate when there is at least one complete packet in the FIFO.
4. Enable the FIFO interrupt by writing 0 to the FIFO_INT_MASK in Register 0x01, Bit 8. Also, configure the interrupt pin (GPIO0 or GPIO1) by writing the appropriate value to the bits in Register 0x02.
5. Enter normal operation mode by setting Register 0x10 to 0x2.
6. When an interrupt occurs,
   a. There is no requirement to read the FIFO_SAMPLES bits because the interrupt is generated only if there is one or more full packets. Optionally, the interrupt routine can check for the presence of more than one available packet by reading these bits.
   b. Read a complete packet using one or more multiword accesses using Register 0x60. Reading the FIFO automatically frees the space for new samples.

The FIFO interrupt automatically clears immediately upon reading any data from the FIFO and is set again only when the FIFO is written and the number of words is more than the threshold.

Polling Method

To read data from the FIFO in a polling method, use the following procedure:

1. In program mode, set the configuration of the time slots as desired for operation.
2. Write to Register 0x11 with the desired data format for each time slot.
3. Enter normal operation mode by setting Register 0x10 to 2.

Next, begin the polling operations.

1. Wait for the polling interval to expire.
2. Read the FIFO_SAMPLES bits (Register 0x00, Bits[15:8]).
3. If FIFO_SAMPLES ≥ the packet size, read a packet using the following steps:
   a. Read a complete packet using one or more multiword accesses via Register 0x60. Reading the FIFO automatically frees the space for new samples.
   b. Repeat Step 1.

When a mode change is required, or any other disruption to normal sampling is necessary, clear the FIFO. Use the following procedure to clear the state and empty the FIFO:

1. Enter program mode by setting Register 0x10 to 0x1.
2. Write 1 to Register 0x00, Bit 15.

Reading Data from Registers Using Interrupts

The latest sample data is always available in the data registers and is updated simultaneously at the end of each time slot. The data value for each photodiode channel is available as a 16-bit value in Register 0x64 through Register 0x67 for Time Slot A, and Register 0x68 through Register 0x6B for Time Slot B. If allowed to reach their maximum value, Register 0x64 through Register 0x6B clip. If Register 0x64 through Register 0x6B saturate, the unsaturated (up to 27 bits) values for each channel are available in Register 0x70 through Register 0x77 for Time Slot A and Register 0x78 through Register 0x7F for Time Slot B. Sample interrupts are available to indicate when the registers are updated and can be read. To use the interrupt for a given time slot, use the following procedure:

1. Enable the sample interrupt by writing a 0 to the appropriate bit in Register 0x01. To enable the interrupt for Time Slot A, write 0 to Bit 5. To enable the interrupt for Time Slot B, write 0 to Bit 6. Either or both interrupts can be set.
2. Configure the interrupt pin (GPIOx) by writing the appropriate value to the bits in Register 0x02.
3. An interrupt generates when the data registers are updated.
4. The interrupt handler must perform the following:
   a. Read Register 0x00 and observe Bit 5 or Bit 6 to confirm which interrupt occurred. This step is not required if only one interrupt is in use.
   b. Read the data registers before the next sample can be written. The system must have interrupt latency and service time short enough to respond before the next data update, based on the output data rate.
   c. Write a 1 to Bit 5 or Bit 6 in Register 0x00 to clear the interrupt.

If both time slots are in use, it is possible to use only the Time Slot B interrupt to signal when all registers can be read. It is recommended to use the multiword read to transfer the data from the data registers.

Reading Data from Registers Without Interrupts

If the system interrupt response is not fast or predictable enough to use the interrupt method, or if the interrupt pin (GPIOx) is not used, it is possible to obtain reliable data access by using the data hold mechanism. To guarantee that the data read from the registers is from the same sample time, it is necessary to prevent the update of samples while reading the current values. The method for performing register reads without interrupt timing is as follows:

1. Write 1 to the SLOTA_DATA_HOLD or SLOTB_DATA_HOLD bits (Register 0x5F, Bit 1 and Bit 2, respectively) for the time slot requiring access (both time slots can be accessed). This setting prevents sample updates.
2. Read the registers as desired.

3. Write 0 to the SLOTA_DATA_HOLD or SLOTB_DATA_HOLD bits (Register 0x5F, Bit 1 and Bit 2, respectively) previously set. Sample updates are allowed again.

Because a new sample may arrive while the reads are occurring, this method prevents the new sample from partially overwriting the data being read.

CLOCKS AND TIMING CALIBRATION

The ADPD1080/ADPD1081 operate using two internal time bases: a 32 kHz clock sets the sample timing, and a 32 MHz clock controls the timing of the internal functions, such as LED pulsing and data capture. Both clocks are internally generated and exhibit device to device variation of approximately 10% (typical).

Heart rate monitoring applications require an accurate time base to achieve an accurate count of beats per minute. The ADPD1080/ADPD1081 provide a simple calibration procedure for both clocks.

Calibrating the 32 kHz Clock

Calibrating the 32 kHz clock also calibrates items associated with the output data rate. Calibration of this clock is important for applications where an accurate data rate is important, such as heart rate measurements.

To calibrate the 32 kHz clock,

1. Set the sampling frequency to the highest the system can handle, such as 2000 Hz. Because the 32 kHz clock controls sample timing, its frequency is readily accessible via the GPIO0 pin. Configure the interrupt by writing the appropriate value to the bits in Register 0x02 and set the interrupt to occur at the sampling frequency by writing 0 to Register 0x01, Bit 5 or Bit 6. Monitor the GPIO0 pin. The interrupt frequency must match the set sample frequency.
2. If the monitored interrupt frequency is less than the set sampling frequency, decrease the CLK32K_ADJUST bit (Register 0x4B, Bits[5:0]). If the monitored interrupt frequency is larger than the set sampling frequency, increase the CLK32K_ADJUST bits.
3. Repeat Step 1 and Step 2 until the monitored interrupt signal frequency is close enough to the set sampling frequency.

After the 32 kHz oscillator calibration completes, set the GPIO0 pin to the mode desired for normal operation.

Calibrating the 32 MHz Clock

Calibrating the 32 MHz clock also calibrates items associated with the fine timing within a sample period, such as LED pulse width and spacing, assuming that the 32 kHz clock is calibrated.

To calibrate the 32 MHz clock, the 32 kHz clock must first be calibrated as previously described. Always start this routine with Register 0x4D set to 0x98, which is the default value at power-up.

1. Write 0x1 to Register 0x5F, Bit 0 (DIGITAL_CLOCK_ENA) to enable the 32 MHz oscillator.
2. Enable the CLK_RATIO calculation by writing 0x1 to Register 0x50, Bit 5 (CLK32M_CAL_EN). This function counts the number of 32 MHz clock cycles in two cycles of the 32 kHz clock. With this function enabled, this cycle value is stored in Register 0x0A, Bits[11:0] and nominally this ratio is 2000 (0x7D0).
3. Calculate the 32 MHz clock error as follows:

   $Clock\ Error = 32\ MHz \times (1 - CLK\_RATIO/2000)$
4. Adjust the frequency of the 32 MHz oscillator by adjusting the setting of Bits[7:0] in Register 0x4D by the amount calculated in the following equation:

   $CLK32M\_ADJUST = Clock\ Error/112\ kHz$
5. Write 0x0 to Register 0x50, Bit 5 (CLK32M_CAL_EN) to reset the CLK_RATIO function.

Repeat Step 2 through Step 5 until the desired accuracy is achieved.

Write 0x0 to Register 0x5F, Bit 0 to disable the 32 MHz oscillator.

OPTIONAL TIMING SIGNALS AVAILABLE ON GPIO0 AND GPIO1

The ADPD1080/ADPD1081 provide a number of different timing signals, available via the GPIO0 and GPIO1 pins, to enable ease of system synchronization and flexible triggering options. Each GPIOx pin can be configured as an open-drain output if the pins are to share the bus with other drivers, or the pins can be configured to always drive the bus. Both outputs also have polarity control in situations where a timing signal must be inverted from the default.

Table 23. GPIOx Control Settings

Mnemonic	Register, Bit	Setting Description
GPIO0	0x02, Bit 0	0: polarity active high 1: polarity active low
	0x02, Bit 1	0: always drives the bus 1: drives the bus when asserted
	0x02, Bit 2	0: disables the GPIO0 pin drive 1: enables the GPIO0 pin drive
GPIO1	0x02, Bit 8	0: polarity active high 1: polarity active low
	0x02, Bit 9	0: always drives the bus 1: drives the bus when asserted
	0x4F, Bit 6	0: disables the GPIO1 pin drive 1: enables the GPIO1 pin drive

The various available timing signals are controlled by the settings in Register 0x0B. Bits[12:8] of this register control the timing signals available on GPIO1, and Bits[4:0] control the timing signals available on GPIO0. All of the timing signals described in this data sheet are available on either (or both) of the GPIO0 and GPIO1 pins. Timing diagrams are shown in Figure 43 and Figure 44. The time slot settings used to generate the timing diagrams are described in Table 24.

Table 24. ADPD1080/ADPD1081 Settings Used for Timing Diagrams Shown in Figure 43 and Figure 44

Register	Setting	Description
0x31	0x0118	Time Slot A: 1 LED pulse
0x36	0x0418	Time Slot B: 4 LED pulses
0x15	0x0120	Time Slot A decimation = 4, Time Slot B decimation = 2

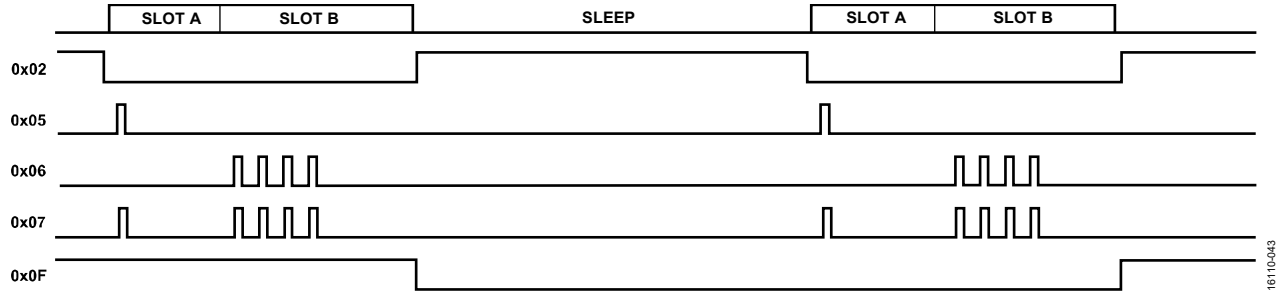

Figure 43. Optional Timing Signals Available on GPIOx—Register 0x0B, Bits[12:8] or Bits[4:0] = 0x02, 0x05, 0x06, 0x07, and 0x0F

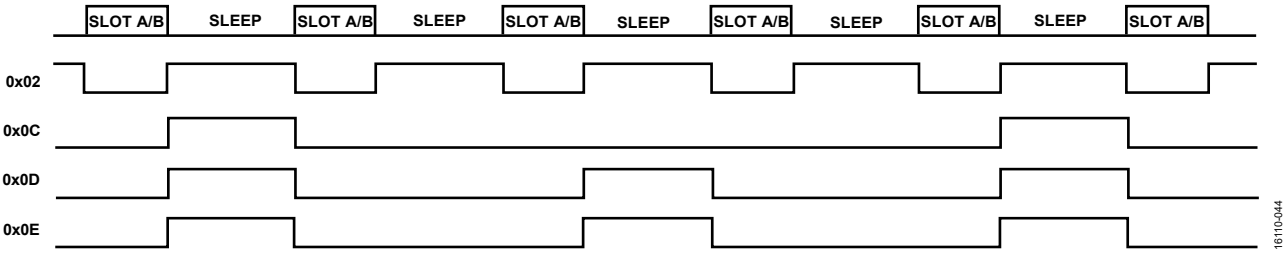

Figure 44. Optional Timing Signals Available on GPIOx—Register 0x0B, Bits[12:8] or Bits[4:0] = 0x02, 0x0C, 0x0D, and 0x0E

ADPD103 Backward Compatibility

Setting Register 0x0B = 0 provides backward compatibility to the ADPD103. The GPIO0 pin mirrors the functionality of the ADPD103 INT pin. The GPIO1 pin mirrors the functionality of the ADPD103 PDSO pin.

Interrupt Function

Setting Register 0x0B, Bits[12:8] or Bits[4:0] = 0x01 configures the respective pin to perform the interrupt function as defined by the settings in Register 0x01.

Sample Timing

Setting Register 0x0B, Bits[12:8] or Bits[4:0] = 0x02 configures the respective pin to provide a signal that asserts at the beginning of the first time slot of the current sample and deasserts at the end of the last time slot of the current sample. For example, if both time slots are enabled, this signal asserts at the beginning of Time Slot A and deasserts at the end of Time Slot B. If only a single time slot is enabled, the signal asserts at the beginning of the enabled time slot and deasserts at the end of this same time slot.

Pulse Outputs

Three options are available to provide a copy of the LED pulse outputs. Setting Register 0x0B, Bits[12:8] or Bits[4:0] = 0x05 provides a copy of the Time Slot A LED pulses on the respective pin. A setting of 0x06 provides the Time Slot B pulses, and a setting of 0x07 provides the pulse outputs of both time slots.

Output Data Cycle Signal

Three options are available to provide a signal that indicates when the output data is written to the output data registers or to the FIFO. Setting Register 0x0B, Bits[12:8] or Bits[4:0] = 0x0C provides a signal that indicates that a data value is written for Time Slot A. A setting of 0x0D provides a signal that indicates that a data value is written for Time Slot B, and a setting of 0x0E provides a signal to indicate that a value is written for either time slot. The signal asserts at the end of the time slot, when the output data is already written, and deasserts at the start of the subsequent sample. This timing signal is especially useful in situations where the FIFO is used. For example, one of the GPIOx pins can provide an interrupt after the FIFO reaches the FIFO threshold set in Register 0x06, Bits[13:8], while the other GPIOx pin can provide the output data cycle signal. This signal can trigger a peripheral device, such as an accelerometer, so that time aligned signals are provided to the processor.

$f_S/2$ Output

Setting Register 0x0B, Bits[12:8] or Bits[4:0] = 0x0F configures the respective pin to provide a signal that toggles at half the sampling rate. This timing signal is useful in, for example, situations where more than two LEDs per sample are required. This signal can be used as a select signal to a multiplexer being used to mux two LEDs into a single LED driver, providing the

ability to drive up to four separate LEDs per sample period. In such a case, the ADPD1080/ADPD1081 operate at 2× the sampling rate, and the LED settings can be reconfigured during the sleep period between samples. If identical LED settings (current and timing) are used for the LEDs being muxed, up to four LEDs can be sampled per sampling period without host intervention. An example of this configuration is shown in Figure 45.

The $f_S/2$ timing signal always starts in an active low state when the device switches from standby mode to normal operating mode and transitions to a high state at the completion of the first sample.

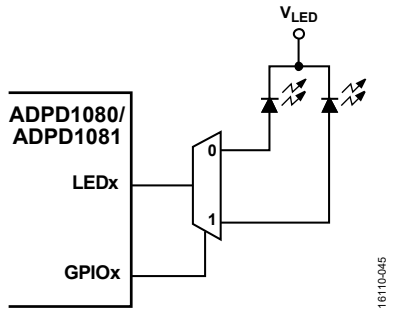

Figure 45. Example Using the $f_S/2$ Timing Signal

Logic 0 Output

Setting Register 0x0B, Bits[12:8] or Bits[4:0] = 0x10 configures the respective pin to provide a Logic 0 output.

Logic 1 Output

Setting Register 0x0B, Bits[12:8] or Bits[4:0] = 0x11 configures the respective pin to provide a Logic 1 output.

32 kHz Oscillator Output

Setting Register 0x0B, Bits[12:8] or Bits[4:0] = 0x13 configures the respective pin to provide a copy of the on-board 32 kHz oscillator.

CALCULATING CURRENT CONSUMPTION

The current consumption of the ADPD1080/ADPD1081 depends on the user selected operating configuration, as determined by the following equations.

Total Power Consumption

To calculate the total power consumption, use Equation 4.

$$Total\ Power = I_{VDD\_AVG} \times V_{DD} + I_{LEDA\_AVG} \times V_{LEDA} + I_{LEDB\_AVG} \times V_{LEDB} \quad (4)$$

Average V_{DD} Supply Current

To calculate the average V_{DD} supply current, use Equation 5.

$$I_{VDD\_AVG} = DR \times ((I_{AFE\_A} \times t_{SLOTA}) + (I_{AFE\_B} \times t_{SLOTB}) + Q_{PROC\_X}) + I_{VDD\_STANDBY} \quad (5)$$

where:
DR is the data rate in Hz.
$I_{VDD\_STANDBY}$ = 0.2 µA.
Q_{PROC_X} is an average charge associated with a processing time.

When only Time Slot A is enabled,

$$Q_{PROC\_A}\ (C) = 0.35 \times 10^{-6}$$

When only Time Slot B is enabled,

$$Q_{PROC\_B}\ (C) = 0.24 \times 10^{-6}$$

When Time Slot A and Time Slot B are enabled,

$$Q_{PROC\_AB}\ (C) = 0.40 \times 10^{-6}$$

$$I_{AFE\_x}\ (A) = 3.0 \times 10^{-3} + (1.5 \times 10^{-3} \times NUM\_CHANNELS) + (4.6 \times 10^{-3} \times I_{LEDX\_PK}/SCALE\_X) \quad (6)$$

$$t_{SLOTx}\ (sec) = LEDx\_OFFSET + LEDx\_PERIOD \times PULSE\_COUNT \quad (7)$$

where:
NUM_CHANNELS is the number of active channels.
I_{LEDX_PK} is the peak LED current, expressed in amps, for whichever LED is enabled in that particular time slot.
SCALE_X is the scale factor for the LED current drive determined by Bit 13 of the ILEDx_COARSE registers, Register 0x22, Register 0x23, and Register 0x24.
LEDx_OFFSET is the pulse start time offset expressed in seconds.
LEDx_PERIOD is the pulse period expressed in seconds.
PULSE_COUNT is the number of pulses.

If either Time Slot A or Time Slot B are disabled, I_{AFE_x} = 0 for that respective time slot. Additionally, if operating in TIA ADC mode, set Register 0x3C, Bits[8:3] = 010010 to achieve power savings. This setting disables the BPFs that are bypassed in TIA ADC mode, changing the AFE power contribution calculation to

$$I_{AFE\_x}\ (mA) = 3.0 \times 10^{-3} + (1.0 \times 10^{-3} \times NUM\_CHANNELS) + (4.6 \times 10^{-3} \times I_{LEDX\_PK}/SCALE\_X) \quad (8)$$

Average V_{LEDA} Supply Current

To calculate the average V_{LEDA} supply current, use Equation 9.

$$I_{LED\_AVG\_A} = SLOTA\_LED\_WIDTH \times I_{LEDA\_PK} \times DR \times PULSE\_COUNT \quad (9)$$

where:
SLOTA_LED_WIDTH is the LED pulse width expressed in seconds.
I_{LEDA_PK} is the peak current, expressed in amps, for whichever LED is selected for Time Slot A.

Average V_{LEDB} Supply Current

To calculate the average V_{LEDB} supply current, use Equation 10.

$$I_{LED\_AVG\_B} = SLOTB\_LED\_WIDTH \times I_{LEDB\_PK} \times DR \times PULSE\_COUNT \quad (10)$$

where:
SLOTB_LED_WIDTH is the LED pulse width expressed in seconds.
I_{LEDB_PK} is the peak current, expressed in amps, for whichever LED is selected for Time Slot B.

OPTIMIZING SNR PER WATT

The ADPD1080/ADPD1081 offer a variety of adjustable parameters to achieve the best signal. One of the key goals of system performance is to obtain the best system SNR for the lowest total power. This goal is often referred to as optimizing SNR per Watt. Even in systems where only the SNR matters and power is a secondary concern, there may be a lower power or a high power means of achieving the same SNR.

Optimizing for Peak SNR

The first step in optimizing for peak SNR is to find a TIA gain and LED level that gives the best performance where the number of LED pulses remains constant. If peak SNR is the goal, use the noise section of Table 4 as a guide. It is important to note that the SNR improves as a square root of the number of pulses averaged together, whereas the increase in the LED power consumed is directly proportional to the number of LED pulses. In other words, for every doubling of the LED pulse count, there is a doubling of the LED power consumed and a 3 dB SNR improvement. As a result, avoid any change in the gain configuration that provides less than 3 dB of improvement for a 2× power penalty; any TIA gain configuration that provides more than 3 dB of improvement for a 2× power penalty is a suitable choice. If peak SNR is the goal and there is no issue saturating the photodiode with LED current at any gain, the 50 kΩ TIA gain setting is an optimal choice. After the SNR per pulse per channel is optimized, the user can then increase the number of pulses to achieve the desired system SNR.

Optimizing SNR per Watt in a Signal Limited System

In practice, optimizing for peak SNR is not always practical. One scenario in which the PPG signal has a poor SNR is the signal limited regime. In this scenario, the LED current reaches an upper limit before the desired dc return level is achieved.

Tuning in this case starts where the peak SNR tuning stops. The starting point is nominally a 50 kΩ gain, as long as the lowest LED current setting of 8 mA does not saturate the photodiode and the 50 kΩ gain provides enough protection against intense background light. In these cases, use a 25 kΩ gain as the starting point.

The goal of the tuning process is to bring the dc return signal to a specific ADC range, such as 50% or 60%. The ADC range choice is a function of the margin of headroom needed to prevent saturation as the dc level fluctuates over time. The SNR of the PPG waveform is always some percentage of the dc level. If the target level cannot be achieved at the base gain, increase the gain and repeat the procedure. The tuning system may need to place an upper limit on the gain to prevent saturation from ambient signals.

Tuning the Pulse Count

After the LED peak current and TIA gain are optimized, increasing the number of pulses per sample increases the SNR by the square root of the number of pulses. There are two ways to increase the pulse count. The pulse count registers (Register 0x31, Bits[15:8], and Register 0x36, Bits[15:8]) change the number of pulses per internal sample. Register 0x15, Bits[6:4] and Bits[10:8], controls the number of internal samples that are averaged together before the data is sent to the output. Therefore, the number of pulses per sample is the pulse count register multiplied by the number of subsequent samples being averaged. In general, the internal sampling rate increases as the number of internal sample averages increase to maintain the desired output data rate. The SNR/Watt is most optimal with pulse count values of 16 or less. Above pulse count values of 16, the square root relationship does not hold in the pulse count register. However, this relationship continues to hold when averaged between samples using Register 0x15.

Note that increasing LED peak current increases SNR almost directly proportional to LED power, whereas increasing the number of pulses by a factor of n results in only a nominal $\sqrt{(n)}$ increase in SNR.

When using the sample sum or average function (Register 0x15), the output data rate decreases by the number of summed samples. To maintain a static output data rate, increase the sample frequency (Register 0x12) by the same factor as that selected in Register 0x15. For example, for a 100 Hz output data rate and a sample sum or average of four samples, set the sample frequency to 400 Hz.

Applying a Reverse Bias to the Photodiode

The photodiode capacitance contributes to higher noise in the signal path. Applying a reverse bias to the photodiode reduces the capacitance of the photodiode, resulting in better noise performance. To apply a reverse bias to the photodiode, set Register 0x54, Bit 7 to 1. The actual reverse bias is then determined by the settings in Register 0x54, Bits[11:10] for Time Slot B and in Register 0x54, Bits[9:8] for Time Slot A. Set these bits equal to 0x2 applies ~250 mV of reverse bias across the photodiode. There is also an option of setting the cathode of the PD equal to the positive supply voltage, which can result in up to 0.9 V of reverse bias; however, any noise on the supply is introduced directly into the signal so this may actually result in higher noise levels. The recommended setting is to set Register 0x54, Bits[11:10] and/or Register 0x54, Bits[9:8] equal to 0x2 for an ~250 mV reverse bias.

Improving SNR Using Integrator Chopping

The last stage in the analog front end that is integrated into the ADPD1080/ADPD1081 data path is a charge integrator. The integrator uses an on and off integration sequence, synchronized to the emitted light pulse, which acts as an additional high-pass filter to remove offsets, drifts, and low frequency noise from the previous stages. However, the integrating amplifier can itself introduce low frequency signal content at a low level. The ADPD1080/ADPD1081 have an integrator chop mode that enables additional chopping in the digital domain to remove this signal. This chopping is achieved by using even numbers of pulses per sample and inverting the integration sequence for half of those sequences. In the calculation to combine the digitized result of each of the pulses of the sample, the sequences with an inverted integrator sequence are subtracted and the sequences with a normal integrator sequence are added. An example diagram of the integrator chopping sequence is shown in Figure 46.

The result is that any low frequency signal contribution from the integrator is eliminated, leaving only the integrated signal, which results in higher SNR, especially at higher numbers of pulses and at lower TIA gains where the noise contribution of the integrator becomes more pronounced.

Digital chopping is enabled using the registers and bits detailed in Table 25. The bit fields define the chopping operation for the first four pulses. This 4-bit sequence is then repeated for all subsequent pulses. In Figure 46, a sequence is shown where the second and fourth pulses are inverted, whereas the first and third pulses remain in the default polarity (noninverted). This configuration is achieved by setting Register 0x17, Bits[3:0] = 0xA and Register 0x1D, Bits[3:0] = 0xA for Time Slot A and Time Slot B, respectively. To complete the operation, the math must be adjusted using Register 0x58. In this example, set Register 0x58, Bits[9:8] and Register 0x58, Bits[11:10] to b01 to add the third pulse and subtract the fourth pulse for Time Slot A and Time Slot B, respectively. Set Register 0x58, Bits[2:1] and Register 0x58, Bits[6:5] to b01 to add the first pulse and subtract the second pulse for Time Slot A and Time Slot B, respectively. This sequence then repeats for every subsequent sequence of four pulses. An even number of pulses must be used with integrator chop mode.

When using integrator chop mode, the ADC offset registers (Register 0x18 through Register 0x1B for Time Slot A, and Register 0x1E through Register 0x21 for Time Slot B) must be set to 0. These settings are required because any digital offsets at the output of the ADC are automatically eliminated when the math is adjusted to subtract the inverted integration sequences while the default integration sequences are added. Integrator chop mode also eliminates the need to manually null the ADC offsets at startup in a typical application. Note that the elimination of the offset using chop mode may clip at least half of the noise signal when no input signal is present, which makes measuring the noise floor during characterization of the system difficult. For this reason, perform noise floor characterization of the system either with chop mode disabled or with chop mode enabled but with a minimal signal present at the input that increases the noise floor enough such that it is no longer clipped.

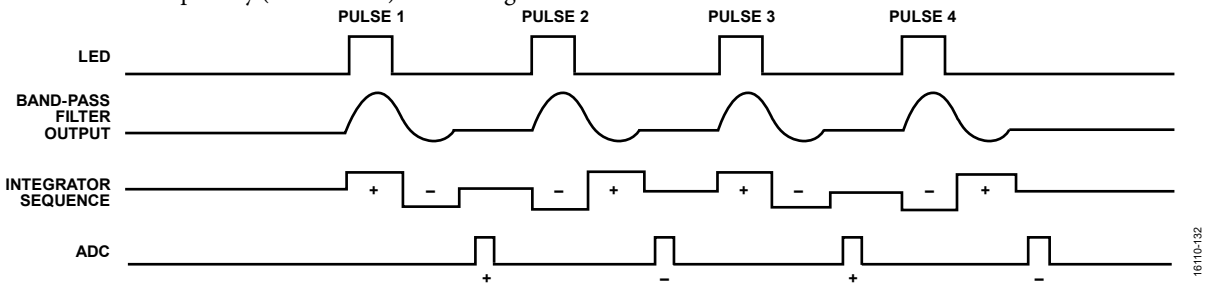

Figure 46. Diagram of Integrator Chopping Sequence

Table 25. Register Settings for Integrator Chop Mode

Hex Addr.	Data Bit(s)	Bit Name	Description
0x17	[3:0]	INTEG_ORDER_A	Integration sequence order for Time Slot A. Each bit corresponds to the polarity of the integration sequence of a single pulse in a four-pulse sequence. Bit 0 controls the integration sequence of Pulse 1, Bit 1 controls Pulse 2, Bit 2 controls Pulse 3, and Bit 3 controls Pulse 4. After four pulses, the sequence repeats. 0: normal integration sequence. 1: reversed integration sequence.
0x1D	[3:0]	INTEG_ORDER_B	Integration sequence order for Time Slot B. Each bit corresponds to the polarity of the integration sequence of a single pulse in a four-pulse sequence. Bit 0 controls the integration sequence of Pulse 1, Bit 1 controls Pulse 2, Bit 2 controls Pulse 3, and Bit 3 controls Pulse 4. After four pulses, the sequence repeats. 0: normal integration sequence. 1: reversed integration sequence

Hex Addr.	Data Bit(s)	Bit Name	Description
0x58	[11:10]	FLT_MATH34_B	Time Slot B control for adding and subtracting Sample 3 and Sample 4 in a four-pulse sequence (or any multiple of four pulses, for example, Sample 15 and Sample 16 in a 16-pulse sequence). 00: add third and fourth. 01: add third and subtract fourth. 10: subtract third and add fourth. 11: subtract third and fourth.
	[9:8]	FLT_MATH34_A	Time Slot A control for adding and subtracting Sample 3 and Sample 4 in a four-pulse sequence (or any multiple of four pulses, for example, Sample 15 and Sample 16 in a 16-pulse sequence). 00: add third and fourth. 01: add third and subtract fourth. 10: subtract third and add fourth. 11: subtract third and fourth.
	[6:5]	FLT_MATH12_B	Time Slot B control for adding and subtracting Sample 1 and Sample 2 in a four-pulse sequence (or any multiple of four pulses, for example, Sample 13 and Sample 14 in a 16-pulse sequence). 00: add first and second. 01: add first and subtract second. 10: subtract first and add second. 11: subtract first and second.
	[2:1]	FLT_MATH12_A	Time Slot A control for adding and subtracting Sample 1 and Sample 2 in a four-pulse sequence (or any multiple of four pulses, for example, Sample 13 and Sample 14 in a 16-pulse sequence). 00: add first and second. 01: add first and subtract second. 10: subtract first and add second. 11: subtract first and second.

OPTIMIZING POWER BY DISABLING UNUSED CHANNELS AND AMPLIFIERS

Single-Channel AFE Mode

When using a single photodiode in an application, with that photodiode connected to a single AFE channel (either Channel 1 or Channel 2), the ADPD1080/ADPD1081 have an option to power down the unused channels, placing the device in single AFE channel mode. Because three of the four AFE channels are off in this mode, the power consumption is reduced considerably.

When only Channel 1 is used, disable Channel 2, Channel 3, and Channel 4 by writing 0x7 to Register 0x3C, Bits[8:6]. If only Channel 2 is used, disable Channel 1 by writing 0x7 to Register 0x3C, Bits[5:3], and disable Channel 3 and Channel 4 by writing 0x7 to Register 0x37, Bits[15:13].

Dual-Channel AFE Mode

In situations where two of the four channels are in use, the other two channels can be disabled. Enable Channel 1 and Channel 2 (with Channel 3 and Channel 4 disabled) by writing 0x7 to Register 0x37, Bits[15:13]. Operate Channel 3 and Channel 4 in dual channel mode (with Channel 1 and Channel 2 disabled) by writing 0x7 to both Register 0x3C, Bits[5:3] and Register 0x37, Bits[12:10].

Three-channel mode can also be achieved with the appropriate settings. See Table 26 for the settings required to power down different combinations of channels. Refer to the Time Slot Switch section to determine the different combinations of the PDx inputs and enabled channels required to optimize the system configuration for maximum SNR and lowest power.

Powering Down Individual Amplifiers for Additional Power Savings

Each channel includes a TIA, a BPF, and an integrator which can also be configured as a buffer (see Figure 47).Options are built into the devices to power down individual amplifiers in the signal path. For example, in TIA ADC mode, the BPF is bypassed but left powered up by default. The BPF can be disabled completely, which saves 1/3 of the power dissipated by the AFE during the sampling phase. See the descriptions for Register 0x3C and Register 0x37 in Table 38 for information on how to disable the individual amplifiers.

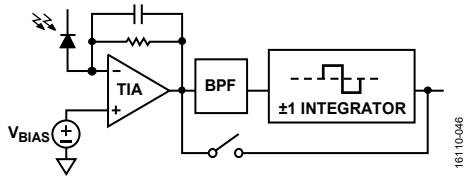

Figure 47. TIA/BPF/Integrator Block Diagram

It is important to leave any unused input channels floating for proper device operation.

Table 26. Channel Power-Down Settings

Number of Channels	Channels Enabled	Register 0x3C, Bits[8:6]	Register 0x3C, Bits[5:3]	Register 0x37, Bits[15:13]	Register 0x37, Bits[12:10]
1	Channel 1	0x7	0x0	Not applicable	Not applicable
1	Channel 2	0x0	0x7	0x7	0x0
2	Channel 1, Channel 2	0x0	0x0	0x7	0x0
2	Channel 3, Channel 4	0x0	0x7	0x0	0x7
3	Channel 2, Channel 3, Channel 4	0x0	0x7	0x0	0x0
4	All channels	0x0	0x0	0x0	0x0

OPTIMIZING DYNAMIC RANGE FOR HIGH AMBIENT LIGHT CONDITIONS

Large amounts of ambient light use large amounts of the available dynamic range of the TIA. The band-pass filter rejects the ambient light prior to the charge being integrated by the integrator; therefore, the ambient light is not a primary concern for the integrator. However, to accommodate increased levels of ambient light, it may be necessary to use lower TIA gain to avoid saturation of the TIA. When the TIA gain is reduced, the referred to input (RTI) noise of the desired signal increases. The impact of this increase can be reversed by increasing the gain of the integrator so that the LED signal gain in mA per LSB remains the same.

For example, start with an amount of pulsed signal (desired) where the TIA gain has been optimized such that the pulsed signal is using the desired amount of ADC dynamic range available, typically ~70% full scale. If the ambient light level increases and the gain of the TIA must be decreased to accommodate for the increase in ambient light without saturating the TIA, then the amount of pulsed signal presented to the ADC is attenuated by the factor that the TIA gain is reduced, which results in the SNR of the desired signal reducing.

To increase the SNR of the desired signal in this situation, use one of the following two methods. The first method simply increases the LED current by the amount required to bring the level of the pulsed signal at the ADC back to the desired amount of full scale. However, this is at the expense of increasing the overall power of the system. The second method is to increase the gain of the integrator to achieve a similar result. Figure 48 shows a block diagram of the receive path. The gain of the signal path is determined by the TIA feedback resistor (R_F) and the input resistor to the integrator (R_{INT}). When R_F is reduced to provide additional dynamic range at the input to the TIA to accommodate additional ambient light, R_{INT} can be reduced to provide more gain through the integrator such that the same amount of pulsed signal at the input to the TIA utilizes the same amount of dynamic range of the ADC before the TIA gain is reduced. Use Bits[9:8] of Register 0x42 (Time Slot A) and Register 0x44 (Time Slot B) to choose the resistor setting of R_{INT} as shown in Table 27.

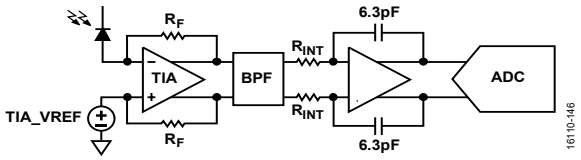

Figure 48. Receive Path Block Diagram

Table 27. Values of R_{INT}

Register 0x42, Bits[9:8], Register 0x44, Bits[9:8]	R_{INT} (kΩ)
00 (default)	400
01	200
10	100

Table 28 shows an example of how the SNR can be optimized as a function of the R_F and R_{INT} vs. the amount of ambient light that must be accommodated. The values shown in Table 28 are for a 2 µs LED pulse and a photodiode capacitance of 30 pF.

Table 28. Examples of SNR vs. R_F and R_{INT} Combinations

R_F (kΩ)	R_{INT} (kΩ)	Pulsed Current at 70% Full Scale (µA)	Noise (nA rms)	Maximum Ambient Current (µA)	TIA Linear Range (µA)	SNR (dB)
200	400	3.3	0.82	2.2	5.5	72.1
100	200	3.3	1.26	7.8	11.1	68.4
50	100	3.3	1.85	18.8	22.1	65
100	400	6.8	1.38	4.3	11.1	73.9
50	200	6.8	2.1	15.3	22.1	70.2
50	400	13.2	2.7	8.9	22.1	73.8

TIA ADC MODE

Figure 49 shows a way to put the devices into a mode that effectively runs the TIA directly into the ADC without using the analog BPF and integrator. This mode is referred to as TIA ADC mode. There are two basic applications of TIA ADC mode. In normal operation, all background light is blocked from the signal chain and, therefore, cannot be measured. TIA ADC mode can measure the amount of background and ambient light. This mode can also measure other dc input currents, such as leakage resistance.

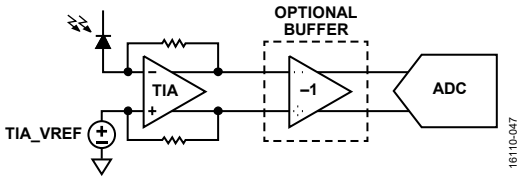

Figure 49. TIA ADC Mode Block Diagram

When the devices are in TIA ADC mode, the BPF and the integrator stage are bypassed. This bypass effectively wires the TIA directly into the ADC. At the set sampling frequency, the ADC samples Channel 1 through Channel 4 in sequential order, and each sample is taken at 1 µs intervals.

There are two modes of operation in TIA ADC mode. One mode is an inverting configuration where TIA ADC mode directly drives the ADC. This mode is enabled by setting Register 0x43 (Time Slot A) and/or Register 0x45 (Time Slot B) to 0xB065, which bypasses the BPF and the integrator. With the ADC offset register(s) for the desired channel set to 0, and the bias voltage for the TIA (TIA_VREF) set to 1.265 V, the output of the ADC is at ~13,000 codes for a single pulse and a zero input current condition. As the input current from the photodiode increases, the ADC output decreases toward 0. This configuration is a legacy TIA ADC mode from the ADPD103 that is kept in the ADPD1080/ADPD1081 for backward compatibility.

The recommended TIA ADC mode is one in which the BPF is bypassed and the integrator is configured as an inverting buffer. This mode is enabled by writing 0xAE65 to Register 0x43 (Time Slot A) and/or Register 0x45 (Time Slot B) to bypass the BPF. Additionally, to configure the integrator as a buffer, set Bit 7 of Register 0x42 (Time Slot A) and/or Register 0x44 (Time Slot B) to 1, and set Bit 7 of Register 0x58 to 1. With the ADC offset register(s) for the desired channel set to 0 and the TIA_VREF set to 1.265 V, the output of the ADC is at ~13,000 codes for a single pulse and a zero input current condition. As the input current from the photodiode increases, the ADC output decreases toward 0.

When configuring the integrator as a buffer, there is the option of either using a gain of 1 or a gain of 0.7. Using the gain of 0.7 increases the usable dynamic range at the input to the TIA; however, it is possible to overrange the ADC in this configuration and care must be taken to not saturate the ADC. To set the buffer gain use Register 0x42, Bit 9 for Time Slot A and Register 0x44, Bit 9 for Time Slot B. Setting this bit to 0 (default) sets a gain of 1. Setting this bit to 1 configures the buffer with a gain of 0.7.

Calculate the ADC output (ADC_{OUT}) as follows:

$$ADC_{OUT} = 8192 \pm (((2 \times TIA\_VREF - 2 \times i \times R_F - 1.8\ V)/146\ \mu V/LSB) \times SLOTx\_BUF\_GAIN) \quad (11)$$

where:
TIA_VREF is the bias voltage for the TIA (the default value is 1.265 V).
i is the input current to the TIA.
R_F is the TIA feedback resistor.
SLOTx_BUF_GAIN is either 0.7 or 1 based on the setting of Register 0x42, Bit 9 and Register 0x44, Bit 9.

Equation 11 is an approximation and does not account for internal offsets and gain errors. The calculation also assumes that the ADC offset registers are set to 0

One time slot can be used in TIA ADC mode at the same time the other time slot is being used in normal pulsed mode. This capability is useful for monitoring ambient and pulsed signals at the same time. The ambient signal is monitored during the time slot configured for TIA ADC mode, while the pulsed signal, with the ambient signal rejected, is monitored in the time slot configured for normal mode.

Protecting Against TIA Saturation in Normal Operation

One of the reasons to monitor TIA ADC mode is to protect against environments that may cause saturation. One concern when operating in high light conditions, especially with larger photodiodes, is that the TIA stage may become saturated while the ADPD1080/ADPD1081 continue to communicate data. The resulting saturation is not typical. The TIA, based on its settings, can only handle a certain level of photodiode current. Based on the way the ADPD1080/ADPD1081 are configured, if there is a current level from the photodiode that is larger than the TIA can handle, the TIA output during the LED pulse effectively extends the current pulse, making it wider. The AFE timing is then violated because the positive portion of the BPF output extends into the negative section of the integration window. Thus, the photo signal is subtracted from itself, causing the output signal to decrease when the effective light signal increases.

To measure the response from the TIA and verify that this stage is not saturating, place the device in TIA ADC mode and slightly modify the timing. Specifically, sweep SLOTx_AFE_OFFSET until two or three of the four channels reach a minimum value (note that TIA is in an inverting configuration). The four channels do not reach this minimum value because, typically, 3 µs LED pulse widths are used, and the ADC samples the four channels sequentially at 1 µs intervals. This procedure aligns the ADC sampling time with the LED pulse to measure the total amount of light falling on the photodetector (for example, background light + LED pulse).

If this minimum value is above 0 LSB, the TIA is not saturated. However, take care, because even if the result is not 0 LSB, operating the device near saturation can quickly result in saturation if light conditions change. A safe operating region is typically at ¾ full scale and lower. Use Table 29 to determine how the input codes map to ADC levels on a per channel per pulse basis. These codes are not the same as in normal mode because the BPF and integrator are not unity-gain elements.

Measuring PCB Parasitic Input Resistance

During the process of mounting the ADPD1080/ADPD1081, undesired resistance can develop on the inputs through assembly errors or debris on the PCB. These resistances can form between the anode and cathode, or between the anode and some other supply or ground. In normal operation, the ambient rejection feature of the ADPD1080/ADPD1081 masks the primary effects of these resistances, making it difficult to detect them. However, even at 1 MΩ to 10 MΩ, such resistance can affect performance significantly through added noise or decreased dynamic range. TIA ADC mode can screen for these assembly issues.

Measuring Shunt Resistance on the Photodiode

A shunt resistor across the photodiode does not generally affect the output level of the device in operation because the effective impedance of the TIA is low, especially if the photodiode is held to 0 V in operation. However, such resistance can add noise to the system, degrading performance. The best way to detect photodiode leakage, also called photodiode shunt resistance, is to place the device in TIA ADC mode in the dark and vary the operation mode cathode voltage. Setting the cathode to 1.3 V places 0 V across the photodiode because the anode is always at 1.3 V while in operation. Setting the cathode to 1.8 V places 0.5 V across the photodiode. Using the register settings in Table 3 to control the cathode voltage, measure the TIA ADC value at both voltages. Next, divide the voltage difference of 0.5 V by the difference of the ADC result after converting it to a current. This result is the approximate shunt resistance. Values greater than 10 MΩ may be difficult to measure, but this method is useful in identifying gross failures.

Measuring TIA Input Shunt Resistance

A resistance to develop between the TIA input and another supply or ground on the PCB is an example of another problem that can occur. These resistances can force the TIA into saturation prematurely. This premature saturation, in turn, takes away dynamic range from the device in operation and adds a Johnson noise component to the input. To measure these resistances, place the device in TIA ADC mode in the dark and start by measuring the TIA ADC offset level with the photodiode inputs disconnected (Register 0x14, Bits[11:8] = 0 or Register 0x14, Bits[7:4] = 0). From this, subtract the value of TIA ADC mode with the darkened photodiode connected and convert the difference into a current. If the value is positive, and the ADC signal decreased, the resistance is to a voltage higher than 1.3 V, such as V_{DD}. Current entering the TIA causes the output to drop. If the output difference is negative due to an increase of codes at the ADC, current is being pulled out of the TIA, and there is a shunt resistance to a lower potential than 1.3 V, such as ground.

Table 29. Analog Specifications for TIA ADC Mode

Parameter	Test Conditions/Comments	Typ	Unit
TIA ADC Saturation Levels	Values expressed per channel, per sample		
	25 kΩ gain	38.32	µA
	50 kΩ gain	19.16	µA
	100 kΩ gain	9.58	µA
	200 kΩ gain	4.79	µA
TIA Linear Range	25 kΩ gain	42.8	µA
	50 kΩ gain	21.4	µA
	100 kΩ gain	10.7	µA
	200 kΩ gain	5.4	µA
TIA ADC Resolution	Values expressed per channel, per sample; TIA feedback resistor		
	25 kΩ	2.92	nA/LSB
	50 kΩ	1.5	nA/LSB
	100 kΩ	0.73	nA/LSB
	200 kΩ	0.37	nA/LSB
Output Without Input Photocurrent	ADC offset (Register 0x18 to Register 0x21) = 0x0	13,000	LSB

Table 30. Configuration Registers to Switch Between the Normal Sample Mode and TIA ADC Mode

Hex Addr.	Data Bit(s)	Bit Name	Normal Mode Value	TIA ADC Mode Value	Description
42	[15:10]	SLOTA_AFE_MODE	0x07	Not applicable	In normal mode, this setting configures the integrator block for optimal operation. This setting is not important for TIA ADC mode.
	[9:8]	SLOTA_INT_GAIN	0x0	0x0	00: buffer gain = 1.0. 01: buffer gain = 1.0. 10: buffer gain = 0.7.
	7	SLOTA_INT_AS_BUF	0x0	0x1	0: normal integrator configuration. 1: convert integrator to buffer amplifier
43	[15:0]	SLOTA_AFE_CFG	0xADA5	0xAE65	Time Slot A AFE connection. 0xAE65 bypasses the band-pass filter. 0xB065 can also be used in TIA ADC mode. This setting bypasses the BPF and the integrator.
44	[15:10]	SLOTB_AFE_MODE	0x07	Not applicable	In normal mode, this setting configures the integrator block for optimal operation. This setting is not important for TIA ADC mode.
	[9:8]	SLOTB_INT_GAIN	0x0	0x0	00: buffer gain = 1.0. 01: buffer gain = 1.0. 10: buffer gain = 0.7.
	7	SLOTB_INT_AS_BUF	0x0	0x1	0: normal integrator configuration. 1: convert integrator to buffer amplifier
45	[15:0]	SLOTB_AFE_CFG	0xADA5	0xAE65	Time Slot B AFE connection. 0xAE65 bypasses the BPF. 0xB065 can also be used in TIA ADC mode. This setting bypasses the BPF and the integrator.
58	7	ENA_INT_AS_BUF	0x0	0x1	Enables the ability to configure the integrator as a buffer in TIA ADC mode.

PULSE CONNECT MODE

In pulse connect mode, the photodiode input connections are pulsed according to the timing set up in the LED pulse timing registers. In this mode, if the LED pulse timing is set up to provide a 2 µs LED pulse, the device pulses the connection to the photodiode input for 2 µs instead of providing a 2 µs LED pulse. This mode is an alternate to TIA ADC mode, allowing the entire signal path, including the BPF and integrator, to measure ambient light as well as other types of measurements with different types of sensors (for example, electrocardiogram (ECG)).

To enable pulse connect mode, the device is configured identically to normal mode, except that Register 0x14, Bits[3:2] = 0 for Time Slot B, and Register 0x14, Bits[1:0] = 0 for Time Slot A.

SYNCHRONOUS ECG AND PPG MEASUREMENT USING TIA ADC MODE

In wearable devices developed for monitoring the health care of patients, it is often necessary to have synchronized measurements of biomedical signals. For example, a synchronous measurement of patient ECG and PPG can determine the pulse wave transit time (PWTT), which can then estimate blood pressure.

The circuit shown in Figure 51 shows a synchronous ECG and PPG measurement using the AD8233 and the ADPD1080. The AD8233 implements a two-pole high-pass filter (HPF) with a cutoff frequency at 0.3 Hz, and a two-pole low-pass filter (LPF) with a cutoff frequency of 37 Hz. The output of the AD8233 is fed to one of the current inputs of the ADPD1080 through a 200 kΩ resistor to convert the voltage output of the AD8233 into a current.

The ADPD1080 is configured to alternately measure the photodiode signal and the ECG signal from the AD8233 on consecutive time slots to provide fully synchronized PPG and ECG measurements. Data can be read out of the on-chip FIFO or straight from data registers. The ADPD1080 channel used to process the ECG signal is set up in TIA ADC mode, and the input bias voltage must be set to the 0.90 V setting using Bits[5:4] of Register 0x42 if the ECG signal is on Time Slot A, or Register 0x44 on Time Slot B. The TIA gain setting can be set to optimize the dynamic range of the signal path. The channel used to process the PPG signal is configured in its normal operating mode. Figure 50 shows a plot of a synchronized ECG and PPG measurement using the AD8233 with the ADPD1080.

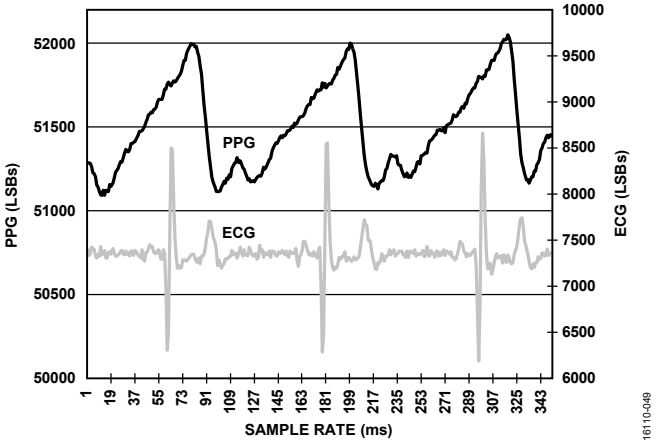

Figure 50. Plot of Synchronized ECG and PPG Waveforms

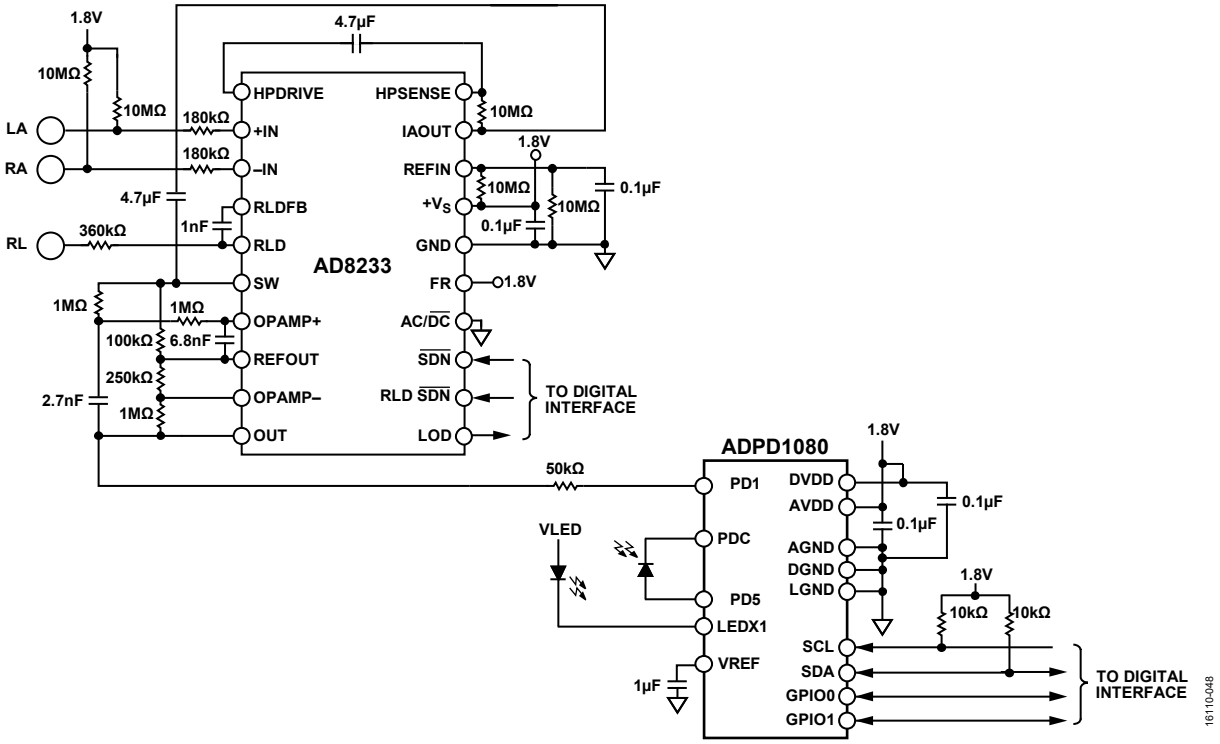

Figure 51. Synchronized PPG and ECG Measurement Using the ADPD1080 with the AD8233

FLOAT MODE

The ADPD1080/ADPD1081 has a unique operating mode, float mode, that allows excellent SNR at low power in low light situations. In float mode, the photodiode is first preconditioned to a known state and then the photodiode anode is disconnected from the receive path of the ADPD1080/ADPD1081 for a preset amount of float time. During the float time, light falls on the photodiode, either from ambient light, pulsed LED light, or a combination of the two depending on the operating mode. Charge from the sensor is stored directly on the capacitance of the sensor. At the end of the float time, the photodiode switches back into the receive path of the ADPD1080/ADPD1081 and an inrush of the accumulated charge occurs, which is subsequently integrated by the integrator of the ADPD1080/ADPD1081, allowing the maximum amount of charge to be processed per pulse with the minimum amount of noise added by the signal path. The charge is integrated externally on the capacitance of the photodiode for as long as it takes to acquire maximum charge, independent of the amplifiers of the signal path, which adds noise to the signal.

Amplifier and ADC noise values are constant for a given measurement. For optimal SNR, it is desirable to have a greater amount of signal (charge) per measurement. In normal mode, because the pulse time is fixed, the charge per measurement can be increased only by increasing the LED drive current. For high light conditions, this is sufficient. In low light conditions, however, there is a limit to the available current. In addition, high current pulses can cause ground noise in some systems. Green LEDs have lower efficiency at high currents, and many battery designs do not deliver high current pulses as efficiently. Float mode allows the user the flexibility to increase the amount of charge per measurement by either increasing the LED drive current or by increasing the float time. This flexibility is especially useful in low current transfer ratio (CTR) conditions, for example, 10 nA/mA, where normal mode requires multiple pulses to achieve an acceptable level of SNR.

In float mode, the signal path bypasses the BPF and uses only the TIA and integrator. In normal mode, the shape of the pulse is known (typically either 2 µs or 3 µs) and is consistent across devices and conditions. The shape of the signal coming through the BPF is also predictable, which allows a user to align the integrator timing with the zero-crossing of the filtered signal. In float mode, the shape of the signal produced by the charge dump can differ across devices and conditions. A filtered signal cannot be reliably aligned; therefore, the BPF cannot be used. In float mode, the entire charge dump is integrated in the negative cycle of the integrator and the positive cycle cancels any offsets.

Float Mode Measurement Cycle

Figure 52 shows the float mode measurement cycle timing diagram, and the following details the points shown:

- The precondition period is shown prior to Point A. The photodiode is connected to the TIA, and the photocurrent flows into the TIA. The photodiode anode is held at 0.9 V (Register 0x42 and Register 0x44, Bits[5:4] = 0x2 sets TIA_VREF = 0.9 V). The photodiode is reverse biased to a maximum reverse bias of ~250 mV by setting Register 0x54, Bit 7 = 1 and Register 0x54, Bits[9:8] = 0x2 (for Time Slot A). At this point, the output of the TIA (TIA_OUT) = TIA_VREF − (I_{PD} × R_F), where I_{PD} is the current flowing from the PD into the ADPD1080/ADPD1081 input, and the integrator is off.
- At Point A, the photodiode is disconnected from the receive path. Light continues to fall on the photodiode, producing a charge that accumulates directly on the photodiode capacitance. As the charge accumulates, the voltage at the floating photodiode anode rises. The TIA is disconnected from the input to the ADPD1080/ADPD1081 so that no current flows through the TIA, and the TIA output is at TIA_VREF. Just prior to Point B, the integrator resets to 0. In the Float Mode for Synchronous LED Measurements section, the LED pulses during the time period between Point A and Point D. Float times of <4 µs are not allowed.
- At Point B, the integrator begins its positive integration phase. Small dc offsets between the TIA output and the integrator reference causes the integrator output to ramp up for positive offsets or ramp down for negative offsets. The photodiode continues to accumulate charge during this period.
- At Point C, the integrator begins its negative integration phase. This reversal in polarity begins to cancel any signal caused by offsets. This offset cancellation continues through Point F, where all offsets are cancelled completely.
- At Point D, the photodiode switches into the receive path where all the charge that has accumulated on the photodiode capacitance during the float time is dumped into the TIA. The typical charge dump time is less than 2 µs. As the current flows through the TIA, the output of the TIA responds with a large negative signal. Because the integrator is in the negative integration phase at this point, the output of the integrator rises as the input current to the device integrates back to total charge. Between Point D and Point E, any light incident on the photodiode produces additional photocurrent, which is immediately integrated by the integrator as charge.
- At Point E, the TIA disconnects from the receive path and the TIA output returns to TIA_VREF. Between Point E and Point F, the integrator completes the negative integration phase and cancellation of the offsets.
- At Point F, the integrator output is held until sampled by the ADC.

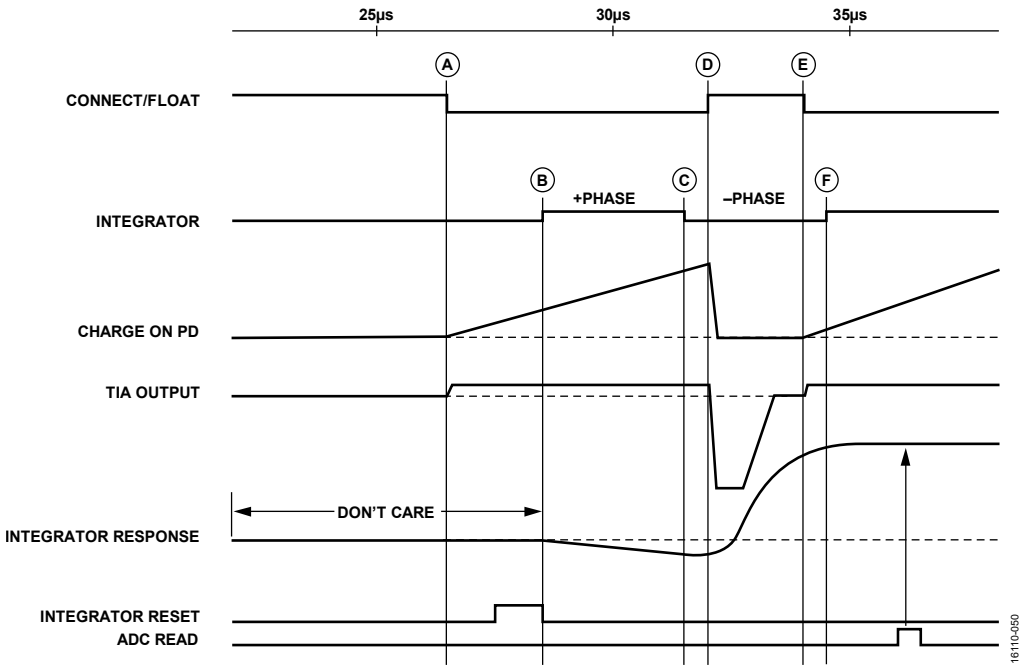

Figure 52. Float Mode Measurement Cycle Timing Diagram

Float Mode Limitations

When using float mode, the limitations of the mode must be well understood. For example, a finite amount of charge can accumulate on the capacitance of the photodiode, and a maximum amount of charge that can be integrated by the integrator. Based on an initial reverse bias of 250 mV on the photodiode and assuming that the photodiode begins to become nonlinear at ~200 mV of forward bias, there is ~450 mV of headroom for the anode voltage to increase from its starting point at the beginning of the float time before the charge ceases to accumulate in a linear fashion. It is desirable to operate only in the linear region of the photodiode (see Figure 53). To verify that float mode is operating in the linear region of the diode, the user can perform a simple check. Record data at a desired float time and then record data at half the float time. The ratio of the two received signals should be 2:1. If this ratio does not hold true, the diode is likely beginning to forward bias at the longer float time and becomes nonlinear.

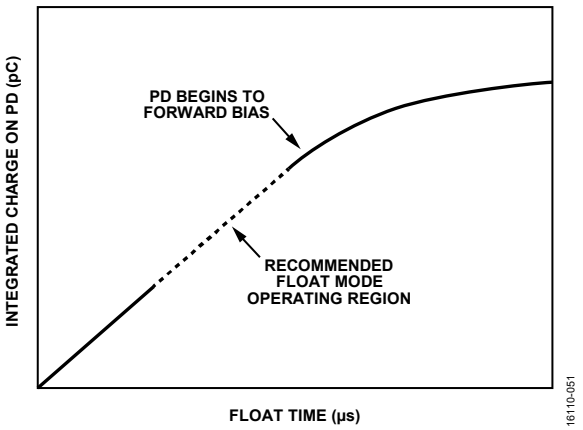

Figure 53. Transfer Function of Integrated Charge on the Photodiode vs. Float Time

The maximum amount of charge that can be stored on the photodiode capacitance and remain in the linear operating region of the sensor can be estimated by

$$Q = CV$$

where:
Q is the integrated charge.
C is the capacitance of the photodiode.
V is the amount of voltage change across the photodiode before the photodiode becomes nonlinear.

For a typical discrete optical design using a 7 mm^2 photodiode with 70 pF capacitance and 450 mV of headroom, the maximum amount of charge that can be stored on the photodiode capacitance is 31.5 pC.

In addition, consider the maximum amount of charge the integrator of the ADPD1080/ADPD1081 can integrate. The integrator can integrate up to 7.6 pC. When this charge is referred back to the input, consider the TIA gain. When the TIA gain is at 200 kΩ, the input referred charge is at a 1:1 ratio to the integrated charge on the integrator. For 100 kΩ gain, it is 2:1; for 50 kΩ gain, it is 4:1; and for 25 kΩ gain, it is 8:1. For the previous example using a photodiode with 70 pF capacitance, use 50 kΩ TIA gain and set the float timing such that, for a single pulse, the output of the ADC is at 70% of full scale, which is a typical operating condition. Under these operating conditions, 5.3 pC integrates per pulse by the integrator for 21.2 pC of charge accumulated on the photodiode capacitance. For small CTR, however, it can take a long time to accumulate 21.2 pC of charge on the photodiode capacitance, in which case, use higher TIA gains according to how much charge can be accumulated in a

given amount of time. Ultimately, the type of measurement being made (ambient or pulsed LED), the photodiode capacitance, and the CTR of the system determine the float times.

Float Mode for Ambient Light Measurements

Float mode is used for ambient light measurements where the background light is sufficiently small. Use TIA ADC mode for ambient light measurements of higher intensities. Small amounts of light can be measured with adequate float times, allowing the incoming charge to accumulate to levels large enough to be measured above the noise floor of the system. The source of this light can be any combination of synchronous light (for example, from a pulsed LED) and asynchronous light (that is, background). If there is no system generated light source, the measurement is simply a measure of the background light.

Use a two pulse differential measurement technique to cancel out electrical drifts and offsets. Take two measurements, each of a different float time. The first float time is considerably shorter than the second pulse. After the two measurements are taken, Measurement 1 is subtracted from Measurement 2, which effectively cancels out any offset and drift common to both measurements. What is left is an ambient light measurement based on an amount of charge that is integrated over a time that is the difference of the first and second float times. For example, if Float Time 1 is 6 µs and Float Time 2 is 26 µs, the ambient light measurement is based on 20 µs of charge integrated on the photodiode capacitance with any offset and drift removed. In float mode for ambient light, the number of pulses must be set to two to cancel drifts and offsets because only the first pulse can be short. More than two pulses can be used; however, pulses two through n are always the same length. If drift cancellation is not required, any number of pulses can be used and added together. Figure 54 shows an example of float ambient mode timing, and Table 31 details the relevant registers that must be configured.

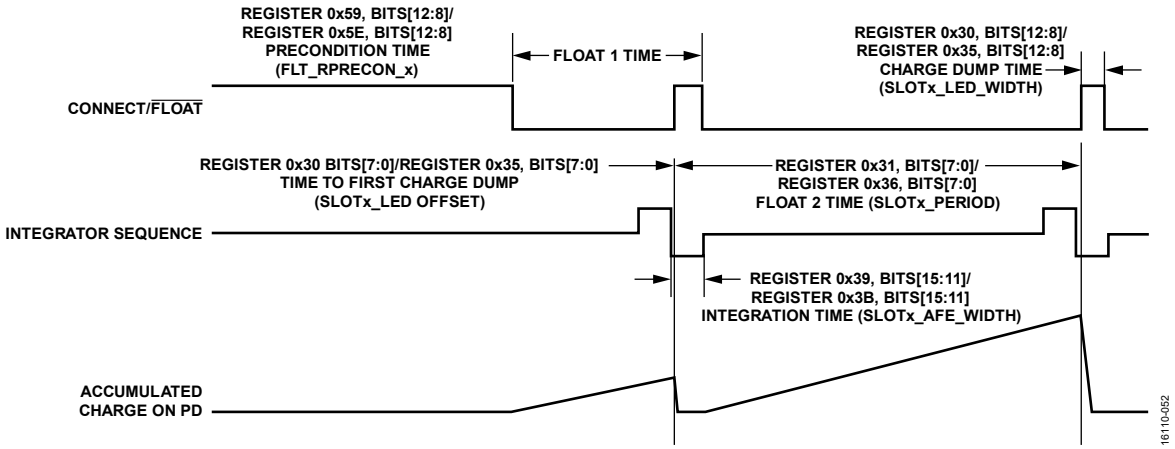

Figure 54. Example of Float Ambient Mode Timing

Table 31. Float Ambient Mode Registers

Group	Register Name	Register		Float Mode Description
		Time Slot A	Time Slot B	
Float Mode Operation	SLOTx_LED_SEL	0x14, Bits[1:0]	0x14, Bits[3:2]	Set to 0 to enable float mode.
	FLT_EN_x	0x5E, Bits[14:13]	0x59, Bits[14:13]	Set to 3 to enable float between connect pulses.
	FLT_MATH12_x	0x58, Bits[2:1]	0x58, Bits[6:5]	Set to 2 to subtract first pulse and add second pulse.
	SLOTx_AFE_CFG	0x43, Bits[15:0]	0x45, Bits[15:0]	Set to 0xAE65 for TIA and integrator, bypass BPF.
	SLOTx_TIA_VREF	0x42, Bits[5:4]	0x44, Bits[5:4]	Set to 2 for TIA_VREF = 0.9 V.
	SLOTx_V_CATHODE	0x54, Bits[9:8]	0x54, Bits[11:10]	Set to 2 for 250 mV reverse bias on the photodiode at the precondition.
	REG54_VCAT_ENABLE	0x54, Bit 7	0x54, Bit 7	Set to 1 to override Register 0x3C cathode voltage settings.

Group	Register Name	Register		Float Mode Description
		Time Slot A	Time Slot B	
Float Mode Timing	FLT_PRECON_x	0x5E, Bits[12:8]	0x59, Bits[12:8]	Precondition time (to start of Float 1 time).
	SLOTx_PERIOD	0x31, Bits[7:0]	0x36, Bits[7:0]	8 LSBs of float period in µs; Float 2 time = SLOTx_PERIOD
	SLOTx_PERIOD	0x37, Bits[1:0]	0x37, Bits[9:8]	2 MSBs of float period.
	SLOTx_LED_WIDTH	0x30, Bits[12:8]	0x35, Bits[12:8]	Connect time in µs; this is the amount of time given to dump the accumulated charge from the photodiode capacitance; typically, this is set to 2 µs.
	SLOTx_LED_OFFSET	0x30, Bits[7:0]	0x35, Bits[7:0]	Time to first charge dump; Float 1 time = (SLOTx_LED_OFFSET + SLOTx_LED_WIDTH) − FLT_PRECONx.
	SLOTx_AFE_WIDTH	0x39, Bits[15:11]	0x3B, Bits[15:11]	Integration time in µs; set to FLT_CONNx + 1.
	SLOTx_AFE_OFFSET	0x39, Bits[10:0]	0x3B, Bits[10:0]	Integrator start time in 31.25 ns increments; set to (SLOTx_LED_OFFSETx − SLOTx_AFE_WIDTH − 9.25) µs.
	SLOTx_PULSES	0x31, Bits[15:8]	0x36, Bits[15:8]	Number of pulses; set to 2 for float ambient mode.

Float Mode for Synchronous LED Measurements

In float LED mode, photocurrent is generated from ambient light and pulsed LED light during the float time. Float LED mode is desirable in low signal conditions where the CTR is <10 nA/mA. In addition, float mode is a good option in situations where the user wants to limit the LED drive current of the green LEDs in a heart rate measurement to keep the forward voltage drop of the green LED to a level that allows the elimination of a boost converter for the LED supply. For example, the LED current can be limited to 10 mA to ensure that the LED voltage drop is ~3 V so that it can operate directly from the battery without the need of a boost converter. Float mode accumulates the received charge during longer LED pulses without adding noise from the signal path, effectively yielding the highest SNR and/or photon attainable.

As with float ambient mode, multiple pulses cancel electrical offsets and drifts; however, in float LED mode, the ambient light must also be cancelled because only the reflected return from the LED pulses is desired. To achieve this ambient light rejection, use an even number of equal length pulses. For every pair of pulses, the LED flashes in one of the pulses and does not flash in the other. The return from the LED + ambient + offset is present in one of the pulses. In the other, only the ambient light and offset is present. A subtraction of the two pulses is made that eliminates ambient light as well as any offset and drift. It is recommended to use groups of four pulses for measurement where the LED is flashed on Pulse 2 and Pulse 3. The accumulator adds Pulse 2 and Pulse 3 and then subtract Pulse 1 and Pulse 4. To gain additional SNR, use multiple groups of four pulses.

The settings of FLT_LED_FIRE_x, Register 0x5A, Bits[15:8] determine if the LED fires in which pulse position. Which pulse positions are added or subtracted is configured in the FLT_MATH12x and FLT_MATH34x bits of Register 0x58. These sequences are repeated in groups of four pulses. The value written to the FIFO or data registers is dependent on the total number of pulses per sample period. For example, if the device is setup for 32 pulses, the 4 pulse sequence, as defined in FLT_LED_FIRE_x and FLT_MATHxxx, repeats eight times and a single register or FIFO write of the final value based on 32 pulses executes. Table 32 details the relevant registers for float LED mode.

Table 32. Float LED Mode Registers

Group	Register Name	Register Address		Float Mode Description
		Time Slot A	Time Slot B	
Float Mode Operation	SLOTx_LED_SEL	0x14, Bits[1:0]	0x14, Bits[3:2]	Set to 0 to enable float mode.
	FLT_EN1_x	0x5E, Bits[14:13]	0x59, Bits[14:13]	Set to 3 to enable float between connect pulses.
	FLT_MATH12_x	0x58, Bits[2:1]	0x58, Bits[6:5]	Set to 2 to subtract first pulse and add second pulse.
	FLT_MATH34_x	0x58, Bits[9:8]	0x58, Bits[11:10]	Set to 1 to add third pulse and subtract fourth pulse.
	SLOTx_AFE_CFG	0x43, Bits[15:0]	0x45, Bits[15:0]	Set to 0xAE65 for TIA + integrator, bypass BPF.
	SLOTx_TIA_VREF	0x42, Bits[5:4]	0x44, Bits[5:4]	Set to 2 for TIA_VREF = 0.9 V.
	SLOTx_V_CATHODE	0x54, Bits[9:8]	0x54, Bits[11:10]	Set to 2 for 250 mV reverse bias on the photodiode at the precondition.
	REG54_VCAT_ENABLE	0x54, Bit 7	0x54, Bit 7	Set to 1 to override Register 0x3C cathode voltage settings.
	FLT_LED_SELECT_x	0x3E, Bits[15:14]	0x3F[15:14]	LED selection for float LED mode. 00 = no LED. 01 = LED1. 10 = LED2. 11 = LED3.
Float Mode Timing	FLT_PRECON_x	0x5E, Bits[12:8]	0x59, Bits[12:8]	Precondition time (to start of float 1 time).
	SLOTx_PERIOD	0x31, Bits[7:0]	0x36, Bits[7:0]	8 LSBs of float period in µs. Float 2 time = SLOTx_PERIOD. Float 2 time is valid for every pulse subsequent to the first pulse. Float 1 time must be set equal to Float 2 time in float LED mode.
	SLOTx_PERIOD	0x37, Bits[1:0]	0x37, Bits[9:8]	2 MSBs of float period.
	SLOTx_LED_WIDTH	0x30, Bits[12:8]	0x35, Bits[12:8]	Connect time in µs, which is the amount of time given to dump the accumulated charge from the photodiode capacitance. Typically, it is set to 2 µs.
	SLOTx_LED_OFFSET	0x30, Bits[7:0]	0x35, Bits[7:0]	Time to first charge dump. Float 1 time = (SLOTx_LED_OFFSET + SLOTx_LED_WIDTH) – FLT_PRECONx. Float 1 time must be equal to Float 2 time for float LED mode.
	SLOTx_AFE_WIDTH	0x39,Bits[15:11]	0x3B, Bits[15:11]	Integration time in µs. set to FLT_CONN + 1.
	SLOTx_AFE_OFFSET	0x39, Bits[10:0]	0x3B, Bits[10:0]	Integrator start time in 31.25 ns increments. Set to (SLOTx_LED_OFFSET – SLOTx_AFE_WIDTH – 9.25) µs.
	SLOTx_PULSES	0x31, Bits[15:8]	0x36, Bits[15:8]	Number of pulses; must be set in multiples of 2, minimum 2.
	FLT_LED_WIDTH_x	0x3E, Bits[12:8]	0x3F, Bits[12:8]	LED pulse width for float LED mode in µs.
	FLT_LED_OFFSET_x	0x3E, Bits[7:0]	0x3F, Bits[7:0]	Time of first LED pulse in float LED mode.
	FLT_LED_FIRE_x	0x5A, Bits[11:8]	0x5A, Bits[15:12]	In any given sequence of four pulses, fire the LED in the selected position. Selections are active low (that is, fire LED if 0). For example, in a sequence of four pulses on Time Slot B, Register 0x5A, Bit 12 is the first pulse, and Register 0x5A, Bit 15 is the fourth pulse. For a sequence of four pulses, fire the LED in the second and third pulses by writing 0x9 to Register 0x5A, Bits[15:12].

A timing diagram for a four pulse float LED sequence for Time Slot B is shown in Figure 55. In this example, the device is set up for LED pulses of 12 µs that fall within a float period of 16 µs, 2 µs of which are used for dumping of the accumulated charge on the photodiode. The integration time is set to 3 µs, which is 1 µs more than the charge dump time to allow timing margin when integrating the incoming charge. Note, there is a 9 µs offset built into the integration start time. Consider this offset when setting the SLOTx_AFE_OFFSET value. As shown in Figure 55, the time of the first charge dump is set to 30 µs. SLOTx_AFE_OFFSET is set to 0x238 (17.75 µs), taking into account the 3 µs integration time, the 9 µs offset, and an additional 250 ns for edge placement margin.

To calculate SLOTx_AFE_OFFSET, use the following equation:

$$SLOTx\_AFE\_OFFSET = SLOTx\_LED\_OFFSET - SLOTx\_AFE\_WIDTH - 9.25\ \mu s$$

Placement of the integration period is such that the negative phase of the integration is centered on the charge dump phase. The TIA is an inverting stage; therefore, placing the negative

phase of the integration during the dumping of the charge from the photodiode causes the integrator to increase with the negative going output signal from the TIA.

The LED flashes in the second and third pulses of the four pulse sequence. Setting Register 0x58, Bits[6:5] = 2 and Register 0x58, Bits[11:10] = 1 forces the device to add the second and third pulses while subtracting the first and fourth pulses, effectively cancelling out the ambient light and electrical offsets and drift.

A comparison of float ambient mode vs. float LED mode is shown in Table 33 and Table 34.

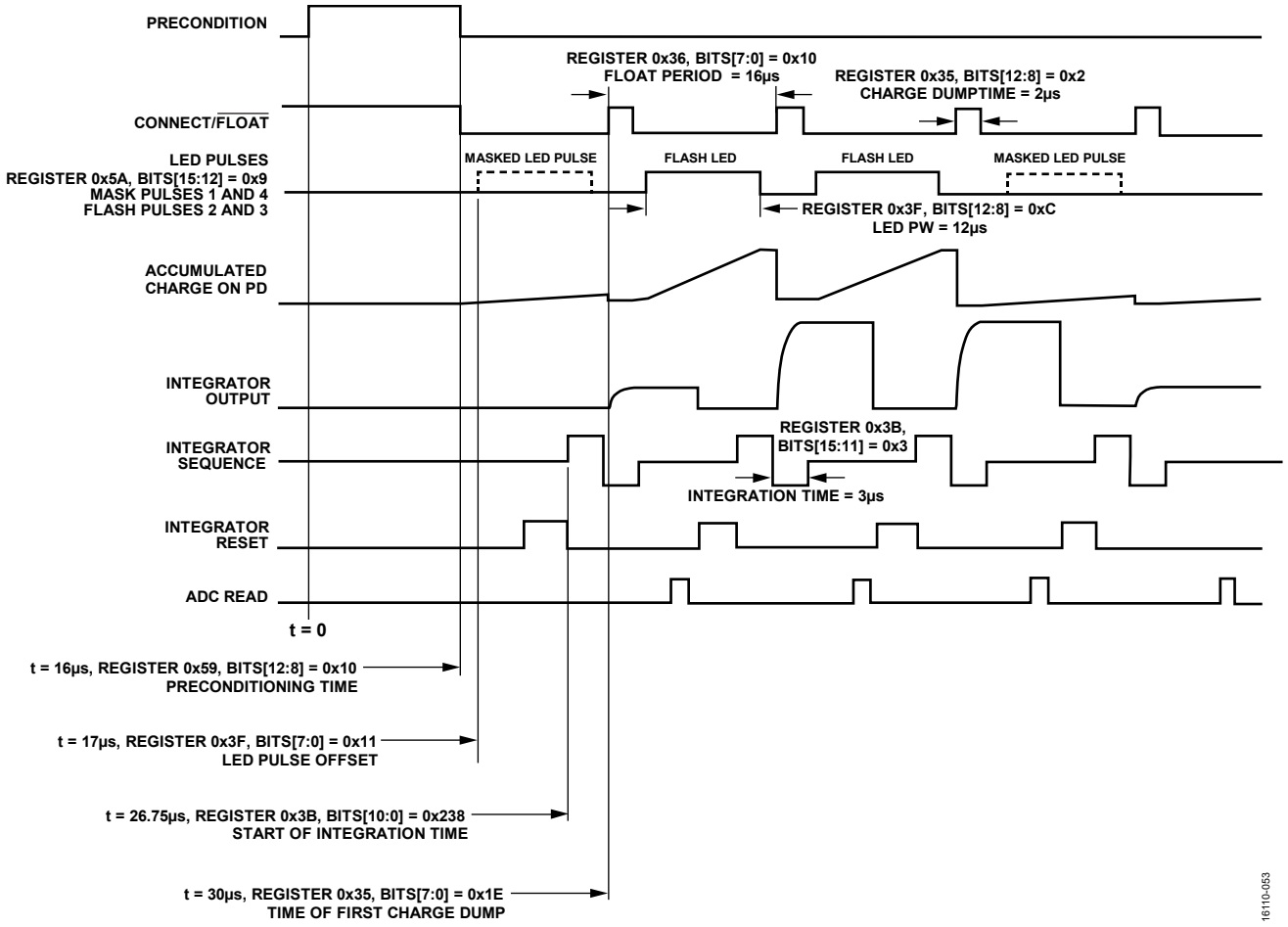

Figure 55. Example Timing Diagram of Four Pulse Float LED Mode Sequence

Table 33. Float Ambient Mode—Measure Ambient Light Level

Pulse	Float Time	Integrated Charge	Calculation	Result
1	Shorter	Offset, Ambient 1 (shorter time)	Subtract	Ambient Measurement = Ambient 2 – Ambient 1 (Offset Cancels)
2	Longer	Offset, Ambient 1 (shorter time)	Add	
3	Not applicable	Not applicable	Not applicable	
4	Not applicable	Not applicable	Not applicable	

Table 34. Float LED Mode—Measurement Synchronous Reflected Light from LED

Pulse	Float Time	Integrated Charge	Calculation	Result
1	Equal	Offset + Ambient	Subtract	Sync LED Response = Reflected LED Return (Offset and Ambient Cancels
2	Equal	Offset + Ambient + LED	Add	
3	Equal	Offset + Ambient + LED	Add	
4	Equal	Offset + Ambient	Subtract	

Monitoring Ambient Light Levels in Float LED Mode

In real-world applications, it is common for the ambient light levels to change constantly. When using float LED mode, increasing the amount of ambient light can approach levels where the ambient light uses an unacceptable amount of dynamic range of the charge that can be stored on the photodiode capacitance. For this reason, it is required that the ambient light level is monitored so that configuration changes can be made when necessary, for example, float time, TIA gain, and operating mode. There are two ways to monitor ambient light levels. One way is to use TIA ADC mode in the alternate time slot and continuously monitor the ambient light level. The other way is to use a feature of the ADPD1080/ADPD1081 where the ambient light level is automatically monitored in the background during float mode operation and is compared against a user-defined threshold. If the ambient light level exceeds this threshold by some user-defined number of times, the device sets a flag that can be read by the user or can be output to a GPIO. Table 35 lists all the registers used to monitor the ambient light level while in float LED mode.

The user sets an ambient level threshold in the BG_THRESH register, which is the threshold by which the ADC result of the subtract cycles in float LED mode are compared against. The subtract cycles in float LED mode are the positions in the pulse sequence in which the LED pulse is masked; therefore, it is the background level measurement. The ADC result is equal to the raw ADC output minus the contents of the ADC offset register (Register 0x18 to Register 0x1B and Register 0x1E to Register 0x21). In the BG_COUNT register, the user sets a limit on the number of cycles that BG_THRESH is exceeded by the ADC result before the BG_STATUS bit is set for any particular channel. Every time the BG_THRESH value is exceeded by the ADC result during a subtract cycle, an internal counter increments. Each channel has its own counter. When this count exceeds the limit set in the BG_COUNT register, the BG_STATUS bit is set for the channel. The user can periodically monitor the BG_STATUS register to check for asserted bits. Alternatively, a GPIOx pin can be asserted if a BG_STATUS flag is set. See Table 35 for the various logical combinations of BG_STATUS flags and interrupts that can be brought out on a GPIOx.

Table 35. Registers for Monitoring the Ambient Light Level in Float LED Mode

	Register		
Float Mode Register Name	**Time Slot A**	**Time Slot B**	**Description**
BG_STATUS_x	0x04, Bits[3:0]	0x04, Bits[7:4]	Status of comparison between background light level and background threshold value (BG_THRESH). A 1 in any bit location means the threshold has been crossed BG_COUNT number of times. This register is cleared once it is read. Bit 0: Time Slot A, Channel 1 exceeded threshold count. Bit 1: Time Slot A, Channel 2 exceeded threshold count. Bit 2: Time Slot A, Channel 3 exceeded threshold count. Bit 3: Time Slot A, Channel 4 exceeded threshold count. Bit 4: Time Slot B, Channel 1 exceeded threshold count. Bit 5: Time Slot B, Channel 2 exceeded threshold count. Bit 6: Time Slot B, Channel 3 exceeded threshold count. Bit 7: Time Slot B, Channel 4 exceeded threshold count.
BG_THRESH_x	0x16, Bits[13:0]	0x1C[13:0]	The background threshold that is compared against the ADC result during the subtract cycles during float mode. If the ADC result exceeds the value in this register, BG_COUNT is incremented.
BG_COUNT_x	0x16, Bits[15:14]	0x1C[15:14]	This is the number of times the ADC value exceeds the BG_THRESH value during the float mode subtract cycles before the BG_STATUS bit is set. 0x0: never set BG_STATUS. 0x1: set when BG_THRESH is exceeded 1 time. 0x02: set when BG_THRESH is exceeded 4 times. 0x03: set when BG_THRESH is exceeded 16 times.
GPIO0_ALT_CFG	0x0B[4:0]	0x0B[4:0]	GPIO0 asserts for the following conditions: 0x10: logical OR of BG_STATUS, Bits[3:0]. 0x1A: logical OR of BG_STATUS, Bits[7:4]. 0x1B: logical OR of BG_STATUS, Bits[7:0]. 0x1C: logical OR of BG_STATUS, Bits[7:0] and INT.
GPIO1_ALT_CFG	0x0B[12:8]	0x0B[12:8]	GPIO1 asserts for the following conditions: 0x10: logical OR of BG_STATUS, Bits[3:0]. 0x1A: logical OR of BG_STATUS, Bits[7:4]. 0x1B: logical OR of BG_STATUS, Bits[7:0]. 0x1C: logical OR of BG_STATUS, Bits[7:0] and INT.

REGISTER LISTING

The recommended values are not shown. Only power-on reset values are shown in Table 36. The recommended values are largely dependent on use case.

Table 36. Numeric Register Listing

Hex. Addr.	Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	R/W
0x00	Status	[15:8]	FIFO_SAMPLES[7:0]								0x0000	R/W
		[7:0]	Reserved	SLOTB_INT	SLOTA_INT	Reserved						
0x01	INT_MASK	[15:8]	Reserved							FIFO_INT_MASK	0x00FF	R/W
		[7:0]	Reserved	SLOTB_INT_MASK	SLOTA_INT_MASK	Reserved						
0x02	GPIO_DRV	[15:8]	Reserved						GPIO1_DRV	GPIO1_POL	0x0000	R/W
		[7:0]	Reserved					GPIO0_ENA	GPIO0_DRV	GPIO0_POL		
0x04	BG_STATUS	[15:8]	Reserved								0x0000	R/W
		[7:0]	BG_STATUS_B[3:0]				BG_STATUS_A[3:0]					
0x06	FIFO_THRESH	[15:8]	Reserved		FIFO_THRESH[5:0]						0x0000	R/W
		[7:0]	Reserved									
0x08	DEVID	[15:8]	REV_NUM[7:0]								0x0A16	R
		[7:0]	DEV_ID[7:0]									
0x09	I2CS_ID	[15:8]	ADDRESS_WRITE_KEY[7:0]								0x00C8	R/W
		[7:0]	SLAVE_ADDRESS[6:0]							Reserved		
0x0A	CLK_RATIO	[15:8]	Reserved				CLK_RATIO[11:8]				0x0000	R
		[7:0]	CLK_RATIO[7:0]									
0x0B	GPIO_CTRL	[15:8]	Reserved			GPIO1_ALT_CFG[4:0]					0x0000	R/W
		[7:0]	Reserved			GPIO0_ALT_CFG[4:0]						
0x0D	SLAVE_ADDRESS_KEY	[15:8]	SLAVE_ADDRESS_KEY[15:8]								0x0000	R/W
		[7:0]	SLAVE_ADDRESS_KEY[7:0]									
0x0F	SW_RESET	[15:8]	Reserved								0x0000	R/W
		[7:0]	Reserved							SW_RESET		
0x10	Mode	[15:8]	Reserved								0x0000	R/W
		[7:0]	Reserved						Mode[1:0]			
0x11	SLOT_EN	[15:8]	Reserved		RDOUT_MODE	FIFO_OVRN_PREVENT	Reserved			SLOTB_FIFO_MODE[2]	0x1000	R/W
		[7:0]	SLOTB_FIFO_MODE[1:0]		SLOTB_EN	SLOTA_FIFO_MODE[2:0]			Reserved	SLOTA_EN		
0x12	FSAMPLE	[15:8]	FSAMPLE[15:8]								0x0028	R/W
		[7:0]	FSAMPLE[7:0]									
0x14	PD_LED_SELECT	[15:8]	Reserved				SLOTB_PD_SEL[3:0]				0x0541	R/W
		[7:0]	SLOTA_PD_SEL[3:0]				SLOTB_LED_SEL[1:0]		SLOTA_LED_SEL[1:0]			
0x15	NUM_AVG	[15:8]	Reserved					SLOTB_NUM_AVG[2:0]			0x0600	R/W
		[7:0]	Reserved	SLOTA_NUM_AVG[2:0]			Reserved					
0x16	BG_MEAS_A	[15:8	BG_COUNT_A[1:0]		BG_THRESH_A[13:8]						0x0000	R/W
		[7:0]	BG_THRESH_A[7:0]									
0x17	INT_SEQ_A	[15:8]	Reserved								0x0000	R/W
		[7:0]	Reserved				INTEG_ORDER_A[3:0]					
0x18	SLOTA_CH1_OFFSET	[15:8]	SLOTA_CH1_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTA_CH1_OFFSET[7:0]									
0x19	SLOTA_CH2_OFFSET	[15:8]	SLOTA_CH2_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTA_CH2_OFFSET[7:0]									
0x1A	SLOTA_CH3_OFFSET	[15:8]	SLOTA_CH3_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTA_CH3_OFFSET[7:0]									
0x1B	SLOTA_CH4_OFFSET	[15:8]	SLOTA_CH4_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTA_CH4_OFFSET[7:0]									
0x1C	BG_MEAS_B	[15:8	BG_COUNT_B[1:0]		BG_THRESH_B[13:8]						0x0000	R/W
		[7:0]	BG_THRESH_B[7:0]									
0x1D	INT_SEQ_B	[15:8]	Reserved								0x0000	R/W
		[7:0]	Reserved				INTEG_ORDER_B[3:0]					

Hex. Addr.	Name	Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Reset	R/W
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
0x1E	SLOTB_CH1_OFFSET	[15:8]	SLOTB_CH1_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTB_CH1_OFFSET[7:0]									
0x1F	SLOTB_CH2_OFFSET	[15:8]	SLOTB_CH2_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTB_CH2_OFFSET[7:0]									
0x20	SLOTB_CH3_OFFSET	[15:8]	SLOTB_CH3_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTB_CH3_OFFSET[7:0]									
0x21	SLOTB_CH4_OFFSET	[15:8]	SLOTB_CH4_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTB_CH4_OFFSET[7:0]									
0x22	ILED3_COARSE	[15:8]	Reserved		ILED3_SCALE	Reserved					0x3000	R/W
		[7:0]	Reserved	ILED3_SLEW[2:0]			ILED3_COARSE[3:0]					
0x23	ILED1_COARSE	[15:8]	Reserved		ILED1_SCALE	Reserved					0x3000	R/W
		[7:0]	Reserved	ILED1_SLEW[2:0]			ILED1_COARSE[3:0]					
0x24	ILED2_COARSE	[15:8]	Reserved		ILED2_SCALE	Reserved					0x3000	R/W
		[7:0]	Reserved	ILED2_SLEW[2:0]			ILED2_COARSE[3:0]					
0x25	ILED_FINE	[15:8]	ILED3_FINE[4:0]					ILED2_FINE[4:2]			0x630C	R/W
		[7:0]	ILED2_FINE[1:0]		Reserved	ILED1_FINE[4:0]						
0x30	SLOTA_LED_PULSE	[15:8]	Reserved			SLOTA_LED_WIDTH[4:0]					0x0320	R/W
		[7:0]	SLOTA_LED_OFFSET[7:0]									
0x31	SLOTA_NUMPULSES	[15:8]	SLOTA_PULSES[7:0]								0x0818	R/W
		[7:0]	SLOTA_PERIOD[7:0]									
0x34	LED_DISABLE	[15:8]	Reserved						SLOTB_LED_DIS	SLOTA_LED_DIS	0x0000	R/W
		[7:0]	Reserved									
0x35	SLOTB_LED_PULSE	[15:8]	Reserved			SLOTB_LED_WIDTH[4:0]					0x0320	R/W
		[7:0]	SLOTB_LED_OFFSET[7:0]									
0x36	SLOTB_NUMPULSES	[15:8]	SLOTB_PULSES[7:0]								0x0818	R/W
		[7:0]	SLOTB_PERIOD[7:0]									
0x37	ALT_PWR_DN	[15:8]	CH34_DISABLE[15:13]			CH2_DISABLE[12:10]			SLOTB_PERIOD[9:8]		0x0000	R/W
		[7:0]	Reserved						SLOTA_PERIOD[9:8]			
0x38	EXT_SYNC_STARTUP	[15:8]	EXT_SYNC_STARTUP[15:8]								0x000	R/W
		[7:0]	EXT_SYNC_STARTUP[7:0]									
0x39	SLOTA_AFE_WINDOW	[15:8]	SLOTA_AFE_WIDTH[4:0]					SLOTA_AFE_OFFSET[10:8]			0x22FC	R/W
		[7:0]	SLOTA_AFE_OFFSET[7:0]									
0x3B	SLOTB_AFE_WINDOW	[15:8]	SLOTB_AFE_WIDTH[4:0]					SLOTB_AFE_OFFSET[10:8]			0x22FC	R/W
		[7:0]	SLOTB_AFE_OFFSET[7:0]									
0x3C	AFE_PWR_CFG1	[15:8]	Reserved		Reserved			Reserved	V_CATHODE	AFE_POWER-DOWN[5]	0x3006	R/W
		[7:0]	AFE_POWERDOWN[4:0]					Reserved				
0x3E	SLOTA_FLOAT_LED	[15:8]	FLT_LED_SELECT_A[1:0]		Reserved	FLT_LED_WIDTH_A[4:0]					0x0320	R/W
		[7:0]	FLT_LED_OFFSET_A[7:0]									
0x3F	SLOTB_FLOAT_LED	[15:8]	FLT_LED_SELECT_B[1:0]		Reserved	FLT_LED_WIDTH_B[4:0]					0x0320	R/W
		[7:0]	FLT_LED_OFFSET_B[7:0]									
0x42	SLOTA_TIA_CFG	[15:8]	SLOTA_AFE_MODE[5:0]						SLOTA_INT_GAIN[1:0]		0x1C38	R/W
		[7:0]	SLOTA_INT_AS_BUF	SLOTA_TIA_IND_EN	SLOTA_TIA_VREF[1:0]		Reserved (write 0x1)		SLOTA_TIA_GAIN[1:0]			
0x43	SLOTA_AFE_CFG	[15:8]	SLOTA_AFE_CFG[15:8]								0xADA5	R/W
		[7:0]	SLOTA_AFE_CFG[7:0]									
0x44	SLOTB_TIA_CFG	[15:8]	SLOTB_AFE_MODE[5:0]							SLOTB_INT_GAIN[1:0]	0x1C38	R/W
		[7:0]	SLOTB_INT_AS_BUF	SLOTB_TIA_IND_EN	SLOTB_TIA_VREF[1:0]		Reserved (write 0x1)		SLOTB_TIA_GAIN[1:0]			
0x45	SLOTB_AFE_CFG	[15:8]	SLOTB_AFE_CFG[15:8]								0xADA5	R/W
		[7:0]	SLOTB_AFE_CFG[7:0]									
0x4B	SAMPLE_CLK	[15:8]	Reserved							CLK32K_BYP	0x2612	R/W
		[7:0]	CLK32K_EN	Reserved	CLK32K_ADJUST[5:0]							
0x4D	CLK32M_ADJUST	[15:8]	Reserved								0x0098	R/W
		[7:0]	CLK32M_ADJUST[7:0]									
0x4F	EXT_SYNC_SEL	[15:8]	Reserved								0x2090	R/W
		[7:0]	Reserved	GPIO1_OE	GPIO1_IE	Reserved	EXT_SYNC_SEL[1:0]		GPIO0_IE	Reserved		

Hex. Addr.	Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	R/W
0x50	CLK32M_ CAL_EN	[15:8]	Reserved								0x0000	R/W
		[7:0]	Reserved	GPIO1_CTRL	CLK32M_ CAL_EN	Reserved						
0x54	AFE_PWR_ CFG2	[15:8]	Reserved		SLEEP_V_CATHODE [1:0]		SLOTB_V_CATHODE[1:0]		SLOTA_V_CATHODE[1:0]		0x0020	R/W
		[7:0]	REG54_VCAT_ ENABLE	Reserved								
0x55	TIA_INDEP_ GAIN	[15:8]	Reserved				SLOTB_TIA_GAIN_4[1:0]		SLOTB_TIA_GAIN_3[1:0]		0x0000	R/W
		[7:0]	SLOTB_TIA_GAIN_2[1:0]		SLOTA_TIA_GAIN_4[1:0]		SLOTA_TIA_GAIN_3[1:0]		SLOTA_TIA_GAIN_2[1:0]			
0x58	MATH	[15:8]	Reserved				FLT_MATH34_B[1:0]		FLT_MATH34_A[1:0]		0x0000	R/W
		[7:0]	ENA_INT_ AS_BUF	FLT_MATH12_B[1:0]		Reserved	Reserved	FLT_MATH12_A[1:0]		Reserved		
0x59	FLT_ CONFIG_B	[15:8]	Reserved	FLT_EN_B[1:0]		FLT_PRECON_B[4:0]					0x0808	R/W
		[7:0]	Reserved									
0x5A	FLT_ LED_FIRE	[15:8]	FLT_LED_FIRE_B[3:0]				FLT_LED_FIRE_A[3:0]				0x0010	R/W
		[7:0]	Reserved (write 0x10)									
0x5E	FLT_ CONFIG_A	[15:8]	Reserved	FLT_EN_A[1:0]		FLT_PRECON_A[4:0]					0x0808	R/W
		[7:0]	Reserved									
0x5F	DATA_ ACCESS_CTL	[15:8]	Reserved								0x0000	R/W
		[7:0]	Reserved					SLOTB_ DATA_ HOLD	SLOTA_ DATA_ HOLD	DIGITAL_ CLOCK_ ENA		
0x60	FIFO_ ACCESS	[15:8]	FIFO_DATA[15:8]								0x0000	R
		[7:0]	FIFO_DATA[7:0]									
0x64	SLOTA_ PD1_16BIT	[15:8]	SLOTA_CH1_16BIT[15:8]								0x0000	R
		[7:0]	SLOTA_CH1_16BIT[7:0]									
0x65	SLOTA_ PD2_16BIT	[15:8]	SLOTA_CH2_16BIT[15:8]								0x0000	R
		[7:0]	SLOTA_CH2_16BIT[7:0]									
0x66	SLOTA_ PD3_16BIT	[15:8]	SLOTA_CH3_16BIT[15:8]								0x0000	R
		[7:0]	SLOTA_CH3_16BIT[7:0]									
0x67	SLOTA_ PD4_16BIT	[15:8]	SLOTA_CH4_16BIT[15:8]								0x0000	R
		[7:0]	SLOTA_CH4_16BIT[7:0]									
0x68	SLOTB_ PD1_16BIT	[15:8]	SLOTB_CH1_16BIT[15:8]								0x0000	R
		[7:0]	SLOTB_CH1_16BIT[7:0]									
0x69	SLOTB_ PD2_16BIT	[15:8]	SLOTB_CH2_16BIT[15:8]								0x0000	R
		[7:0]	SLOTB_CH2_16BIT[7:0]									
0x6A	SLOTB_ PD3_16BIT	[15:8]	SLOTB_CH3_16BIT[15:8]								0x0000	R
		[7:0]	SLOTB_CH3_16BIT[7:0]									
0x6B	SLOTB_ PD4_16BIT	[15:8]	SLOTB_CH4_16BIT[15:8]								0x0000	R
		[7:0]	SLOTB_CH4_16BIT[7:0]									
0x70	A_PD1_LOW	[15:8]	SLOTA_CH1_LOW[15:8]								0x0000	R
		[7:0]	SLOTA_CH1_LOW[7:0]									
0x71	A_PD2_LOW	[15:8]	SLOTA_CH2_LOW[15:8]								0x0000	R
		[7:0]	SLOTA_CH2_LOW[7:0]									
0x72	A_PD3_LOW	[15:8]	SLOTA_CH3_LOW[15:8]								0x0000	R
		[7:0]	SLOTA_CH3_LOW[7:0]									
0x73	A_PD4_LOW	[15:8]	SLOTA_CH4_LOW[15:8]								0x0000	R
		[7:0]	SLOTA_CH4_LOW[7:0]									
0x74	A_PD1_HIGH	[15:8]	SLOTA_CH1_HIGH[15:8]								0x0000	R
		[7:0]	SLOTA_CH1_HIGH[7:0]									
0x75	A_PD2_HIGH	[15:8]	SLOTA_CH2_HIGH[15:8]								0x0000	R
		[7:0]	SLOTA_CH2_HIGH[7:0]									
0x76	A_PD3_HIGH	[15:8]	SLOTA_CH3_HIGH[15:8]								0x0000	R
		[7:0]	SLOTA_CH3_HIGH[7:0]									
0x77	A_PD4_HIGH	[15:8]	SLOTA_CH4_HIGH[15:8]								0x0000	R
		[7:0]	SLOTA_CH4_HIGH[7:0]									
0x78	B_PD1_LOW	[15:8]	SLOTB_CH1_LOW[15:8]								0x0000	R
		[7:0]	SLOTB_CH1_LOW[7:0]									
0x79	B_PD2_LOW	[15:8]	SLOTB_CH2_LOW[15:8]								0x0000	R
		[7:0]	SLOTB_CH2_LOW[7:0]									

Hex. Addr.	Name	Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Reset	R/W
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
0x7A	B_PD3_LOW	[15:8]	SLOTB_CH3_LOW[15:8]								0x0000	R
		[7:0]	SLOTB_CH3_LOW[7:0]									
0x7B	B_PD4_LOW	[15:8]	SLOTB_CH4_LOW[15:8]								0x0000	R
		[7:0]	SLOTB_CH4_LOW[7:0]									
0x7C	B_PD1_HIGH	[15:8]	SLOTB_CH1_HIGH[15:8]								0x0000	R
		[7:0]	SLOTB_CH1_HIGH[7:0]									
0x7D	B_PD2_HIGH	[15:8]	SLOTB_CH2_HIGH[15:8]								0x0000	R
		[7:0]	SLOTB_CH2_HIGH[7:0]									
0x7E	B_PD3_HIGH	[15:8]	SLOTB_CH3_HIGH[15:8]								0x0000	R
		[7:0]	SLOTB_CH3_HIGH[7:0]									
0x7F	B_PD4_HIGH	[15:8]	SLOTB_CH4_HIGH[15:8]								0x0000	R
		[7:0]	SLOTB_CH4_HIGH[7:0]									

LED CONTROL REGISTERS

Table 37. LED Control Registers

Address	Data Bit	Default Value	Access	Name	Description
0x14	[15:12]	0x0	R/W	Reserved	Write 0x0 to these bits for proper operation.
	[11:8]	0x5	R/W	SLOTB_PD_SEL	PDx connection selection for Time Slot B. See the Time Slot Switch section for detailed descriptions.
	[7:4]	0x4	R/W	SLOTA_PD_SEL	PDx connection selection for Time Slot A. See the Time Slot Switch section for detailed descriptions.
	[3:2]	0x0	R/W	SLOTB_LED_SEL	Time Slot B LED configuration. These bits determine which LED is associated with Time Slot B. 0x0: pulse PDx connection to AFE. Float mode and pulse connect mode enable. 0x1: LEDX1 pulses during Time Slot B. 0x2: LEDX2 pulses during Time Slot B. 0x3: LEDX3 pulses during Time Slot B.
	[1:0]	0x1	R/W	SLOTA_LED_SEL	Time Slot A LED configuration. These bits determine which LED is associated with Time Slot A. 0x0: pulse PDx connection to AFE. Float mode and pulse connect mode enable. 0x1: LEDX1 pulses during Time Slot A. 0x2: LEDX2 pulses during Time Slot A. 0x3: LEDX3 pulses during Time Slot A.
0x22	[15:14]	0x0	R/W	Reserved	Write 0x0.
	13	0x1	R/W	ILED3_SCALE	LEDX3 current scale factor. 1: 100% strength. 0: 10% strength; sets the LEDX3 driver in low power mode. LEDX3 Current Scale = 0.1 + 0.9 × (Register 0x22, Bit 13).
	12	0x1	R/W	Reserved	Write 0x1.
	[11:7]	0x0	R/W	Reserved	Write 0x0.
	[6:4]	0x0	R/W	ILED3_SLEW	LEDX3 driver slew rate control. The slower the slew rate, the safer the performance in terms of reducing the risk of overvoltage of the LED driver. 0x0: the slowest slew rate. … 0x7: the fastest slew rate.
	[3:0]	0x0	R/W	ILED3_COARSE	LEDX3 coarse current setting. Coarse current sink target value of LEDX3 in standard operation. 0x0: lowest coarse setting. … 0xF: highest coarse setting. $LED3_{PEAK} = LED3_{COARSE} \times LED3_{FINE} \times LED3_{SCALE}$ where: $LED3_{PEAK}$ is the LEDX3 peak target value (mA). $LED3_{COARSE}$ = 50.3 + 19.8 × (Register 0x22, Bits[3:0]). $LED3_{FINE}$ = 0.74 + 0.022 × (Register 0x25, Bits[15:11]). $LED3_{SCALE}$ = 0.1 + 0.9 × (Register 0x22, Bit 13).
0x23	[15:14]	0x0	R/W	Reserved	Write 0x0.
	13	0x1	R/W	ILED1_SCALE	LEDX1 current scale factor. 1: 100% strength. 0: 10% strength; sets the LEDX1 driver in low power mode. *LEDX1 Current Scale* = 0.1 + 0.9 × (Register 0x23, Bit 13).
	12	0x1	R/W	Reserved	Write 0x1.
	[11:7]	0x0	R/W	Reserved	Write 0x0.

Address	Data Bit	Default Value	Access	Name	Description
	[6:4]	0x0	R/W	ILED1_SLEW	LEDX1 driver slew rate control. The slower the slew rate, the safer the performance in terms of reducing the risk of overvoltage of the LED driver. 0: the slowest slew rate. … 7: the fastest slew rate.
	[3:0]	0x0	R/W	ILED1_COARSE	LEDX1 coarse current setting. Coarse current sink target value of LEDX1 in standard operation. 0x0: lowest coarse setting. … 0xF: highest coarse setting. $LED1_{PEAK} = LED1_{COARSE} \times LED1_{FINE} \times LED1_{SCALE}$ where: $LED1_{PEAK}$ is the LEDX1 peak target value (mA). $LED1_{COARSE}$ = 50.3 + 19.8 × (Register 0x23, Bits[3:0]). $LED1_{FINE}$ = 0.74 + 0.022 × (Register 0x25, Bits[4:0]). $LED1_{SCALE}$ = 0.1 + 0.9 × (Register 0x23, Bit 13).
0x24	[15:14]	0x0	R/W	Reserved	Write 0x0.
	13	0x1	R/W	ILED2_SCALE	LEDX2 current scale factor. 1: 100% strength. 0: 40% strength; sets the LEDX2 driver in low power mode. *LED2 Current Scale* = 0.1 + 0.9 × (Register 0x24, Bit 13)
	12	0x1	R/W	Reserved	Write 0x1.
	[11:7]	0x0	R/W	Reserved	Write 0x0.
	[6:4]	0x0	R/W	ILED2_SLEW	LEDX2 driver slew rate control. The slower the slew rate, the safer the performance in terms of reducing the risk of overvoltage of the LED driver. 0: the slowest slew rate. … 7: the fastest slew rate.
	[3:0]	0x0	R/W	ILED2_COARSE	LEDX2 coarse current setting. Coarse current sink target value of LEDX2 in standard operation. 0x0: lowest coarse setting. … 0xF: highest coarse setting. $LED2_{PEAK} = LED2_{COARSE} \times LED2_{FINE} \times LED2_{SCALE}$ where: $LED2_{PEAK}$ is the LEDX2 peak target value (mA). $LED2_{COARSE}$ = 50.3 + 19.8 × (Register 0x24, Bits[3:0]). $LED2_{FINE}$ = 0.74 + 0.022 × (Register 0x25, Bits[10:6]). $LED2_{SCALE}$ = 0.1 + 0.9 × (Register 0x24, Bit 13).
0x25	[15:11]	0xC	R/W	ILED3_FINE	LEDX3 fine adjust. Current adjust multiplier for LED3. *LEDX3 fine adjust* = 0.74 + 0.022 × (Register 0x25, Bits[15:11]). See Register 0x22, Bits[3:0], for the full LED3 formula.
	[10:6]	0xC	R/W	ILED2_FINE	LEDX2 fine adjust. Current adjust multiplier for LED2. *LEDX2 fine adjust* = 0.74 + 0.022 × (Register 0x25, Bits[10:6]). See Register 0x24, Bits[3:0], for the full LED2 formula.
	5	0x0	R/W	Reserved	Write 0x0.
	[4:0]	0xC	R/W	ILED1_FINE	LEDX1 fine adjust. Current adjust multiplier for LED1. *LEDX1 Fine Adjust* = 0.74 + 0.022 × (Register 0x25, Bits[4:0]). See Register 0x23, Bits[3:0], for the full LED1 formula.
0x30	[15:13]	0x0	R/W	Reserved	Write 0x0.
	[12:8]	0x3	R/W	SLOTA_LED_WIDTH	LED pulse width (in 1 µs step) for Time Slot A.
	[7:0]	0x20	R/W	SLOTA_LED_OFFSET	LED offset width (in 1 µs step) for Time Slot A.

Address	Data Bit	Default Value	Access	Name	Description
0x31	[15:8]	0x08	R/W	SLOTA_PULSES	LED Time Slot A pulse count. n_A: number of LED pulses in Time Slot A.
	[7:0]	0x18	R/W	SLOTA_PERIOD	LED Time Slot A pulse period (in 1 µs step).
0x34	[15:10]	0x00	R/W	Reserved	Write 0x0.
	9	0x0	R/W	SLOTB_LED_DIS	Time Slot B LED disable. 1: disables the LED assigned to Time Slot B. Register 0x34 keeps the drivers active and prevents them from pulsing current to the LEDs. Disabling both LEDs via this register is often used to measure the dark level. Use Register 0x11 instead to enable or disable the actual time slot usage and not only the LED.
	8	0x0	R/W	SLOTA_LED_DIS	Time Slot A LED disable. 1: disables the LED assigned to Time Slot A. Use Register 0x11 instead to enable or disable the actual time slot usage and not only the LED.
	[7:0]	0x00	R/W	Reserved	Write 0x00.
0x35	[15:13]	0x0	R/W	Reserved	Write 0x0.
	[12:8]	0x3		SLOTB_LED_WIDTH	LED pulse width (in 1 µs step) for Time Slot B.
	[7:0]	0x20		SLOTB_LED_OFFSET	LED offset width (in 1 µs step) for Time Slot B.
0x36	[15:8]	0x08	R/W	SLOTB_PULSES	LED Time Slot B pulse count. n_B: number of LED pulses in Time Slot B.
	[7:0]	0x18	R/W	SLOTB_PERIOD	LED Time Slot B pulse period (in 1 µs step).

AFE CONFIGURATION REGISTERS

Table 38. AFE Global Configuration Registers

Address	Data Bit	Default Value	Access	Name	Description
0x37	[15:13]	0x0	R/W	CH34_DISABLE	Power-down options for Channel 3 and Channel 4 only. Bit 13: power down Channel 3, Channel 4 TIA op amp. Bit 14: power down Channel 3, Channel 4 BPF op amp. Bit 15: power down Channel 3, Channel 4 integrator op amp.
	[12:10]	0x0	R/W	CH2_DISABLE	Bit 10: power down Channel 2 TIA op amp. Bit 11: power down Channel 2 BPF op amp. Bit 12: power down Channel 2 integrator op amp.
	[9:8]	0x0	R/W	SLOTB_PERIOD	8 MSBs of LED Time Slot B pulse period.
	[7:2]	0x000	R/W	Reserved	Write 0x000.
	[1:0]	0x0	R/W	SLOTA_PERIOD	8 MSBs of LED Time Slot A pulse period.
0x3C	[15:14]	0x0	R/W	Reserved	Write 0x0.
	[13:11]	0x6	R/W	Reserved	Write 0x6.
	10	0x0	R/W	Reserved	Reserved.
	9	0x0	R/W	V_CATHODE	0x0: 1.3 V (identical to anode voltage). 0x1: 1.8 V (reverse bias photodiode by 550 mV). This setting may add noise.
	[8:3]	0x00	R/W	AFE_POWERDOWN	AFE channels power-down select. 0x0: keeps all channels on. Bit 3: power down Channel 1 TIA op amp. Bit 4: power down Channel 1 BPF op amp. Bit 5: power down Channel 1 integrator op amp. Bit 6: power down Channel 2, Channel 3, and Channel 4 TIA op amp. Bit 7: power down Channel 2, Channel 3, and Channel 4 BPF op amp. Bit 8: power down Channel 2, Channel 3, and Channel 4 integrator op amp.
	[2:0]	0x6	R/W	Reserved	Write 0x6.

Address	Data Bit	Default Value	Access	Name	Description
0x54	[15:14]	0x0	R/W	Reserved	Write 0x0.
	[13:12]	0x0	R/W	SLEEP_V_CATHODE	If Bit 7 = 1; this setting is applied to the cathode voltage while the device is in sleep mode. 0x0: V_{DD}. 0x1: AFE VREF during idle, V_{DD} during sleep. 0x2: floating. 0x3: 0.0 V.
	[11:10]	0x0	R/W	SLOTB_V_CATHODE	If Bit 7 = 1; this setting is applied to the cathode voltage while the device is in Time Slot B operation. The anode voltage is determined by Register 0x44, Bits[5:4]. 0x0: V_{DD} (1.8 V). 0x1: equal to PD anode voltage. 0x2: sets a reverse PD bias of ~250 mV (recommended setting). 0x3: 0.0 V (this forward biases a diode at the input).
	[9:8]	0x0	R/W	SLOTA_V_CATHODE	If Bit 7 = 1; this setting is applied to the cathode voltage while the device is in Time Slot A operation. The anode voltage is determined by Register 0x42, Bits[5:4]. 0x0: V_{DD} (1.8 V). 0x1: equal to PD anode voltage. 0x2: sets a reverse PD bias of ~250 mV (recommended setting). 0x3: 0.0 V (this forward biases a diode at the input).
	7	0x0	R/W	REG54_VCAT_ENABLE	0: use the cathode voltage settings defined by Register 0x3C, Bit 9. 1: override Register 0x3C, Bit 9 with cathode settings defined by Register 0x54, Bits[13:8].
	[6:0]	0x20	R/W	Reserved	Reserved.
0x55	[15:12]	0x0	R/W	Reserved	Write 0x0.
	[11:10]	0x0	R/W	SLOTB_TIA_GAIN_4	TIA gain for Time Slot B, Channel 4 when Register 0x44, Bit 6 = 1. 0: 200 kΩ. 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
	[9:8]	0x0	R/W	SLOTB_TIA_GAIN_3	TIA gain for Time Slot B, Channel 3 when Register 0x44, Bit 6 = 1. 0: 200 kΩ 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
	[7:6]	0x0	R/W	SLOTB_TIA_GAIN_2	TIA gain for Time Slot B, Channel 2 when Register 0x44, Bit 6 = 1. 0: 200 kΩ 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
	[5:4]	0x0	R/W	SLOTA_TIA_GAIN_4	TIA gain for Time Slot A, Channel 4 when Register 0x42, Bit 6 = 1. 0: 200 kΩ 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.

Address	Data Bit	Default Value	Access	Name	Description
	[3:2]	0x0	R/W	SLOTA_TIA_GAIN_3	TIA gain for Time Slot A, Channel 3 when Register 0x42, Bit 6 = 1. 0: 200 kΩ 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
	[1:0]	0x0	R/W	SLOTA_TIA_GAIN_2	TIA gain for Time Slot A, Channel 2 when Register 0x42, Bit 6 = 1. 0: 200 kΩ 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.

Table 39. AFE Configuration Registers, Time Slot A

Address	Data Bit	Default Value	Access	Name	Description
0x17	[15:4]	0x000	R/W	Reserved	Write 0x000
	[3:0]	0x0	R/W	INTEG_ORDER_A	Integration sequence order for Time Slot A. Each bit corresponds to the polarity of the integration sequence of a single pulse in a four-pulse sequence. Bit 0 controls the integration sequence of Pulse 1, Bit 1 controls Pulse 2, Bit 2 controls Pulse 3, and Bit 3 controls Pulse 4. After four pulses, the sequence repeats. 0: normal integration sequence. 1: reversed integration sequence.
0x39	[15:11]	0x4	R/W	SLOTA_AFE_WIDTH	AFE integration window width (in 1 µs step) for Time Slot A.
	[10:0]	0x2FC	R/W	SLOTA_AFE_OFFSET	AFE integration window offset for Time Slot A in 31.25 ns steps.
0x42	[15:10]	0x07	R/W	SLOTA_AFE_MODE	Set to 0x07.
	[9:8]	0x0	R/W	SLOTA_INT_GAIN	For normal mode, 00: R_{INT} = 400 kΩ. 01: R_{INT} = 200 kΩ. 10: R_{INT} = 100 kΩ. For TIA ADC mode with integrator configured as buffer, 00: integrator as buffer gain = 1.0. 01: integrator as buffer gain = 1.0. 10: integrator as buffer gain = 0.7.
	7	0x0	R/W	SLOTA_INT_AS_BUF	0: normal integrator configuration. 1: converts integrator to buffer amplifier (used in TIA ADC mode only).
	6	0x0	R/W	SLOTA_TIA_IND_EN	Enable Time Slot A TIA gain individual settings. When it is enabled, the Channel 1 TIA gain is set via Register 0x42, Bits[1:0], and the Channel 2 through Channel 4 TIA gain is set via Register 0x55, Bits[5:0]. 0: disable TIA gain individual setting. 1: enable TIA gain individual setting.
	[5:4]	0x3	R/W	SLOTA_TIA_VREF	Set V_{REF} of the TIA for Time Slot A. 0: 1.14 V. 1: 1.01 V. 2: 0.90 V. 3: 1.27 V (default recommended).
	[3:2]	0x2	R/W	Reserved	Reserved. Write 0x1.

Address	Data Bit	Default Value	Access	Name	Description
	[1:0]	0x0	R/W	SLOTA_TIA_GAIN	Transimpedance amplifier gain for Time Slot A. When SLOTA_TIA_IND_EN is enabled, this value is for Time Slot B, Channel 1 TIA gain. When this bit is disabled, it is for all four Time Slot A channel, TIA gain settings. 0: 200 kΩ. 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
0x43	[15:0]	0xADA5	R/W	SLOTA_AFE_CFG	AFE connection in Time Slot A. 0xADA5: analog full path mode (TIA_BPF_INT_ADC). 0xAE65: TIA ADC mode (must set Register 0x42, Bit 7 = 1 and Register 0x58, Bit 7 = 1). 0xB065: TIA ADC mode (if Register 0x42, Bit 7 = 0). Others: reserved.

Table 40. AFE Configuration Registers, Time Slot B

Address	Data Bit	Default Value	Access	Name	Description
0x1D	[15:4]	0x000	R/W	Reserved	Write 0x000
	[3:0]	0x0	R/W	INTEG_ORDER_B	Integration sequence order for Time Slot B. Each bit corresponds to the polarity of the integration sequence of a single pulse in a four-pulse sequence. Bit 0 controls the integration sequence of Pulse 1, Bit 1 controls Pulse 2, Bit 2 controls Pulse 3, and Bit 3 controls Pulse 4. After four pulses, the sequence repeats. 0: normal integration sequence. 1: reversed integration sequence
0x3B	[15:11]	0x04	R/W	SLOTB_AFE_WIDTH	AFE integration window width (in 1 µs step) for Time Slot B.
	[10:0]	0x17	R/W	SLOTB_AFE_OFFSET	AFE integration window offset for Time Slot B in 31.25 ns steps.
0x44	[15:10]	0x07	R/W	SLOTB_AFE_MODE	Set to 0x07.
	[9:8]	0x0	R/W	SLOTB_INT_GAIN	For normal mode, 00: R_{INT} = 400 kΩ. 01: R_{INT} = 200 kΩ. 10: R_{INT} = 100 kΩ. For TIA ADC mode with integrator configured as buffer, 00: integrator as buffer gain = 1.0. 01: integrator as buffer gain = 1.0. 10: integrator as buffer gain = 0.7.
	7	0x0	R/W	SLOTB_INT_AS_BUF	0: normal integrator configuration. 1: convert integrator to buffer amplifier (used in TIA ADC mode only).
	6	0x0	R/W	SLOTB_TIA_IND_EN	Enable Time Slot B TIA gain individual settings. When it is enabled, the Channel 1 TIA gain is set via Register 0x44, Bits[1:0], and the Channel 2 through Channel 4 TIA gain is set via Register 0x55, Bits[11:6]. 0: disable TIA gain individual setting. 1: enable TIA gain individual setting.
	[5:4]	0x3	R/W	SLOTB_TIA_VREF	Set VREF of the TIA for Time Slot B. 0: 1.14 V. 1: 1.01 V. 2: 0.90 V. 3: 1.27 V (default recommended).
	[3:2]	0x2	R/W	Reserved	Write 0x1.

Address	Data Bit	Default Value	Access	Name	Description
	[1:0]	0x0	R/W	SLOTB_TIA_GAIN	Transimpedance amplifier gain for Time Slot B. When SLOTB_TIA_IND_EN is enabled, this value is for Time Slot B, Channel 1 TIA gain. When SLOTB_TIA_IND_EN is disabled, it is for all four Time Slot B channel TIA gain settings. 0: 200 kΩ. 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
0x45	[15:0]	0xADA5	R/W	SLOTB_AFE_CFG	AFE connection in Time Slot B. 0xADA5: analog full path mode (TIA_BPF_INT_ADC). 0xAE65: TIA ADC mode (must set Register 0x44, Bit 7 = 1 and Register 0x58, Bit 7 = 1). 0xB065: TIA ADC mode (if Register 0x44, Bit 7 = 0). Others: reserved.

FLOAT MODE REGISTERS

Table 41. Float Mode Registers

Address	Data Bit	Default Value	Access	Name	Description
0x04	[15:8]	0x0	R	Reserved	Not applicable.
	[7:4]	0x0	R	BG_STATUS_B	Status of comparison between background light level and background threshold value for Time Slot B (BG_THRESH_B). A 1 in any bit location means the threshold has been crossed BG_COUNT_B number of times. This register is cleared after it is read. Bit 4: Time Slot B, Channel 1 exceeded threshold count. Bit 5: Time Slot B, Channel 2 exceeded threshold count. Bit 6: Time Slot B, Channel 3 exceeded threshold count. Bit 7: Time Slot B, Channel 4 exceeded threshold count.
	[3:0]	0x0	R	BG_STATUS_A	Status of comparison between background light level and background threshold value for Time Slot A (BG_THRESH_A). A 1 in any bit location means the threshold has been crossed BG_COUNT_A number of times. This register is cleared once it is read. Bit 0: Time Slot A, Channel 1 exceeded threshold count. Bit 1: Time Slot A, Channel 2 exceeded threshold count. Bit 2: Time Slot A, Channel 3 exceeded threshold count. Bit 3: Time Slot A, Channel 4 exceeded threshold count.
0x16	[15:14]	0x0	R/W	BG_COUNT_A	For Time Slot A, this is the number of times the ADC value exceeds the BG_THRESH_A value during the float mode subtract cycles before the BG_STATUS_A bit is set. 0: never set BG_STATUS_A. 1: set when BG_THRESH_A is exceeded 1 time. 2: set when BG_THRESH_A is exceeded 4 times. 3: set when BG_THRESH_A is exceeded 16 times.
	[13:0]	0x0	R/W	BG_THRESH_A	The background threshold for Time Slot A that is compared against the ADC result during the subtract cycles during float mode. If the ADC result exceeds the value in this register, BG_COUNT_A is incremented.
0x1C	[15:14]	0x0	R/W	BG_COUNT_B	For Time Slot B, this is the number of times the ADC value exceeds the BG_THRESH_B value during the float mode subtract cycles before the BG_STATUS_B bit is set. 0: never set BG_STATUS_B. 1: set when BG_THRESH_B is exceeded 1 time. 2: set when BG_THRESH_B is exceeded 4 times. 3: set when BG_THRESH_B is exceeded 16 times.

Address	Data Bit	Default Value	Access	Name	Description
	[13:0]	0x0	R/W	BG_THRESH_B	The background threshold for Time Slot B that is compared against the ADC result during the subtract cycles during float mode. If the ADC result exceeds the value in this register, BG_COUNT_B is incremented.
0x3E	[15:14]	0x0	R/W	FLT_LED_SELECT_A	Time Slot A LED selection for float LED mode. 0: no LED selected. 1: LED1. 2: LED2. 3: LED3.
	13	0	R/W	Reserved	Write 0x0.
	[12:8]	0x03	R/W	FLT_LED_WIDTH_A	Time Slot A LED pulse width for LED float mode in 1 µs steps.
	[7:0]	0x20	R/W	FLT_LED_OFFSET_A	Time to first LED pulse in float mode for Time Slot A.
0x3F	[15:14]	0x0	R/W	FLT_LED_SELECT_B	Time Slot B LED selection for float LED mode. 0: no LED selected. 1: LED1. 2: LED2. 3: LED3.
	13	0	R/W	Reserved	Write 0x0.
	[12:8]	0x03	R/W	FLT_LED_WIDTH_B	Time Slot B LED pulse width for LED float mode in 1 µs steps.
	[7:0]	0x20	R/W	FLT_LED_OFFSET_B	Time to first LED pulse in Float mode for Time Slot A.
0x58	[15:12]	0x0	R/W	Reserved	Reserved.
	[11:10]	0x0	R/W	FLT_MATH34_B	Time Slot B control for adding and subtracting Sample 3 and Sample 4 in a 4 pulse sequence (or any multiple of 4 pulses, for example, Sample 15 and Sample 16 in a 16-pulse sequence). 00: add third and fourth. 01: add third and subtract fourth. 10: subtract third and add fourth. 11: subtract third and fourth.
	[9:8]	0x0	R/W	FLT_MATH34_A	Time Slot A control for adding and subtracting Sample 3 and Sample 4 in a 4 pulse sequence (or any multiple of 4 pulses, for example, Sample 15 and Sample 16 in a 16-pulse sequence). 00: add third and fourth. 01: add third and subtract fourth. 10: subtract third and add fourth. 11: subtract third and fourth.
	7	0x0	R/W	ENA_INT_AS_BUF	Set to 1 to enable the configuration of the integrator as a buffer in TIA ADC mode.
	[6:5]	0x0	R/W	FLT_MATH12_B	Time Slot B control for adding and subtracting Sample 1 and Sample 2 in a 4 pulse sequence (or any multiple of 4 pulses, for example, Sample 13 and Sample 14 in a 16-pulse sequence). 00: add first and second. 01: add first and subtract second. 10: subtract first and add second. 11: subtract first and second.
	[4:3]	0x0	R/W	Reserved	Write 0x0.
	[2:1]	0x0	R/W	FLT_MATH12_A	Time Slot A control for adding and subtracting Sample 1 and Sample 2 in a 4 pulse sequence (or any multiple of 4 pulses, for example, Sample 13 and Sample 14 in a 16-pulse sequence). 00: add first and second. 01: add first and subtract second. 10: subtract first and add second. 11: subtract first and second.
	0	0x0	R/W	Reserved	Write 0x0.

Address	Data Bit	Default Value	Access	Name	Description
0x59	15	0x0	R/W	Reserved	Write 0x0.
	[14:13]	0x0	R/W	FLT_EN_B	0: default setting, float disabled for Time Slot B. 1: reserved. 2: reserved. 3: enable float mode.
	[12:8]	0x08	R/W	FLT_PRECON_B	Float mode preconditioning time for Time Slot B. Time to start of first float time, which is typically 16 µs.
	[7:0]	0x08	R/W	Reserved	Write 0x08.
0x5A	[15:12]	0x0	R/W	FLT_LED_FIRE_B	In any given sequence of four pulses, fire the LED in the selected position by writing a zero into that pulse position. Mask the LED pulse (that is, do not fire LED) by writing a 1 into that position. In a sequence of four pulses on Time Slot B, Register 0x5A, Bit 12, is the first pulse, Bit 13 is the second pulse, Bit 14 is the third pulse, and Bit 15 is the fourth pulse.
	[11:8]	0x0	R/W	FLT_LED_FIRE_A	In any given sequence of four pulses, fire the LED in the selected position by writing a zero into that pulse position. Mask the LED pulse (that is, do not fire LED) by writing a 1 into that position. In a sequence of four pulses on Time Slot A, Register 0x5A, Bit 8, is the first pulse, Bit 9 is the second pulse, Bit 10 is the third pulse, and Bit 11 is the fourth pulse.
	[7:0]	0x10	R/W	Reserved	Write 0x10.
0x5E	15	0x0	R/W	Reserved	Write 0x0.
	[14:13]	0x0	R/W	FLT_EN_A	0: default setting, float disabled for Time Slot A. 1: reserved 2: reserved 3: enable float mode in Time Slot A.
	[12:8]	0x08	R/W	FLT_PRECON_A	Float mode preconditioning time for Time Slot A. Time to start of first float time, which is typically 16 µs.
	[7:0]	0x08	R/W	Reserved	Write 0x08.

SYSTEM REGISTERS

Table 42. System Registers

Address	Data Bit	Default Value	Access	Name	Description
0x00	[15:8]	0x00	R/W	FIFO_SAMPLES	FIFO status. Number of available bytes to be read from the FIFO. When comparing this to the FIFO length threshold (Register 0x06, Bits[13:8]), note that the FIFO status value is in bytes and the FIFO length threshold is in words, where one word = two bytes. Write 1 to Bit 15 to clear the contents of the FIFO.
	7	0x0	R/W	Reserved	Write 0x1 to clear this bit to 0x0.
	6	0x0	R/W	SLOTB_INT	Time Slot B interrupt. Describes the type of interrupt event. A 1 indicates an interrupt of a particular event type has occurred. Write a 1 to clear the corresponding interrupt. After clearing, the register goes to 0. Writing a 0 to this register has no effect.
	5	0x0	R/W	SLOTA_INT	Time Slot A interrupt. Describes the type of interrupt event. A 1 indicates an interrupt of a particular event type has occurred. Write a 1 to clear the corresponding interrupt. After clearing, the register goes to 0. Writing a 0 to this register has no effect.
	[4:0]	0x00	R/W	Reserved	Write 0x1F to clear these bits to 0x00.
0x01	[15:9]	0x00	R/W	Reserved	Write 0x00.
	8	0x1	R/W	FIFO_INT_MASK	Sends an interrupt when the FIFO data length has exceeded the FIFO length threshold in Register 0x06, Bits[13:8]. A 0 enables the interrupt.

Address	Data Bit	Default Value	Access	Name	Description
	7	0x1	R/W	Reserved	Write 0x1.
	6	0x1	R/W	SLOTB_INT_MASK	Sends an interrupt on the Time Slot B sample. Write a 1 to disable the interrupt. Write a 0 to enable the interrupt.
	5	0x1	R/W	SLOTA_INT_MASK	Sends an interrupt on the Time Slot A sample. Write a 1 to disable the interrupt. Write a 0 to enable the interrupt.
	[4:0]	0x1F	R/W	Reserved	Write 0x1F.
0x02	[15:10]	0x00	R/W	Reserved	Write 0x0000.
	9	0x0	R/W	GPIO1_DRV	GPIO1 drive. 0: the GPIO1 pin is always driven. 1: the GPIO1 pin is driven when the interrupt is asserted; otherwise, it is left floating and requires a pull-up or pull-down resistor, depending on polarity (operates as open drain). Use this setting if multiple devices must share the GPIO1 pin.
	8	0x0	R/W	GPIO1_POL	GPIO1 polarity. 0: the GPIO1 pin is active high. 1: the GPIO1 pin is active low.
	[7:3]	0x00	R/W	Reserved	Write 0x00.
	2	0x0	R/W	GPIO0_ENA	GPIO0 pin enable. 0: disable the GPIO0 pin. The GPIO0 pin floats, regardless of interrupt status. The status register (Address 0x00) remains active. 1: enable the GPIO0 pin.
	1	0x0	R/W	GPIO0_DRV	GPIO0 drive. 0: the GPIO0 pin is always driven. 1: the GPIO0 pin is driven when the interrupt is asserted; otherwise, it is left floating and requires a pull-up or pull-down resistor, depending on polarity (operates as open drain). Use this setting if multiple devices must share the GPIO0 pin.
	0	0x0	R/W	GPIO0_POL	GPIO0 polarity. 0: the GPIO0 pin is active high. 1: the GPIO0 pin is active low.
0x06	[15:14]	0x0	R/W	Reserved	Write 0x0.
	[13:8]	0x00	R/W	FIFO_THRESH	FIFO length threshold. An interrupt is generated when the number of data-words in the FIFO exceeds the value in FIFO_THRESH. The interrupt pin automatically deasserts when the number of data-words available in the FIFO no longer exceeds the value in FIFO_THRESH.
	[7:0]	0x00	R/W	Reserved	Write 0x00.
0x08	[15:8]	0x0A	R	REV_NUM	Revision number.
	[7:0]	0x16	R	DEV_ID	Device ID.
0x09	[15:8]	0x00	W	ADDRESS_WRITE_KEY	Write 0xAD when writing to SLAVE_ADDRESS. Otherwise, do not access.
	[7:1]	0x64	R/W	SLAVE_ADDRESS	I^2C slave address.
	0	0x0	R	Reserved	Do not access.
0x0A	[15:12]	0x0	R	Reserved	Write 0x0.
	[11:0]	0x000	R	CLK_RATIO	When the CLK32M_CAL_EN bit (Register 0x50, Bit 5) is set, the device calculates the number of 32 MHz clock cycles in two cycles of the 32 kHz clock. The result, nominally 2000 (0x07D0), is stored in the CLK_RATIO bits.
0x0B	[15:13]	0x0	R/W	Reserved	Write 0x0.
	[12:8]	0x00	R/W	GPIO1_ALT_CFG	Alternate configuration for the GPIO1 pin. 0x00: GPIO1 is backward compatible to the ADPD103 PDSO pin functionality. 0x01: interrupt function provided on GPIO1, as defined in Register 0x01. 0x02: asserts at the start of the first time slot, deasserts at end of last time slot.

Address	Data Bit	Default Value	Access	Name	Description
					0x05: Time Slot A pulse output. 0x06: Time Slot B pulse output. 0x07: pulse output of both time slots. 0x0C: output data cycle occurred for Time Slot A. 0x0D: output data cycle occurred for Time Slot B. 0x0E: output data cycle occurred. 0x0F: toggles on every sample, which provides a signal at half the sampling rate. 0x10: output = 0. 0x11: output = 1. 0x13: 32 kHz oscillator output. Remaining settings are not supported.
	[7:5]	0x0	R/W	Reserved	Write 0x0.
	[4:0]	0x00	R/W	GPIO0_ALT_CFG	Alternate configuration for the GPIO0 pin. 0x0: GPIO0 is backward compatible to the ADPD103 INT pin functionality. 0x1: interrupt function provided on GPIO0, as defined in Register 0x01. 0x2: asserts at the start of the first time slot, deasserts at end of last time slot. 0x5: Time Slot A pulse output. 0x6: Time Slot B pulse output. 0x7: pulse output of both time slots. 0xC: output data cycle occurred for Time Slot A. 0xD: output data cycle occurred for Time Slot B. 0xE: output data cycle occurred. 0xF: toggles on every sample, which provides a signal at half the sampling rate. 0x10: output = 0. 0x11: output = 1. 0x13: 32 kHz oscillator output. Remaining settings are not supported.
0x0D	[15:0]	0x0000	R/W	SLAVE_ADDRESS_KEY	Enable changing the I²C address using Register 0x09. 0x04AD: enable address change always. 0x44AD: enable address change if GPIO0 is high. 0x84AD: enable address change if GPIO1 is high. 0xC4AD: enable address change if both GPIO0 and GPIO1 are high.
0x0F	[15:1]	0x0000	R	Reserved	Write 0x0000.
	0	0x0	R/W	SW_RESET	Software reset. Write 0x1 to reset the devices. This bit clears itself after a reset. For I²C communications, this command returns an acknowledge and the device subsequently returns to standby mode with all registers reset to the default state.
0x10	[15:2]	0x0000	R/W	Reserved	Write 0x000.
	[1:0]	0x0	R/W	Mode	Determines the operating mode of the ADPD1080/ADPD1081. 0x0: standby. 0x1: program. 0x2: normal operation.
0x11	[15:14]	0x0	R/W	Reserved	Reserved.
	13	0x0	R/W	RDOUT_MODE	Readback data mode for extended data registers. 0x0: block sum of N samples. 0x1: block average of N samples.
	12	0x1	R/W	FIFO_OVRN_PREVENT	0x0: wrap around FIFO, overwriting old data with new. 0x1: new data if FIFO is not full (recommended setting).

Address	Data Bit	Default Value	Access	Name	Description
	[11:9]	0x0	R/W	Reserved	Reserved.
	[8:6]	0x0	R/W	SLOTB_FIFO_MODE	Time Slot B FIFO data format. 0: no data to FIFO. 1: 16-bit sum of all four channels. 2: 32-bit sum of all four channels. 4: four channels of 16-bit sample data for Time Slot B. 6: four channels of 32-bit extended sample data for Time Slot B. Others: reserved. The selected Time Slot B data is saved in the FIFO. Available only if Time Slot A has the same averaging factor, N (Register 0x15, Bits[10:8] = Bits[6:4]), or if Time Slot A is not saving data to the FIFO (Register 0x11, Bits[4:2] = 0).
	5	0x0	R/W	SLOTB_EN	Time Slot B enable. 1: enables Time Slot B.
	[4:2]	0x0	R/W	SLOTA_FIFO_MODE	Time Slot A FIFO data format. 0: no data to FIFO. 1: 16-bit sum of all four channels. 2: 32-bit sum of all four channels. 4: four channels of 16-bit sample data for Time Slot A. 6: four channels of 32-bit extended sample data for Time Slot A. Others: reserved.
	1	0x0	R/W	Reserved	Write 0x0.
	0	0x0	R/W	SLOTA_EN	Time Slot A enable. 1: enables Time Slot A.
0x38	[15:0]	0x0000	R/W	EXT_SYNC_STARTUP	Write 0x4000 when EXT_SYNC_SEL is 01 or 10. Otherwise, write 0x0.
0x4B	[15:9]	0x13	R/W	Reserved	Write 0x13.
	8	0x0	R/W	CLK32K_BYP	Bypass internal 32 kHz oscillator. 0x0: normal operation. 0x1: provide external clock on the GPIO1 pin. The user must set Register 0x4F, Bits[6:5] = 01 to enable the GPIO1 pin as an input.
	7	0x0	R/W	CLK32K_EN	Sample clock power-up. Enables the data sample clock. 0x0: clock disabled. 0x1: normal operation.
	6	0x0	R/W	Reserved	Write 0x0.
	[5:0]	0x12	R/W	CLK32K_ADJUST	Data sampling (32 kHz) clock frequency adjust. This register is used to calibrate the sample frequency of the device to achieve high precision on the data rate as defined in Register 0x12. Adjusts the sample master 32 kHz clock by 0.6 kHz per LSB. For a 100 Hz sample rate as defined in Register 0x12, 1 LSB of Register 0x4B, Bits[5:0], is 1.9 Hz. Note that a larger value produces a lower frequency. See the Clocks and Timing Calibration section for more information regarding clock adjustment. 00 0000: maximum frequency. 10 0010: typical center frequency. 11 1111: minimum frequency.
0x4D	[15:8]	0x00	R/W	Reserved	Write 0x00.
	[7:0]	0x98	R/W	CLK32M_ADJUST	Internal timing (32 MHz) clock frequency adjust. This register is used to calibrate the internal clock of the device to achieve precisely timed LED pulses. Adjusts the 32 MHz clock by 109 kHz per LSB. See the Clocks and Timing Calibration section for more information regarding clock adjustment. 0000 0000: minimum frequency. 1001 1000: default frequency. 1111 1111: maximum frequency.

Address	Data Bit	Default Value	Access	Name	Description
0x4F	[15:8]	0x20	R/W	Reserved	Write 0x20.
	7	0x1	R/W	Reserved	Write 0x1.
	6	0x0	R/W	GPIO1_OE	GPIO1 pin output enable.
	5	0x0	R/W	GPIO1_IE	GPIO1 pin input enable.
	4	0x1	R/W	Reserved	Write 0x1.
	[3:2]	0x0	R/W	EXT_SYNC_SEL	Sample sync select. 00: use the internal 32 kHz clock with FSAMPLE to select sample timings. 01: use the GPIO0 pin to trigger sample cycle. 10: use the GPIO1 pin to trigger sample cycle. 11: reserved.
	1	0x0	R/W	GPIO0_IE	GPIO0 pin input enable.
	0	0x0	R/W	Reserved	Write 0x0.
0x50	[15:7]	0x000	R/W	Reserved	Write 0x000.
	6	0x0	R/W	GPIO1_CTRL	Controls the GPIO1 output when the GPIO1 output is enabled (GPIO1_OE = 0x1). 0x0: GPIO1 output driven low. 0x1: GPIO1 output driven by the AFE power-down signal.
	5	0x0	R/W	CLK32M_CAL_EN	As part of the 32 MHz clock calibration routine, write 1 to begin the clock ratio calculation. Read the result of this calculation from the CLK_RATIO bits in Register 0x0A. Reset this bit to 0 prior to reinitiating the calculation.
	[4:0]	0x00	R/W	Reserved	Write 0x0.
0x5F	[15:3]	0x0000	R/W	Reserved	Write 0x0000.
	2	0x0	R/W	SLOTB_DATA_HOLD	Setting this bit prevents the update of the data registers corresponding to Time Slot B. Set this bit to ensure that unread data registers are not updated, guaranteeing a contiguous set of data from all four photodiode channels. 1: hold data registers for Time Slot B. 0: allow data register update.
	1	0x0	R/W	SLOTA_DATA_HOLD	Setting this bit prevents the update of the data registers corresponding to Time Slot A. Set this bit to ensure that unread data registers are not updated, guaranteeing a contiguous set of data from all four photodiode channels. 1: hold data registers for Time Slot A. 0: allow data register update.
	0	0x0	R/W	DIGITAL_CLOCK_ENA	Set to 1 in order to enable the 32 MHz clock when calibrating the 32 MHz clock. Always disable the 32 MHz clock following the calibration by resetting this bit to 0.

ADC REGISTERS

Table 43. ADC Registers

Address	Data Bits	Default Value	Access	Name	Description
0x12	[15:0]	0x0028	R/W	FSAMPLE	Sampling frequency: f_{SAMPLE} = 32 kHz/(Register 0x12, Bits[15:0] × 4). For example, 100 Hz = 0x0050; 200 Hz = 0x0028.
0x15	[15:11]	0x00	R/W	Reserved	Write 0x0.
	[10:8]	0x6	R/W	SLOTB_NUM_AVG	Sample sum/average for Time Slot B. Specifies the averaging factor, N_B, which is the number of consecutive samples that is summed and averaged after the ADC. Register 0x70 to Register 0x7F hold the data sum. Register 0x64 to Register 0x6B and the data buffer in Register 0x60 hold the data average, which can be used to increase SNR without clipping, in 16-bit registers. The data rate is decimated by the value of the SLOTB_NUMB_AVG bits. 0: 1. 1: 2. 2: 4. 3: 8. 4: 16. 5: 32. 6: 64. 7: 128.
	7	0x0	R/W	Reserved	Write 0x0.
	[6:4]	0x0	R/W	SLOTA_NUM_AVG	Sample sum/average for Time Slot A. N_A: same as Bits[10:8] but for Time Slot A. See description in Register 0x15, Bits[10:8].
	[3:0]	0x0	R/W	Reserved	Write 0x0.
0x18	[15:0]	0x2000	R/W	SLOTA_CH1_OFFSET	Time Slot A Channel 1 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x19	[15:0]	0x2000	R/W	SLOTA_CH2_OFFSET	Time Slot A Channel 2 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x1A	[15:0]	0x2000	R/W	SLOTA_CH3_OFFSET	Time Slot A Channel 3 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x1B	[15:0]	0x2000	R/W	SLOTA_CH4_OFFSET	Time Slot A Channel 4 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x1E	[15:0]	0x2000	R/W	SLOTB_CH1_OFFSET	Time Slot B Channel 1 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x1F	[15:0]	0x2000	R/W	SLOTB_CH2_OFFSET	Time Slot B Channel 2 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x20	[15:0]	0x2000	R/W	SLOTB_CH3_OFFSET	Time Slot B Channel 3 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x21	[15:0]	0x2000	R/W	SLOTB_CH4_OFFSET	Time Slot B Channel 4 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.

DATA REGISTERS

Table 44. Data Registers

Address	Data Bits	Access	Name	Description
0x60	[15:0]	R	FIFO_DATA	Next available word in FIFO.
0x64	[15:0]	R	SLOTA_CH1_16BIT	16-bit value of Channel1 in Time Slot A.
0x65	[15:0]	R	SLOTA_CH2_16BIT	16-bit value of Channel 2 in Time Slot A.
0x66	[15:0]	R	SLOTA_CH3_16BIT	16-bit value of Channel 3 in Time Slot A.
0x67	[15:0]	R	SLOTA_CH4_16BIT	16-bit value of Channel 4 in Time Slot A.
0x68	[15:0]	R	SLOTB_CH1_16BIT	16-bit value of Channel 1 in Time Slot B.
0x69	[15:0]	R	SLOTB_CH2_16BIT	16-bit value of Channel 2 in Time Slot B.
0x6A	[15:0]	R	SLOTB_CH3_16BIT	16-bit value of Channel 3 in Time Slot B.
0x6B	[15:0]	R	SLOTB_CH4_16BIT	16-bit value of Channel 4 in Time Slot B.
0x70	[15:0]	R	SLOTA_CH1_LOW	Low data-word for Channel 1 in Time Slot A.
0x71	[15:0]	R	SLOTA_CH2_LOW	Low data-word for Channel 2 in Time Slot A.
0x72	[15:0]	R	SLOTA_CH3_LOW	Low data-word for Channel 3 in Time Slot A.
0x73	[15:0]	R	SLOTA_CH4_LOW	Low data-word for Channel 4 in Time Slot A.
0x74	[15:0]	R	SLOTA_CH1_HIGH	High data-word for Channel 1 in Time Slot A.
0x75	[15:0]	R	SLOTA_CH2_HIGH	High data-word for Channel 2 in Time Slot A.
0x76	[15:0]	R	SLOTA_CH3_HIGH	High data-word for Channel 3 in Time Slot A.
0x77	[15:0]	R	SLOTA_CH4_HIGH	High data-word for Channel 4 in Time Slot A.
0x78	[15:0]	R	SLOTB_CH1_LOW	Low data-word for Channel 1 in Time Slot B.
0x79	[15:0]	R	SLOTB_CH2_LOW	Low data-word for Channel 2 in Time Slot B.
0x7A	[15:0]	R	SLOTB_CH3_LOW	Low data-word for Channel 3 in Time Slot B.
0x7B	[15:0]	R	SLOTB_CH4_LOW	Low data-word for Channel 4 in Time Slot B.
0x7C	[15:0]	R	SLOTB_CH1_HIGH	High data-word for Channel 1 in Time Slot B.
0x7D	[15:0]	R	SLOTB_CH2_HIGH	High data-word for Channel 2 in Time Slot B.
0x7E	[15:0]	R	SLOTB_CH3_HIGH	High data-word for Channel 3 in Time Slot B.
0x7F	[15:0]	R	SLOTB_CH4_HIGH	High data-word for Channel 4 in Time Slot B.

REQUIRED START-UP LOAD PROCEDURE

The required start-up load procedure is as follows:

1. Write to 0x1 to Register 0x4B, Bit 7 to enable the clock that drives the state machine.
2. Write 0x0001 to Register 0x10 to enter program mode.
3. Write to the other registers; the register order is not important while the device is in program mode.
4. Write 0x0002 to Register 0x10 to start normal sampling operation.

OUTLINE DIMENSIONS

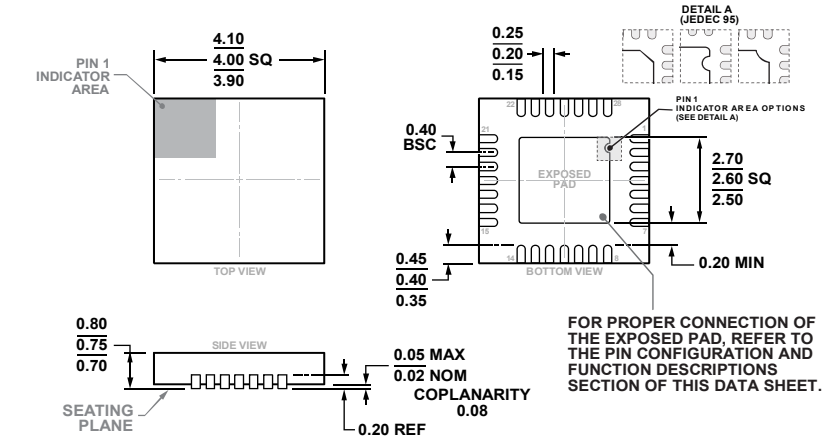

Figure 56. 28-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-28-5)
Dimensions shown in millimeters

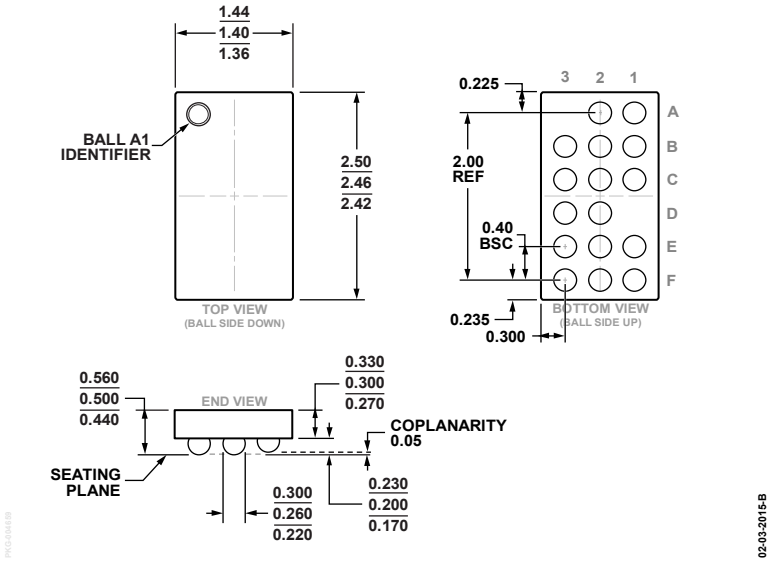

Figure 57. 16-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-16-18)
Dimensions shown in millimeters