Micropower, High Accuracy Voltage References

Data Sheet

ADR3525/ADR3530/ADR3533/ADR3540/ADR3550

FEATURES

- **Maximum temperature coefficient: 5 ppm/°C (B grade)**
- **Low long-term drift (LTD): 30 ppm (initial 1 khr typical)**
- **Initial output voltage error: ±0.1% (maximum)**
- **Operating temperature range: −40°C to +125°C**
- **Output current: +10 mA source/−3 mA sink**
- **Low quiescent current: 100 µA (maximum)**
- **Low dropout voltage: 250 mV at 2 mA**
- **Output voltage noise (0.1 Hz to 10 Hz): 29 µV p-p at 4.096 V (typical)**
- **Qualified for automotive applications**

APPLICATIONS

- **Automotive battery monitors**
- **Portable instrumentation**
- **Process transmitters**
- **Remote sensors**
- **Medical instrumentation**

PIN CONFIGURATION

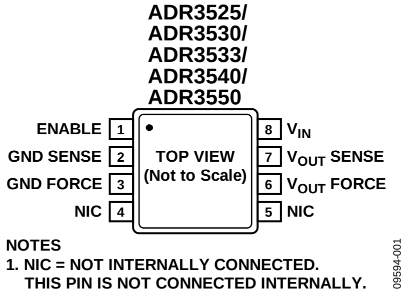

Figure 1. 8-Lead MSOP (RM-8 Suffix)

GENERAL DESCRIPTION

The ADR3525W, ADR3530W, ADR3533W, ADR3540W, and ADR3550W are low cost, low power, high precision CMOS voltage references, featuring a maximum temperature coefficient (TC) of 5 ppm/°C (B grade), 8 ppm/°C (A grade), low operating current, and low output noise in an 8-lead MSOP package. For high accuracy, the output voltage and temperature coefficient are trimmed digitally during final assembly using the Analog Devices, Inc., proprietary DigiTrim® technology.

The low output voltage hysteresis and low long-term output voltage drift improve lifetime system accuracy.

These CMOS references are available in five output voltages, all of which are specified over the automotive temperature range of −40°C to +125°C.

Table 1. Selection Guide

Model	Output Voltage (V)	Input Voltage Range (V)
ADR3525W	2.500	2.7 to 5.5
ADR3530W	3.000	3.2 to 5.5
ADR3533W	3.300	3.5 to 5.5
ADR3540W	4.096	4.3 to 5.5
ADR3550W	5.000	5.2 to 5.5

Rev. B

Document Feedback

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9/2018—Rev. A to Rev. B

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6/2018—Rev. 0 to Rev. A

Changed Patented to Proprietary ... Throughout
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9/2011—Revision 0: Initial Version

SPECIFICATIONS

ADR3525 ELECTRICAL CHARACTERISTICS

V_{IN} = 2.7 V to 5.5 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}		2.4975	2.500	2.5025	V
INITIAL OUTPUT VOLTAGE ERROR	V_{OERR}				±0.1	%
					±2.5	mV
TEMPERATURE COEFFICIENT	TCV_{OUT}	$-40°C \le T_A \le +125°C$				
A Grade				2.5	8	ppm/°C
B Grade				2.5	5	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 2.7 V to 5.5 V		5	50	ppm/V
		V_{IN} = 2.7 V to 5.5 V, $-40°C \le T_A \le +125°C$			120	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$					
Sourcing		I_L = 0 mA to 10 mA, V_{IN} = 3.0 V, $-40°C \le T_A \le +125°C$		10	30	ppm/mA
Sinking		I_L = 0 mA to −3 mA, V_{IN} = 3.0 V, $-40°C \le T_A \le +125°C$		10	50	ppm/mA
OUTPUT CURRENT CAPACITY	I_L					
Sourcing		V_{IN} = 3.0 V to 5.5 V	10			mA
Sinking		V_{IN} = 3.0 V to 5.5 V	−3			mA
QUIESCENT CURRENT	I_Q					
Normal Operation		ENABLE ≥ V_{IN} × 0.85			85	µA
		ENABLE = V_{IN}, $-40°C \le T_A \le +125°C$			100	µA
Shutdown		ENABLE ≤ 0.7 V			5	µA
DROPOUT VOLTAGE[1]	V_{DO}	I_L = 0 mA, $T_A = -40°C \le T_A \le +125°C$		50	200	mV
		I_L = 2 mA, $T_A = -40°C \le T_A \le +125°C$		75	250	mV
ENABLE PIN						
Shutdown Voltage	V_L		0		0.7	V
ENABLE Voltage	V_H		V_{IN} × 0.85		V_{IN}	V
ENABLE Pin Leakage Current	I_{EN}	ENABLE = V_{IN}, $T_A = -40°C \le T_A \le +125°C$		1	3	µA
OUTPUT VOLTAGE NOISE	e_n p-p	f = 0.1 Hz to 10 Hz		18		µV p-p
		f = 10 Hz to 10 kHz		42		µV rms
OUTPUT VOLTAGE NOISE DENSITY	e_n	f = 1 kHz		1		µV/√Hz
OUTPUT VOLTAGE HYSTERESIS[2]	ΔV_{OUT_HYS}	T_A = +25°C to −40°C to +125°C to +25°C		70		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 60 Hz		−60		dB
LONG-TERM OUTPUT VOLTAGE DRIFT	ΔV_{OUT_LTD}	1000 hours at 50°C		30		ppm
TURN-ON SETTLING TIME	t_R	C_{IN} = 0.1 µF, C_L = 0.1 µF, R_L = 1 kΩ		600		µs

[1] Refers to the minimum difference between V_{IN} and V_{OUT} such that V_{OUT} maintains a minimum accuracy of 0.1%. See the Terminology section.

[2] See the Terminology section. The part is placed through the temperature cycle in the order of temperatures shown.

ADR3530 ELECTRICAL CHARACTERISTICS

V_{IN} = 3.2 V to 5.5 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}		2.9970	3.0000	3.0030	V
INITIAL OUTPUT VOLTAGE ERROR	V_{OERR}				±0.1	%
					±3.0	mV
TEMPERATURE COEFFICIENT	TCV_{OUT}	−40°C ≤ T_A ≤ +125°C				
A Grade				2.5	8	ppm/°C
B Grade				2.5	5	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 3.2 V to 5.5 V		5	50	ppm/V
		V_{IN} = 3.2 V to 5.5 V, −40°C ≤ T_A ≤ +125°C			120	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$					
Sourcing		I_L = 0 mA to 10 mA, V_{IN} = 3.5 V, −40°C ≤ T_A ≤ +125°C		9	30	ppm/mA
Sinking		I_L = 0 mA to −3 mA, V_{IN} = 3.5 V, −40°C ≤ T_A ≤ +125°C		10	50	ppm/mA
OUTPUT CURRENT CAPACITY	I_L					
Sourcing		V_{IN} = 3.5 V to 5.5 V	10			mA
Sinking		V_{IN} = 3.5 V to 5.5 V	−3			mA
QUIESCENT CURRENT	I_Q					
Normal Operation		ENABLE ≥ V_{IN} × 0.85			85	µA
		ENABLE = V_{IN}, −40°C ≤ T_A ≤ +125°C			100	µA
Shutdown		ENABLE ≤ 0.7 V			5	µA
DROPOUT VOLTAGE[1]	V_{DO}	I_L = 0 mA, T_A = −40°C ≤ T_A ≤ +125°C		50	200	mV
		I_L = 2 mA, T_A = −40°C ≤ T_A ≤ +125°C		75	250	mV
ENABLE PIN						
Shutdown Voltage	V_L		0		0.7	V
ENABLE Voltage	V_H		V_{IN} × 0.85		V_{IN}	V
ENABLE Pin Leakage Current	I_{EN}	ENABLE = V_{IN}, T_A = −40°C ≤ T_A ≤ +125°C		0.85	3	µA
OUTPUT VOLTAGE NOISE	e_n p-p	f = 0.1 Hz to 10 Hz		22		µV p-p
		f = 10 Hz to 10 kHz		45		µV rms
OUTPUT VOLTAGE NOISE DENSITY	e_n	f = 1 kHz		1.1		µV/√Hz
OUTPUT VOLTAGE HYSTERESIS[2]	ΔV_{OUT_HYS}	T_A = +25°C to −40°C to +125°C to +25°C		70		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 60 Hz		−60		dB
LONG-TERM OUTPUT VOLTAGE DRIFT	ΔV_{OUT_LTD}	1000 hours at 50°C		30		ppm
TURN-ON SETTLING TIME	t_R	C_{IN} = 0.1 µF, C_L = 0.1 µF, R_L = 1 kΩ		700		µs

[1] Refers to the minimum difference between V_{IN} and V_{OUT} such that V_{OUT} maintains a minimum accuracy of 0.1%. See the Terminology section.

[2] See the Terminology section. The part is placed through the temperature cycle in the order of temperatures shown.

ADR3533 ELECTRICAL CHARACTERISTICS

V_{IN} = 3.5 V to 5.5 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}		3.2967	3.3000	3.3033	V
INITIAL OUTPUT VOLTAGE ERROR	V_{OERR}				±0.1	%
					±3.3	mV
TEMPERATURE COEFFICIENT	TCV_{OUT}	−40°C ≤ T_A ≤ +125°C				
A Grade				2.5	8	ppm/°C
B Grade				2.5	5	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 3.5 V to 5.5 V		5	50	ppm/V
		V_{IN} = 3.5 V to 5.5 V, −40°C ≤ T_A ≤ +125°C			120	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$					
Sourcing		I_L = 0 mA to 10 mA, V_{IN} = 3.8 V, −40°C ≤ T_A ≤ +125°C		9	30	ppm/mA
Sinking		I_L = 0 mA to −3 mA, V_{IN} = 3.8 V, −40°C ≤ T_A ≤ +125°C		10	50	ppm/mA
OUTPUT CURRENT CAPACITY	I_L					
Sourcing		V_{IN} = 3.8 V to 5.5 V	10			mA
Sinking		V_{IN} = 3.8 V to 5.5 V	−3			mA
QUIESCENT CURRENT	I_Q					
Normal Operation		ENABLE ≥ V_{IN} × 0.85			85	µA
		ENABLE = V_{IN}, −40°C ≤ T_A ≤ +125°C			100	µA
Shutdown		ENABLE ≤ 0.7 V			5	µA
DROPOUT VOLTAGE[1]	V_{DO}	I_L = 0 mA, T_A = −40°C ≤ T_A ≤ +125°C		50	200	mV
		I_L = 2 mA, T_A = −40°C ≤ T_A ≤ +125°C		75	250	mV
ENABLE PIN						
Shutdown Voltage	V_L		0		0.7	V
ENABLE Voltage	V_H		V_{IN} × 0.85		V_{IN}	V
ENABLE Pin Leakage Current	I_{EN}	ENABLE = V_{IN}, T_A = −40°C ≤ T_A ≤ +125°C		0.85	3	µA
OUTPUT VOLTAGE NOISE	e_n p-p	f = 0.1 Hz to 10 Hz		25		µV p-p
		f = 10 Hz to 10 kHz		46		µV rms
OUTPUT VOLTAGE NOISE DENSITY	e_n	f = 1 kHz		1.2		µV/√Hz
OUTPUT VOLTAGE HYSTERESIS[2]	ΔV_{OUT_HYS}	T_A = +25°C to −40°C to +125°C to +25°C		70		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 60 Hz		−60		dB
LONG-TERM OUTPUT VOLTAGE DRIFT	ΔV_{OUT_LTD}	1000 hours at 50°C		30		ppm
TURN-ON SETTLING TIME	t_R	C_{IN} = 0.1 µF, C_L = 0.1 µF, R_L = 1 kΩ		750		µs

[1] Refers to the minimum difference between V_{IN} and V_{OUT} such that V_{OUT} maintains a minimum accuracy of 0.1%. See the Terminology section.

[2] See the Terminology section. The part is placed through the temperature cycle in the order of temperatures shown.

ADR3540 ELECTRICAL CHARACTERISTICS

V_{IN} = 4.3 V to 5.5 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}		4.0919	4.0960	4.1000	V
INITIAL OUTPUT VOLTAGE ERROR	V_{OERR}				±0.1	%
					±4.096	mV
TEMPERATURE COEFFICIENT	TCV_{OUT}	$-40°C \le T_A \le +125°C$				
A Grade				2.5	8	ppm/°C
B Grade				2.5	5	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 4.3 V to 5.5 V		3	50	ppm/V
		V_{IN} = 4.3 V to 5.5 V, $-40°C \le T_A \le +125°C$			120	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$					
Sourcing		I_L = 0 mA to 10 mA, V_{IN} = 4.6 V, $-40°C \le T_A \le +125°C$		6	30	ppm/mA
Sinking		I_L = 0 mA to −3 mA, V_{IN} = 4.6 V, $-40°C \le T_A \le +125°C$		15	50	ppm/mA
OUTPUT CURRENT CAPACITY	I_L					
Sourcing		V_{IN} = 4.6 V to 5.5 V	10			mA
Sinking		V_{IN} = 4.6 V to 5.5 V	−3			mA
QUIESCENT CURRENT	I_Q					
Normal Operation		ENABLE ≥ V_{IN} × 0.85			85	µA
		ENABLE = V_{IN}, $-40°C \le T_A \le +125°C$			100	µA
Shutdown		ENABLE ≤ 0.7 V			5	µA
DROPOUT VOLTAGE[1]	V_{DO}	I_L = 0 mA, $T_A = -40°C \le T_A \le +125°C$		50	200	mV
		I_L = 2 mA, $T_A = -40°C \le T_A \le +125°C$		75	250	mV
ENABLE PIN						
Shutdown Voltage	V_L		0		0.7	V
ENABLE Voltage	V_H		V_{IN} × 0.85		V_{IN}	V
ENABLE Pin Leakage Current	I_{EN}	ENABLE = V_{IN}, $T_A = -40°C \le T_A \le +125°C$		0.85	3	µA
OUTPUT VOLTAGE NOISE	e_n p-p	f = 0.1 Hz to 10 Hz		29		µV p-p
		f = 10 Hz to 10 kHz		53		µV rms
OUTPUT VOLTAGE NOISE DENSITY	e_n	f = 1 kHz		1.4		µV/√Hz
OUTPUT VOLTAGE HYSTERESIS[2]	ΔV_{OUT_HYS}	T_A = +25°C to −40°C to +125°C to +25°C		70		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 60 Hz		−60		dB
LONG-TERM OUTPUT VOLTAGE DRIFT	ΔV_{OUT_LTD}	1000 hours at 50°C		30		ppm
TURN-ON SETTLING TIME	t_R	C_{IN} = 0.1 µF, C_L = 0.1 µF, R_L = 1 kΩ		800		µs

[1] Refers to the minimum difference between V_{IN} and V_{OUT} such that V_{OUT} maintains a minimum accuracy of 0.1%. See the Terminology section.
[2] See the Terminology section. The part is placed through the temperature cycle in the order of temperatures shown.

ADR3550 ELECTRICAL CHARACTERISTICS

V_{IN} = 5.2 V to 5.5 V, T_A = 25°C, I_{LOAD} = 0 mA, unless otherwise noted.

Table 6.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}		4.995	5.000	5.005	V
INITIAL OUTPUT VOLTAGE ERROR	V_{OERR}				±0.1	%
					±5.0	mV
TEMPERATURE COEFFICIENT	TCV_{OUT}	$-40°C \le T_A \le +125°C$				
A Grade				2.5	8	ppm/°C
B Grade				2.5	5	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 5.2 V to 5.5 V		3	50	ppm/V
		V_{IN} = 5.2 V to 5.5 V, $-40°C \le T_A \le +125°C$			120	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$					
Sourcing		I_L = 0 mA to 10 mA, V_{IN} = 5.5 V, $-40°C \le T_A \le +125°C$		3	30	ppm/mA
Sinking		I_L = 0 mA to −3 mA, V_{IN} = 5.5 V, $-40°C \le T_A \le +125°C$		19	50	ppm/mA
OUTPUT CURRENT CAPACITY	I_L					
Sourcing		V_{IN} = 5.5 V	10			mA
Sinking		V_{IN} = 5.5 V	−3			mA
QUIESCENT CURRENT	I_Q					
Normal Operation		ENABLE > V_{IN} × 0.85			85	µA
		ENABLE = V_{IN}, $-40°C \le T_A \le +125°C$			100	µA
Shutdown		ENABLE < 0.7 V			5	µA
DROPOUT VOLTAGE[1]	V_{DO}	I_L = 0 mA, $-40°C \le T_A \le +125°C$		50	200	mV
		I_L = 2 mA, $-40°C \le T_A \le +125°C$		75	250	mV
ENABLE PIN						
Shutdown Voltage	V_L		0		0.7	V
ENABLE Voltage	V_H		V_{IN} × 0.85		V_{IN}	V
ENABLE Pin Leakage Current	I_{EN}	ENABLE = V_{IN}, $-40°C \le T_A \le +125°C$		0.85	3	µA
OUTPUT VOLTAGE NOISE	e_n p-p	f = 0.1 Hz to 10 Hz		35		µV p-p
		f = 10 Hz to 10 kHz		60		µV rms
OUTPUT VOLTAGE NOISE DENSITY	e_n	f = 1 kHz		1.5		µV/√Hz
OUTPUT VOLTAGE HYSTERESIS[2]	ΔV_{OUT_HYS}	T_A = +25°C to −40°C to +125°C to +25°C		70		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 60 Hz		−58		dB
LONG-TERM OUTPUT VOLTAGE DRIFT	ΔV_{OUT_LTD}	1000 hours at 50°C		30		ppm
TURN-ON SETTLING TIME	t_R	C_{IN} = 0.1 µF, C_L = 0.1 µF, R_L = 1 kΩ		900		µs

[1] Refers to the minimum difference between V_{IN} and V_{OUT} such that V_{OUT} maintains a minimum accuracy of 0.1%. See the Terminology section.

[2] See the Terminology section. The part is placed through the temperature cycle in the order of temperatures shown.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
Supply Voltage	6 V
ENABLE to GND SENSE Voltage	V_{IN}
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (RM-8 Suffix)	132.5	43.9	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

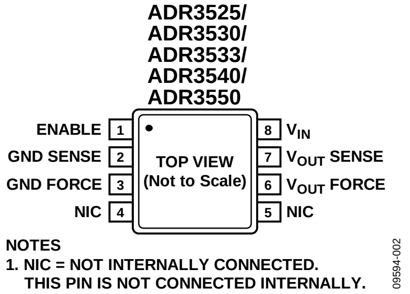

Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	ENABLE	Enable Connection. Enables or disables the device.
2	GND SENSE	Ground Voltage Sense Connection. Connect directly to the point of lowest potential in the application.
3	GND FORCE	Ground Force Connection.
4, 5	NIC	Not Internally Connected. This pin is not connected internally.
6	V_{OUT} FORCE	Reference Voltage Output.
7	V_{OUT} SENSE	Reference Voltage Output Sensing Connection. Connect directly to the voltage input of the load devices.
8	V_{IN}	Input Voltage Connection.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

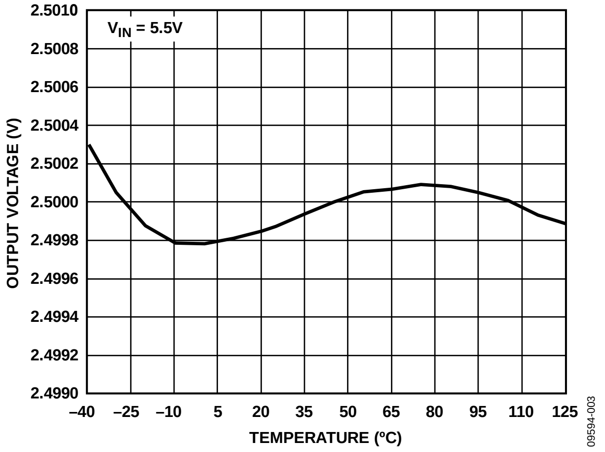

Figure 3. ADR3525 Output Voltage vs. Temperature

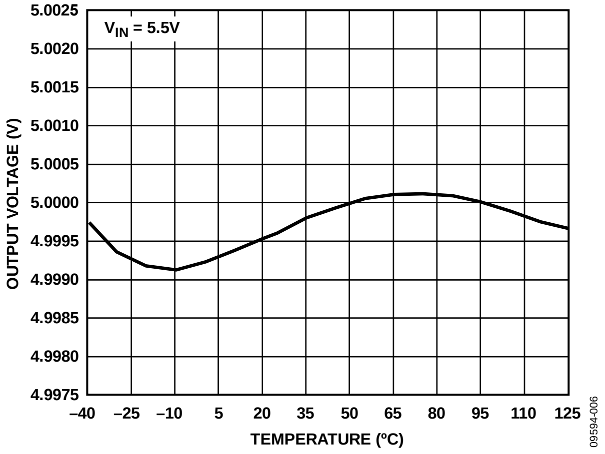

Figure 6. ADR3550 Output Voltage vs. Temperature

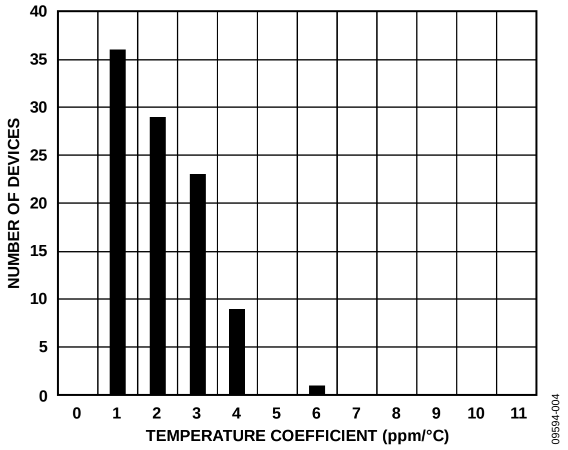

Figure 4. ADR3525 Temperature Coefficient Distribution

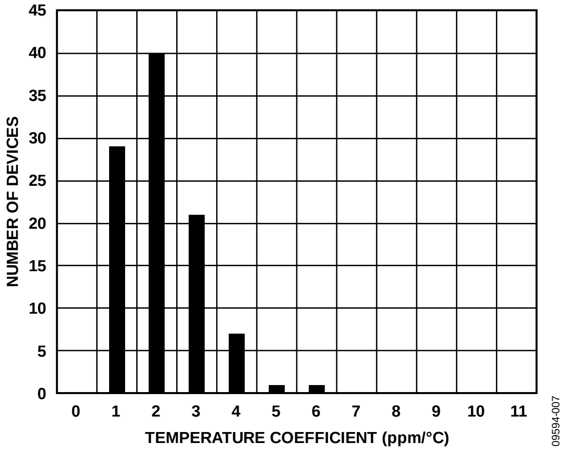

Figure 7. ADR3550 Temperature Coefficient Distribution

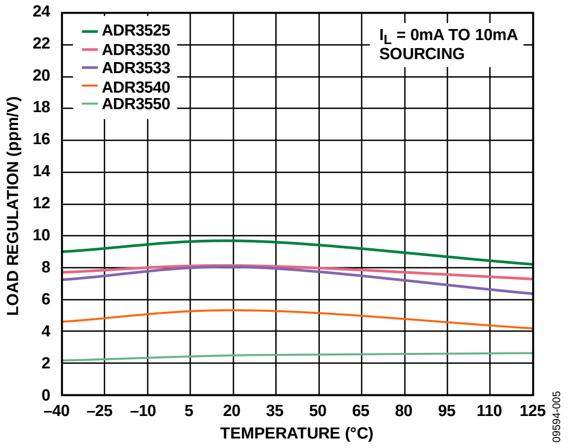

Figure 5. Load Regulation vs. Temperature (Sourcing)

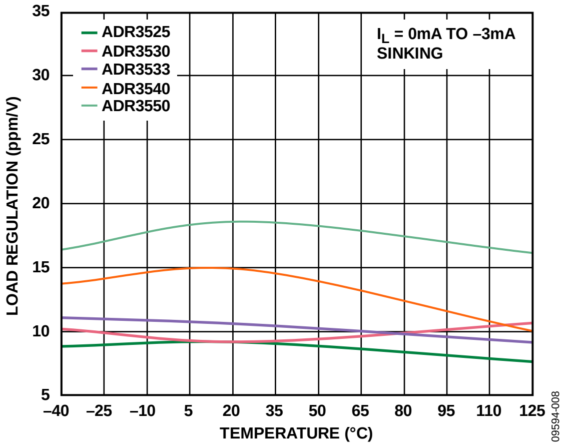

Figure 8. Load Regulation vs. Temperature (Sinking)

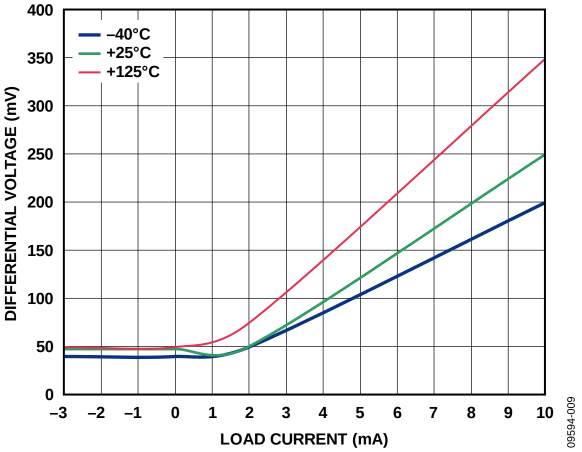

Figure 9. ADR3525 Dropout Voltage vs. Load Current

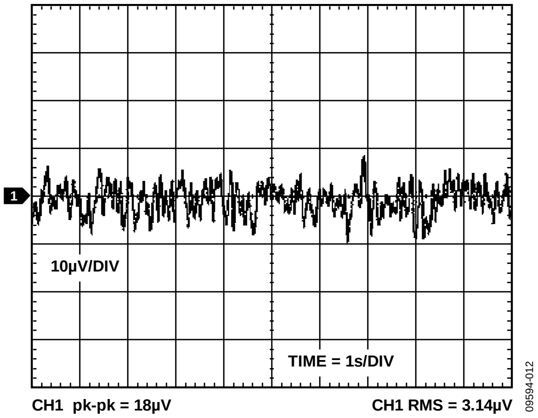

Figure 12. ADR3525 Output Voltage Noise (0.1 Hz to 10 Hz)

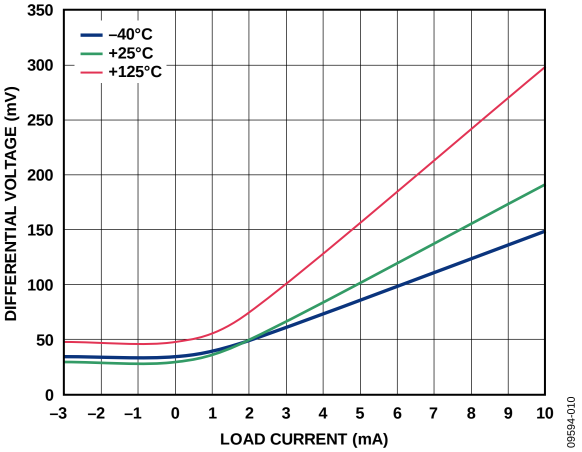

Figure 10. ADR3550 Dropout Voltage vs. Load Current

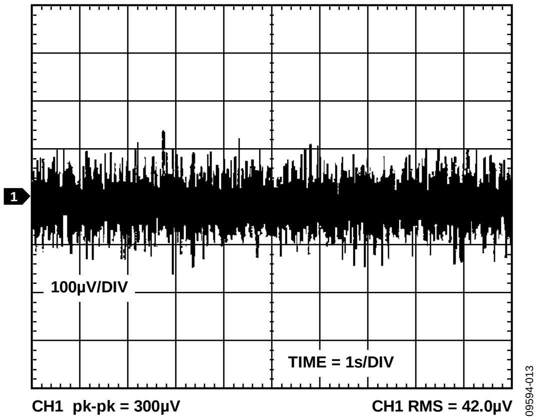

Figure 13. ADR3525 Output Voltage Noise (10 Hz to 10 kHz)

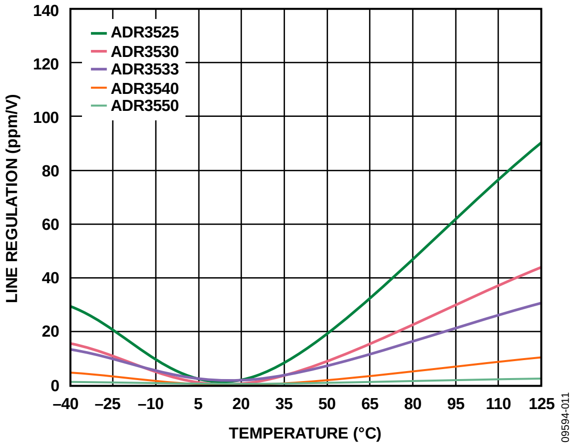

Figure 11. Line Regulation vs. Temperature

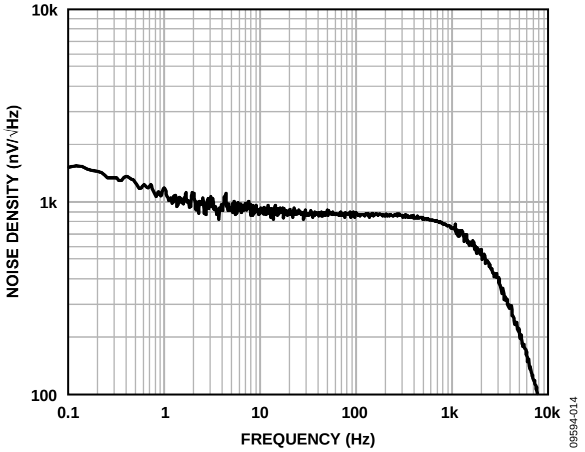

Figure 14. ADR3525 Output Noise Spectral Density

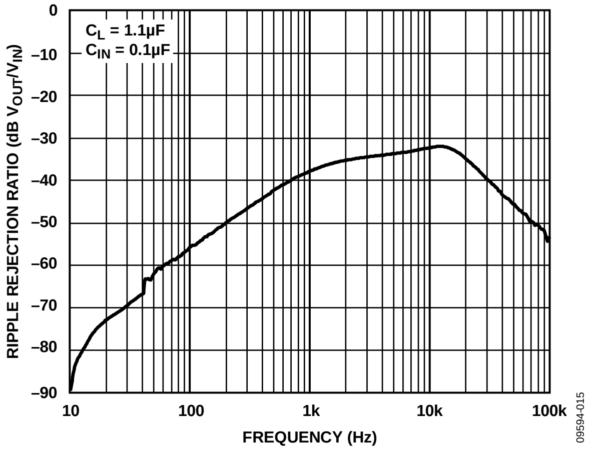

Figure 15. ADR3525 Ripple Rejection Ratio vs. Frequency

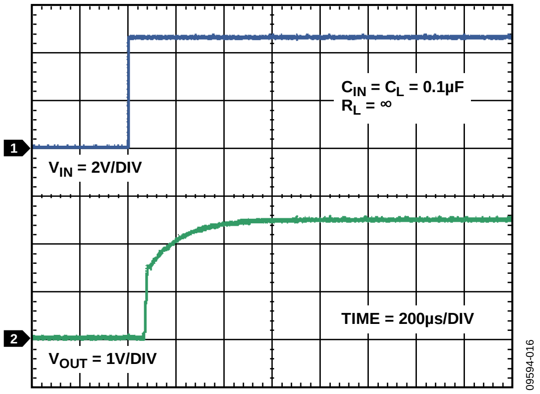

Figure 16. ADR3525 Start-Up Response

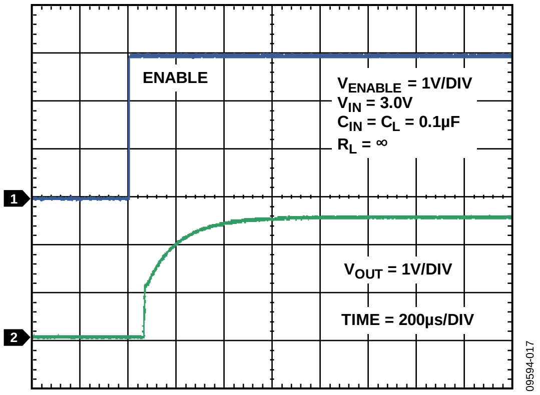

Figure 17. ADR3525 Restart Response from Shutdown

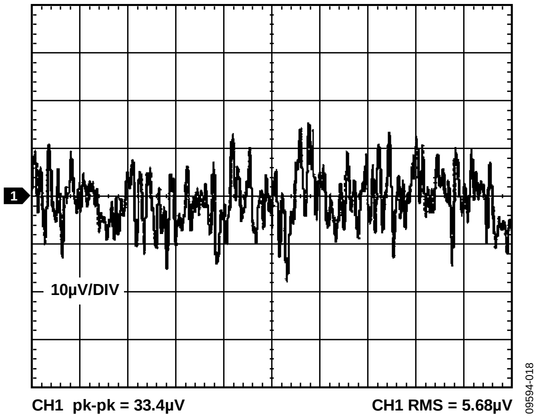

Figure 18. ADR3550 Output Voltage Noise (0.1 Hz to 10 Hz)

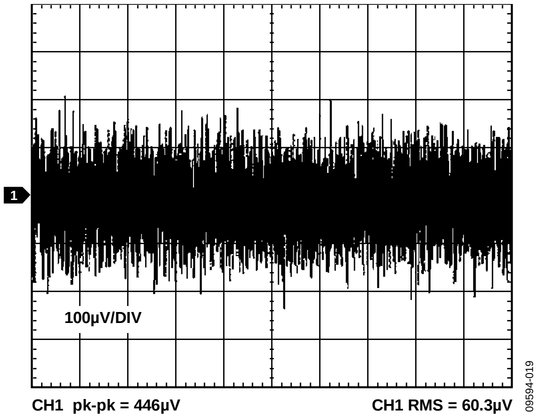

Figure 19. ADR3550 Output Voltage Noise (10 Hz to 10 kHz)

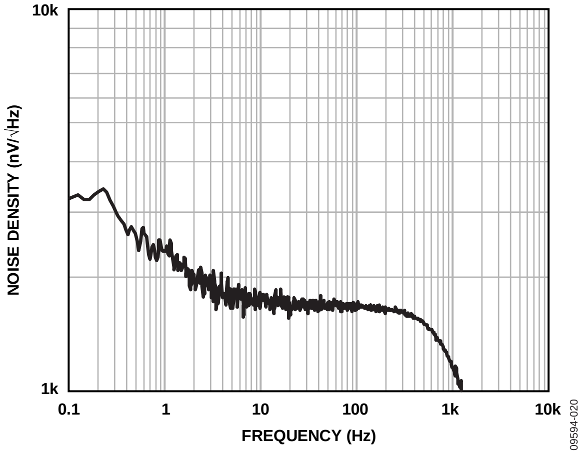

Figure 20. ADR3550 Output Noise Spectral Density

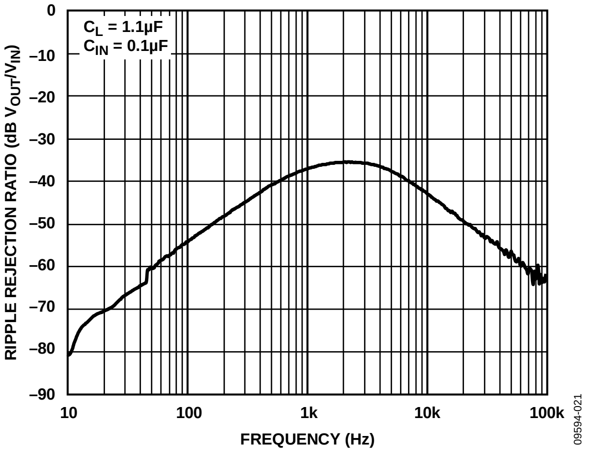

Figure 21. ADR3550 Ripple Rejection Ratio vs. Frequency

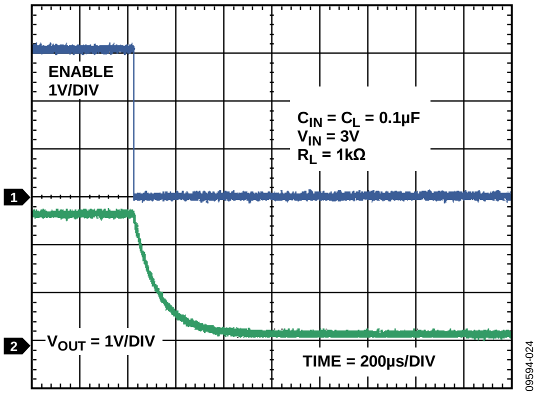

Figure 24. ADR3525 Shutdown Response

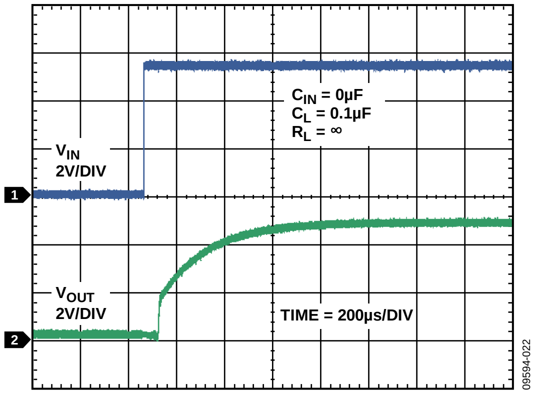

Figure 22. ADR3550 Start-Up Response

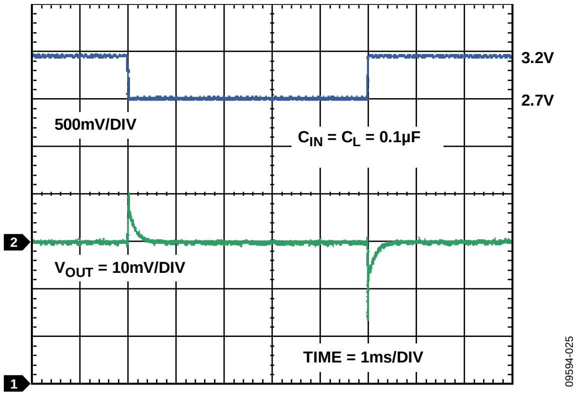

Figure 25. ADR3525 Line Transient Response

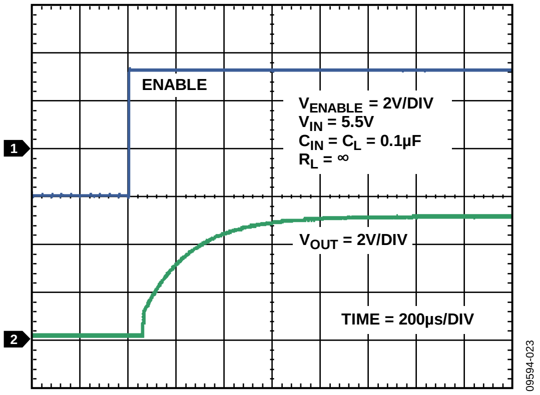

Figure 23. ADR3550 Restart Response from Shutdown

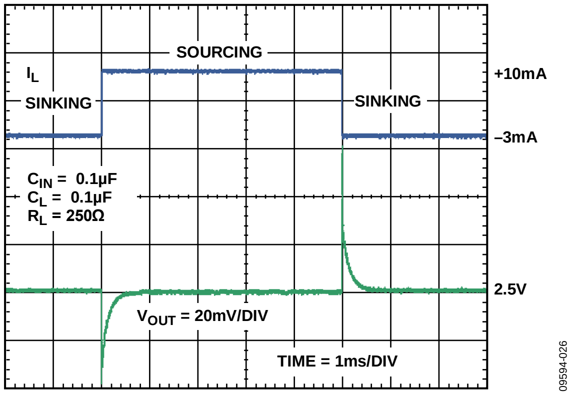

Figure 26. ADR3525 Load Transient Response

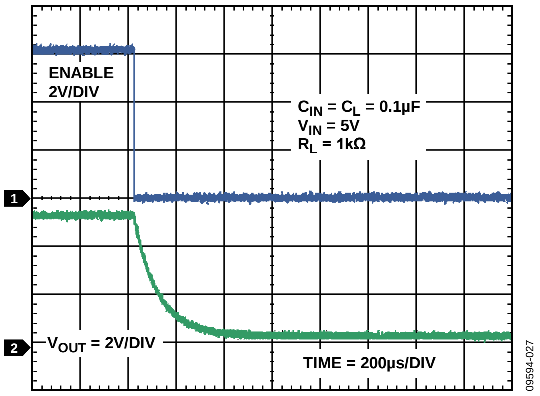

Figure 27. ADR3550 Shutdown Response

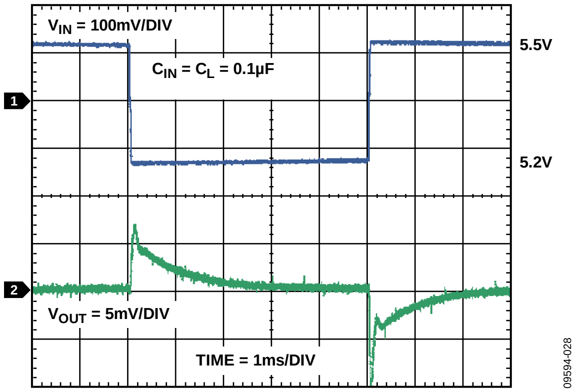

Figure 28. ADR3550 Line Transient Response

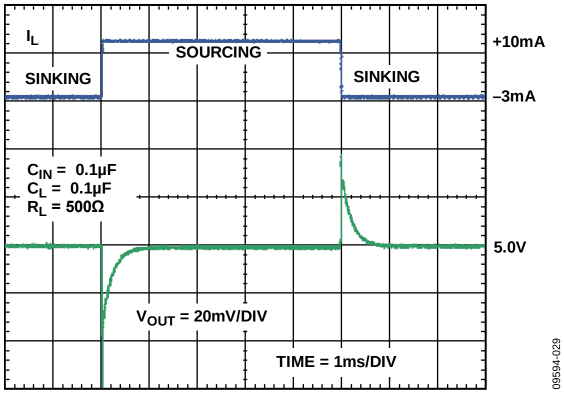

Figure 29. ADR3550 Load Transient Response

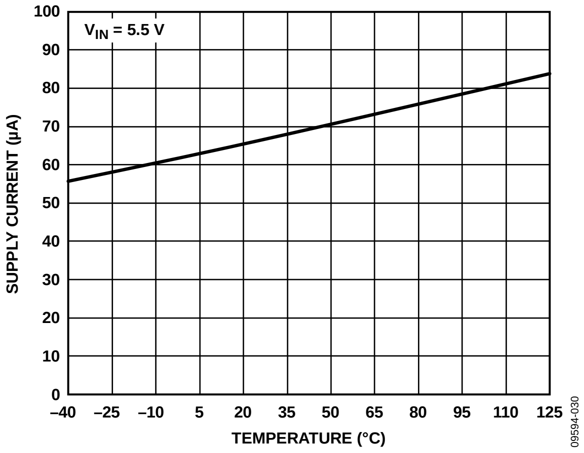

Figure 30. Supply Current vs. Temperature

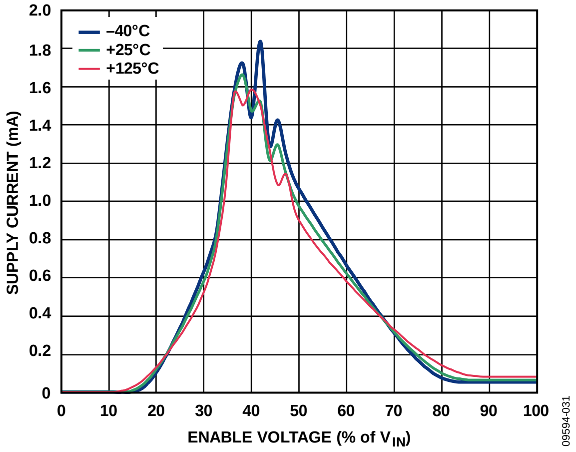

Figure 31. Supply Current vs. ENABLE Pin Voltage

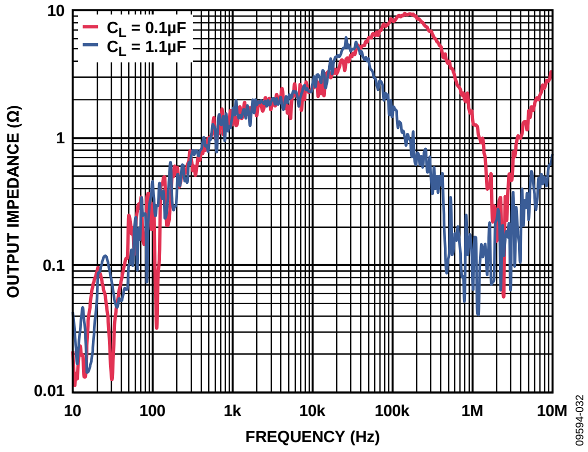

Figure 32. ADR3550 Output Impedance vs. Frequency

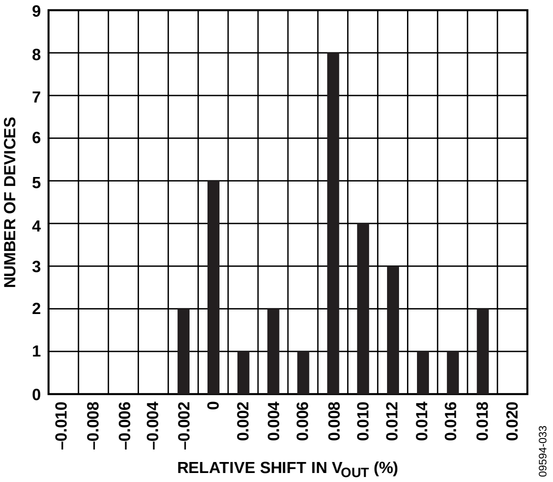

Figure 33. Output Voltage Shift Distribution After Reflow (SHR Drift)

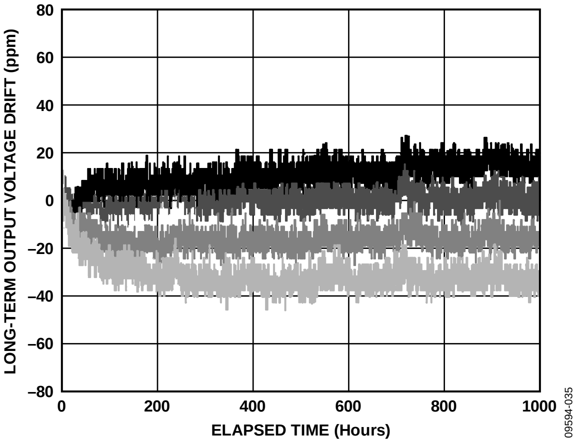

Figure 35. ADR3550 Typical Long-Term Output Voltage Drift (Four Devices, 1000 Hours)

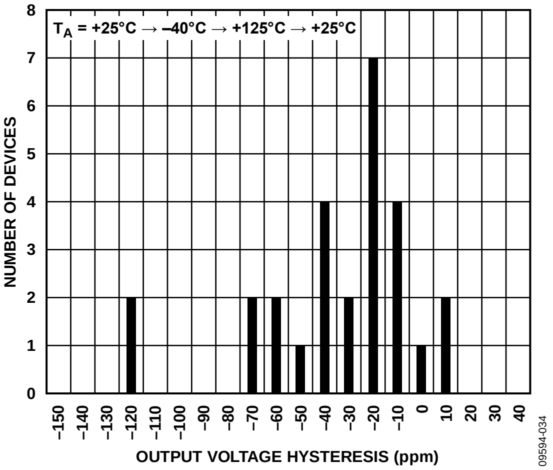

Figure 34. ADR3550 Thermally Induced Output Voltage Hysteresis Distribution

TERMINOLOGY

Dropout Voltage (V_{DO})

Dropout voltage, sometimes referred to as supply voltage headroom or supply-output voltage differential, is defined as the minimum voltage differential between the input and output such that the output voltage is maintained to within 0.1% accuracy.

$$V_{DO} = (V_{IN} - V_{OUT})_{min} \,|\, I_L = constant$$

Because the dropout voltage depends upon the current passing through the device, it is always specified for a given load current. In series-mode devices, dropout voltage typically increases proportionally to load current (see Figure 9 and Figure 10).

Temperature Coefficient (TCV_{OUT})

The temperature coefficient relates the change in output voltage to the change in ambient temperature of the device, as normalized by the output voltage at 25°C. This parameter is expressed in ppm/°C and can be determined by the following equations:

$$TCV_{OUT1} = \left| \frac{\max\{V_{OUT}(T_1,T_2)\} - \min\{V_{OUT}(T_1,T_2)\}}{V_{OUT}(T_2) \times (T_2 - T_1)} \right| \times 10^6 \ [ppm/°C]$$

$$TCV_{OUT2} = \left| \frac{\max\{V_{OUT}(T_2,T_3)\} - \min\{V_{OUT}(T_2,T_3)\}}{V_{OUT}(T_2) \times (T_3 - T_2)} \right| \times 10^6 \ [ppm/°C]$$

$$TCV_{OUT} = \max\{TCV_{OUT1}, TCV_{OUT2}\} \quad (1)$$

where:

$V_{OUT}(T)$ is the output voltage at Temperature T.

T_1 = −40°C.

T_2 = +25°C.

T_3 = +125°C.

This three-point method ensures that TCV_{OUT} accurately portrays the maximum difference between any of the three temperatures at which the output voltage of the part is measured.

Thermally Induced Output Voltage Hysteresis (ΔV_{OUT_HYS})

Thermally induced output voltage hysteresis represents the change in output voltage after the device is exposed to a specified temperature cycle. This is expressed as either a shift in voltage or a difference in ppm from the nominal output.

$$\Delta V_{OUT\_HYS} = V_{OUT}(25°C) - V_{OUT\_TC} \quad [V]$$

$$\Delta V_{OUT\_HYS} = \frac{V_{OUT}(25°C) - V_{OUT\_TC}}{V_{OUT}(25°C)} \times 10^6 \quad [ppm]$$

where:

$V_{OUT}(25°C)$ is the output voltage at 25°C.

V_{OUT_TC} is the output voltage after temperature cycling.

Long-Term Output Voltage Drift (ΔV_{OUT_LTD})

Long-term output voltage drift refers to the shift in output voltage after 1000 hours of operation in a constant 50°C environment. This is expressed as either a shift in voltage or a difference in ppm from the nominal output.

$$\Delta V_{OUT\_LTD} = \left| V_{OUT}(t_1) - V_{OUT}(t_0) \right| \quad [V]$$

$$\Delta V_{OUT\_LTD} = \left| \frac{V_{OUT}(t_1) - V_{OUT}(t_0)}{V_{OUT}(t_0)} \right| \times 10^6 \quad [ppm]$$

where:

$V_{OUT}(t_0)$ is the V_{OUT} at 50°C at Time 0.

$V_{OUT}(t_1)$ is the V_{OUT} at 50°C after 1000 hours of operation at 50°C.

Line Regulation

Line regulation refers to the change in output voltage in response to a given change in input voltage and is expressed in percent per volt, ppm per volt, or microvolts per volt change in input voltage. This parameter accounts for the effects of self-heating.

Load Regulation

Load regulation refers to the change in output voltage in response to a given change in load current and is expressed in microvolts per mA, ppm per mA, or ohms of dc output resistance. This parameter accounts for the effects of self-heating.

Solder Heat Resistance (SHR) Drift

SHR drift refers to the permanent shift in output voltage induced by exposure to reflow soldering, expressed in units of ppm. This is caused by changes in the stress exhibited upon the die by the package materials when exposed to high temperatures. This effect is more pronounced in lead-free soldering processes due to higher reflow temperatures.

THEORY OF OPERATION

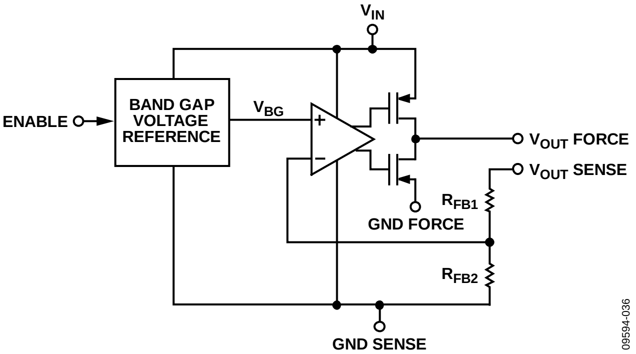

Figure 36. Block Diagram

The ADR3525W/ADR3530W/ADR3533W/ADR3540W/ ADR3550W use a proprietary voltage reference architecture to achieve high accuracy, low temperature coefficient (TC), and low noise in a CMOS process. Like all band gap references, the references combine two voltages of opposite TCs to create an output voltage that is nearly independent of ambient temperature. However, unlike traditional band gap voltage references, the temperature-independent voltage of the references is arranged to be the base-emitter voltage, V_{BE}, of a bipolar transistor at room temperature rather than the V_{BE} extrapolated to 0 K (the V_{BE} of bipolar transistor at 0 K is approximately V_{G0}, the band gap voltage of silicon). A corresponding positive TC voltage is then added to the V_{BE} voltage to compensate for its negative TC.

The key benefit of this technique is that the trimming of the initial accuracy and TC can be performed without interfering with one another, thereby increasing overall accuracy across temperature. Curvature correction techniques further reduce the temperature variation.

The band gap voltage (V_{BG}) is then buffered and amplified to produce stable output voltages of 2.5 V and 5.0 V. The output buffer can source up to 10 mA and sink up to −3 mA of load current.

The ADR35xx references leverage Analog Devices proprietary DigiTrim technology to achieve high initial accuracy and low TC, and precision layout techniques lead to very low long-term drift and thermal hysteresis.

LONG-TERM OUTPUT VOLTAGE DRIFT

One of the key parameters of the ADR35xx references is long-term output voltage drift. Independent of the output voltage model and in a 50°C environment, these devices exhibit a typical drift of approximately 30 ppm after 1000 hours of continuous, unloaded operation.

It is important to understand that long-term output voltage drift is not tested or guaranteed by design and that the output from the device may shift beyond the typical 30 ppm specification. Because most of the drift occurs in the first 200 hours of device operation, burning in the system board with the reference mounted can reduce subsequent output voltage drift over time. See the AN-713 Application Note, *The Effect of Long-Term Drift on Voltage References*, at www.analog.com for more information regarding the effects of long-term drift and how it can be minimized.

POWER DISSIPATION

The ADR35xx voltage references are capable of sourcing up to 10 mA of load current at room temperature across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current should be carefully monitored to ensure that the device does not exceed its maximum power dissipation rating. The maximum power dissipation of the device can be calculated via the following equation:

$$P_D = \frac{T_J - T_A}{\theta_{JA}} [W]$$

where:
P_D is the device power dissipation.
T_J is the device junction temperature.
T_A is the ambient temperature.
θ_{JA} is the package (junction-to-air) thermal resistance.

Because of this relationship, the acceptable load current in high temperature conditions may be less than the maximum current-sourcing capability of the device. In no case should the part be operated outside of its maximum power rating because doing so can result in premature failure or permanent damage to the device.

APPLICATIONS INFORMATION

BASIC VOLTAGE REFERENCE CONNECTION

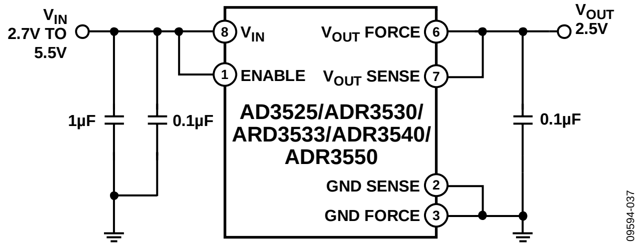

Figure 37. Basic Reference Connection

The circuit shown in Figure 37 illustrates the basic configuration for the ADR35xx references. Bypass capacitors should be connected according to the following guidelines.

INPUT AND OUTPUT CAPACITORS

A 1 µF to 10 µF electrolytic or ceramic capacitor can be connected to the input to improve transient response in applications where the supply voltage may fluctuate. An additional 0.1 µF ceramic capacitor should be connected in parallel to reduce high frequency supply noise.

A ceramic capacitor of at least a 0.1 µF must be connected to the output to improve stability and help filter out high frequency noise. An additional 1 µF to 10 µF electrolytic or ceramic capacitor can be added in parallel to improve transient performance in response to sudden changes in load current; however, the designer should keep in mind that doing so increases the turn-on time of the device.

Best performance and stability is attained with low ESR (for example, less than 1 Ω), low inductance ceramic chip-type output capacitors (X5R, X7R, or similar). If using an electrolytic capacitor on the output, a 0.1 µF ceramic capacitor should be placed in parallel to reduce overall ESR on the output.

4-WIRE KELVIN CONNECTIONS

Current flowing through a PCB trace produces an IR voltage drop, and with longer traces, this drop can reach several millivolts or more, introducing a considerable error into the output voltage of the reference. A 1 inch long, 5 millimeter wide trace of 1 ounce copper has a resistance of approximately 100 mΩ at room temperature; at a load current of 10 mA, this can introduce a full millivolt of error. In an ideal board layout, the reference should be mounted as close to the load as possible to minimize the length of the output traces, and, therefore, the error introduced by voltage drop. However, in applications where this is not possible or convenient, force and sense connections (sometimes referred to as Kelvin sensing connections) are provided as a means of minimizing the IR drop and improving accuracy.

Kelvin connections work by providing a set of high impedance voltage-sensing lines to the output and ground nodes. Because very little current flows through these connections, the IR drop across their traces is negligible, and the output and ground voltages can be sensed accurately. These voltages are fed back into the internal amplifier and used to automatically correct for the voltage drop across the current-carrying output and ground lines, resulting in a highly accurate output voltage across the load. To achieve the best performance, the sense connections should be connected directly to the point in the load where the output voltage should be the most accurate. See Figure 38 for an example application.

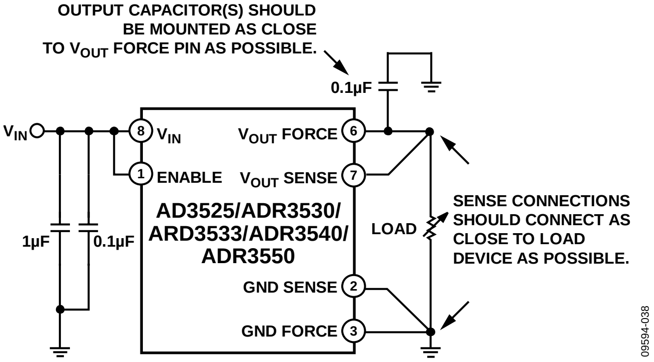

Figure 38. Application Showing Kelvin Connection

It is always advantageous to use Kelvin connections whenever possible. However, in applications where the IR drop is negligible or an extra set of traces cannot be routed to the load, the force and sense pins for both V_{OUT} and GND can simply be tied together, and the device can be used in the same way as a normal 3-terminal reference (as shown in Figure 37).

V_{IN} SLEW RATE CONSIDERATIONS

In applications with slow rising input voltage signals, the reference exhibits overshoot or other transient anomalies that appear on the output. These phenomena also appear during shutdown as the internal circuitry loses power.

To avoid such conditions, ensure that the input voltage waveform has both a rising and falling slew rate of at least 0.1 V/ms.

SHUTDOWN/ENABLE FEATURE

The ADR35xx references can be switched to a low power shutdown mode when a voltage of 0.7 V or lower is input to the ENABLE pin. Likewise, the reference becomes operational for ENABLE voltages of 0.85 × V_{IN} or higher. During shutdown, the supply current drops to less than 5 µA, useful in applications that are sensitive to power consumption.

If using the shutdown feature, ensure that the ENABLE pin voltage does not fall between 0.7 V and 0.85 × V_{IN} because this causes a large increase in the supply current of the device and may keep the reference from starting up correctly (see Figure 31). If not using the shutdown feature, however, the ENABLE pin can simply be tied to the V_{IN} pin, and the reference remains operational continuously.

SAMPLE APPLICATIONS

Negative Reference

Figure 39 shows how to connect the ADR3550 and a standard CMOS op amp, such as the AD8663, to provide a negative reference voltage. This configuration provides two main advantages: first, it requires only two devices and, therefore, does not require excessive board space; second, and more importantly, it does not require any external resistors, meaning that the performance of this circuit does not rely on choosing expensive parts with low temperature coefficients to ensure accuracy.

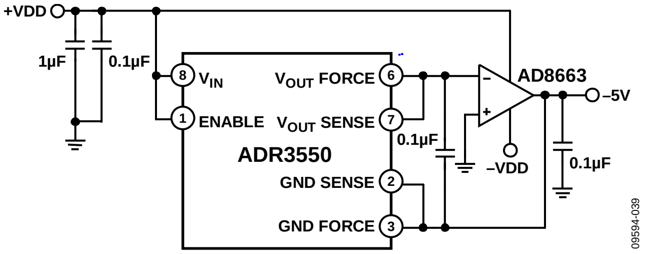

Figure 39. ADR3550 Negative Reference

In this configuration, the V_{OUT} FORCE and V_{OUT} SENSE pins of the reference sit at virtual ground, and the negative reference voltage and load current are taken directly from the output of the operational amplifier. Note that in applications where the negative supply voltage is close to the reference output voltage, a dual-supply, low offset, rail-to-rail output amplifier must be used to ensure an accurate output voltage. The operational amplifier must also be able to source or sink an appropriate amount of current for the application.

Bipolar Output Reference

Figure 40 shows a bipolar reference configuration. By connecting the output of the ADR3550 to the inverting terminal of an operational amplifier, it is possible to obtain both positive and negative reference voltages. R1 and R2 must be matched as closely as possible to ensure minimal difference between the negative and positive outputs. Resistors with low temperature coefficients must also be used if the circuit is used in environments with large temperature swings; otherwise, a voltage difference develops between the two outputs as the ambient temperature changes.

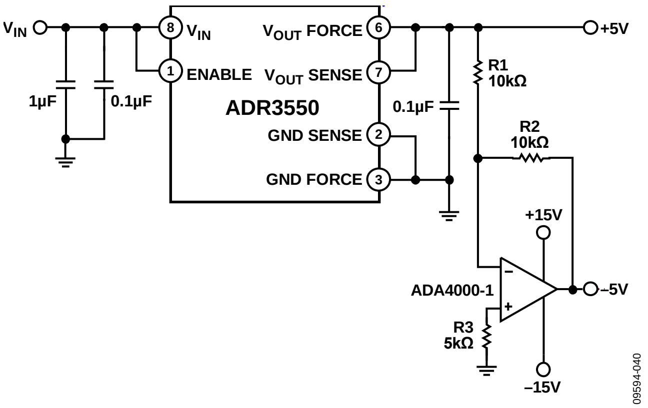

Figure 40. ADR3550 Bipolar Output Reference

Boosted Output Current Reference

Figure 41 shows a configuration for obtaining higher current drive capability from the ADR35xx references without sacrificing accuracy. The op amp regulates the current flow through the MOSFET until V_{OUT} equals the output voltage of the reference; current is then drawn directly from V_{IN} instead of from the reference itself, allowing increased current drive capability.

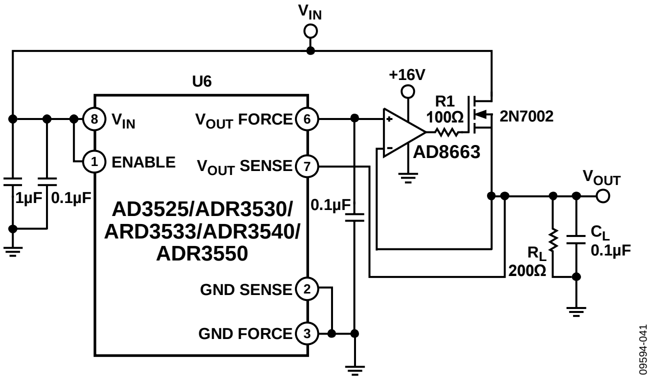

Figure 41. Boosted Output Current Reference

Because the current-sourcing capability of this circuit depends only on the I_D rating of the MOSFET, the output drive capability can be adjusted to the application simply by choosing an appropriate MOSFET. In all cases, the V_{OUT} SENSE pin should be tied directly to the load device to maintain maximum output voltage accuracy.