Ultralow Noise, LDO XFET Voltage References with Current Sink and Source

Data Sheet

ADR440/ADR441/ADR443/ADR444/ADR445

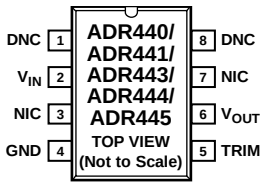
FEATURES

- **Ultralow noise (0.1 Hz to 10 Hz)**
  - **ADR440: 1 µV p-p**
  - **ADR441: 1.2 µV p-p**
  - **ADR443: 1.4 µV p-p**
  - **ADR444: 1.8 µV p-p**
  - **ADR445: 2.25 µV p-p**
- **Superb temperature coefficient**
  - **A grade: 10 ppm/°C**
  - **B grade: 3 ppm/°C**
- **Low dropout operation (supply voltage headroom): 500 mV**
- **Input range: (V_{OUT} + 500 mV) to 18 V**
- **High output source and sink current**
  - **+10 mA and −5 mA, respectively**
- **Wide temperature range: −40°C to +125°C**

APPLICATIONS

- **Precision data acquisition systems**
- **High resolution data converters**
- **Battery-powered instrumentation**
- **Portable medical instruments**
- **Industrial process control systems**
- **Precision instruments**
- **Optical control circuits**

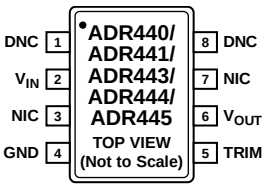
PIN CONFIGURATIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED.
THIS PIN IS NOT CONNECTED INTERNALLY.
2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

05428-001

Figure 1. 8-Lead SOIC_N (R Suffix)



NOTES
1. NIC = NOT INTERNALLY CONNECTED.
THIS PIN IS NOT CONNECTED INTERNALLY.
2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

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Figure 2. 8-Lead MSOP (RM Suffix)

GENERAL DESCRIPTION

The ADR440/ADR441/ADR443/ADR444/ADR445[1] series is a family of XFET® voltage references featuring ultralow noise, high accuracy, and low temperature drift performance. Using Analog Devices, Inc., temperature drift curvature correction and extra implanted junction FET (XFET) technology, voltage change vs. temperature nonlinearity in the ADR440/ADR441/ADR443/ADR444/ADR445 is greatly minimized.

The XFET references offer better noise performance than buried Zener references, and XFET references operate off low supply voltage headroom (500 mV). This combination of features makes the ADR440/ADR441/ADR443/ADR444/ ADR445 family ideally suited for precision signal conversion applications in high end data acquisition systems, optical networks, and medical applications.

The ADR440/ADR441/ADR443/ADR444/ADR445 family has the capability to source up to 10 mA of output current and sink up to −5 mA. It also comes with a trim terminal to adjust the output voltage over a 0.5% range without compromising performance.

[1] Protected by U.S. Patent Number 5,838,192.

The ADR440/ADR441/ADR443/ADR444/ADR445 family is available in 8-lead MSOP and narrow SOIC packages and offered in two electrical grades. All versions are specified over the extended industrial temperature range of −40°C to +125°C.

Table 1. Selection Guide

Model	Output Voltage (V)	Initial Accuracy (mV)	Temperature Coefficient (ppm/°C)
ADR440A	2.048	±3	10
ADR440B	2.048	±1	3
ADR441A	2.500	±3	10
ADR441B	2.500	±1	3
ADR443A	3.000	±4	10
ADR443B	3.000	±1.2	3
ADR444A	4.096	±5	10
ADR444B	4.096	±1.6	3
ADR445A	5.000	±6	10
ADR445B	5.000	±2	3

Rev. G **Document Feedback**

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SPECIFICATIONS

ADR440 ELECTRICAL CHARACTERISTICS

V_{IN} = 3 V to 18 V, T_A = 25°C, C_{IN} = C_{OUT} = 0.1 µF, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}					
A Grade			2.045	2.048	2.051	V
B Grade			2.047	2.048	2.049	V
INITIAL ACCURACY	V_{OERR}					
A Grade					±3	mV
					0.15	%
B Grade					±1	mV
					0.05	%
TEMPERATURE COEFFICIENT	TCV_{OUT}					
A Grade		−40°C < T_A < +125°C		2	10	ppm/°C
B Grade		−40°C < T_A < +125°C		1	3	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	−40°C < T_A < +125°C	−20	+10	+20	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to 10 mA, V_{IN} = 3.5 V, −40°C < T_A < +125°C	−50		+50	ppm/mA
	$\Delta V_{OUT}/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to −5 mA, V_{IN} = 3.5 V, −40°C < T_A < +125°C	−50		+50	ppm/mA
OUTPUT CURRENT CAPACITY	I_{LOAD}					
Sourcing				10		mA
Sinking				−5		mA
QUIESCENT CURRENT	I_{IN}	No load, −40°C < T_A < +125°C		3	3.75	mA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10 Hz		1		µV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		45		nV/√Hz
TURN-ON SETTLING TIME	t_R			10		µs
LONG-TERM STABILITY[1]	ΔV_{OUT}	1000 hours		50		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{O_HYS}			70		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−80		dB
SHORT CIRCUIT TO GND	I_{SC}			27		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		3		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_O$		500			mV

[1] The long-term stability specification is noncumulative. The drift in the subsequent 1000 hour period is significantly lower than in the first 1000 hour period.

ADR441 ELECTRICAL CHARACTERISTICS

V_{IN} = 3 V to 18 V, T_A = 25°C, C_{IN} = C_{OUT} = 0.1 µF, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}					
A Grade			2.497	2.500	2.503	V
B Grade			2.499	2.500	2.501	V
INITIAL ACCURACY	V_{OERR}					
A Grade					±3	mV
					0.12	%
B Grade					±1	mV
					0.04	%
TEMPERATURE DRIFT	TCV_{OUT}					
A Grade		−40°C < T_A < +125°C		2	10	ppm/°C
B Grade		−40°C < T_A < +125°C		1	3	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	−40°C < T_A < +125°C		10	20	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to 10 mA, V_{IN} = 4 V, −40°C < T_A < +125°C	−50		+50	ppm/mA
	$\Delta V_{OUT}/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to −5 mA, V_{IN} = 4 V, −40°C < T_A < +125°C	−50		+50	ppm/mA
OUTPUT CURRENT CAPACITY	I_{LOAD}					
Sourcing				10		mA
Sinking				−5		mA
QUIESCENT CURRENT	I_{IN}	No load, −40°C < T_A < +125°C		3	3.75	mA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10 Hz		1.2		µV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		48		nV/√Hz
TURN-ON SETTLING TIME	t_R			10		µs
LONG-TERM STABILITY[1]	ΔV_{OUT}	1000 hours		50		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{OUT_HYS}			70		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−80		dB
SHORT CIRCUIT TO GND	I_{SC}			27		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		3		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_{OUT}$		500			mV

[1] The long-term stability specification is noncumulative. The drift in the subsequent 1000 hour period is significantly lower than in the first 1000 hour period.

ADR443 ELECTRICAL CHARACTERISTICS

V_{IN} = 3.5 V to 18 V, T_A = 25°C, C_{IN} = C_{OUT} = 0.1 µF, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}					
A Grade			2.996	3.000	3.004	V
B Grade			2.9988	3.000	3.0012	V
INITIAL ACCURACY	V_{OERR}					
A Grade					±4	mV
					0.13	%
B Grade					±1.2	mV
					0.04	%
TEMPERATURE DRIFT	TCV_{OUT}					
A Grade		−40°C < T_A < +125°C		2	10	ppm/°C
B Grade		−40°C < T_A < +125°C		1	3	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	−40°C < T_A < +125°C		10	20	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to 10 mA, V_{IN} = 5 V, −40°C < T_A < +125°C	−50		+50	ppm/mA
	$\Delta V_{OUT}/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to −5 mA, V_{IN} = 5 V, −40°C < T_A < +125°C	−50		+50	ppm/mA
OUTPUT CURRENT CAPACITY	I_{LOAD}					
Sourcing				10		mA
Sinking				−5		mA
QUIESCENT CURRENT	I_{IN}	No load, −40°C < T_A < +125°C		3	3.75	mA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10 Hz		1.4		µV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		57.6		nV/√Hz
TURN-ON SETTLING TIME	t_R			10		µs
LONG-TERM STABILITY[1]	ΔV_{OUT}	1000 hours		50		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{OUT_HYS}			70		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−80		dB
SHORT CIRCUIT TO GND	I_{SC}			27		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		3.5		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_{OUT}$		500			mV

[1] The long-term stability specification is noncumulative. The drift in the subsequent 1000 hour period is significantly lower than in the first 1000 hour period.

ADR444 ELECTRICAL CHARACTERISTICS

V_{IN} = 4.6 V to 18 V, T_A = 25°C, C_{IN} = C_{OUT} = 0.1 µF, unless otherwise noted.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}					
A Grade			4.091	4.096	4.101	V
B Grade			4.0944	4.096	4.0976	V
INITIAL ACCURACY	V_{OERR}					
A Grade					±5	mV
					0.13	%
B Grade					±1.6	mV
					0.04	%
TEMPERATURE DRIFT	TCV_{OUT}					
A Grade		−40°C < T_A < +125°C		2	10	ppm/°C
B Grade		−40°C < T_A < +125°C		1	3	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	−40°C < T_A < +125°C		10	20	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to 10 mA, V_{IN} = 5.5 V, −40°C < T_A < +125°C	−50		+50	ppm/mA
	$\Delta V_{OUT}/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to −5 mA, V_{IN} = 5.5 V, −40°C < T_A < +125°C	−50		+50	ppm/mA
OUTPUT CURRENT CAPACITY	I_{LOAD}					
Sourcing				10		mA
Sinking				−5		mA
QUIESCENT CURRENT	I_{IN}	No load, −40°C < T_A < +125°C		3	3.75	mA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10 Hz		1.8		µV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		78.6		nV/√Hz
TURN-ON SETTLING TIME	t_R			10		µs
LONG-TERM STABILITY[1]	ΔV_{OUT}	1000 hours		50		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{OUT_HYS}			70		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−80		dB
SHORT CIRCUIT TO GND	I_{SC}			27		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		4.6		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_{OUT}$		500			mV

[1] The long-term stability specification is noncumulative. The drift in the subsequent 1000 hour period is significantly lower than in the first 1000 hour period.

ADR445 ELECTRICAL CHARACTERISTICS

V_{IN} = 5.5 V to 18 V, T_A = 25°C, C_{IN} = C_{OUT} = 0.1 µF, unless otherwise noted.

Table 6.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}					
A Grade			4.994	5.000	5.006	V
B Grade			4.998	5.000	5.002	V
INITIAL ACCURACY	V_{OERR}					
A Grade					±6	mV
					0.12	%
B Grade					±2	mV
					0.04	%
TEMPERATURE DRIFT	TCV_{OUT}					
A Grade		−40°C < T_A < +125°C		2	10	ppm/°C
B Grade		−40°C < T_A < +125°C		1	3	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	−40°C < T_A < +125°C		10	20	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to 10 mA, V_{IN} = 6.5 V, −40°C < T_A < +125°C	−50		+50	ppm/mA
	$\Delta V_{OUT}/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to −5 mA, V_{IN} = 6.5 V, −40°C < T_A < +125°C	−50		+50	ppm/mA
OUTPUT CURRENT CAPACITY	I_{LOAD}					
Sourcing				10		mA
Sinking				−5		mA
QUIESCENT CURRENT	I_{IN}	No load, −40°C < T_A < +125°C		3	3.75	mA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10 Hz		2.25		µV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		90		nV/√Hz
TURN-ON SETTLING TIME	t_R			10		µs
LONG-TERM STABILITY[1]	ΔV_{OUT}	1000 hours		50		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{OUT_HYS}			70		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−80		dB
SHORT CIRCUIT TO GND	I_{SC}			27		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		5.5		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_{OUT}$		500			mV

[1] The long-term stability specification is noncumulative. The drift in the subsequent 1000 hour period is significantly lower than in the first 1000 hour period.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
Supply Voltage	20 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature, Soldering (60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

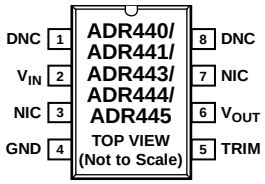
Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC (R Suffix)	130	43	°C/W
8-Lead MSOP (RM Suffix)	132.5	43.9	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED.
THIS PIN IS NOT CONNECTED INTERNALLY.
2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

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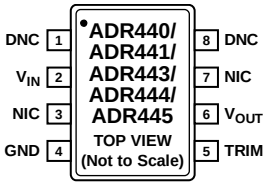
Figure 3. 8-Lead SOIC Pin Configuration



NOTES
1. NIC = NOT INTERNALLY CONNECTED.
THIS PIN IS NOT CONNECTED INTERNALLY.
2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

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Figure 4. 8-Lead MSOP Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8	DNC	Do Not Connect. Do not connect to these pins.
2	V_{IN}	Input Voltage Connection.
3, 7	NIC	Not Internally Connected. These pins are not connected internally.
4	GND	Ground.
5	TRIM	Output Voltage Trim.
6	V_{OUT}	Output Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 7 V, T_A = 25°C, C_{IN} = C_{OUT} = 0.1 µF, unless otherwise noted.

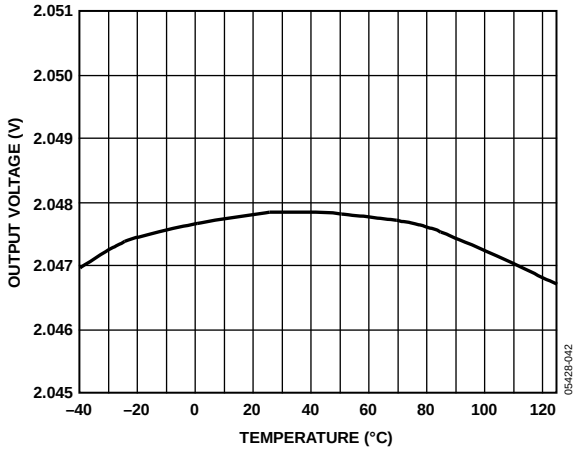


Figure 5. ADR440 Output Voltage vs. Temperature

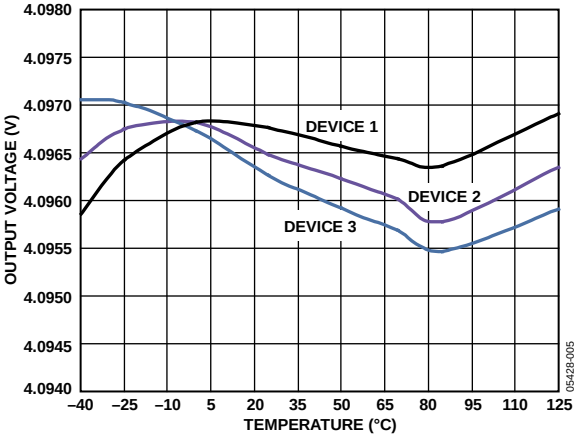


Figure 8. ADR444 Output Voltage vs. Temperature

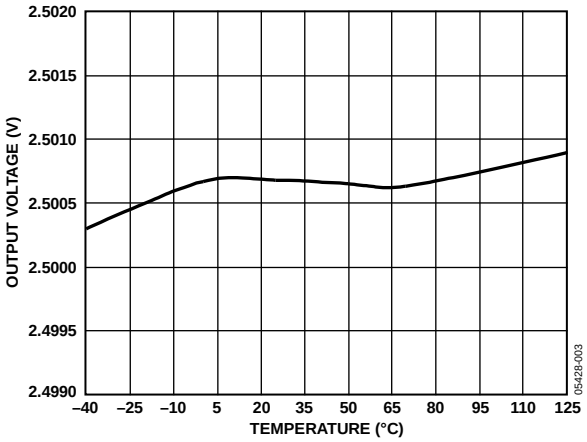


Figure 6. ADR441 Output Voltage vs. Temperature

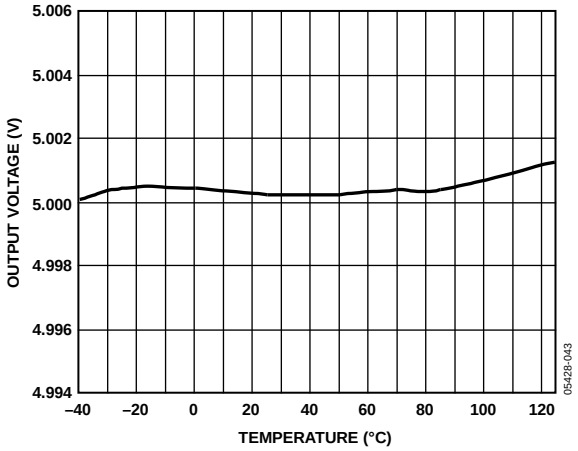


Figure 9. ADR445 Output Voltage vs. Temperature

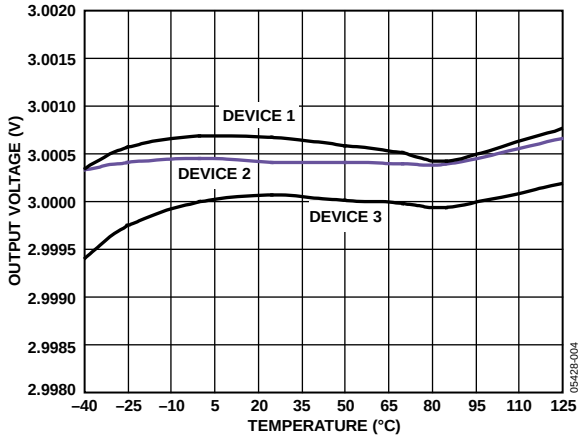


Figure 7. ADR443 Output Voltage vs. Temperature

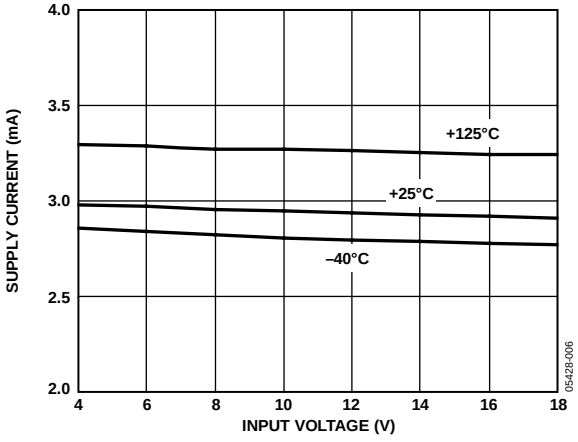


Figure 10. ADR441 Supply Current vs. Input Voltage

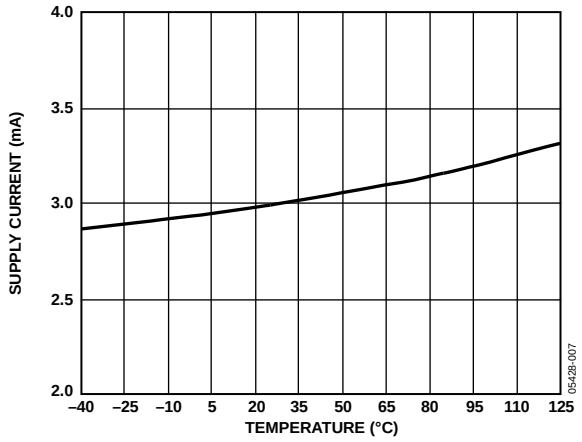


Figure 11. ADR441 Supply Current vs. Temperature

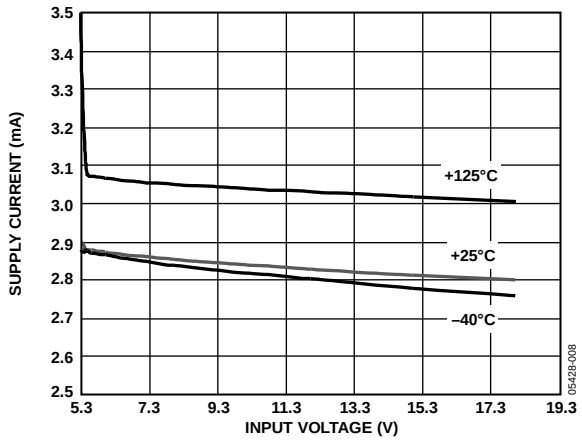


Figure 12. ADR445 Supply Current vs. Input Voltage

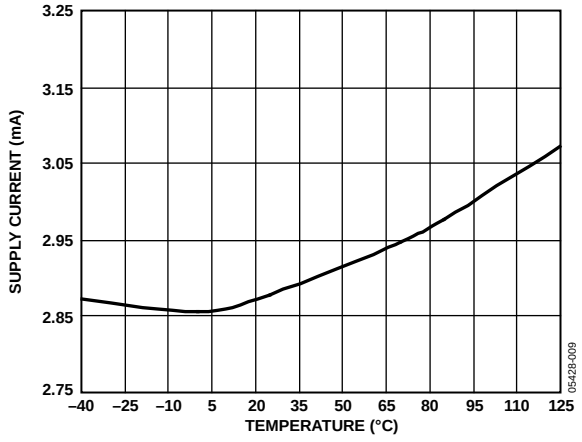


Figure 13. ADR445 Supply Current vs. Temperature

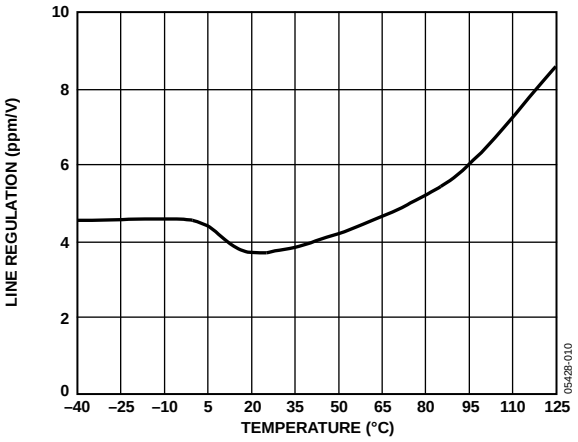


Figure 14. ADR441 Line Regulation vs. Temperature

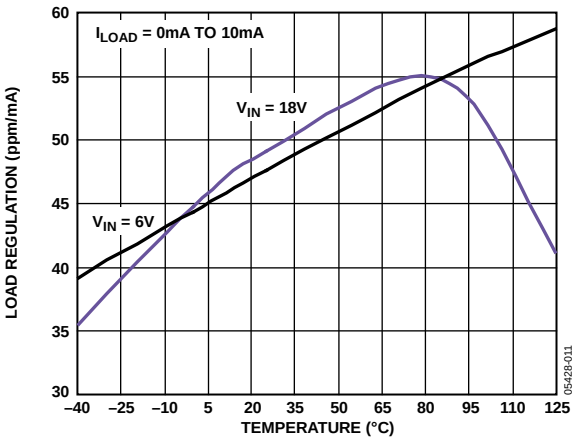


Figure 15. ADR441 Load Regulation vs. Temperature

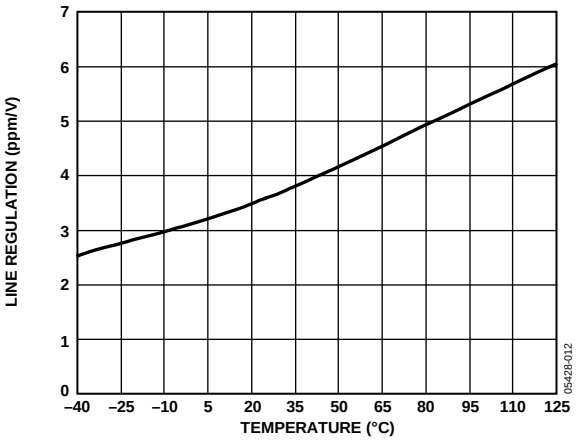


Figure 16. ADR445 Line Regulation vs. Temperature

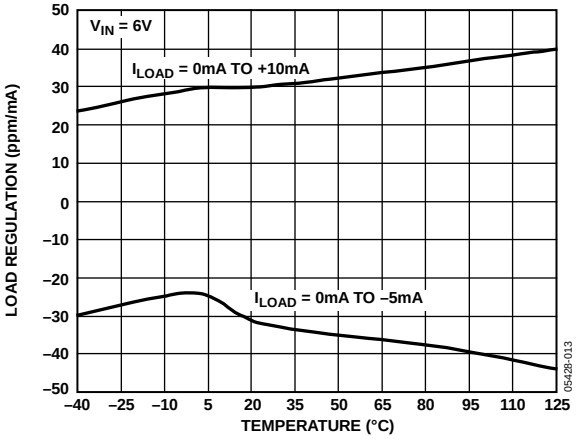


Figure 17. ADR445 Load Regulation vs. Temperature

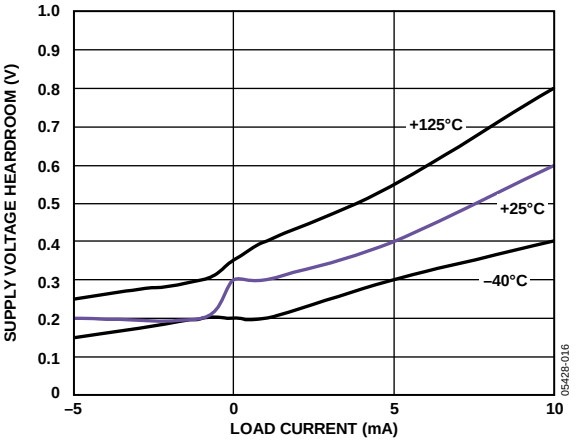


Figure 20. ADR445 Supply Voltage Headroom vs. Load Current

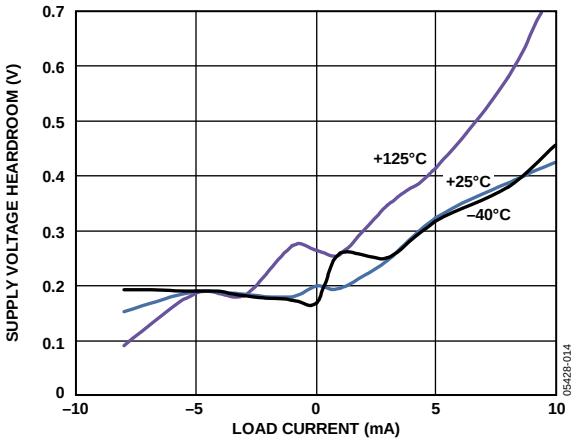


Figure 18. ADR441 Supply Voltage Headroom vs. Load Current

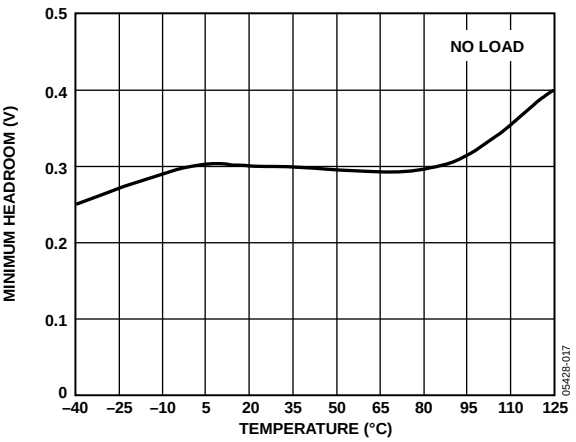


Figure 21. ADR445 Minimum Headroom vs. Temperature

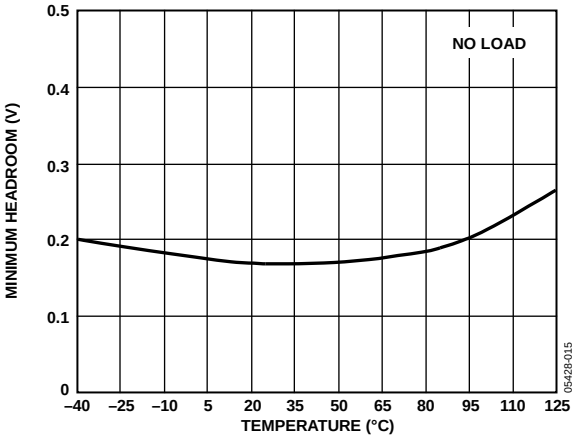


Figure 19. ADR441 Minimum Headroom vs. Temperature

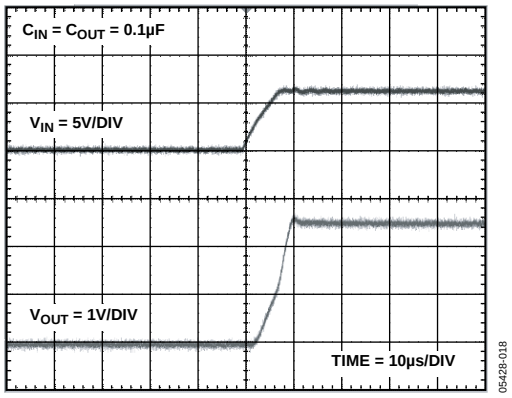


Figure 22. ADR441 Turn On Response

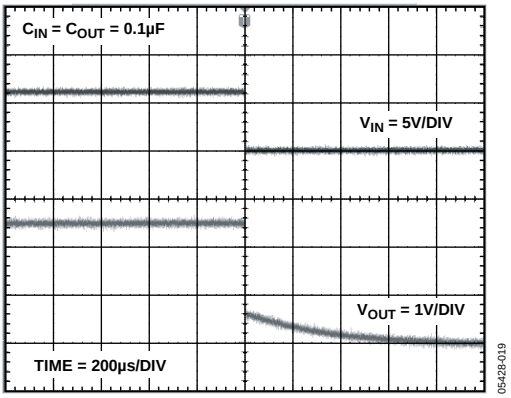


Figure 23. ADR441 Turn Off Response

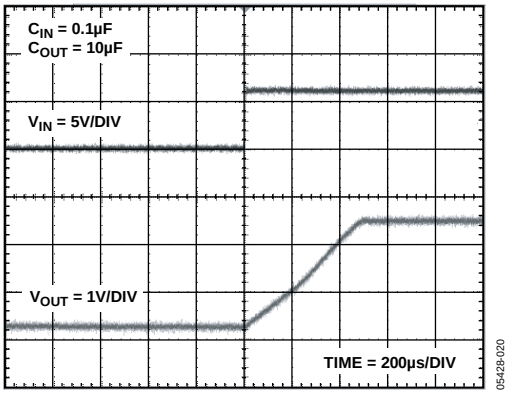


Figure 24. ADR441 Turn On Response

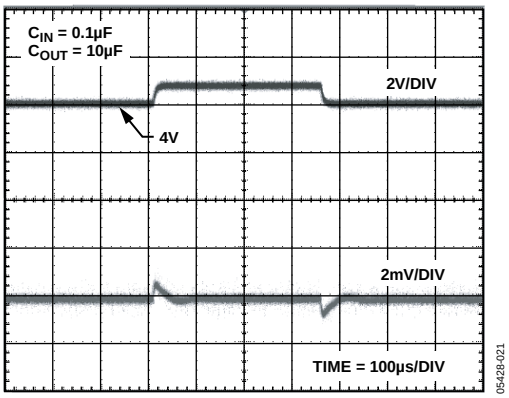


Figure 25. ADR441 Line Transient Response

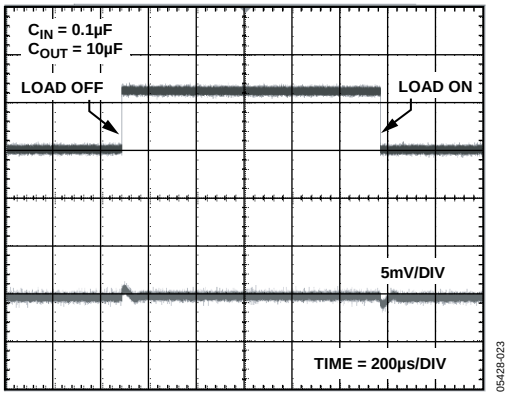


Figure 26. ADR441 Load Transient Response

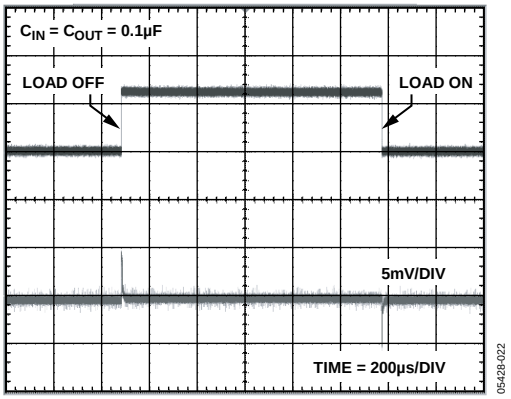


Figure 27. ADR441 Load Transient Response

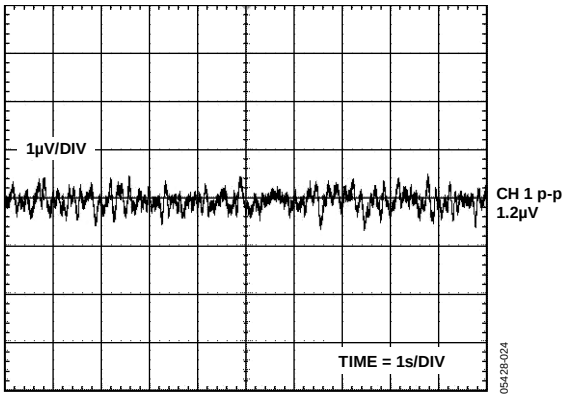


Figure 28. ADR441 0.1 Hz to 10.0 Hz Voltage Noise

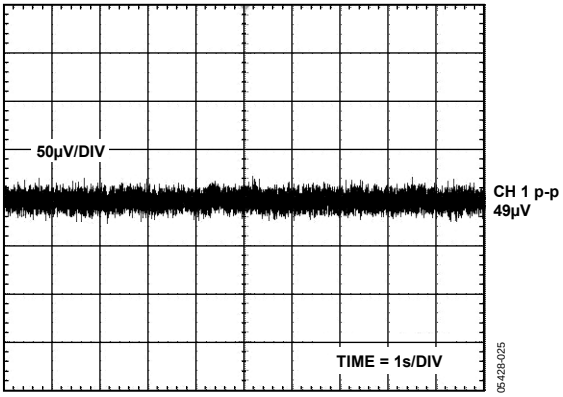


Figure 29. ADR441 10 Hz to 10 kHz Voltage Noise

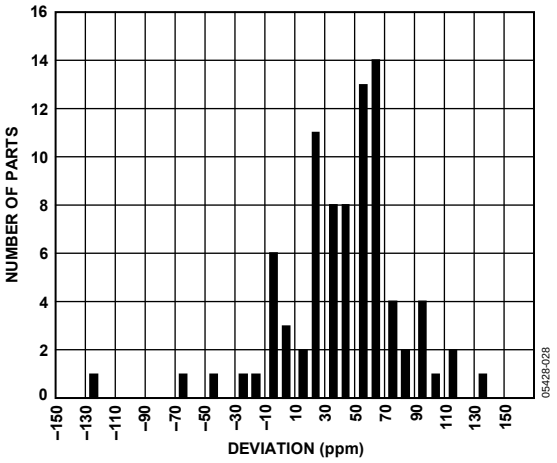


Figure 32. ADR441 Typical Output Voltage Hysteresis

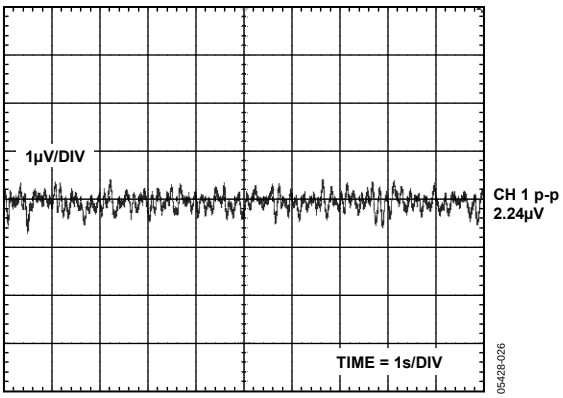


Figure 30. ADR445 0.1 Hz to 10.0 Hz Voltage Noise

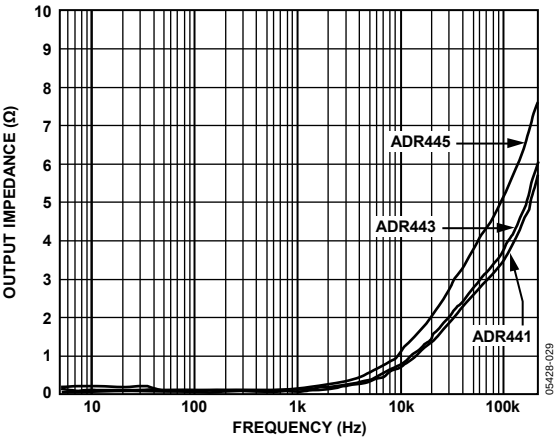


Figure 33. Output Impedance vs. Frequency

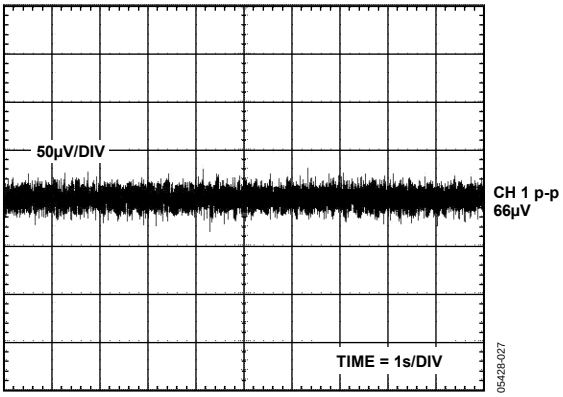


Figure 31. ADR445 10 Hz to 10 kHz Voltage Noise

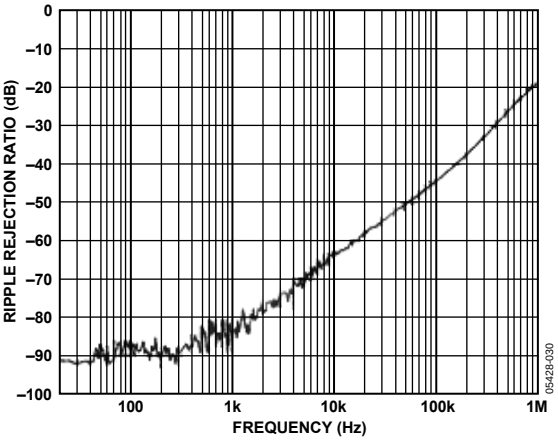


Figure 34. Ripple Rejection Ratio vs. Frequency

THEORY OF OPERATION

The ADR440/ADR441/ADR443/ADR444/ADR445 series of references uses a new reference generation technique known as XFET. This technique yields a reference with low dropout, optimal thermal hysteresis, and exceptionally low noise. The core of the XFET reference consists of two junction field effect transistors (JFETs), one of which has an extra channel implant to raise its pinch-off voltage. By running the two JFETs at the same drain current, the difference in pinch off voltage can be amplified and used to form a highly stable voltage reference.

The intrinsic reference voltage is around 0.5 V with a negative temperature coefficient of about −120 ppm/°C. This slope is essentially constant to the dielectric constant of silicon, and it can be closely compensated for by adding a correction term generated in the same fashion as the proportional to absolute temperature (PTAT) term used to compensate band gap references. The advantage of an XFET reference is its correction term, which is approximately 20 times lower and requires less correction than that of a band gap reference. Because most of the noise of a band gap reference comes from the temperature compensation circuitry, the XFET results in much lower noise.

Figure 35 shows the basic topology of the ADR440/ADR441/ADR443/ADR444/ADR445 series. The temperature correction term is provided by a current source with a value designed to be proportional to the absolute temperature. The general equation is

$$V_{OUT} = G\,(\Delta V_P - R1 \times I_{PTAT}) \quad (1)$$

where:
G is the gain of the reciprocal of the divider ratio.
ΔV_P is the difference in pinch off voltage between the two JFETs.
I_{PTAT} is the positive temperature coefficient correction current.

The ADR440/ADR441/ADR443/ADR444/ADR445 devices are created by on-chip adjustment of R2 and R3 to achieve the different voltage options at the reference output.

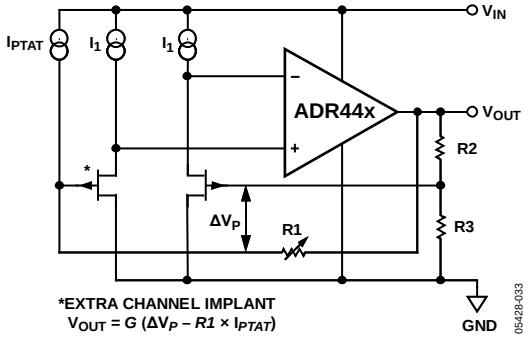


Figure 35. Simplified Schematic Device

POWER DISSIPATION CONSIDERATIONS

The ADR440/ADR441/ADR443/ADR444/ADR445 family of references is guaranteed to deliver load currents to 10 mA with an input voltage that ranges from 3 V to 18 V. When these devices are used in applications at higher currents, use the following equation to account for the temperature effects of increases in power dissipation:

$$T_J = P_D \times \theta_{JA} + T_A \quad (2)$$

where:
T_J and T_A are the junction and ambient temperatures, respectively.
P_D is the device power dissipation.
θ_{JA} is the device package thermal resistance.

BASIC VOLTAGE REFERENCE CONNECTIONS

The ADR440/ADR441/ADR443/ADR444/ADR445 family requires a 0.1 µF capacitor on the input and the output for stability. Although not required for operation, a 10 µF capacitor at the input can help with line voltage transient performance.

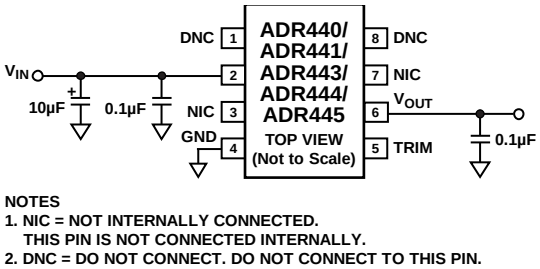


Figure 36. Basic Voltage Reference Configuration

NOISE PERFORMANCE

The noise generated by the ADR440/ADR441/ADR443/ADR444/ADR445 family of references is typically less than or equal to 2.25 µV p-p over the 0.1 Hz to 10.0 Hz band for the ADR440, ADR441, and ADR443. Figure 28 shows the 0.1 Hz to 10 Hz noise of the ADR441, which is only 1.2 µV p-p. The noise measurement is made with a band-pass filter composed of a two-pole high-pass filter with a corner frequency at 0.1 Hz and a two-pole low-pass filter with a corner frequency at 10.0 Hz.

TURN ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is defined as the turn on settling time. Two variables normally associated with this settling time are the time for the active circuits to settle and the time for the thermal gradients on the chip to stabilize. Figure 22 and Figure 23 show the turn on and turn off settling times for the ADR441.

APPLICATIONS INFORMATION

OUTPUT ADJUSTMENT

The ADR440/ADR441/ADR443/ADR444/ADR445 family features a TRIM pin that allows the user to adjust the output voltage of the device over a limited range. The TRIM pin allows errors from the reference and overall system errors to be trimmed out by connecting a potentiometer between the output and the ground, with the wiper connected to the TRIM pin. Figure 37 shows the optimal trim configuration. R1 allows fine adjustment of the output and is not always required. R_P must be sufficiently large so that the maximum output current from the ADR440/ADR441/ADR443/ADR444/ADR445 is not exceeded.

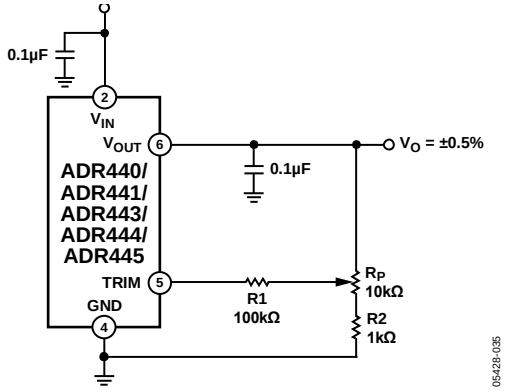


Figure 37. ADR440/ADR441/ADR443/ADR444/ADR445 Trim Function

Using the trim function has a negligible effect on the temperature performance of the ADR440/ADR441/ADR443/ADR444/ADR445. However, all resistors need to be low temperature coefficient resistors, or errors may occur.

BIPOLAR OUTPUTS

It is possible to obtain both positive and negative reference voltages by connecting the output of the ADR440/ADR441/ADR443/ADR444/ADR445 to the inverting terminal of an operational amplifier. Care must be taken when choosing Resistors R1 and R2 (see Figure 38). These resistors must be matched as closely as possible to ensure minimal differences between the negative and positive outputs. In addition, care must be taken to ensure performance over temperature. Use low temperature coefficient resistors if the circuit is used over temperature; otherwise, differences exist between the two outputs.

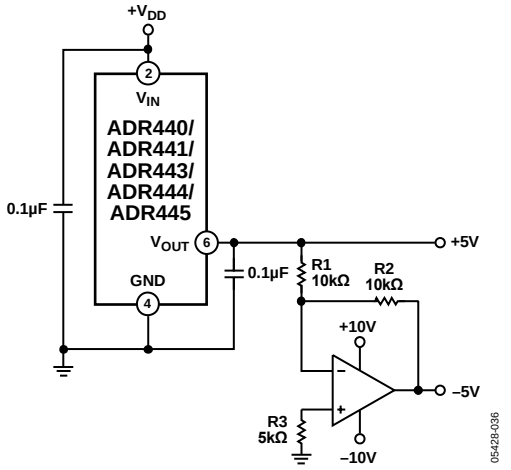


Figure 38. ADR440/ADR441/ADR443/ADR444/ADR445 Bipolar Outputs

PROGRAMMABLE VOLTAGE SOURCE

Extra components are needed to obtain different voltages than those offered by the ADR440/ADR441/ADR443/ADR444/ADR445. Two potentiometers set the desired voltage and the buffering amplifier, as shown in Figure 39. The potentiometer connected between V_{OUT} and GND, with its wiper connected to the noninverting input of the operational amplifier, takes care of coarse trim. The second potentiometer, with its wiper connected to the trim terminal of the ADR440/ADR441/ADR443/ADR444/ADR445, is used for fine adjustment. Resolution depends on the end to end resistance value and the resolution of the selected potentiometer.

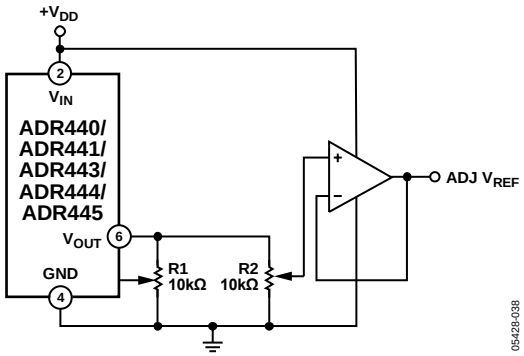


Figure 39. Programmable Voltage Source

For a completely programmable solution, replace the two potentiometers in Figure 39 with one Analog Devices dual digital potentiometer, offered with either a serial peripheral interface (SPI) or an I^2C interface. These interfaces set the position of the wiper on both potentiometers and allow the output voltage to be set. Table 10 lists compatible Analog Devices digital potentiometers.

Table 10. Digital Potentiometer Devices

Device No.	No. of Channels	No. of Positions	Interface	R (kΩ)	V_{DD}[1] (V)
AD5251	2.00	64.00	I²C	1, 10, 50, 100	5.5
AD5207	2.00	256.00	SPI	10, 50, 100	5.5
AD5242	2.00	256.00	I²C	10, 100, 1000	5.5
AD5262	2.00	256.00	SPI	20, 50, 200	15
AD5282	2.00	256.00	I²C	20, 50, 100	15
AD5252	2.00	256.00	I²C	1, 10, 50, 100	5.5
AD5232	2.00	256.00	SPI	10, 50, 100	5.5
AD5235	2.00	1024.00	SPI	25, 250	5.5
ADN2850	2.00	1024.00	SPI	25, 250	5.5

[1] Can also use a negative supply.

Adding a negative supply to the operational amplifier allows the user to produce a negative programmable reference by connecting the reference output to the inverting terminal of the operational amplifier. Choose feedback resistors to minimize errors over temperature.

PROGRAMMABLE CURRENT SOURCE

It is possible to build a programmable current source using a setup similar to the programmable voltage source, as shown in Figure 40. The constant voltage on the gate of the transistor sets the current through the load. Varying the voltage on the gate changes the current. This circuit does not require a dual digital potentiometer.

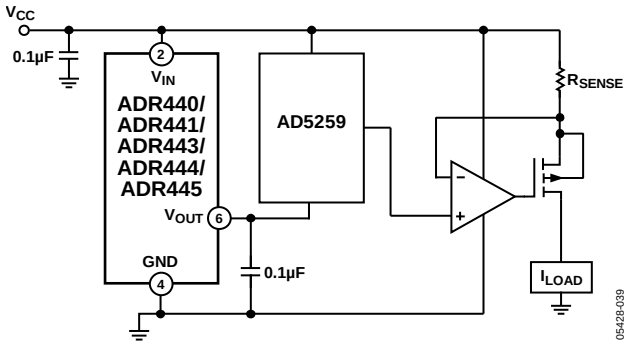


Figure 40. Programmable Current Source

HIGH VOLTAGE FLOATING CURRENT SOURCE

Use the circuit in Figure 41 to generate a floating current source with minimal self heating. This particular configuration can operate on high supply voltages, determined by the breakdown voltage of the N-channel JFET.

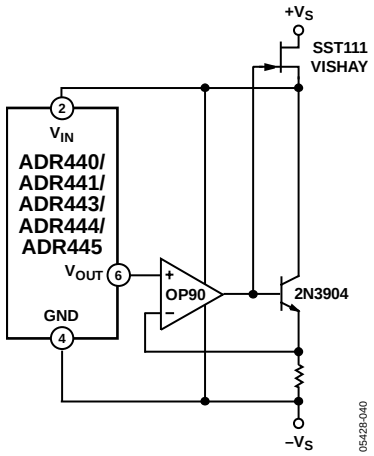


Figure 41. Floating Current Source

PRECISION OUTPUT REGULATOR (BOOSTED REFERENCE)

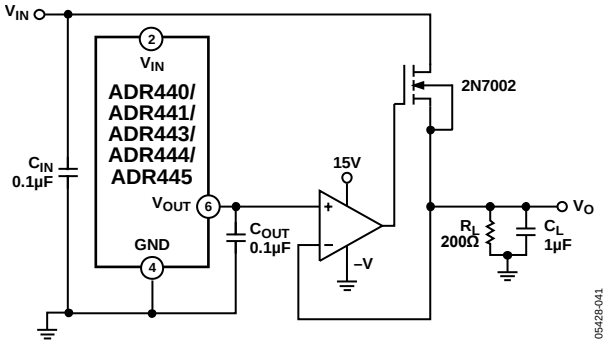
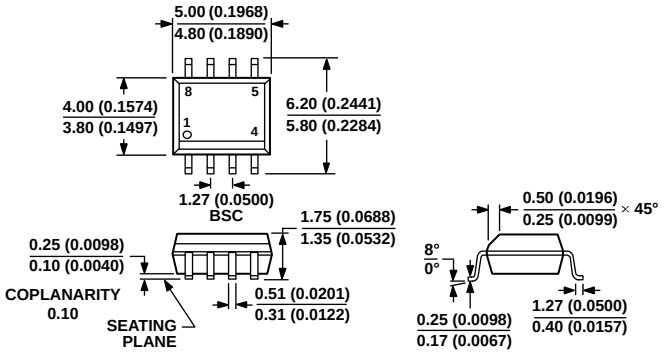


Figure 42. Boosted Output Reference

Higher current drive capability can be obtained without sacrificing accuracy by using the circuit in Figure 42. The operational amplifier regulates the MOSFET turn on, forcing V_O to equal the V_{REF}. Current is then drawn from V_{IN}, allowing increased current drive capability. The circuit allows a 50 mA load; use a larger MOSFET if higher current drive is required.

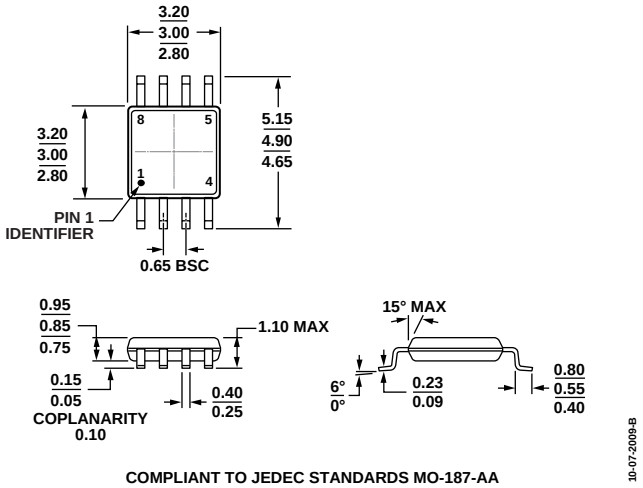
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 43. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

10-07-2009-B

Figure 44. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions show in millimeters