1 GHz to 60 GHz, Reflective, Silicon SP4T Switch

FEATURES

- Ultrawideband frequency range: 1 GHz to 60 GHz
- Low insertion loss
  - 2.2 dB typical up to 40 GHz
  - 2.8 dB typical up to 55 GHz
  - 3.2 dB typical up to 60 GHz
- High isolation
  - 33 dB typical up to 40 GHz
  - 28 dB typical up to 55 GHz
  - 28 dB typical up to 60 GHz
- High input linearity
  - P0.1dB: 25 dBm typical
  - IP3: 47 dBm typical
- High RF power handling
  - Through path: 24 dBm
  - Hot switching path: 24 dBm
- CMOS-/LVTTL-compatible
- No low frequency spur
- Fast RF switching time: 25 ns
- RF settling time (50% V_{CTRL} to 0.1 dB of RF_{OUT}): 35 ns
- Single-supply operation capability (VDD = 3.3 V, VSS = 0 V)
- 24-terminal, 3 mm × 3 mm, RoHS-compliant, LGA package

APPLICATIONS

- Industrial scanners
- Test instrumentation
- Cellular infrastructure—mmWave 5G
- Military radios, radars, and electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

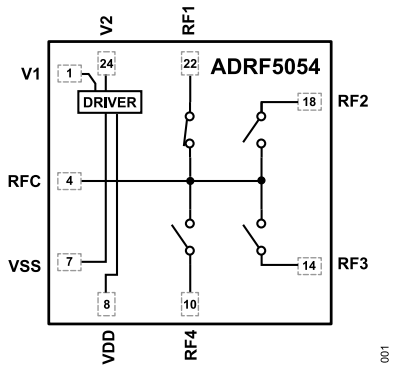

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5054 is a reflective, SP4T switch manufactured in a silicon process. The ADRF5054 operates from 1 GHz to 60 GHz. The switch has a low insertion loss of 2.2 dB and 3.2 dB with 33 dB and 28 dB isolation at 40 GHz and 60 GHz, respectively. The ADRF5054 has an RF input power handling capability of 24 dBm for the through and hot switching paths. The ADRF5054 requires dual-supply voltages of ±3.3 V. The ADRF5054 employs complementary metal-oxide semiconductor (CMOS)- and low voltage transistor logic (LVTTL)-compatible control.

The ADRF5054 can also operate with a single positive supply voltage (V_{DD}) applied while the negative supply voltage (V_{SS}) is tied to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance are derated (see Table 2 for more details).

The ADRF5054 comes in a 24-terminal, 3 mm × 3 mm, RoHS compliant, land grid array (LGA) package and can operate from −40°C to +105°C.

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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REVISION HISTORY

5/2023—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V1 = 0 V or V_{DD}, V2 = 0 V or V_{DD}, T_{CASE} = 25°C for a 50 Ω system, unless otherwise noted. RFx refers to RF1 to RF4, and V_{CTRL} is voltages of the digital inputs, V1 and V2.

Table 1. Electrical Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		1		60	GHz
INSERTION LOSS						
Between RFC and RFx (On)		1 GHz to 18 GHz		1.7		dB
		18 GHz to 40 GHz		2.2		dB
		40 GHz to 55 GHz		2.8		dB
		55 GHz to 60 GHz		3.2		dB
RETURN LOSS						
RFC		1 GHz to 18 GHz		19		dB
		18 GHz to 40 GHz		20		dB
		40 GHz to 55 GHz		22		dB
		55 GHz to 60 GHz		18		dB
RF1 to RF4 (On)		1 GHz to 18 GHz		23		dB
		18 GHz to 40 GHz		15		dB
		40 GHz to 55 GHz		22		dB
		55 GHz to 60 GHz		20		dB
ISOLATION						
Between RFC and RF1 (Off) or RFC and RF4 (Off)		1 GHz to 18 GHz		42		dB
		18 GHz to 40 GHz		37		dB
		40 GHz to 55 GHz		28		dB
		55 GHz to 60 GHz		28		dB
Between RFC and RF2 (Off) or RFC and RF3 (Off)		1 GHz to 18 GHz		41		dB
		18 GHz to 40 GHz		33		dB
		40 GHz to 55 GHz		31		dB
		55 GHz to 60 GHz		32		dB
Between RF1 and RF4 (Selected) and RF2 and RF3 (Off)		1 GHz to 18 GHz		43		dB
		18 GHz to 40 GHz		36		dB
		40 GHz to 55 GHz		33		dB
		55 GHz to 60 GHz		36		dB
Between RF2 and RF3 (Selected) and RF1 and RF4 (Off)		1 GHz to 18 GHz		45		dB
		18 GHz to 40 GHz		36		dB
		40 GHz to 55 GHz		37		dB
		55 GHz to 60 GHz		33		dB
SWITCHING CHARACTERISTICS						
Rise Time and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output (RF_{OUT})		5		ns
On Time and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		25		ns
RF Settling Time						
0.1 dB		50% V_{CTRL} to 0.1 dB of final RF_{OUT}		35		ns
INPUT LINEARITY[1]		1 GHz to 60 GHz				
0.1 dB Power Compression	P0.1dB			25		dBm
Third-Order Intercept	IP3	Two-tone input power = 12 dBm each tone, Δf = 1 MHz		47		dBm
SUPPLY CURRENT		VDD and VSS pins				
Positive Supply Current	I_{DD}			145		µA
Negative Supply Current	I_{SS}			510		µA

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL CONTROL INPUTS		V1 and V2 pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low and High	I_{INL}, I_{INH}			<1		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Voltage	V_{CTRL}		0		V_{DD}	V
RF Input Power[2, 3]	P_{IN}	f = 3 GHz to 60 GHz, T_{CASE} = 85°C				
Through Path		RF signal is applied to RFC or through connected RFx			24	dBm
Hot Switching		RF signal is present at RFC while switching between RFx			24	dBm
Case Temperature	T_{CASE}		−40		+105	°C

[1] For input linearity performance over frequency, see Figure 20 to Figure 23.

[2] For power derating over frequency, see Figure 2.

[3] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

SINGLE-SUPPLY OPERATION

V_{DD} = 3.3 V, V_{SS} = 0 V, V1 = 0 V or V_{DD}, V2 = 0 V or V_{DD}, and T_{CASE} = 25°C for a 50 Ω system, unless otherwise noted.

Table 2. Single-Supply Operation Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		1		60	GHz
SWITCHING CHARACTERISTICS						
Rise Time and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF_{OUT}		20		ns
On Time and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		58		ns
0.1 dB RF Settling Time		50% V_{CTRL} to 0.1 dB of final RF_{OUT}		62		ns
INPUT LINEARITY		f = 1 GHz to 60 GHz				
0.1 dB Power Compression	P0.1dB			13		dBm
Input Third-Order Intercept	IIP3	Two-tone input power = 0 dBm each tone, Δf = 1 MHz		41		dBm
RECOMMENDED OPERATING CONDITONS						
RF Input Power[1]	P_{IN}	f = 3 GHz to 60 GHz, T_{CASE} = 85°C				
Through Path		RF signal is applied to the RFC or through connected RFx			13	dBm
Hot Switching		RF signal is applied to the RFC while switching between RFx			13	dBm

[1] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 1 dB.

ABSOLUTE MAXIMUM RATINGS

For the recommended operating conditions, see Table 1.

Table 3. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	−0.3 V to +3.6 V
V_{SS}	−3.6 V to +0.3 V
Digital Control Input Voltage[1]	
Voltage	−0.3 V to V_{DD} + 0.3 V
Current	3 mA
RF Input Power[2] (f = 3 GHz to 60 GHz, T_{CASE} = 85°C[3])	
Through Path	25 dBm
Hot Switching	25 dBm
RF Input Power, Single Supply (V_{DD} = 3.3 V, V_{SS} = 0 V, f = 3 GHz to 60 GHz, T_{CASE} = 85°C[3])	
Through Path	14 dBm
Hot Switching (RFC)	14 dBm
RF Input Power, Unbiased (V_{DD} and V_{SS} = 0 V)	14 dBm
Temperature	
Junction, T_J	135°C
Storage Range	−65°C to +150°C
Reflow	260°C

[1] Overvoltages at digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.

[2] For power derating over frequency, see Figure 2.

[3] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB for the dual supply and 1 dB for the single supply.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-24-19, Through Path	345	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVE

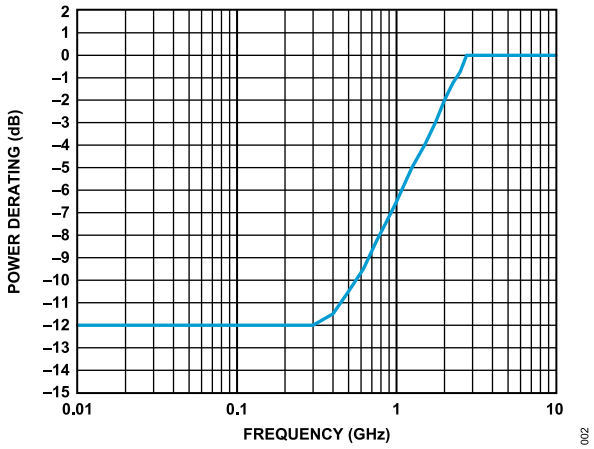

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADRF5054

Table 5. ADRF5054, 24-Terminal LGA

ESD Model	Withstand Threshold (V)
HBM	±1000 for RFx pins
	±2000 for supply and digital control pins
CDM	±500 for all pins

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

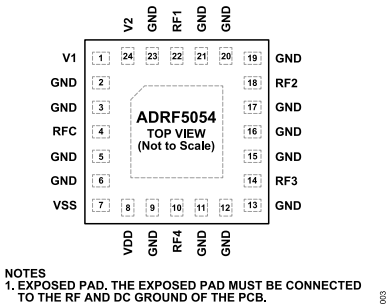

Figure 3. Pin Configuration (Top View)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V1	Control Input 1. See Figure 6 for the interface schematic.
2, 3, 5, 6, 9, 11 to 13, 15 to 17, 19 to 21, 23	GND	Ground. The GND pins must be connected to the RF and DC ground of the PCB.
4	RFC	RF Common Port. The RFC pin is DC-coupled to 0 V. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
7	VSS	Negative Supply Voltage. See Figure 7 for the interface schematic.
8	VDD	Positive Supply Voltage. See Figure 5 for the interface schematic.
10	RF4	RF Throw Port 4. The RF4 pin is DC-coupled to 0 V. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
14	RF3	RF Throw Port 3. The RF3 pin is DC-coupled to 0 V. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
18	RF2	RF Throw Port 2. The RF2 pin is DC-coupled to 0 V. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
22	RF1	RF Throw Port 1. The RF1 pin is DC-coupled to 0 V. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
24	V2	Control Input 2. See Figure 6 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and DC ground of the PCB.

INTERFACE SCHEMATICS

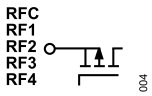

Figure 4. RFx Pins Interface Schematic

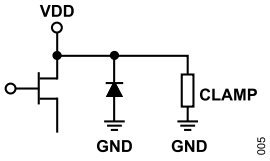

Figure 5. VDD Interface Schematic

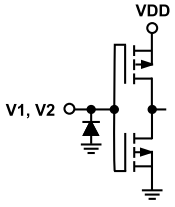

Figure 6. V1, V2 Pin Interface Schematic

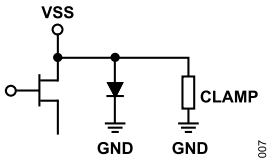

Figure 7. VSS Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V1 = 0 V or V_{DD}, V2 = 0 V or V_{DD}, and T_{CASE} = 25°C for a 50 Ω system, unless otherwise noted. RFx refers to RF1 to RF4.

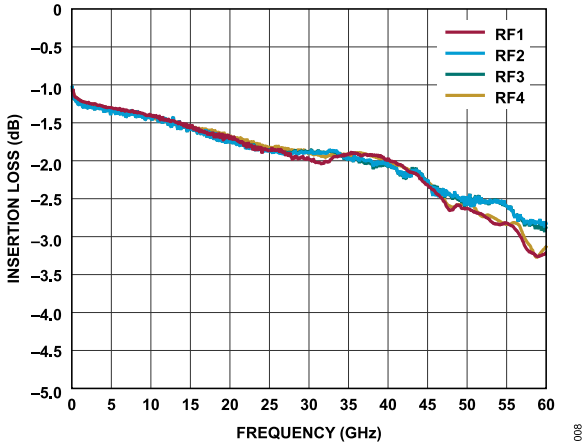

Figure 8. Insertion Loss vs. Frequency for RFx

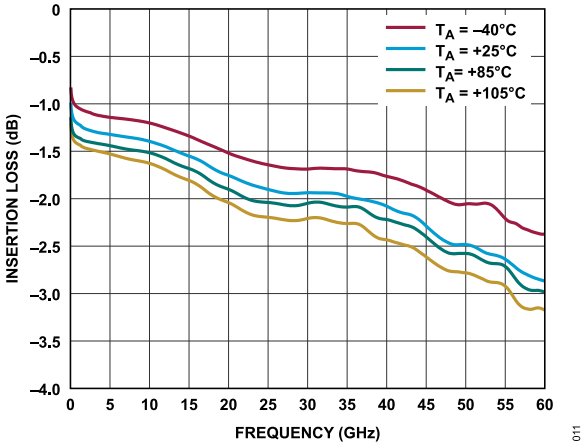

Figure 11. Insertion Loss for RF2 Selected vs. Frequency over Temperature

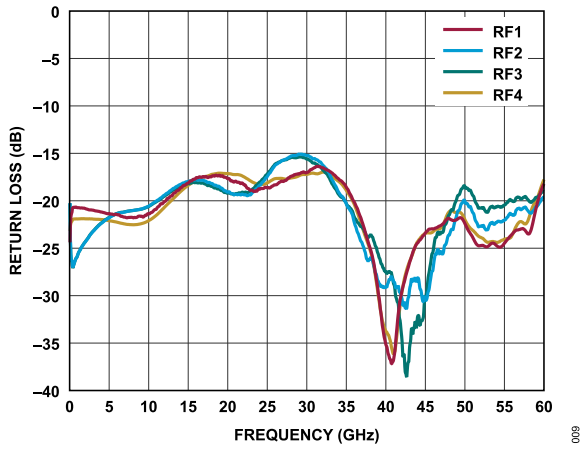

Figure 9. Return Loss for RFC when RFx Selected vs. Frequency

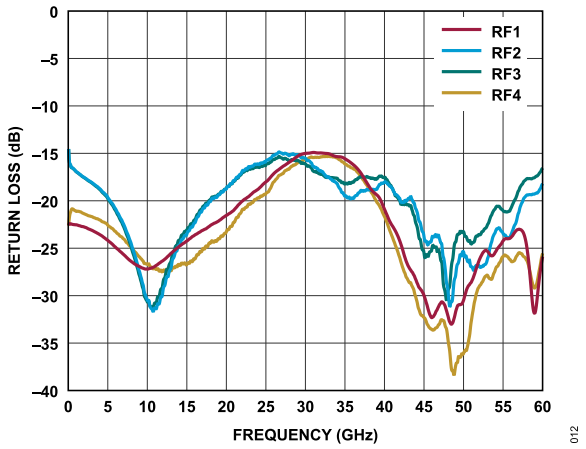

Figure 12. Return Loss for RFx Selected vs. Frequency

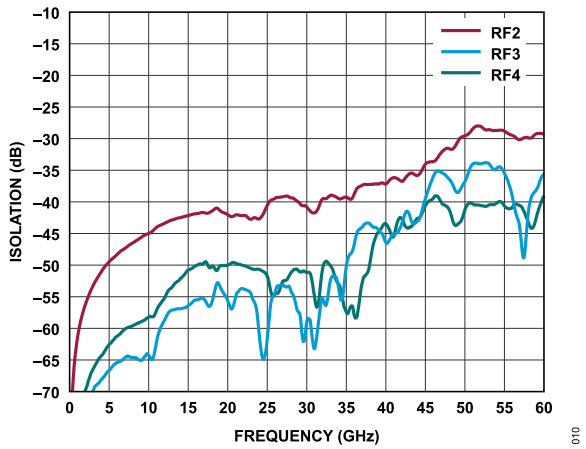

Figure 10. RFC to RF2, RF3, and RF4 Isolation vs. Frequency, RF1 Selected

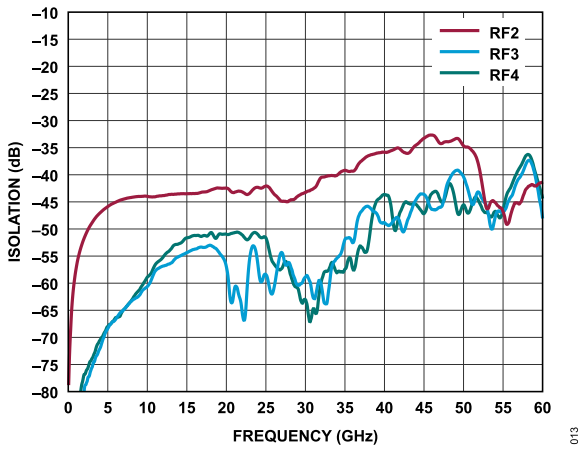

Figure 13. RFC to RFx Isolation vs. Frequency, RF1 Selected

TYPICAL PERFORMANCE CHARACTERISTICS

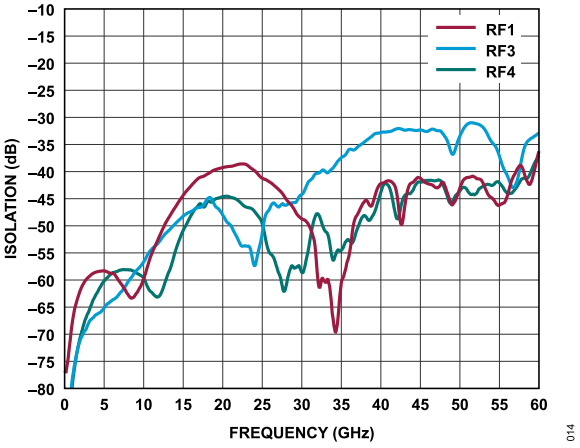

Figure 14. RFC to RFx Isolation vs. Frequency, RF2 Selected

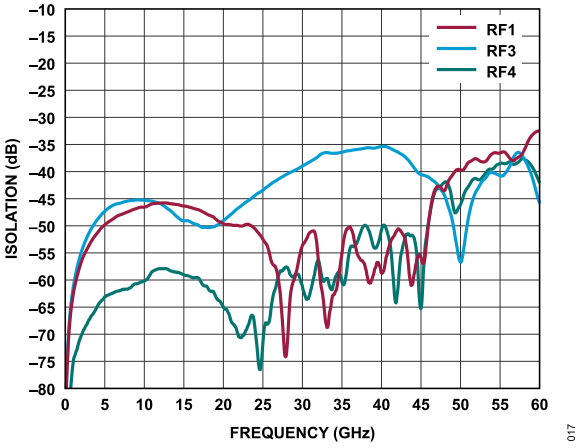

Figure 17. RF2 to RFx Isolation vs. Frequency, RF2 Selected

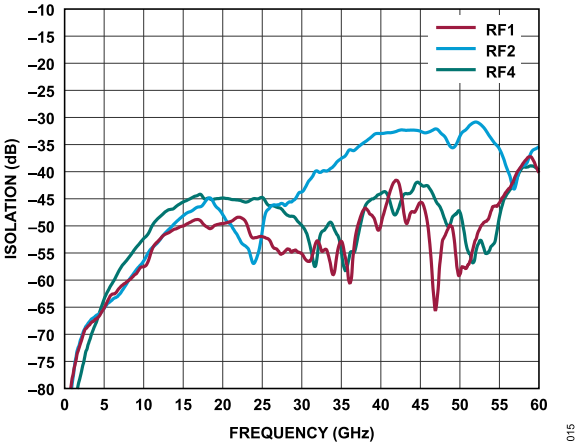

Figure 15. RFC to RFx Isolation vs. Frequency, RF3 Selected

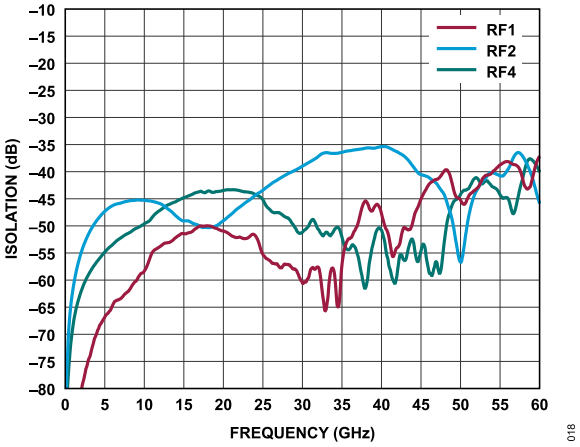

Figure 18. RF3 to RFx Isolation vs. Frequency, RF3 Selected

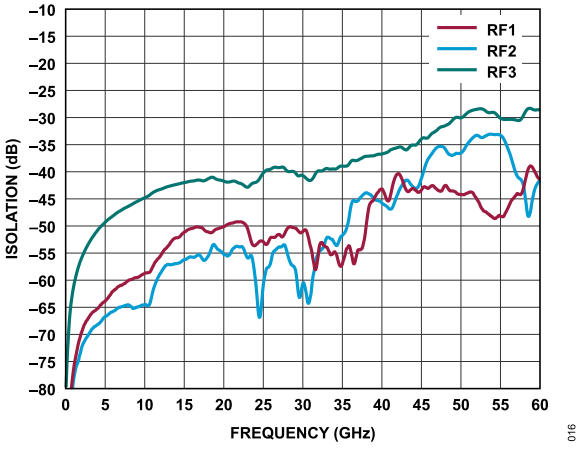

Figure 16. RFC to RFx Isolation vs. Frequency, RF4 Selected

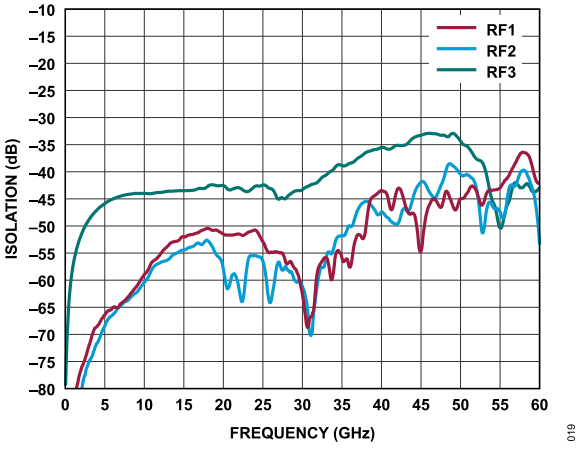

Figure 19. RF4 to RFx Isolation vs. Frequency, RF4 Selected

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V1 = 0 V or V_{DD}, V2 = 0 V or V_{DD}, and T_{CASE} = 25°C for a 50 Ω system, unless otherwise noted. RFx refers to RF1 to RF4.

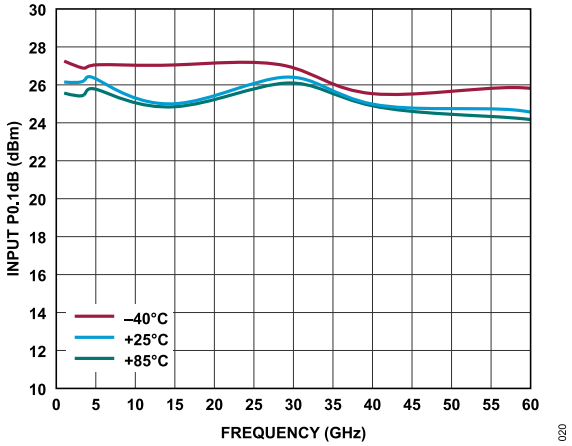

Figure 20. Input P0.1dB vs. Frequency over Temperature

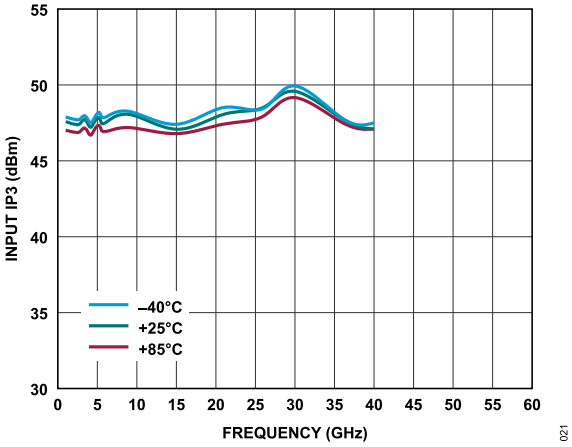

Figure 21. Input IP3 vs. Frequency over Temperature

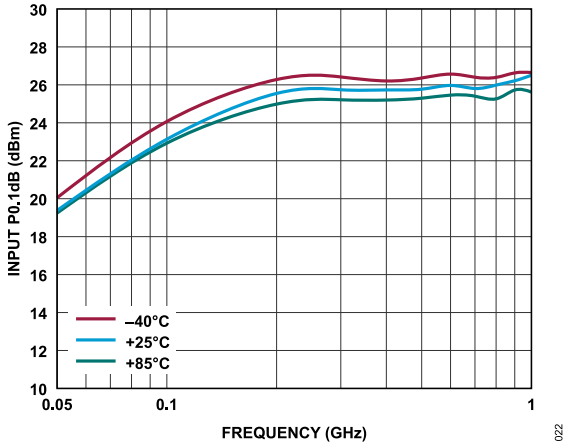

Figure 22. Input P0.1dB vs. Frequency (Low Frequency Detail) over Temperature

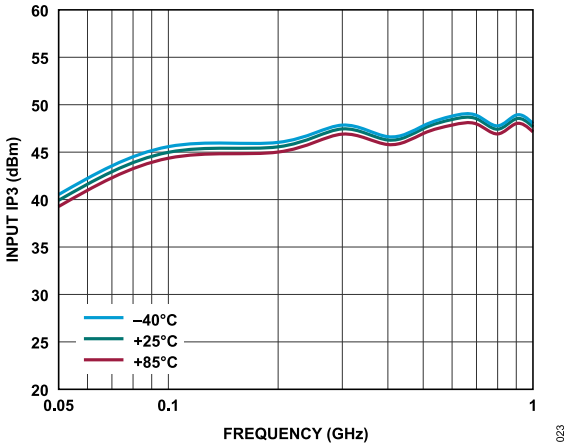

Figure 23. Input IP3 vs. Frequency (Low Frequency Detail) over Temperature

THEORY OF OPERATION

The ADRF5054 can interface CMOS-/LVTTL-compatible logic directly. The V1 and V2 pins determine which RF port is in the insertion loss state and in the isolation state. See Table 7 for the control voltage truth table.

RF INPUT AND OUTPUT

The RF ports (RFC, RF1 to RF4) are DC-coupled to 0 V, and no DC blocking is required at the RF ports when the RF line potential is equal to 0 V. The RF ports are internally matched to 50 Ω.

The ADRF5054 is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation paths provide high loss between the insertion loss path and the unselected RF throw ports. The unselected RF ports of the ADRF5054 are reflective.

The power handling of the ADRF5054 derates with frequencies less than 3 GHz. See Figure 2 for the derating of the RF power toward the lower frequencies.

POWER SUPPLY

The ADRF5054 requires a positive supply voltage applied to the VDD pin, and a negative supply voltage applied to the VSS pin.

Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp-up.
3. Apply digital control inputs. The relative order of the control inputs is not important. However, powering the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller is in a high impedance state after VDD is powered up and the control pins are not driven to a valid logic state.
4. Apply the RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

Table 7. Control Voltage Truth Table

Digital Control Inputs		RFx Paths			
V1	V2	RFC to RF1	RFC to RF2	RFC to RF3	RFC to RF4
Low	Low	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
High	Low	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	High	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
High	High	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)

APPLICATIONS INFORMATION

The ADRF5054 has two power supply pins (VDD and VSS) and two control pins (V1 and V2). Figure 24 shows the external components and connections for the supply pins. The VDD and VSS pins are decoupled with a 100 pF multilayer ceramic capacitor. The device pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RF pins when the RF lines are biased at a voltage different than 0 V. See the Pin Configuration and Function Descriptions section for additional information.

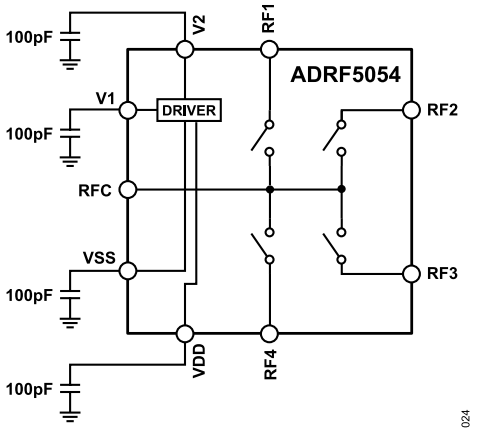

Figure 24. Recommended Schematic

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50 Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with 50 Ω characteristic impedance on the PCB. Figure 25 shows the referenced CPWG RF trace design for an RF substrate with 8 mil thick Rogers RO4003C dielectric material. The RF trace with a 16 mil width and a 13 mil clearance is recommended for 1.7 mil finished copper thickness.

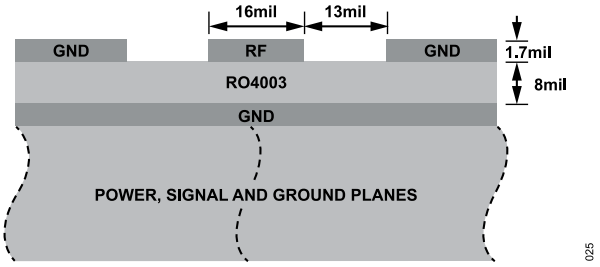

Figure 25. Example PCB Stackup

Figure 26 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with densely filled through vias for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

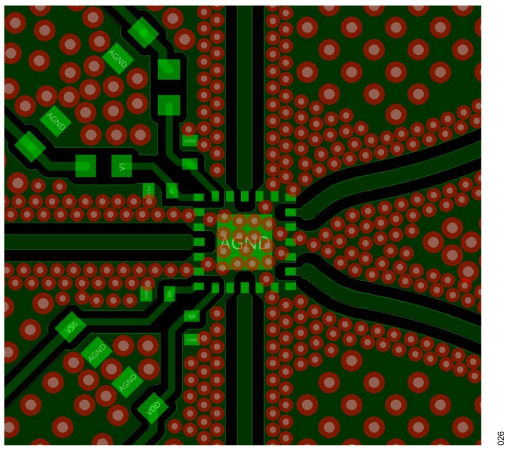

Figure 26. PCB Layout

Figure 27 and Figure 28 show the recommended layout from the device RFx pins to the 50 Ω CPWG on the referenced stackup. PCB pads are drawn 1:1 to device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The paste mask is designed to match the device pads without any aperture reduction. The paste mask is divided into multiple openings for the paddle.

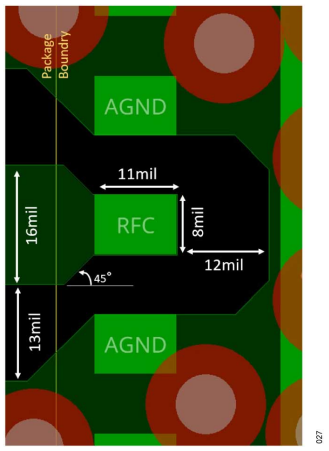

Figure 27. Recommended RFC, RF1 and RF4 Pin Transition

APPLICATIONS INFORMATION

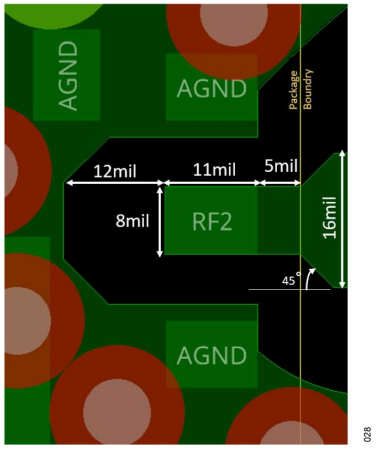

Figure 28. Recommended RF2 and RF3 Pin Transition

For alternate PCB stackups with different dielectric thickness and RF trace design, contact Analog Devices, Inc., Technical Support Request for further recommendations.