ADRF5080

Reflective, Silicon SP8T Switch, 100 MHz to 20 GHz

FEATURES

- Ultrawideband frequency range: 100 MHz to 20 GHz
- Low insertion loss
  - 1.3 dB up to 6 GHz
  - 1.5 dB up to 12 GHz
  - 1.85 dB up to 20 GHz
- High isolation: >40 dB up to 20 GHz
- High input linearity
  - P0.1dB: 33 dBm typical
  - IP3: 55 dBm typical
- High RF power handling
  - Insertion loss path
    - Average: 30 dBm
    - Pulse (100 µs pulse width, 15% duty cycle): 33 dBm
  - Hot switching: 30 dBm
- Switching on and off time: 65 ns
- 0.1 dB settling time (50% V_{CTRL} to 0.1 dB final RF_{OUT}): 50 ns
- Single-supply operation with derated power handling
- All off state control
- Logic select control
- No low frequency spurs
- 36-terminal, 5.50 mm x 5.50 mm LGA package

APPLICATIONS

- Test and instrumentation
- Military radios, radars, and electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

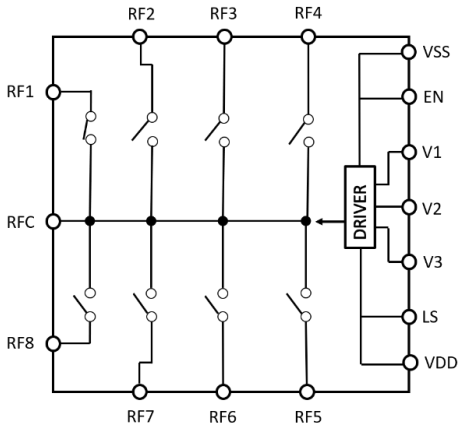

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5080 is a reflective, SP8T switch manufactured in the silicon process. The ADRF5080 operates from 100 MHz to 20 GHz with an insertion loss of lower than 1.85 dB and an isolation higher than 40 dB. The device has an RF input power handling capability of 30 dBm continuous wave power for the insertion loss path.

The ADRF5080 operates with a dual-supply voltage, +3.3 V and −3.3 V. The device can also operate with a single-supply voltage (VDD) applied while the negative supply pin (VSS) is tied to ground. The single-supply operation condition requires a lower operating power while the excellent small signal performance is maintained (see Table 2).

The ADRF5080 employs complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls. The logic select pin is functioned to the toggle state sequence.

The ADRF5080 comes in a 36-terminal, 5.50 mm × 5.50 mm, RoHS compliant, land grid array (LGA) package and can operate from −40°C to +105°C.

TABLE OF CONTENTS

SPECIFICATIONS

VDD = 3.3 V, VSS = −3.3 V, LS voltage (V_{LS}), EN voltage (V_{EN}), V1, V2 or V3 = 0 V or VDD, and T_{CASE} = 25°C, with a 50 Ω system, unless otherwise noted. RFx refers to RF1 to RF8, and V_{CTRL} is the digital control inputs voltage of the V1, V2, and V3 pins.

Table 1. Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		100		20,000	MHz
INSERTION LOSS						
Between RFC and RFx (On)		100 MHz to 6 GHz		1.3		dB
		6 GHz to 12 GHz		1.5		dB
		12 GHz to 20 GHz		1.85		dB
ISOLATION						
Between RFC and RFx		100 MHz to 12 GHz		50		dB
		12 GHz to 20 GHz		45		dB
Between RFx and RFx		100 MHz to 12 GHz		46		dB
		12 GHz to 20 GHz		40		dB
RETURN LOSS						
RFC (On)		100 MHz to 6 GHz		21		dB
		6 GHz to 20 GHz		17		dB
RFx (On)		100 MHz to 6 GHz		22		dB
		6 GHz to 12 GHz		19		dB
		12 GHz to 20 GHz		17		dB
SWITCHING CHARACTERISTICS						
Rise Time and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output (RF_{OUT})		10		ns
On Time and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		55		ns
RF Settling Time						
0.1 dB		50% V_{CTRL} to 0.1 dB of final RF_{OUT}		100		ns
INPUT LINEARITY[1]						
Compression Point						
0.1 dB	P0.1dB	f = 100 MHz to 20 GHz		33		dBm
1 dB	P1dB	f = 100 MHz to 20 GHz		33.5		dBm
Third-Order Intercept	IIP3	Two tone input power = 15 dBm each tone, f = 100 MHz to 20 GHz, Δf = 1 MHz		55		dBm
VIDEO FEEDTHROUGH[2]				TBD		mV p-p
SUPPLY CURRENT		VDD and VSS pins				
Positive Supply Current	I_{DD}			220		µA
Negative Supply Current	I_{SS}			580		µA
DIGITAL CONTROL INPUTS		LS, EN, V1, V2, and V3 pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			<1		µA
High	I_{INH}	V1, V2, and V3 pins		<1		µA
		EN and LS pins		33		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Input Voltage	V_{CTRL}		0		VDD	V
RF Power Handling[3]	P_{IN}	f = 100 MHz to 20 GHz, T_{CASE} = 85°C[4]				
Insertion Loss Path						

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Average					30	dBm
Pulse		100 µs pulse width, 15% duty cycle			33	dBm
Hot Switching					30	dBm
Case Temperature	T_{CASE}		−40		+105	°C

[1] For input linearity performance over frequency, see the Input Power Compression and Third-Order Intercept section.

[2] Video feedthrough is the peak transient measured at the RF ports in a 50 Ω test setup, without an RF signal present while switching the control voltage.

[3] For power derating over frequency, see Figure 2.

[4] For 105°C operation, the power handling derates from the T_{CASE} = 85°C specification by 3 dB.

SINGLE-SUPPLY OPERATION SPECIFICATIONS

VDD = 3.3 V, VSS = 0 V, V_{CTRL} = 0 V or VDD, and T_{CASE} = 25°C, with a 50 Ω system, unless otherwise noted.

The small signal and bias characteristics are maintained for the single-supply operation.

Table 2. Single-Supply Operation Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			100		20,000	MHz
SWITCHING						
Rise Time and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF_{OUT}		TBD		ns
On Time and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		TBD		ns
0.1 dB Settling Time		50% V_{CTRL} to 0.1 dB of final RF_{OUT}		TBD		ns
INPUT LINEARITY						
0.1 dB Power Compression	P0.1dB	f = 100 MHz to 20 GHz		TBD		dBm
Third-Order Intercept	IP3	Two-tone input power = 15 dBm each tone, f = 100 MHz to 20 GHz, Δf = 1 MHz		TBD		dBm
Second-Order Intercept	IP2	Two-tone input power = 15 dBm each tone, f = TBD GHz, Δf = 1 MHz		TBD		dBm
RECOMMENDED OPERATING CONDITIONS						
RF Power Handling		f = 100 MHz to 20 GHz, T_{CASE} = 85°C				
Insertion Loss Path						
Average					TBD	dBm
Pulse		100 µs pulse width, 15% Duty cycle			TBD	dBm
Hot Switching					TBD	dBm
Case Temperature	T_{CASE}		−40		+105	°C

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1 and Table 2.

Table 3. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
VDD	−0.3 V to +3.6 V
VSS	−3.6 V to +0.3 V
Digital Control Input[1]	
Voltage	−0.3 V to VDD + 0.3 V or 3.3 V
Current	3 mA
RF Input Power[2]	
Dual Supply (VDD = 3.3 V, VSS = −3.3 V, f = 100 MHz to 20 GHz, T_{CASE} = 85°C[3])	
Through Path	33.5 dBm
Hot Switching	30.5 dBm
Single Supply (VDD = 3.3 V, VSS = 0 V, f = 100 MHz to 20 GHz, T_{CASE} = 85°C[3])	
Through Path	TBD dBm
Hot Switching	TBD dBm
Unbiased (VDD, VSS = 0V)	TBD dBm
Temperature	
Junction (T_J)	135°C
Storage	−65°C to +150°C
Reflow	260°C

1 Overvoltages at digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.

2 For power derating over frequency, see Figure 2.

3 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-36-2		
Insertion Loss Path	130	°C/W

1 θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the round pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVE

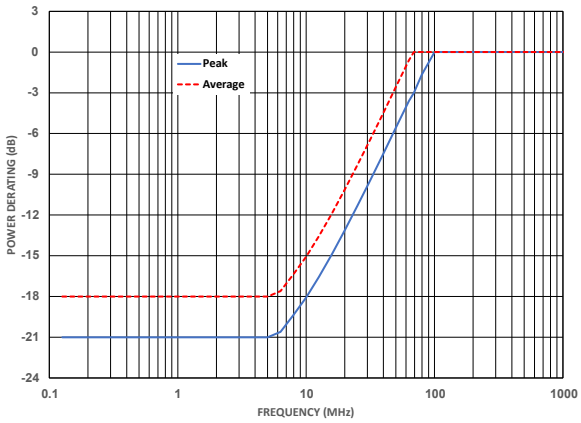

Figure 2. Power Derating vs. Frequency, T_{CASE} = 85°C

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5080

Table 5. ADRF5080, 36-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM		
RFx and RFC Pins	2000	2
Supply and Control Pins	2000	2
CDM	500	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

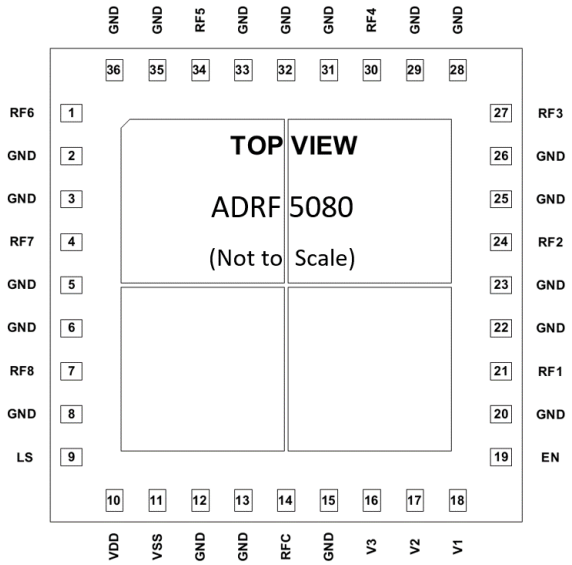

Figure 3. Pin Configuration (Top View)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RF6	RF Throw Port 6. The RF6 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
2, 3, 5, 6, 8, 12, 13, 15, 20, 22, 23, 25, 26, 28, 29, 31 to 33, 35, 36	GND	Ground. The GND pins must be connected to the RF and DC ground of the PCB.
4	RF7	RF Throw Port 7. The RF7 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
7	RF8	RF Throw Port 8. The RF8 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
9	LS	Logic Select. See Table 7 for the truth table. See Figure 6 for the interface schematic.
10	VDD	Positive Supply Voltage.
11	VSS	Negative Supply Voltage.
14	RFC	RF Common Port. The RFC pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
16	V3	Digital Input 3. See Table 7 for the truth table. See Figure 5 for the interface schematic.
17	V2	Digital Input 2. See Table 7 for the truth table. See Figure 5 for the interface schematic.
18	V1	Digital Input 1. See Table 7 for the truth table. See Figure 5 for the interface schematic.
19	EN	Enable Input. See Table 7 for the truth table. See Figure 6 for the interface schematic.
21	RF1	RF Throw Port 1. The RF1 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
24	RF2	RF Throw Port 2. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
27	RF3	RF Throw Port 3. The RF3 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
30	RF4	RF Throw Port 4. The RF4 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
34	RF5	RF Throw Port 5. The RF5 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and DC ground of the PCB.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

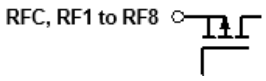

Figure 4. RFx (RFC, RF1 to RF8) Interface Schematic

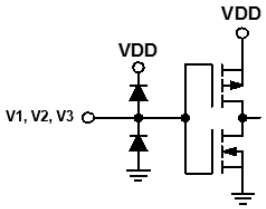

Figure 5. V1 to V3 Interface Schematic

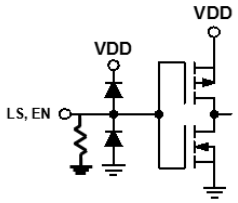

Figure 6. EN and LS Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

VDD = 3.3 V, VSS = −3.3 V, V_{LS}, V_{EN}, V1, V2, or V3 = 0 V or V_{DD}, and T_{CASE} = 25°C in a 50 Ω system, unless otherwise noted. Measured on the evaluation board.

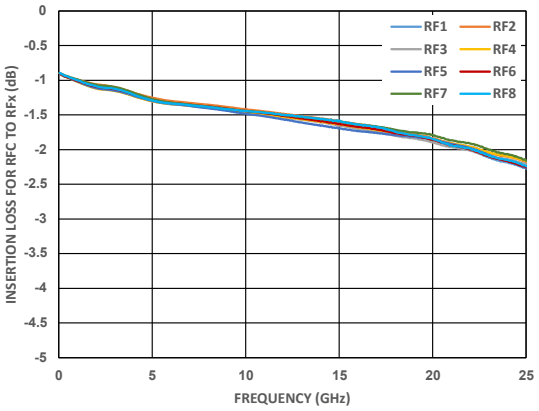

Figure 7. Insertion Loss for RFC to RFx (On) vs. Frequency

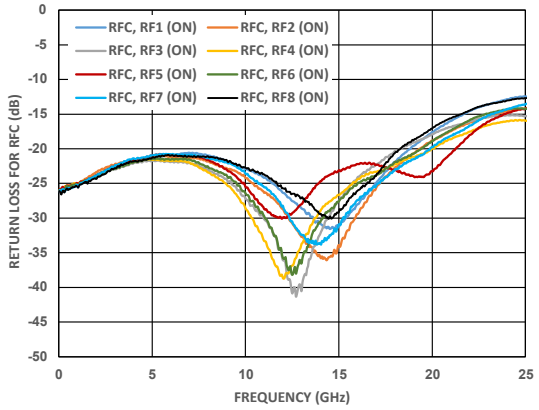

Figure 8. Return Loss for RFC (On) vs. Frequency

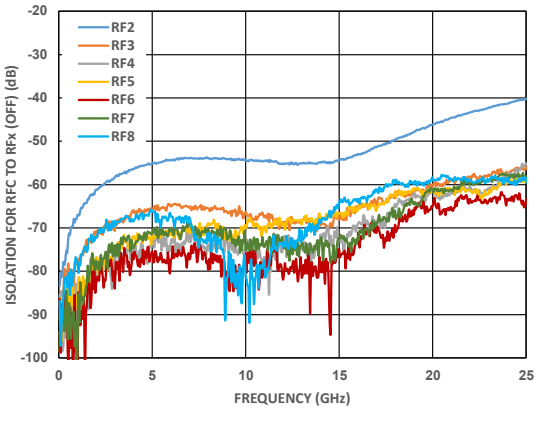

Figure 9. Isolation for RFC to RFx (Off) vs. Frequency, RFC to RF1 Path On

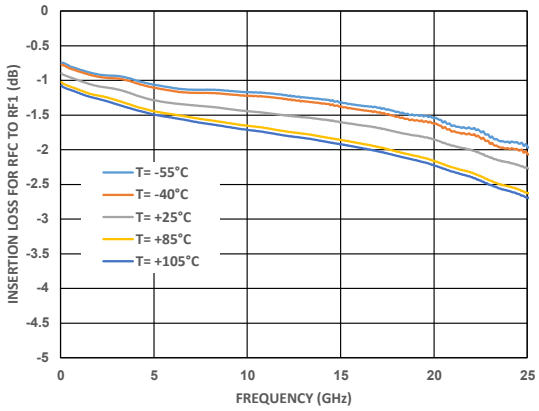

Figure 10. Insertion Loss for RFC to RF1 (On) vs. Frequency over Temperature

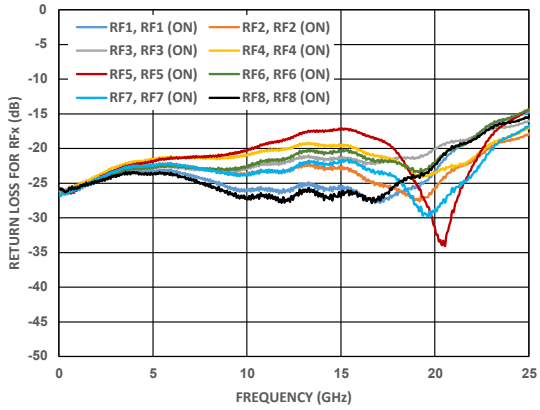

Figure 11. Return Loss for RFx (On) vs. Frequency

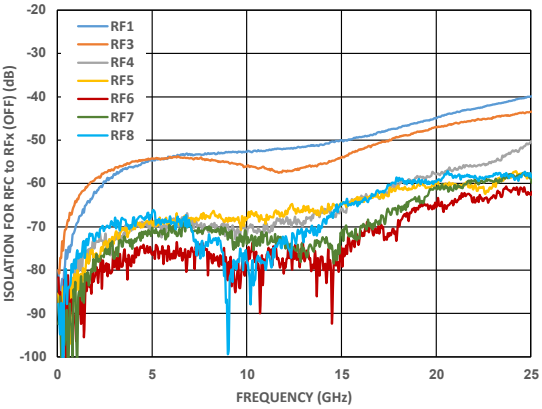

Figure 12. Isolation for RFC to RFx (Off) vs. Frequency, RFC to RF2 Path On

TYPICAL PERFORMANCE CHARACTERISTICS

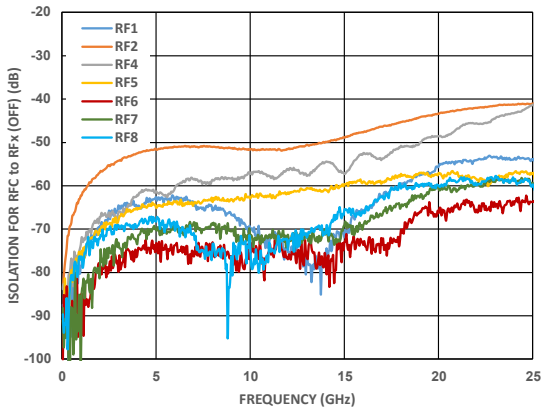

Figure 13. Isolation for RFC to RFx (Off) vs. Frequency, RFC to RF3 Path On

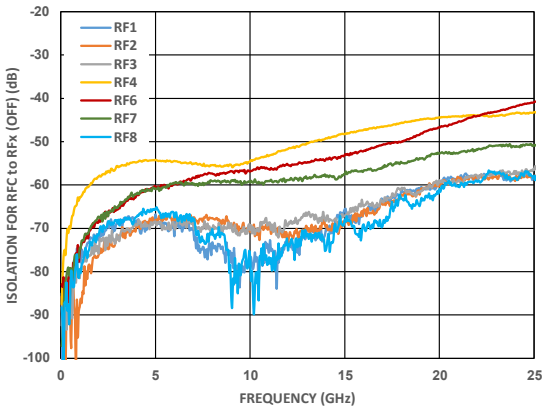

Figure 14. Isolation for RFC to RFx (Off) vs. Frequency, RFC to RF5 Path On

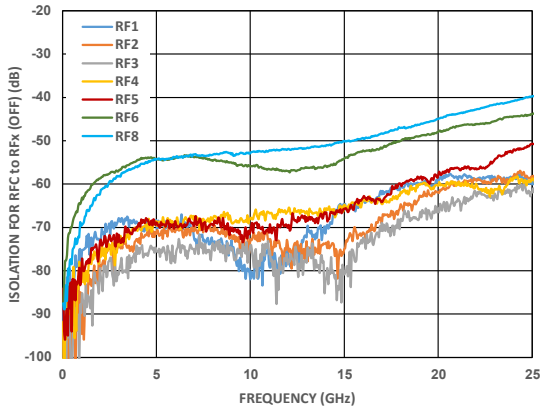

Figure 15. Isolation for RFC to RFx (Off) vs. Frequency, RFC to RF7 Path On

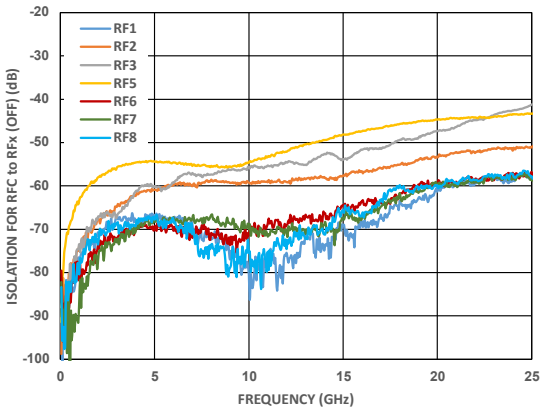

Figure 16. Isolation for RFC to RFx (Off) vs. Frequency, RFC to RF4 Path On

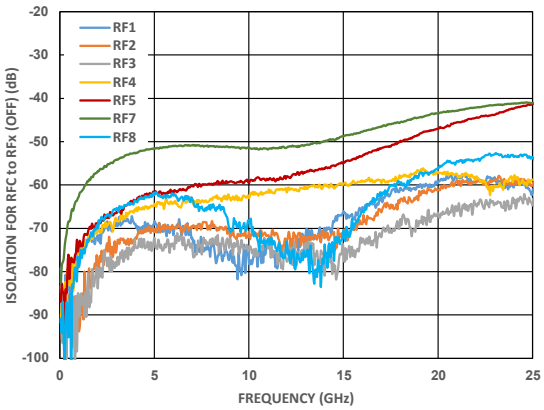

Figure 17. Isolation for RFC to RFx (Off) vs. Frequency, RFC to RF6 Path On

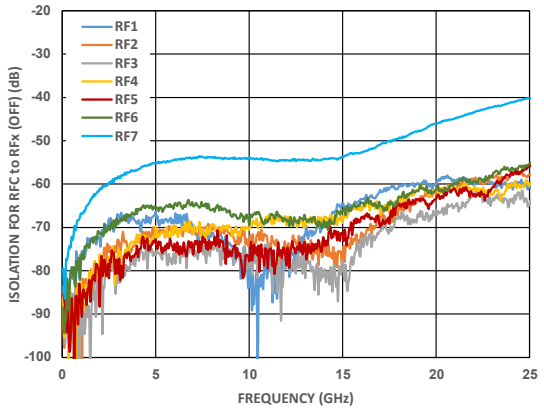

Figure 18. Isolation for RFC to RFx (Off) vs. Frequency, RFC to RF8 Path On

TYPICAL PERFORMANCE CHARACTERISTICS

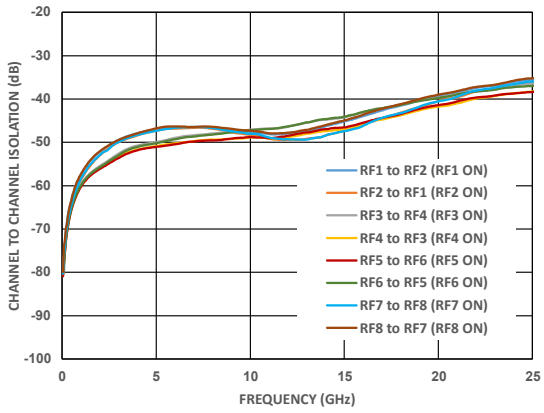

Figure 19. Channel to Channel Isolation (Worst Case) vs. Frequency, RFC to RFx Path On

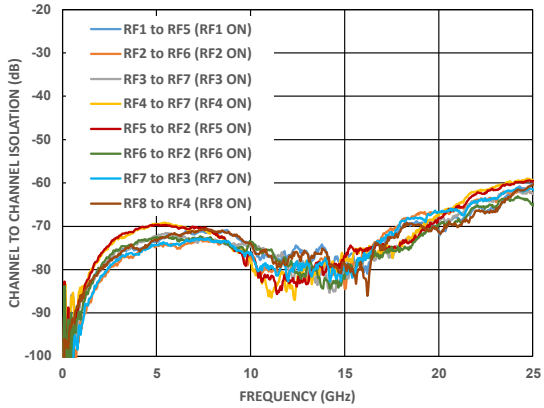

Figure 20. Channel to Channel Isolation (Best Case) vs. Frequency, RFC to RFx Path On

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

VDD = 3.3 V, VSS = −3.3 V, V_{LS}, V_{EN}, V1, V2, or V3 = 0 V or V_{DD}, and T_{CASE} = 25°C on a 50 Ω system, unless otherwise noted. Measured on the evaluation board.

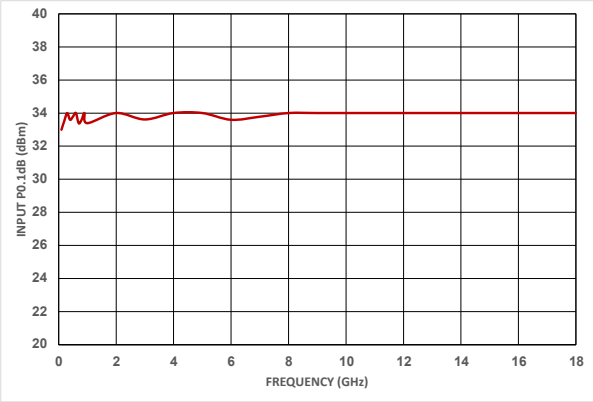

Figure 21. Input P0.1dB vs. Frequency

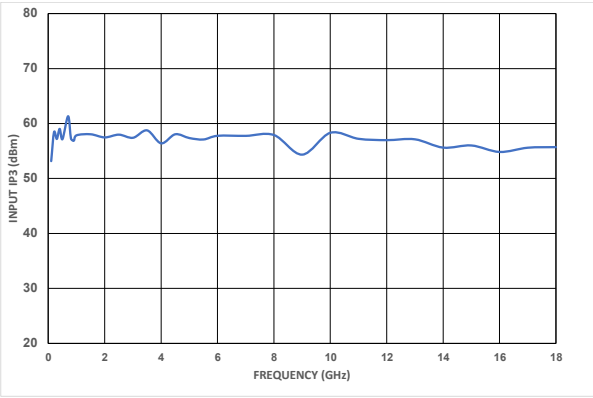

Figure 22. Input IP3 vs. Frequency

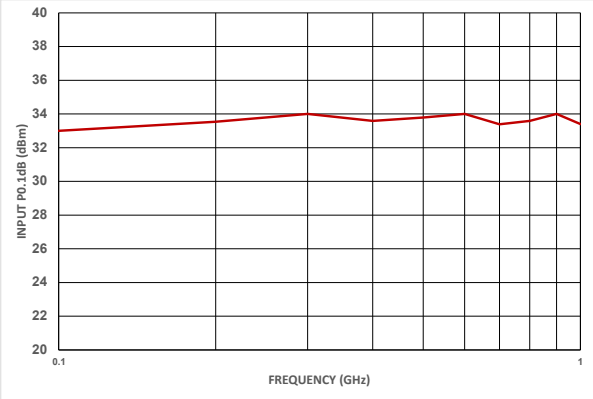

Figure 23. Input P0.1dB vs. Frequency, Low Frequency Detail

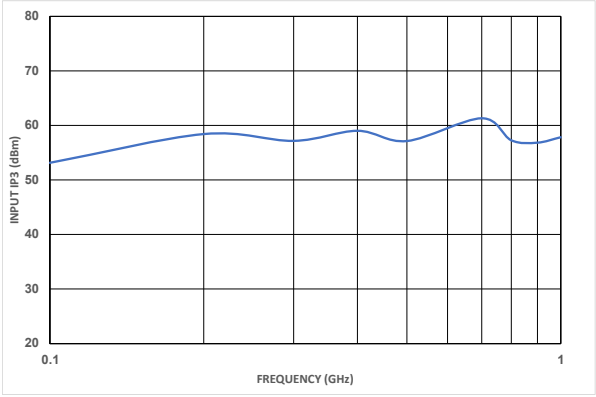

Figure 24. Input IP3 vs. Frequency, Low Frequency Detail

THEORY OF OPERATION

The ADRF5080 integrates a driver to perform logic function internally and to provide the advantage of a simplified CMOS-/LVTTL-compatible control interface. The driver features five digital control input pins (LS, EN, V1, V2, and V3) that control the state of the RFx paths (see Table 7).

When the EN pin is logic low, the logic level applied to the CMOS control input pin determines which RF port is in the insertion loss state and which RF port is in the isolation state. The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation path provides high loss between the insertion loss path and the unselected RF throw port. The unselected RF port of the ADRF5080 is reflective.

When the EN pin is logic high, the switch is in an all off state regardless of the logic state of the LS, V1, V2 and V3 pins, and all of the RFx to RFC path is in an isolation state.

The LS input allows the user to define the control input logic sequence for the RF path selections. The logic level applied to the V1, V2, and V3 pins determine which RF port is in the insertion loss state while the other three paths are in the isolation state.

RF INPUT AND OUTPUT

All of the RF ports (RFC, RF1to RF8) are DC-coupled to 0 V, and no DC blocking is required at the RF ports when the RF line potential is equal to 0 V. The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

The switch design is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port.

POWER SUPPLY

The ADRF5080 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect GND to ground.
2. Power up VDD and VSS. Powering up VSS after VDD avoids current transients on VDD during ramp up.
3. Apply a control voltage to the digital control inputs (EN, LS, V1, V2, and V3). Applying a control voltage to the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. Use a series 1 kΩ resistor to limit the current flowing into the control pin in such cases. If the control pins are not driven to a valid logic state (that is, controller output is in high impedance state) after VDD is powered up, it is recommended to use a pull-up or pull-down resistor.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

SINGLE-SUPPLY OPERATION

The ADRF5080 can operate with a single positive supply voltage applied to the VDD pin and VSS pin connected to ground. However, some performance degradations can occur in the input compression and input third-order intercept.

Table 7. Control Voltage Truth Table

Digital Control Inputs					RFx Paths							
EN	LS	V3	V2	V1	RF1 to RFC	RF2 to RFC	RF3 to RFC	RF4 to RFC	RF5 to RFC	RF6 to RFC	RF7 to RFC	RF8 to RFC
Low	Low	Low	Low	Low	On	Off	Off	Off	Off	Off	Off	Off
Low	Low	Low	Low	High	Off	On	Off	Off	Off	Off	Off	Off
Low	Low	Low	High	Low	Off	Off	On	Off	Off	Off	Off	Off
Low	Low	Low	High	High	Off	Off	Off	On	Off	Off	Off	Off
Low	Low	High	Low	Low	Off	Off	Off	Off	On	Off	Off	Off
Low	Low	High	Low	High	Off	Off	Off	Off	Off	On	Off	Off
Low	Low	High	High	Low	Off	Off	Off	Off	Off	Off	On	Off
Low	Low	High	High	High	Off	Off	Off	Off	Off	Off	Off	On
Low	High	Low	Low	Low	Off	Off	Off	Off	Off	Off	Off	On
Low	High	Low	Low	High	Off	Off	Off	Off	Off	Off	On	Off
Low	High	Low	High	Low	Off	Off	Off	Off	Off	On	Off	Off
Low	High	Low	High	High	Off	Off	Off	Off	On	Off	Off	Off
Low	High	High	Low	Low	Off	Off	Off	On	Off	Off	Off	Off
Low	High	High	Low	High	Off	Off	On	Off	Off	Off	Off	Off
Low	High	High	High	Low	Off	On	Off	Off	Off	Off	Off	Off
Low	High	High	High	High	On	Off	Off	Off	Off	Off	Off	Off
High	Low or high	Low or high	Low or high	Low or high	Off	Off	Off	Off	Off	Off	Off	Off

APPLICATIONS INFORMATION

The ADRF5080 has two power supply pins (VDD and VSS) and five digital control pins (LS, EN, V1, V2, and V3). Figure 25 shows the external components and connections for the supply and control pins. Supply and control pins are decoupled with a 10 pF or 100 pF multilayer ceramic capacitor. The device pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RFx pins when the RF lines are biased at a voltage different than 0 V. Refer to Pin Configuration and Function Descriptions section for further details.

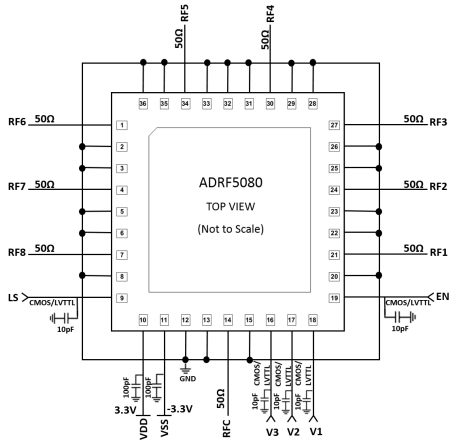

Figure 25. Recommended Schematic

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50 Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with 50 Ω characteristic impedance on the PCB. Figure 26 shows the referenced CPWG RF trace design for an RF substrate with 8 mil thick Rogers RO4003 dielectric material. The RF trace with a 14 mil width and a 7 mil clearance is recommended for 2.8 mil finished copper thickness.

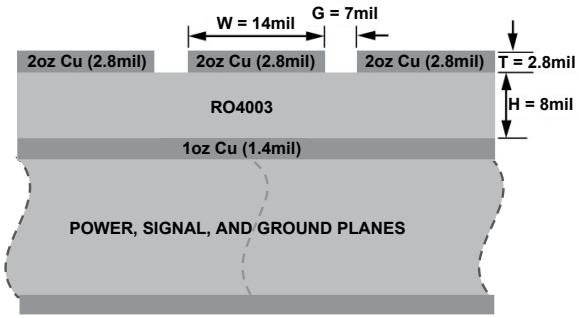

Figure 26. Example PCB Stackup

Figure 27 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with as many filled through vias as allowed for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

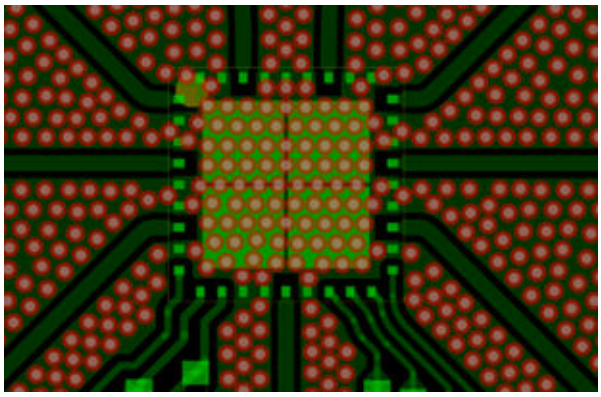

Figure 27. PCB Routings

Figure 28 shows the recommended layout from the device RFx pins to the 50 Ω CPWG on the referenced stackup. PCB pads are drawn 1:1 to device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width by 2 mils and tapered to an RF trace with 45° angle. The paste mask is also designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

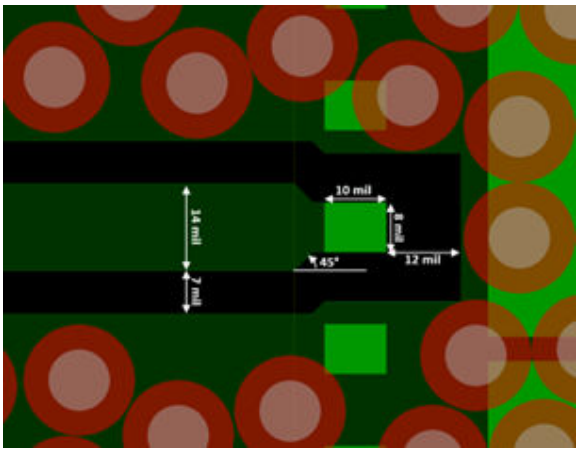

Figure 28. Recommended RFx Pin Transitions

For alternate PCB stackups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support Request for further recommendations.