Data Sheet

ADRF5141

Silicon, Transmit and Receive Switch with Limiter, 6 GHz to 12 GHz

FEATURES

- High-power transmit and receive switch with an integrated power limiter on receive path
- Frequency range: 6 GHz to 12 GHz
- Reflective 50 Ω design
- Low insertion loss
  - TX to ANT: 0.9 dB at 8 GHz to 11 GHz
  - ANT to RX: 1.4 dB at 8 GHz to 11 GHz
- High isolation: 55 dB typical for TX to RX when TX selected
- High-power handling (T_{CASE} = 50°C)
  - Input at TX: pulsed 40 dBm, >100 ns pulse width at 15% duty cycle
  - Input at ANT: pulsed 40 dBm, >100 ns pulse width at 15% duty cycle
- RX flat leakage: 17 dBm
- High linearity
  - Input P0.1dB at TX arm: 41 dBm
- Fast switching time: 50 ns
- Fast response and recovery time: <10 ns
- Dual-supply, with no low-frequency spurious
- Positive control interface: CMOS-/LVTTL-compatible
- 20-lead, 3 mm × 3 mm LGA package
- Pin compatible with the ADRF5144

APPLICATIONS

- X-band communications and radars
- Electronic warfare
- Satellite communications
- GaN and PIN diode replacement

FUNCTIONAL BLOCK DIAGRAM

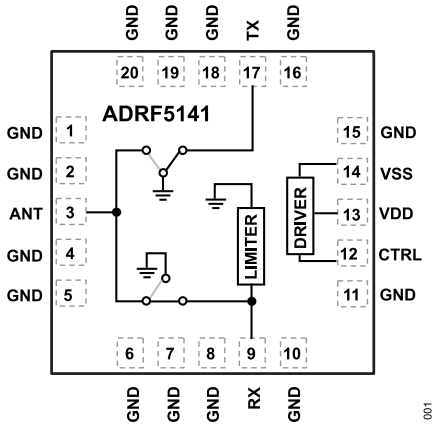

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5141 is a reflective, SPDT switch manufactured in the silicon process. The ADRF5141 is used in transmit and receive applications with an integrated power limiter on the receive path.

The ADRF5141 operates from 6 GHz to 12 GHz. The RX arm with the integrated power limiter has a flat leakage of 17 dBm with a low insertion loss of 1.4 dB at 8 GHz to 11 GHz. The TX arm has an insertion loss of 0.9 dB at 8 GHz to 11 GHz.

The ADRF5141 draws a low current of 13 µA on the positive supply of +3.3 V and 360 µA on the negative supply of −3.3 V. The device employs complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls. The ADRF5141 requires no additional driver circuitry, making it an ideal alternative to gallium nitride (GaN) and PIN diode-based switches.

The ADRF5141 comes in a 20-lead, 3.0 mm × 3.0 mm, RoHS-compliant, land grid array (LGA) package and can operate from −40°C to +105°C.

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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TABLE OF CONTENTS

Features 1
Applications 1
Functional Block Diagram 1
General Description 1
Specifications 3
Absolute Maximum Ratings 5
Thermal Resistance 5
Power Derating Curve 5
Electrostatic Discharge (ESD) Ratings 5
ESD Caution 5
Pin Configuration and Function Descriptions 6
Interface Schematics 6
Typical Performance Characteristics 7
Insertion Loss, Isolation, and Return Loss 7
Input Power Compression, P_{OUT} vs. P_{IN}, and Input IP3 8
Theory of Operation 10
Power Supply 10
RF Input and Output 10
Applications Information 11
Recommendations for PCB Design 11
Outline Dimensions 13
Ordering Guide 13
Evaluation Boards 13

REVISION HISTORY

10/2022—Revision 0: Initial Version

SPECIFICATIONS

Positive supply voltage (V_{DD}) = 3.3 V, negative supply voltage (V_{SS}) = −3.3 V, CTRL voltage (V_{CTRL}) = 0 V or 3.3 V, and T_{CASE} = 25°C, with a 50 Ω system, unless otherwise noted.

Table 1. Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		6		12	GHz
INSERTION LOSS		8 GHz to 11 GHz				
TX to ANT				0.9		dB
ANT to RX				1.4		dB
		6 GHz to 12 GHz				
TX to ANT				1.1		dB
ANT to RX				1.7		dB
RETURN LOSS		8 GHz to 11 GHz				
ANT				13		dB
TX (On)				16		dB
RX (On)				18		dB
		6 GHz to 12 GHz				
ANT				11		dB
TX (On)				13		dB
RX (On)				12		dB
ISOLATION		8 GHz to 11 GHz				
TX to ANT		RX selected		28		dB
ANT to RX		TX selected		58		dB
TX to RX		TX selected		55		dB
		6 GHz to 12 GHz				
TX to ANT		RX selected		26		dB
ANT to RX		TX selected		55		dB
TX to RX		TX selected		55		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		15		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		50		ns
RF Settling Time						
0.1 dB		50% V_{CTRL} to 0.1 dB of final RF output		65		ns
LIMITER		Pulsed 40 dBm, 5% duty cycle, >100 ns pulse width				
Response Time				<10		ns
Recovery Time				<10		ns
RX Flat Leakage				17		dBm
INPUT LINEARITY		8 GHz to 11 GHz				
TX Arm						
0.1dB Compression	P0.1dB			41		dBm
1dB Compression	P1dB			43		dBm
Third-Order Intercept	IP3	2-tone input power = 20 dBm each tone, Δf = 1 MHz		58		dBm
RX Arm						
0.1dB Compression	P0.1dB			14		dBm
1dB Compression	P1dB			17		dBm
Third-Order Intercept	IP3	2-tone input power = 2 dBm each tone, Δf = 1 MHz		43		dBm
DIGITAL CONTROL INPUTS		CTRL pin				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						

SPECIFICATIONS

Table 1. Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Low and High	I_{INL}, I_{INH}			<1		µA
SUPPLY CURRENT		VDD and VSS pins				
Positive Supply Current	I_{DD}			13		µA
Negative Supply Current	I_{SS}			360		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Voltage	V_{CTRL}		0		V_{DD}	V
RF Power	P_{IN}					
Input at TX[1]		f = 8 GHz to 11 GHz, T_{CASE} = 85°C[2]				
Continuous Wave					36	dBm
Pulsed[3]		5% duty cycle, >100 ns pulse width, T_{CASE} = 85°C			40	dBm
		15% duty cycle, >100 ns pulse width, T_{CASE} = 50°C			40	dBm
Peak		5% duty cycle, ≤100 ns peak duration			43	dBm
Input at ANT		f = 6 GHz to 12 GHz, T_{CASE} = 85°C[2]				
Continuous Wave					33	dBm
Pulsed[3]		5% duty cycle, >100 ns pulse width, T_{CASE} = 85°C			40	dBm
		15% duty cycle, >100 ns pulse width, T_{CASE} = 50°C			40	dBm
Peak		5% duty cycle, ≤100 ns peak duration			40	dBm
Case Temperature	T_{CASE}		−40		+105	°C

1 For power derating vs. frequency for input at TX, see Figure 2.

2 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specifications by 3 dB.

3 For different pulsed conditions, please contact applications support.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	−0.3 V to +3.6 V
V_{SS}	−3.6 V to +0.3 V
Digital Control Input	
Voltage	−0.3 V to V_{DD} + 0.3 V
Current	3 mA
RF Power	
Input at TX[1] (f = 8 GHz to 11 GHz, T_{CASE} = 85°C[2])	
Continuous Wave	36.5 dBm
Pulsed (5% duty cycle, >100 ns pulse width, T_{CASE} = 85°C)	40.5 dBm
Pulsed (15% duty cycle, >100 ns pulse width, T_{CASE} = 50°C)	40.5 dBm
Peak	43.5 dBm
Input at ANT (f = 6 GHz to 12 GHz, T_{CASE} = 85°C[2])	
Continuous Wave	33.5 dBm
Pulsed (5% duty cycle, >100 ns pulse width, T_{CASE} = 85°C)	40.5 dBm
Pulsed (15% duty cycle, >100 ns pulse width, T_{CASE} = 50°C)	40.5 dBm
Peak	40.5 dBm
RF Power Under Unbiased Condition (V_{DD} and V_{SS} = 0 V)	
Input at ANT	33 dBm
Temperature	
Junction, T_J	135°C
Storage	−65°C to +150°C
Reflow	260°C

[1] For power derating vs. frequency for the input at TX, see Figure 2.

[2] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specifications by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-20-9		

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
TX Path	45	°C/W
RX Path	28.6	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVE

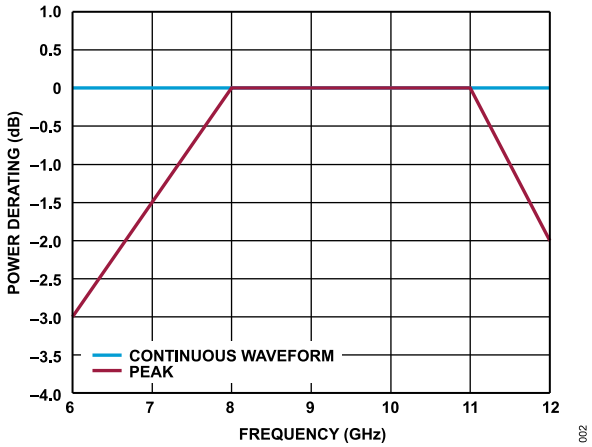

Figure 2. Power Derating vs. Frequency for Input at TX, T_{CASE} = 85°C

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5141

Table 4. ADRF5141, 20-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	±2000 for All Pins	2
CDM	±1250 for All Pins	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

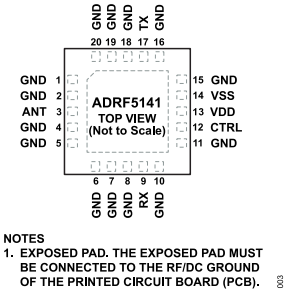

Figure 3. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 8, 10, 11, 15, 16, 18 to 20	GND	Ground. The GND pins must be connected to the RF and DC ground of the PCB.
3	ANT	Antenna Port. Th ANT pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
9	RX	Receive Port. Th RX pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
12	CTRL	Control Input. See Figure 5 for the interface schematic.
13	VDD	Positive Supply Voltage Pin. See Figure 6 for the interface schematic.
14	VSS	Negative Supply Voltage Pin. See Figure 7 for the interface schematic.
17	TX	Transmit Port. The TX pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and DC ground of the PCB.

INTERFACE SCHEMATICS

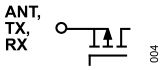

Figure 4. ANT, TX, and RX Pins Interface Schematic

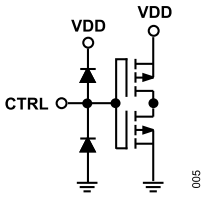

Figure 5. CTRL Interface Schematic

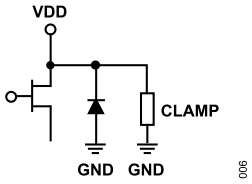

Figure 6. VDD Pin Interface Schematic

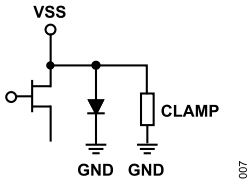

Figure 7. VSS Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, ISOLATION, AND RETURN LOSS

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V_{CTRL} = 0 V or V_{DD}, and T_{CASE} = 25°C, with a 50 Ω system, unless otherwise noted. Measured on the ADRF5141-EVALZ.

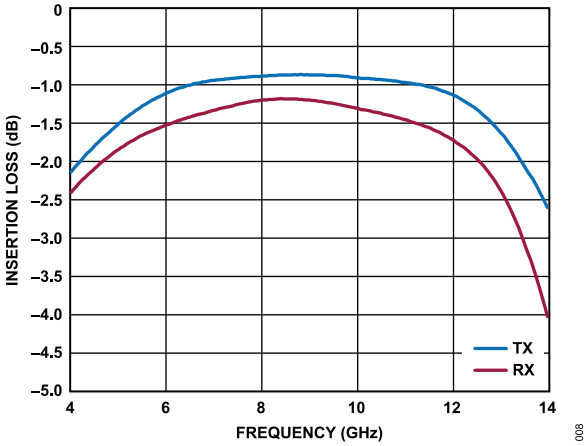

Figure 8. Insertion Loss vs. Frequency at Room Temperature for TX and RX

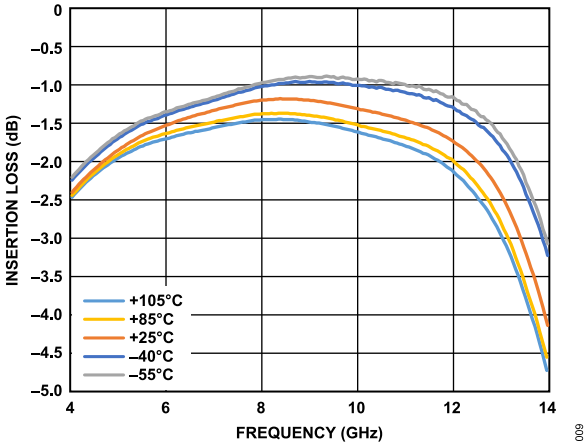

Figure 9. Insertion Loss vs. Frequency over Temperature for RX

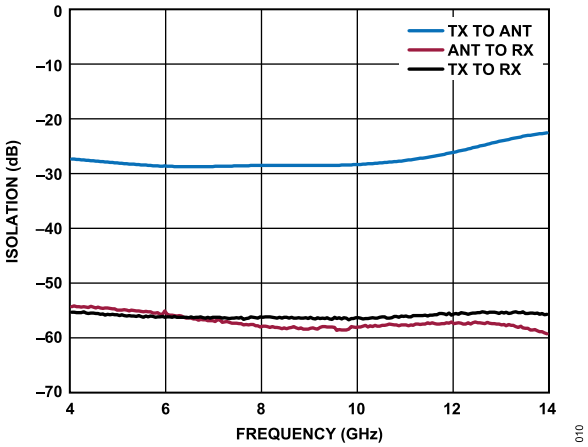

Figure 10. Isolation vs. Frequency

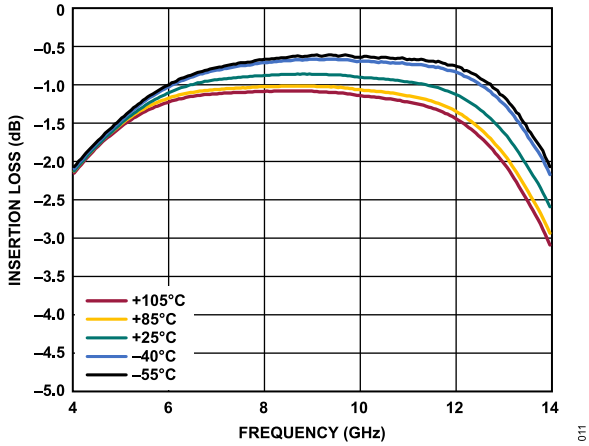

Figure 11. Insertion Loss vs. Frequency over Temperature for TX

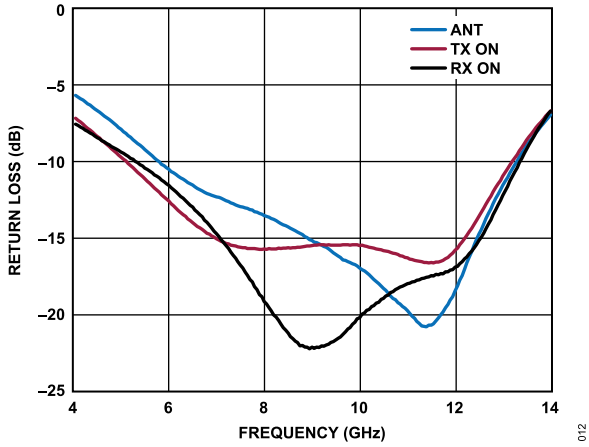

Figure 12. Return Loss vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION, P_{OUT} VS. P_{IN}, AND INPUT IP3

V_{DD} = 3.3 V, V_{SS} = -3.3 V, V_{CTRL} = 0 V or V_{DD} V, and T_{CASE} = 25°C in a 50 Ω system, unless otherwise noted. All of the large-signal performance parameters are measured on the ADRF5141-EVALZ.

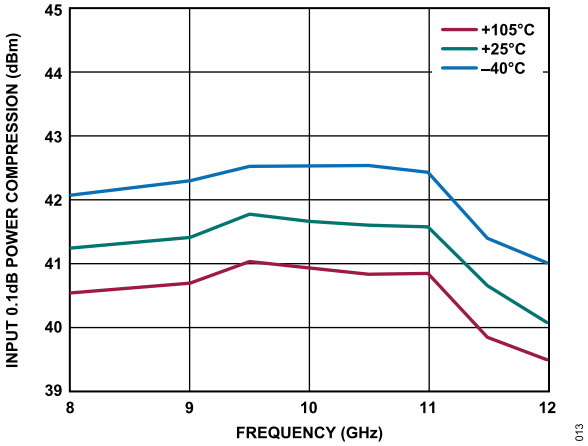

Figure 13. Input 0.1dB Power Compression vs. Frequency over Temperature for TX

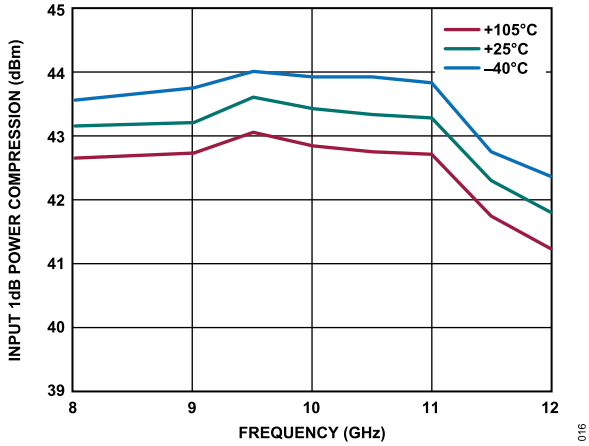

Figure 15. Input 1dB Power Compression vs. Frequency over Temperature for TX

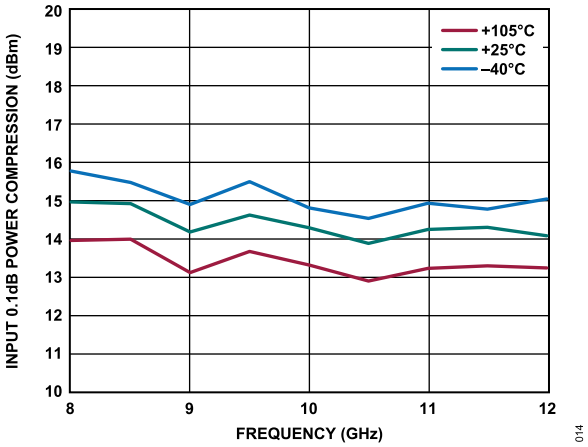

Figure 14. Input 0.1dB Power Compression vs. Frequency over Temperature for RX

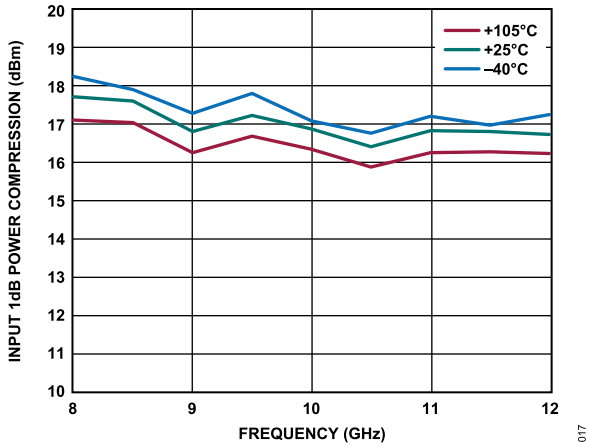

Figure 16. Input 1dB Power Compression vs. Frequency over Temperature for RX

TYPICAL PERFORMANCE CHARACTERISTICS

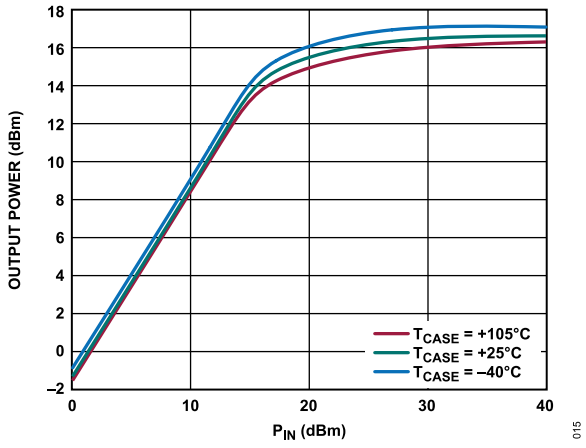

Figure 17. Output Power (P_{OUT}) vs. P_{IN} over Temperature at 10 GHz for RX

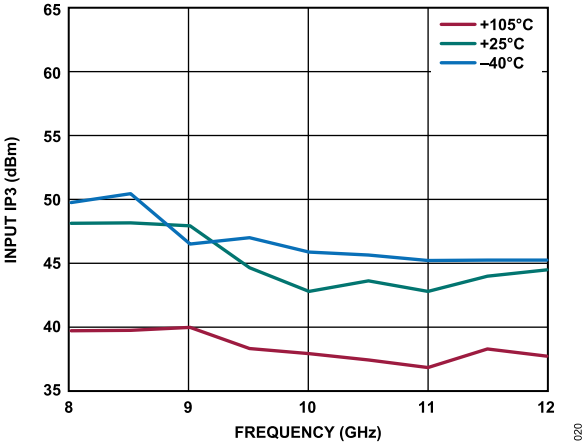

Figure 20. Input IP3 vs. Frequency for RX

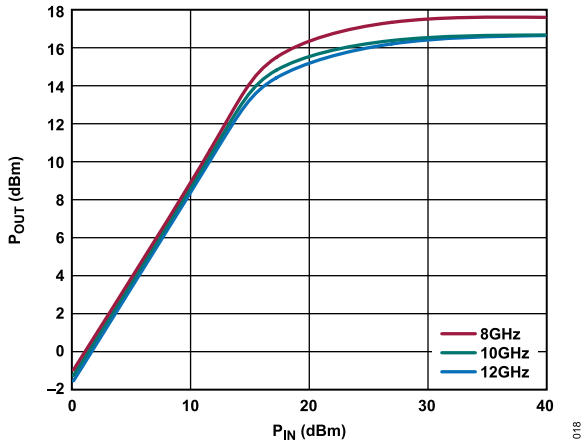

Figure 18. P_{OUT} vs. P_{IN} over Frequency at Room Temperature for RX

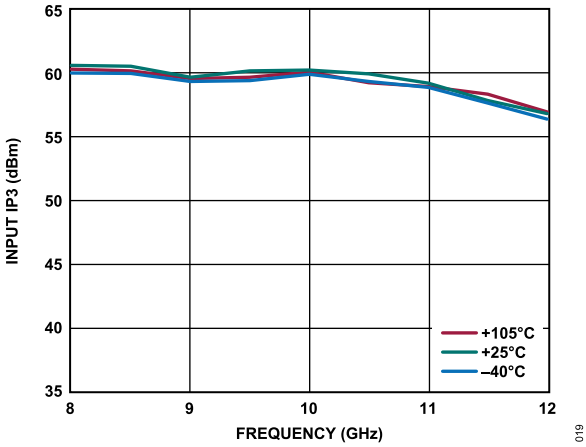

Figure 19. Input IP3 vs. Frequency for TX

THEORY OF OPERATION

The ADRF5141 integrates a driver to perform logic function internally and to provide the advantage of a simplified control interface. The driver features a single-control input pin (CTRL) that controls the state of the RF paths, determining which RF port is in an insertion loss state and which RF port is in an isolation state (see Table 6).

POWER SUPPLY

The ADRF5141 requires a positive supply voltage applied to the V_{DD} pin and a negative supply voltage applied to the V_{SS} pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect to ground.
2. Power up V_{DD} and V_{SS}. Power up V_{SS} after V_{DD} to avoid current transients on V_{DD} during ramp-up.
3. Power up the digital control input (CTRL). Power up CTRL before the V_{DD} supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the CTRL pin. Use pull-up or pull-down resistors if the controller output is in a high-impedance state after V_{DD} is powered up and the CTRL pin is not driven to a valid logic state
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

RF INPUT AND OUTPUT

All RF ports (ANT, RX, and TX) are DC-coupled to 0 V. When the RF line DC potential is at 0 V, no DC blocking is required at the RF ports.

The RF ports are internally matched to 50 Ω; therefore, no external matching networks are required.

Table 6. Control Voltage Truth Table

Digital Control Input	RF Paths	
CTRL	TX to ANT	ANT to RX
Low	Insertion loss (on)	Isolation (off)
High	Isolation (off)	Insertion loss (on)

APPLICATIONS INFORMATION

The ADRF5141 has two power-supply pins (V_{DD} and V_{SS}) and one control pin (CTRL). Figure 21 shows the external components and connections for the supply and control pins. The V_{DD} pin is decoupled with 100 pF and 1000 pF multilayer ceramic capacitor, while the V_{SS} pin and the control pin are decoupled with 100 pF multilayer ceramic capacitor. The device pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC-blocking capacitors on the ANT, TX, and RX pins when the RF lines are biased at a voltage different than 0 V. Refer to the Pin Configuration and Function Descriptions section for details.

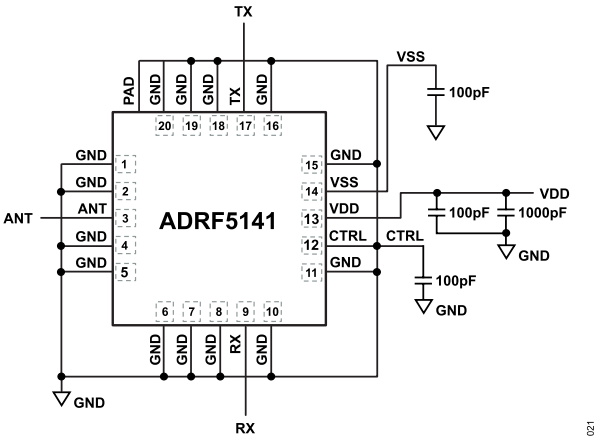

Figure 21. Recommended Schematic

The power limiter at the RX arm engages and limits the input power from the ANT power. See the Table 1 section for the RX flat Leakage power level. A typical application of the ADRF5141 is to connect an antenna at the ANT pin, a power amplifier (PA) at the TX pin, and a low-noise amplifier (LNA) at the RX pin. The integrated power limiter at the RX arm provides protection to the LNA input connected to the RX pin (see Figure 22).

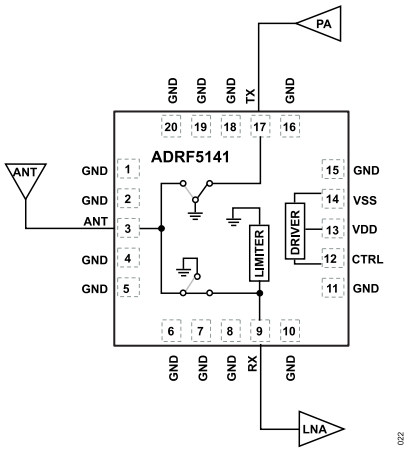

Figure 22. Typical Application Diagram

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50 Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with 50 Ω characteristic impedance on the PCB. Figure 23 shows the referenced CPWG RF trace design for an RF substrate with 8 mil thick Rogers RO4003 dielectric material. RF trace with 14 mil width and 7 mil clearance is recommended for 1.5 mil finished copper thickness.

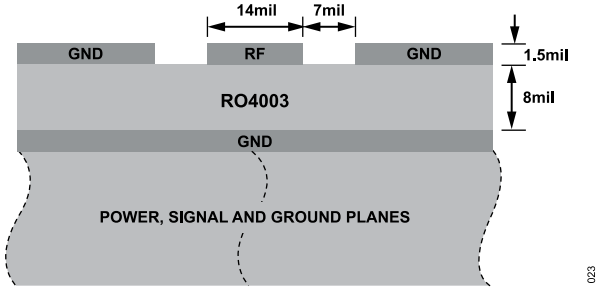

Figure 23. Example PCB Stack-Up

Figure 24 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with as many filled, through vias as allowed for optimal RF and thermal performance. The primary thermal path for the device is the bottom side; therefore, a heatsink is required underneath the PCB to ensure maximum heat dissipation and to reduce thermal rise on the PCB during high-power applications.

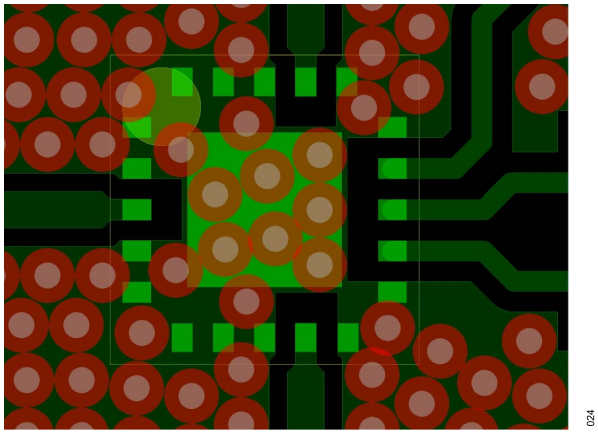

Figure 24. PCB Routings

Figure 25 shows the recommended layout from the device RF pins to the 50 Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to device pads. The ground pads are drawn soldermask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width till the package edge and tapered to the RF trace with a 45° angle. The paste mask is also designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

APPLICATIONS INFORMATION

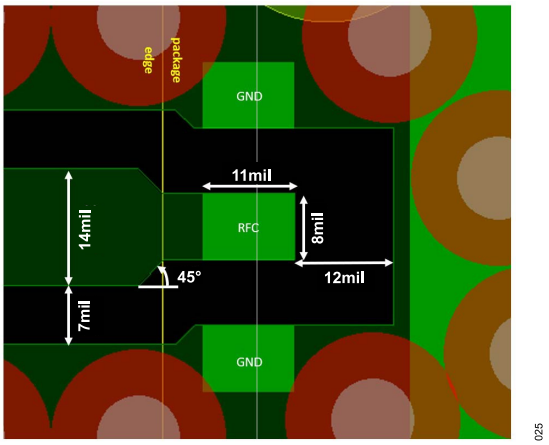

Figure 25. Recommended RF Pin Transitions

For alternate PCB stack-ups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support Request for further recommendations.