Silicon, SPDT Switch, Reflective, 24 GHz to 32 GHz

Data Sheet

ADRF5300

FEATURES

- Reflective design
- Low insertion loss: 1.1 dB
- High isolation: 38 dB
- High input linearity
  - P0.1dB: 37 dBm
  - IP3: 65 dBm
- High RF input power handling
  - 28 dBm average
  - 36 dBm peak
- 3.3 V single-supply operation
  - Internal negative voltage generator
- RF settling time (0.1 dB final RF output): 70 ns
- 20-terminal, 3 mm × 3 mm, RoHS-compliant, land grid array package

APPLICATIONS

- Industrial scanner
- Test instrumentation
- Cellular infrastructure: 5G millimeter wave
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

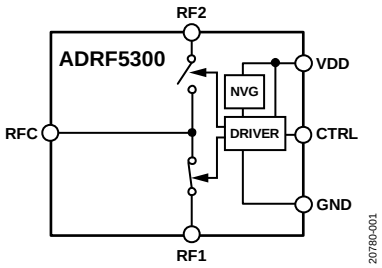

Figure 1.

GENERAL DESCRIPTION

The ADRF5300 is a reflective, SPDT switch manufactured in the silicon process.

The ADRF5300 is developed for 5G applications ranging from 24 GHz to 32 GHz. The ADRF5300 has a low insertion loss of 1.1 dB, a high isolation of 38 dB, and an RF input power handling capability of 28 dBm average and 36 dBm peak.

The ADRF5300 incorporates a negative voltage generator (NVG) to operate with a single positive supply of 3.3 V (V_{DD}) applied to the VDD pin. The device employs CMOS- and low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5300 is packaged in a 20-terminal, 3 mm × 3 mm, RoHS-compliant, land grid array (LGA) package and can operate from −40°C to +105°C.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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REVISION HISTORY

9/2020—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.3 V, control voltage (V_{CTRL}) = 0 V or V_{DD}, T_{CASE} = 25°C, and a 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		24		32	GHz
INSERTION LOSS					
Between RFC and RF1 or RFC and RF2			1.1		dB
ISOLATION					
Between RFC and RF1 or RFC and RF2			38		dB
Between RF1 and RF2			38		dB
RETURN LOSS					
RFC, RF1 (On) and RF2 (On)			22		dB
SWITCHING CHARACTERISTICS					
Rise Time (t_{RISE}) and Fall Time (t_{FALL})	10% to 90% of RF output		25		ns
On Time (t_{ON}) and Off Time (t_{OFF})	50% V_{CTRL} to 90% of RF output		60		ns
RF Settling Time					
0.1 dB	50% V_{CTRL} to 0.1 dB of final RF output		70		ns
0.05 dB	50% V_{CTRL} to 0.05 dB of final RF output		80		ns
INPUT LINEARITY	f = 24 GHz to 32 GHz				
0.1 dB Power Compression (P0.1dB)			37		dBm
Input Third-Order Intercept (IP3)[1]	Two-tone input power = 20 dBm per tone, Δf = 1 MHz		65		dBm
SUPPLY CURRENT	VDD pin				
Positive Supply Current (I_{DD})			450		µA
DIGITAL CONTROL INPUTS	CTRL pin				
Input Voltage					
Low (V_{INL})		0		0.8	V
High (V_{INH})		1.2		3.3	V
Input Current					
Low (I_{INL})			<1		µA
High (I_{INH})			~11		µA
RECOMMENDED OPERATING CONDITIONS					
V_{DD}		3.15		3.45	V
Digital V_{CTRL}		0		V_{DD}	V
RF Input (RF_{IN}) Power[2]	f = 24 GHz to 32 GHz, T_{CASE} = 85°C, input at RFC, RF1, or RF2				
Steady State Average				28	dBm
Steady State Peak				36	dBm
Hot Switching Average				28	dBm
Hot Switching Peak				36	dBm
T_{CASE}		−40		+105	°C

[1] Performance is limited by the test setup.
[2] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

TIMING SPECIFICATIONS

See Figure 14 for the timing diagram.

Table 2.

Parameter	Description	Min	Typ	Max	Unit
$t_{POWERUP}$[1]	Minimum wait time after power-up	50			µs
t_{HOLD}	Minimum control switching time	40			µs
t_{SLEW}	Maximum control rise and fall time			10	µs

[1] A maximum of 10 dBm RF input power can be applied during the $t_{POWERUP}$ wait time.

ABSOLUTE MAXIMUM RATINGS

For the recommended operating conditions, see Table 1.

Table 3.

Parameter	Rating
Positive Supply Voltage	−0.3 V to +3.6 V
Digital Control Inputs	
Voltage	−0.3 V to V_{DD} + 0.3 V
Current	3 mA
RF Input Power (V_{DD} = 3.3 V, f = 24 GHz to 32 GHz at T_{CASE} = 85 °C)	
Average	28.5 dBm
Peak	36.5 dBm
RF Input Power Under Unbiased Condition (V_{DD} = 0 V)	
Average	28 dBm
Peak	36 dBm
Temperature	
Junction	135°C
Storage	−65°C to +150°C
Reflow	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is linked directly to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
CC-20-9	385	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5300

Table 5. ADRF5300, 20-Terminal LGA

ESD Model	Withstand Threshold (V)
HBM	
All Pins	±1000
Supply and Control Pins	±4000
FICDM	±1250

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

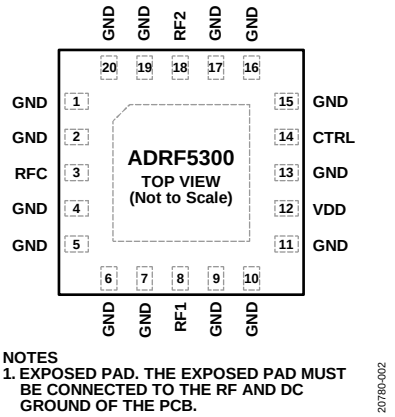

Figure 2. Pin Configuration (Top View)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 7, 9 to 11, 13, 15 to 17, 19, 20	GND	Ground. The GND pins must be connected to the RF and dc ground of the PCB.
3	RFC	RF Common Port. The RFC pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 3 for the interface schematic.
8	RF1	RF Throw Port 1. The RF1 pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 3 for the interface schematic.
12	VDD	Positive Supply Voltage Input. See Figure 5 for the interface schematic.
14	CTRL	Control Voltage Input. See Figure 4 for the interface schematic.
18	RF2	RF Throw Port 2. The RF2 pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 3 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and dc ground of the PCB.

INTERFACE SCHEMATICS

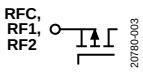

Figure 3. RFC, RF1, and RF2 Pins Interface Schematic

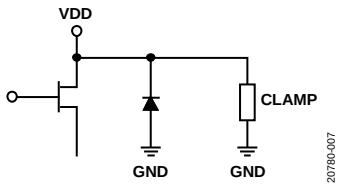

Figure 5. VDD Pin Interface Schematic

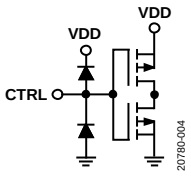

Figure 4. CTRL Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{CTRL} = 0 V or V_{DD}, T_{CASE} = 25°C, and a 50 Ω system, unless otherwise noted. Measured on the probe matrix board using ground signal ground (GSG) probes close to the RFC, RF1, and RF2 pins.

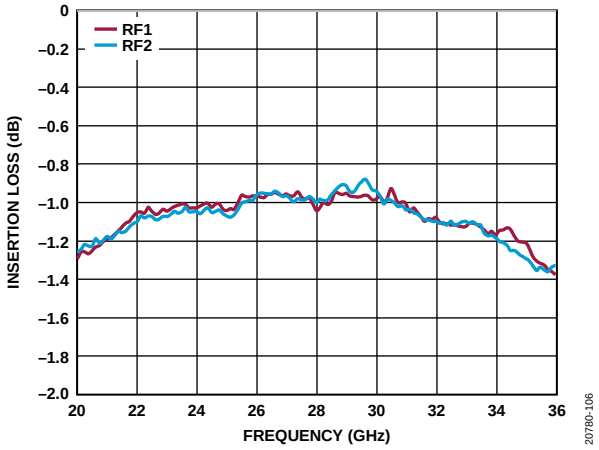

Figure 6. Insertion Loss vs. Frequency

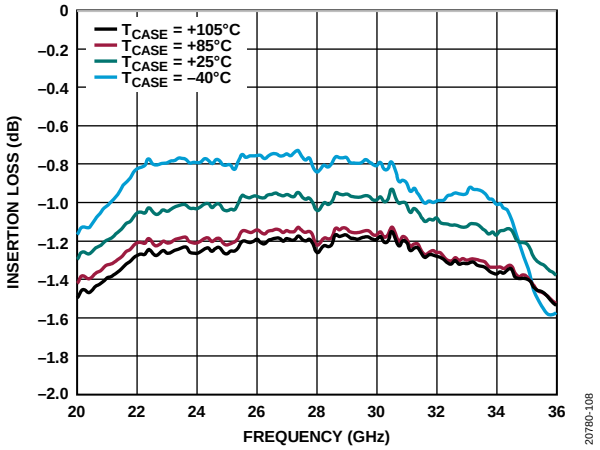

Figure 8. Insertion Loss vs. Frequency, RF1 Selected

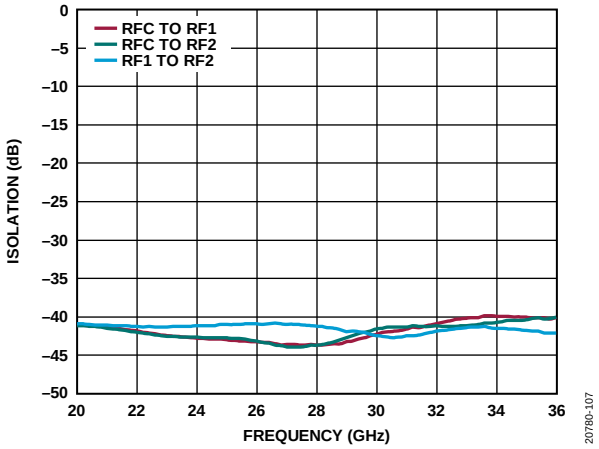

Figure 7. Isolation vs. Frequency

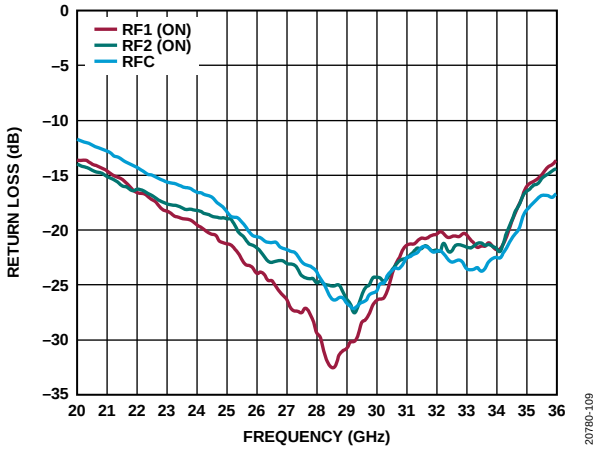

Figure 9. Return Loss vs. Frequency

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = 3.3 V, V_{CTRL} = 0 V or V_{DD}, T_{CASE} = 25°C, and a 50 Ω system, unless otherwise noted. All of the large signal performance parameters are measured on the ADRF5300-EVALZ.

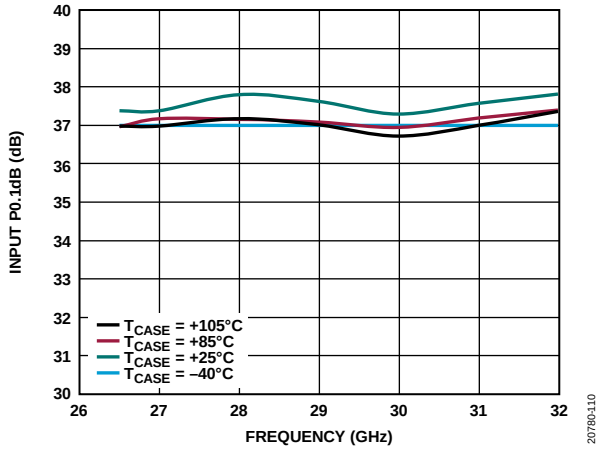

Figure 10. Input P0.1dB vs. Frequency, RF1 Selected

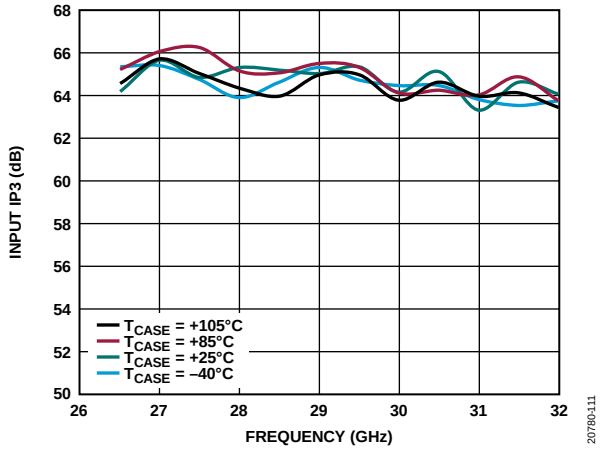

Figure 11. Input IP3 vs. Frequency, RF1 Selected

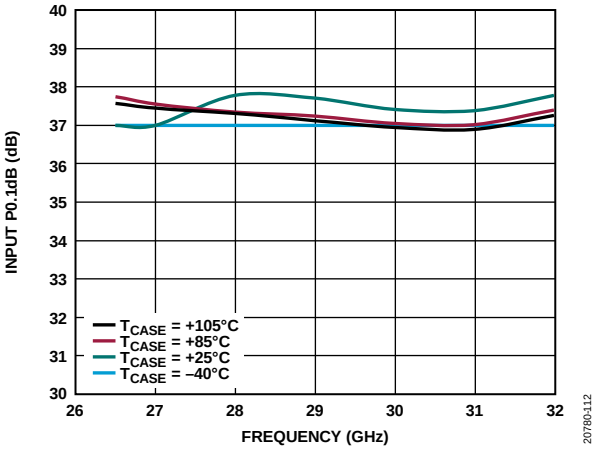

Figure 12. Input P0.1dB vs. Frequency, RF2 Selected

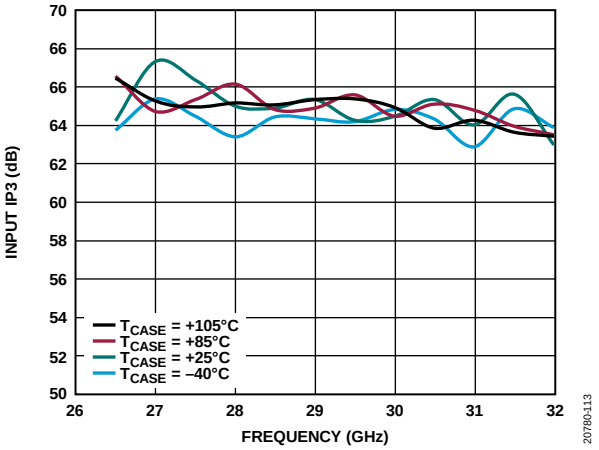

Figure 13. Input IP3 vs. Frequency, RF2 Selected

THEORY OF OPERATION

The ADRF5300 incorporates a driver to perform logic functions internally and to provide the user with the advantage of a simplified positive voltage control interface. The driver features a single digital control input pin (CTRL) that controls the state of the RF paths. The logic level applied to the CTRL pin determines which RF port is in the insertion loss state and which port is in the isolation state (see Table 7).

RF INPUT AND OUTPUT

All of the RF ports (RFC, RF1, and RF2) are dc-coupled to 0 V. When the RF line potential is equal to 0 V, no dc blocking capacitor is required at the RF ports.

The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

The ADRF5300 is bidirectional with equal power handling capabilities. An RF input signal (RF_{IN}) can be applied to the RFC port, RF1 port, or RF2 port.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation path provides high loss between the insertion loss path and the unselected, reflective RF throw port.

POWER SUPPLY

The ADRF5300 operates on a positive single supply and includes an NVG with ultralow spurious performance. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The power-up sequence is as follows:

1. Connect GND to ground.
2. Power up the supply input, VDD.
3. Apply the digital control input, CTRL. Applying CTRL before applying the VDD supply inadvertently forward biases and damages the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the CTRL pin. Pull the CTRL pin to VDD or GND using a resistor if the controller output is in a high impedance state after VDD is powered up and the CTRL pin is not driven to a valid logic state.
4. Apply the RF input signal.

The power-down sequence is the reverse order of the power-up sequence.

TIMING REQUIREMENTS

There are timing requirements for the proper operation of the bias and control circuits. See Table 2 for the timing specifications. See Figure 14 for the timing requirements.

After VDD reaches the operating range, $t_{POWERUP}$ defines the wait time before the recommended maximum RF power can be applied. During this time, a maximum of 10 dBm RF input power can be applied.

The minimum wait time before switching states is defined by t_{HOLD}.

The maximum rise and fall time of the CTRL pulse is defined by t_{SLEW}.

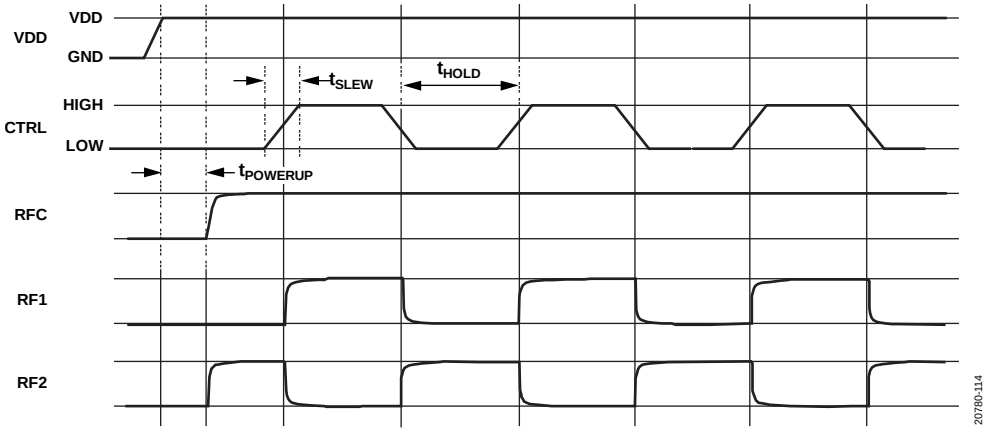

Figure 14. Timing Requirements

Table 7. Control Voltage Truth Table

Digital Control Input	RF Paths	
CTRL	**RF1 to RFC**	**RF2 to RFC**
High	Insertion loss (on)	Isolation (off)
Low	Isolation (off)	Insertion loss (on)

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS

The design of the ADRF5300-EVALZ serves as a layout recommendation for the ADRF5300 application.

The ADRF5300-EVALZ is a 4-layer evaluation board. The outer copper (Cu) layers are 0.5 oz (0.7 mil) plated to 1.5 oz (2.2 mil) separated by dielectric materials. Figure 15 shows the ADRF5300-EVALZ stack up.

For additional information on application circuit design, see the ADRF5300-EVALZ user guide.

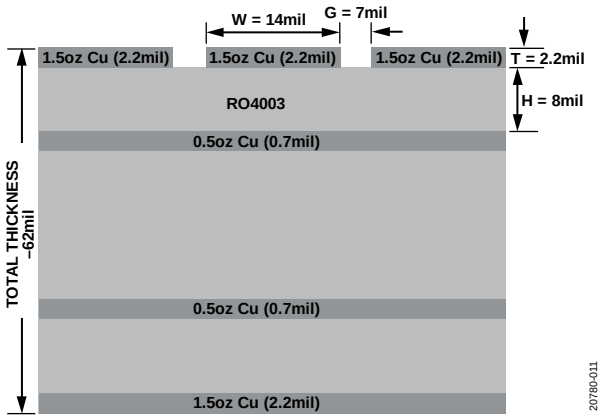

Figure 15. ADRF5300-EVALZ Stack Up

All RF and dc traces are routed on the top copper layer, whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The top dielectric material is 8 mil Rogers RO4003, offering optimal high frequency performance. The middle and bottom dielectric materials provide mechanical strength. The total board thickness is 62 mil, which allows 2.4 mm RF launchers to connect at the board edges.

RF AND DIGITAL CONTROLS

The RF transmission lines are designed using a coplanar waveguide (CPWG) model, with a trace width of 14 mil and a ground clearance of 7 mil to have a characteristic impedance of 50 Ω. For optimal RF and thermal grounding, as many plated through vias as possible are arranged around transmission lines and under the exposed pad of the package.

The RF ports (RFC, RF1, and RF2) connect through 50 Ω transmission lines to the 2.4 mm RF launchers. On the VDD pin, a 100 pF bypass capacitor filters high frequency noise.

Figure 16 shows the simplified application circuit for the ADRF5300-EVALZ.

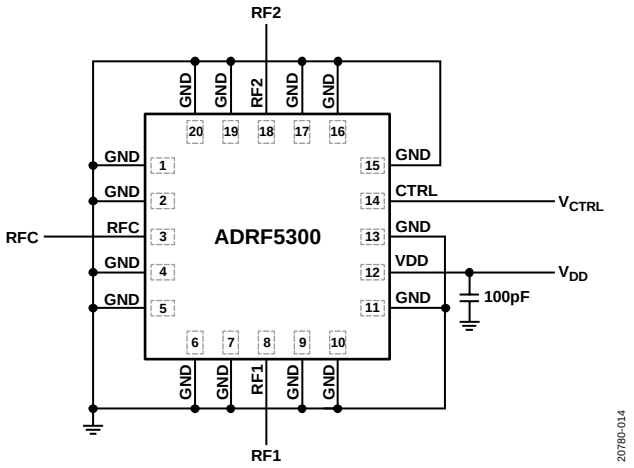

Figure 16. ADRF5300-EVALZ Simplified Application Circuit

PROBE MATRIX BOARD

The probe matrix board is a 4-layer evaluation board. This board also uses an 8 mil Rogers RO4003 dielectric. The outer copper (Cu) layers are 0.5 oz (0.7 mil) plated to 1.5 oz (2.2 mil). The RF transmission lines were designed using a CPWG model with a width of 14 mil and a ground spacing of 7 mil to have a characteristic impedance of 50 Ω.

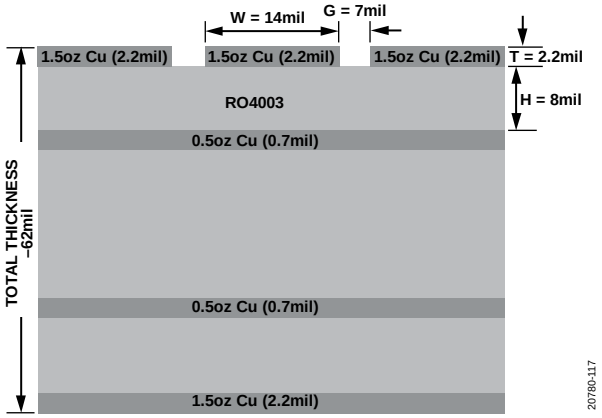

Figure 17. Probe Matrix Board Stack Up

Figure 17 shows the probe matrix board stack up, which is the same as the ADRF5300-EVALZ, but with a different layout that is designed to perform measurements using GSG probes at close proximity to the RFC, RF1, and RF2 pins. Probing reduces the reflections caused by mismatch arising from the connectors, cables, and board layout, which results in a more accurate measurement of the insertion loss and the return loss. Signal coupling between the RF probes limits the isolation measurement. Figure 18 shows the top view of the probe matrix board layout.

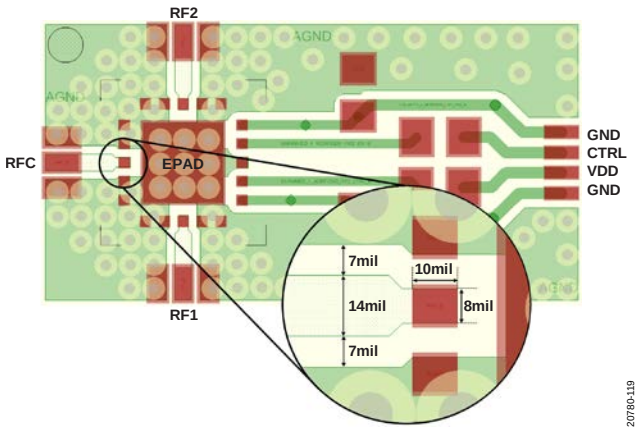

Figure 18. Probe Matrix Board, Top Layer

The probe matrix board includes a through reflect line (TRL) calibration kit allowing board loss de-embedding. The actual board duplicates the same layout in matrix form, which allows multiple devices to assemble at once. Insertion loss and return loss measurements are made on the probe matrix board, whereas isolation measurements are made on the ADRF5300-EVALZ.