Data Sheet

ADRF5301

Silicon, SPDT Switch, 37 GHz to 49 GHz

FEATURES

- Reflective design
- Low insertion loss: 1.4 dB typical
- High isolation: 30 dB typical
- High input linearity:
  - P0.1dB: 36 dBm
  - Input IP3: 52 dBm
- High RF power handling
  - 28 dBm average
  - 36 dBm peak
- Single-supply operation: 3.3V
  - Internal NVG
- RF settling time (0.1 dB final RF output): 50 ns
- 20-terminal, 3 mm × 3 mm, land grid array (LGA) package

APPLICATIONS

- Industrial scanner
- Test instrumentation
- Cellular infrastructure mmWave 5G
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

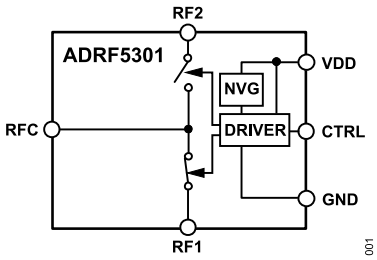

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5301 is a reflective, SPDT switch manufactured in the silicon process.

The ADRF5301 was developed for 5G applications from 37 GHz to 49 GHz. This device has a low insertion loss of 1.4 dB, high isolation of 30 dB, and RF input power handling capability of 28 dBm average and 36 dBm peak.

The ADRF5301 incorporates a negative voltage generator (NVG) to operate with a single positive supply of 3.3 V applied to the VDD pin. The device employs complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible control.

The ADRF5301 comes in a 20-terminal, 3 mm × 3 mm, RoHS-compliant, land grid array package and can operate from −40°C to +105°C.

Rev. 0

TABLE OF CONTENTS

REVISION HISTORY

10/2022—Revision 0: Initial Version

SPECIFICATIONS

Supply voltage (V_{DD}) = 3.3 V, CTRL voltage (V_{CTRL}) = 0 V or V_{DD}, T_{CASE} = +25°C, 50 Ω system, unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			37		49	GHz
INSERTION LOSS						
Between RFC and RF1/RF2				1.4		dB
ISOLATION						
Between RFC and RF1/RF2				30		dB
Between RF1 and RF2				30		dB
RETURN LOSS						
RFC and RF1/RF2 (On)				15		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		10		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		45		ns
RF Settling Time						
0.1 dB		50% V_{CTL} to 0.1 dB of final RF output		50		ns
0.05 dB		50% V_{CTL} to 0.05 dB of final RF output		55		ns
INPUT LINEARITY		f = 37 GHz to 40 GHz				
0.1 dB Power Compression	P0.1dB			36		dBm
Third-Order Intercept	IP3	Two-tone input power = 20 dBm per tone, Δf = 1 MHz		52		dBm
SUPPLY CURRENT	I_{DD}			450		µA
DIGITAL CONTROL INPUTS		CTRL pin				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			<1		µA
High	I_{INH}			14		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage	V_{DD}		3.15		3.45	V
Digital Control Voltage	V_{CTRL}		0		V_{DD}	V
RF Input Power[1]	P_{IN}	f = 37 GHz to 40 GHz, T_{CASE} = +85 °C[2]				
Average					28	dBm
Peak		100 ns pulse width, 2% duty cycle			36	dBm
Case Temperature	T_{CASE}		−40		+105	°C

[1] For power derating over frequency, see Figure 2.

[2] For operation at +105°C, the power handling degrades from the T_{CASE} = +85°C specification by 3 dB.

TIMING SPECIFICATIONS

See Figure 13 for the timing diagram.

Table 2. Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
$t_{POWERUP}$[1]	Minimum wait time after power-up	50			µs
t_{HOLD}	Minimum control switching time	40			µs
t_{SLEW}	Maximum control rise and fall time			10	µs

[1] A maximum of 10 dBm RF input power can be applied during the $t_{POWERUP}$ wait time.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 3. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	−0.3 V to +3.6 V
Digital Control Input Voltage	
Voltage	−0.3 V to VDD + 0.3 V
Current	3 mA
RF Input Power (V_{DD} = 3.3 V, f = 37 GHz to 40 GHz at T_{CASE} = 85°C)	
Average	28.5 dBm
Peak	36.5 dBm
RF Input Power Under Unbiased Condition (V_{DD} = 0 V)	
Average	28 dBm
Peak	36 dBm
Temperature	
Junction (T_J)	135°C
Storage	−65°C to +150°C
Reflow	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction-to-case bottom (channel-to-package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-20-17, Through Path	235	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of +85°C.

POWER DERATING CURVE

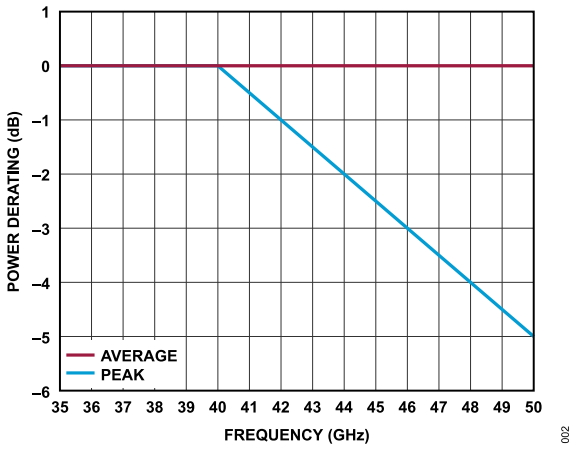

Figure 2. Power Derating vs. Frequency, T_{CASE} = +85°C

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) ratings are per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) ratings are per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5301

Table 5. ADRF5301, 20-Terminal LGA

ESD Model	Withstand Threshold (V)
HBM	±500 for RF Pins
	±2000 for Supply and Digital Control Pins
CDM	±1250 for all Pins

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

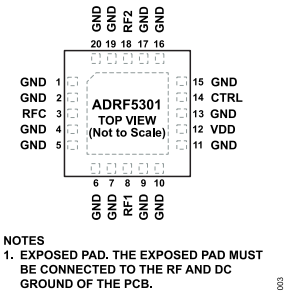

Figure 3. Pin Configuration (Top View)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 7, 9 to 11, 13, 15 to 17, 19, 20	GND	Ground. These pins must be connected to the RF and DC ground of the PCB. See Figure 6 for the interface schematic.
3	RFC	RF Common Port. This pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
8	RF1	RF Throw Port 1. This pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
12	VDD	Positive Supply Voltage Input. See Figure 6 for the interface schematic.
14	CTRL	Control Voltage Input. See Figure 5 for the interface schematic.
18	RF2	RF Throw Port 2. This pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and DC ground of the PCB.

INTERFACE SCHEMATICS

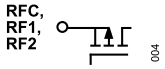

Figure 4. RFC, RF1, and RF2 Pins Interface Schematic

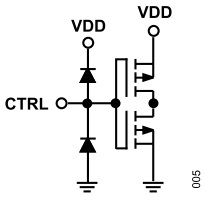

Figure 5. CTRL Pin Interface Schematic

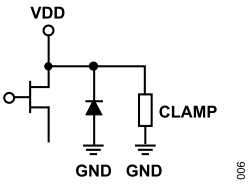

Figure 6. VDD Pin and GND Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{CTRL} = 0 V or V_{DD}, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted. Measured on the ADRF5301-EVALZ evaluation board.

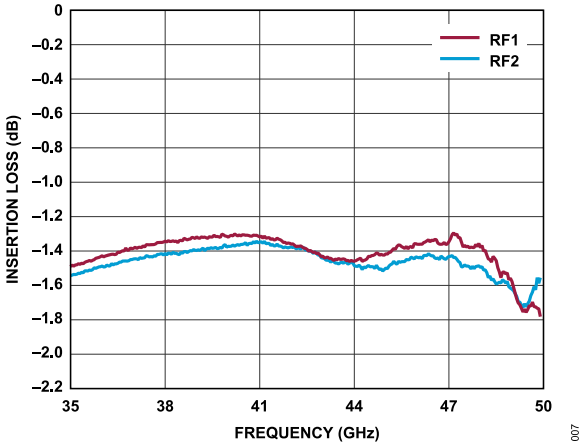

Figure 7. Insertion Loss vs. Frequency

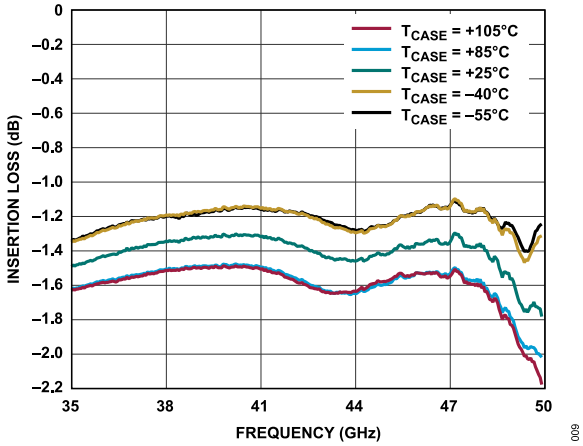

Figure 9. Insertion Loss vs. Frequency Over Temperature

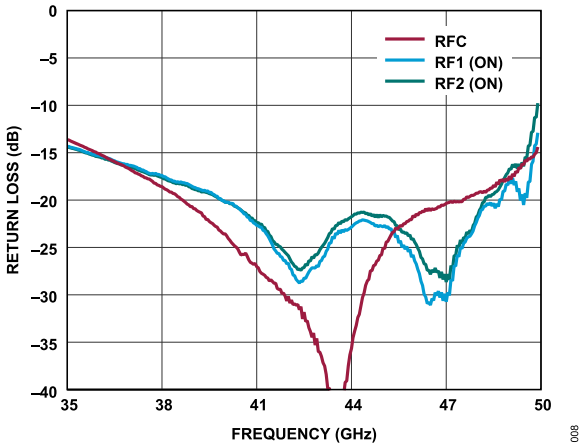

Figure 8. Return Loss vs. Frequency

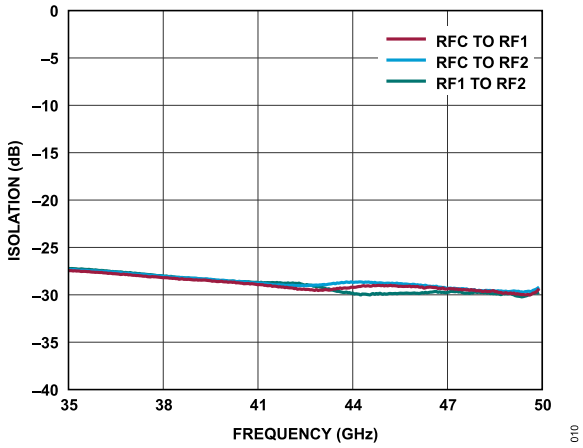

Figure 10. Isolation vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = 3.3 V, V_{CTRL} = 0 V or V_{DD}, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted. All of the large signal performance parameters are measured on the ADRF5301-EVALZ evaluation board.

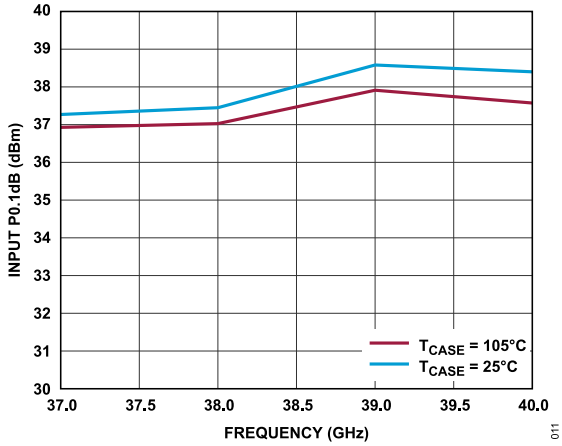

Figure 11. Input P0.1dB vs. Frequency

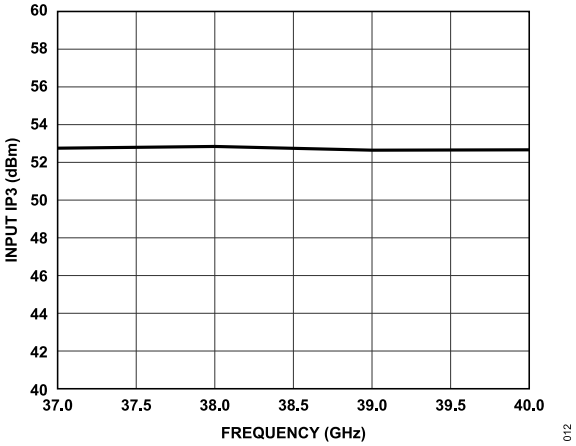

Figure 12. Input IP3 vs. Frequency

THEORY OF OPERATION

The ADRF5301 integrates a driver to perform logic functions internally and to provide the user with the advantage of a simplified control interface. The driver features a single digital control input pin, CTRL, which controls the state of the RF paths. The logic level applied to the CTRL pin determines which RF port is in the insertion loss state while the other path is in the isolation state (see Table 7).

RF INPUT AND OUTPUT

All of the RF ports (RFC, RF1, and RF2) are DC-coupled to 0 V, and no DC blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

The ADRF5301 is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation paths provide high loss between the insertion loss path and the unselected RF throw port that is reflective.

POWER SUPPLY

The ADRF5301 integrates a negative voltage generator (NVG) and requires a single positive supply voltage applied to the VDD pin. Bypassing capacitors are recommended on the supply line to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect GND reference.
2. Power-up supply input VDD.
3. Apply digital control input CTRL. Applying the CTRL control before applying the VDD supply inadvertently forward biases and damages the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller output is in a high-impedance state after VDD is powered up and the control pins are not driven to a valid logic state.
4. Apply RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

TIMING REQUIREMENTS

There are timing requirements for the proper operation of the bias and control circuits. See Table 2 for the timing specifications. See Figure 13 for the timing requirements.

After VDD reaches the operating range, $t_{POWERUP}$ defines the wait time before the recommended maximum RF power can be applied. During this time, a maximum of 10 dBm RF input power can be applied.

The minimum wait time before switching states is defined by t_{HOLD}.

The maximum rise and fall time of the CTRL pulse is defined by t_{SLEW}.

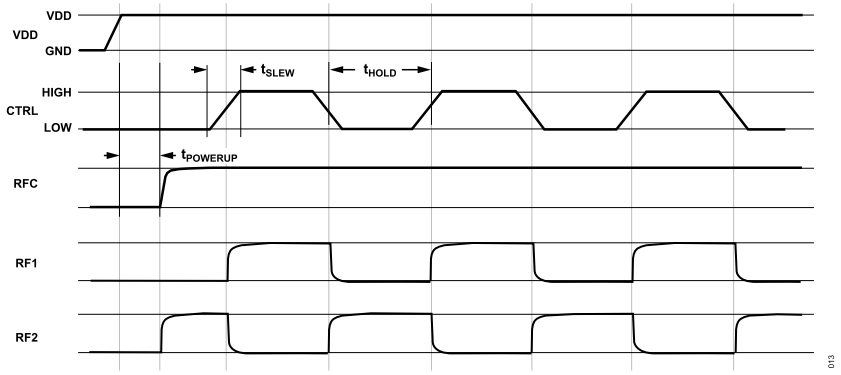

Figure 13. Timing Requirements

Table 7. Control Voltage Truth Table

Digital Control Input	RF Paths	
CTRL	RF1 to RFC	RF2 to RFC
High	Insertion loss (on)	Isolation (off)
Low	Isolation (off)	Insertion loss (on)

APPLICATIONS INFORMATION

The ADRF5301 has one power supply pin (VDD) and one control pin (CTRL). Figure 14 shows the external components and connections for the supply pin. The VDD pin is decoupled with a 100pF multilayer ceramic capacitor. The device pin-out allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RF pins when the RF lines are biased at a voltage different than 0 V. See the Pin Configuration and Function Descriptions section for details.

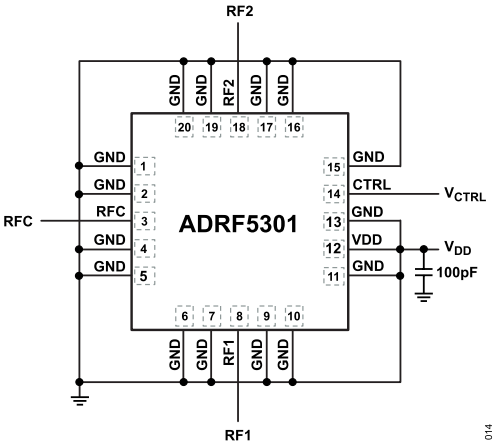

Figure 14. Recommended Schematic

RECOMMENDATIONS FOR PRINTED CIRCUIT BOARD DESIGN

The RF ports are matched to 50 Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with 50 Ω characteristic impedance on the PCB. Figure 15 shows the referenced CPWG RF trace design for an RF substrate with 8 mil thick Rogers RO4003 dielectric material. RF trace with 14mil width and 7 mil clearance is recommended for 2.2 mil finished copper thickness.

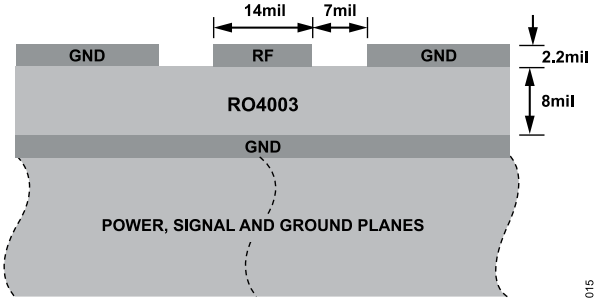

Figure 15. Example PCB Stack-Up

Figure 16 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with as many filled, through vias as allowed for optimal RF, and thermal performance. The primary thermal path for the device is the bottom side.

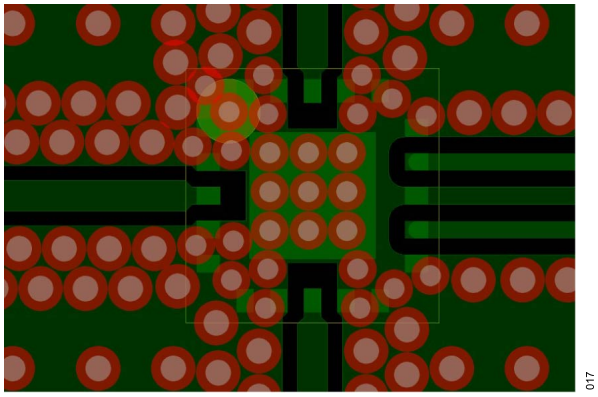

Figure 16. PCB Routings

Figure 17 shows the recommended layout from the device RF pins to the 50 Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to device pads. The ground pads are drawn soldermask defined and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width by 2 mils and tapered to RF trace with a 45° angle. The paste mask is also designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

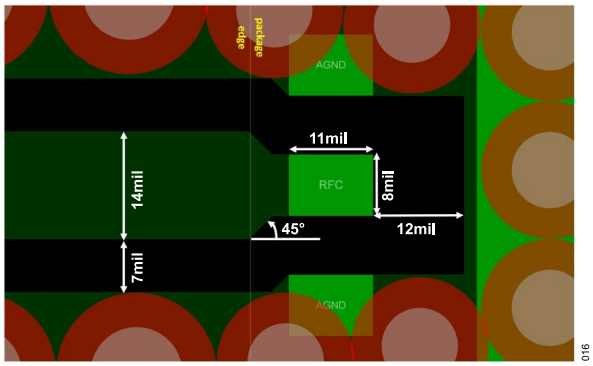

Figure 17. Recommended RF Pin Transitions

For alternate PCB stack-ups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support Request for further recommendations.