3.1 GHz to 4.2 GHz, Receiver Front End

FEATURES

- Integrated RF front end
  - LNA and high-power silicon SPDT switch
  - On-chip bias and matching
  - Single-supply operation
- Gain: 35.5 dB typical at 3.6 GHz
- Gain flatness: 1.5 dB at 25°C across 400 MHz bandwidth
- Low noise figure: 1.3 dB typical at 3.6 GHz
- Low insertion loss: 0.8 dB typical at 3.6 GHz
- High-power handling at T_{CASE} = 105°C
  - Full lifetime
    - LTE average power (8 dB PAR): 37 dBm
  - Single event (<10 sec operation)
    - LTE average power (8 dB PAR): 39 dBm
- High Input IP3: −4 dBm
- Low-supply current
  - Receive operation: 120 mA typical at 5 V
  - Transmit operation: 15 mA typical at 5 V
- Positive logic control
- 5 mm × 3 mm, 24-lead LFCSP package

APPLICATIONS

- Wireless infrastructure
- TDD massive multiple input and multiple output (MIMO) and active antenna systems
- TDD-based communication systems

FUNCTIONAL BLOCK DIAGRAM

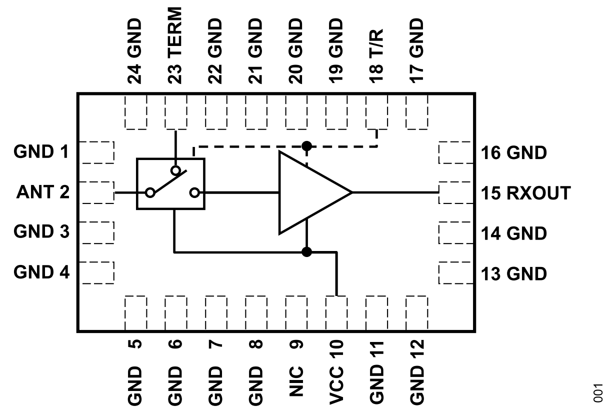

Figure 1.

GENERAL DESCRIPTION

The ADRF5534 is an integrated RF, front-end multichip module designed for time division duplex (TDD) applications. The device operates from 3.1 GHz to 4.2 GHz. The ADRF5534 is configured with an LNA and a high-power, silicon, SPDT switch.

In the receive operation at 3.6 GHz, the LNA offers a low noise figure (NF) of 1.3 dB and a high gain of 35.5 dB with a third order input intercept point (IIP3) of −4 dBm.

In the transmit operation, the switch provides a low insertion loss of 0.8 dB and handles a long-term evolution (LTE) average power of 37 dBm for a full lifetime operation (8 dB peak to average ratio (PAR)) and 39 dBm for a single event (<10 sec) LNA protection operation.

The device is featured in an RoHS compliant, compact, 5 mm × 3 mm, 24-lead LFCSP package.

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REVISION HISTORY

3/2023—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VCC = 5 V, T/R = 0 V or 5 V, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		3.1		4.2	GHz
RECEIVE OPERATION	At 3.6 GHz, unless otherwise noted				
Gain	ANT to RXOUT		35.5		dB
Gain Flatness	Over any 400 MHz bandwidth		1.5		dB
Input Return Loss	ANT port		20		dB
Output Return Loss	RXOUT port		25		dB
Reverse Isolation	RXOUT to ANT		53		dB
Term Isolation	ANT to TERM		20		dB
NF			1.3		dB
IIP3	Two-tone input power = −30 dBm per tone at 1 MHz tone spacing		−4		dBm
Input 1 dB Compression (IP1dB)			−17		dBm
Switching Speed	ANT to RXOUT, 50% of T/R to 10%, 90% of RF output		800		ns
Settling Time	ANT to RXOUT, 50% of T/R to 0.3 dB of RF output		950		ns
TRANSMIT OPERATION	At 3.6 GHz, unless otherwise noted				
Insertion Loss	ANT to TERM		0.8		dB
Input Return Loss	ANT port		20		dB
Output Return Loss	TERM port		18		dB
IIP3	Two-tone input power = 30 dBm per tone at 80 MHz tone spacing		65		dBm
IP1dB			45		dBm
Input 0.1 dB Compression (IP0.1dB)			43		dBm
Switching Speed	ANT to TERM, 50% of T/R to 10%, 90% of RF output		600		ns
Settling Time	ANT to TERM, 50% of T/R to 0.3 dB of RF output		650		ns
RECOMMENDED OPERATING CONDITIONS					
Supply Voltage (VCC) Range	VCC	4.75	5	5.25	V
Control Voltage Range	T/R	0		VCC	V
RF Input Power at ANT	T/R = 5 V, T_C = 105°C				
	8 dB PAR LTE full lifetime average			37	dBm
	8 dB PAR LTE single event (<10 sec) average			39	dBm
T_{CASE}		−40		+105	°C
T_{CASE} at Maximum					
	Receive operation			145	°C
	Transmit operation			135	°C
SUPPLY CURRENT (I_{CC})	VCC = 5 V				
Receive Operation			120		mA
Transmit Operation			15		mA
DIGITAL INPUT	T/R				
Low (V_{IL})		−0.3		0.7	V
High (V_{IH})		1.07		VCC	V
DIGITAL INPUT CURRENT	T/R = 5 V		5		μA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Positive Supply Voltage	
VCC	5.4 V
Digital Control Input Voltage	
T/R	−0.3 V to VCC + 0.3 V
Digital Control Input Current	
T/R	15 mA
RF Input Power	
Transmit Input Power (LTE Peak, 8 dB PAR)	47.5 dBm
Receive Input Power (LTE Peak, 8 dB PAR)	12 dBm
Temperature	
Storage	−65°C to +150°C
Reflow Moisture Sensitivity Level 3 (MSL3) Rating	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction-to-case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-24-27		
Receive Operation	61	°C/W
Transmit Operation	32	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

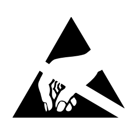
Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADRF5534

Table 4. ADRF5534, 24-Lead LFCSP

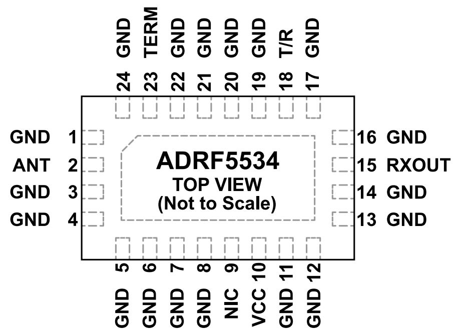
ESD Model	Withstand Threshold (V)	Class
HBM	1000	1C
CDM	500	C2

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED. IT IS RECOMMENDED TO CONNECT NIC TO THE RF GROUND OF THE PCB.
2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO RF OR DC GROUND.

002

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3 to 8, 11 to 14, 16, 17, 19 to 22, 24	GND	Ground. These pins must be connected to the RF or DC ground of the PCB.
2	ANT	Antenna Input. Pin 2 is DC-coupled to 0 V and AC-matched to 50 Ω.
9	NIC	Not Internally Connected. It is recommended to connect NIC to the RF ground of the PCB.
10	VCC	Positive Supply Voltage.
15	RXOUT	Receive LNA Output. Pin 15 is DC-coupled to 0 V and AC-matched to 50 Ω.
18	T/R	Transmit/Receive Operation Control Logic Input.
23	TERM	Termination Output. Pin 23 is DC-coupled to 0 V and AC-matched to 50 Ω.
	EPAD	Exposed Pad. The exposed pad must be connected to RF or DC ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

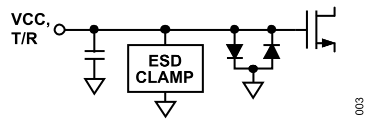


Figure 3. VCC and T/R Interface Schematic

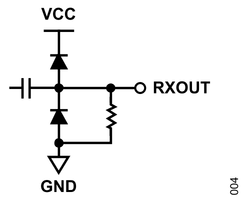


Figure 4. RXOUT Interface Schematic

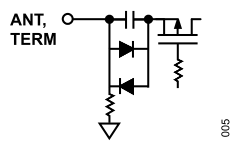


Figure 5. ANT and TERM Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

RECEIVE OPERATION

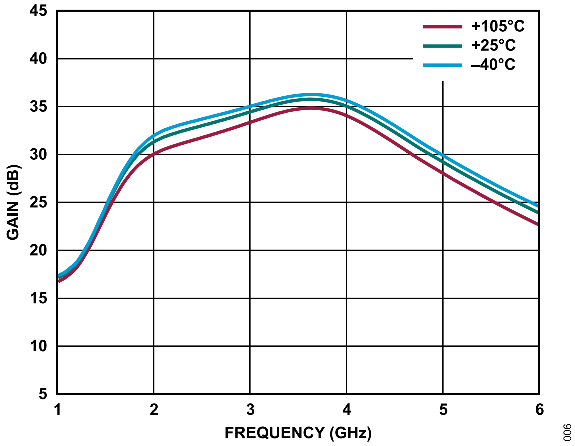


Figure 6. Gain vs. Frequency at Various Temperatures

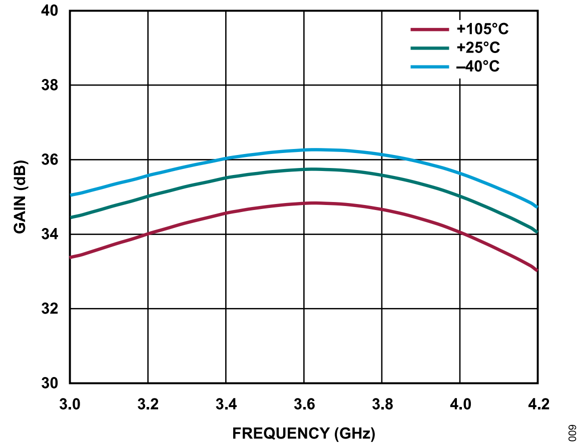


Figure 9. Gain vs. Frequency at Various Temperatures, 3.0 GHz to 4.2 GHz

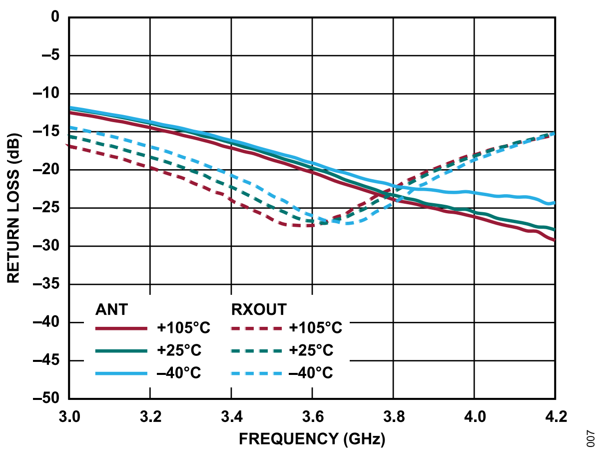


Figure 7. Return Loss vs. Frequency

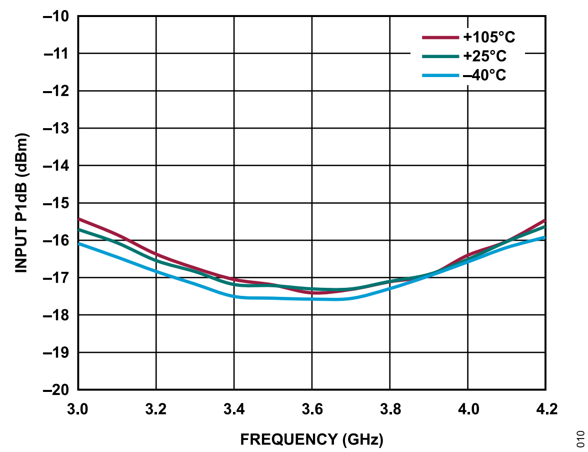


Figure 10. Input P1dB vs. Frequency at Various Temperatures

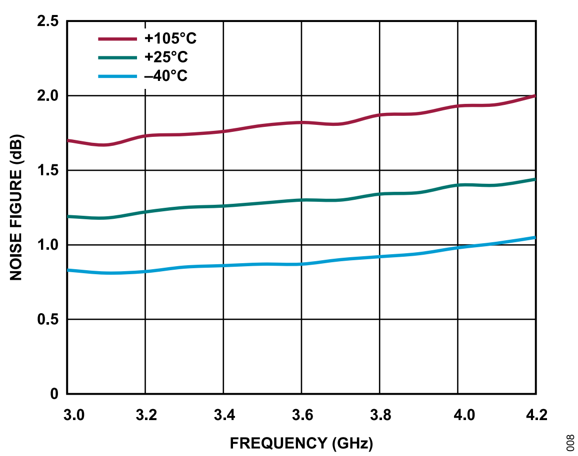


Figure 8. Noise Figure vs. Frequency

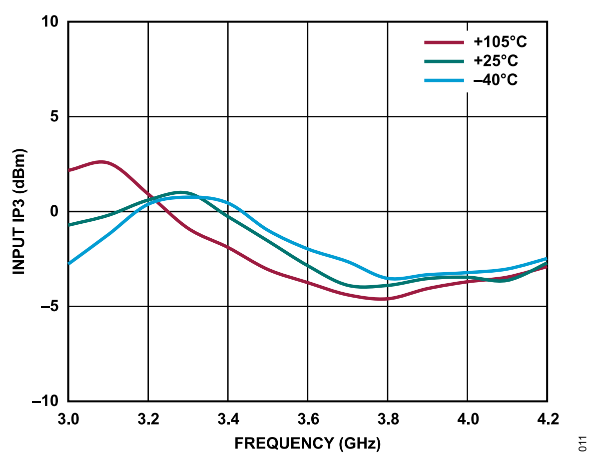


Figure 11. Input IP3 vs. Frequency at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

TRANSMIT OPERATION

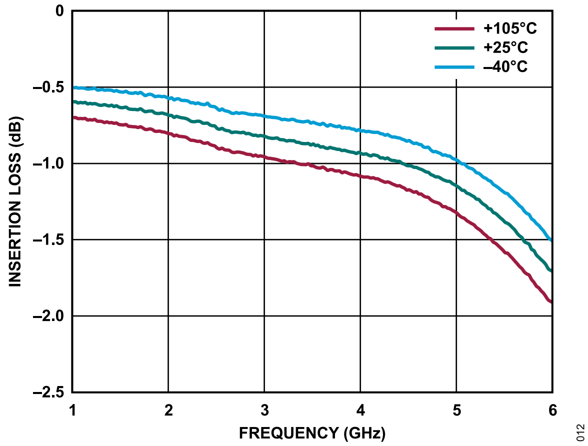


Figure 12. Insertion Loss vs. Frequency at Various Temperatures

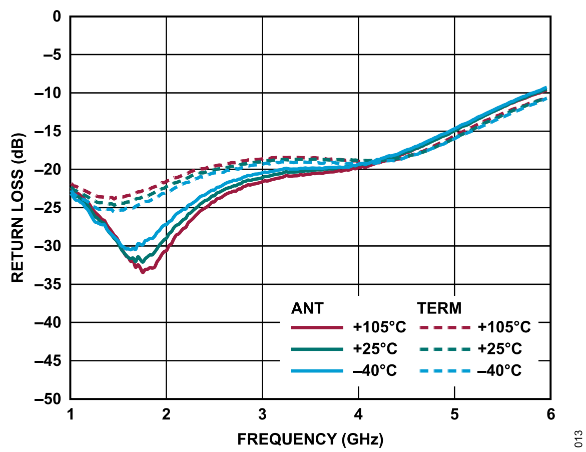


Figure 13. Return Loss vs. Frequency

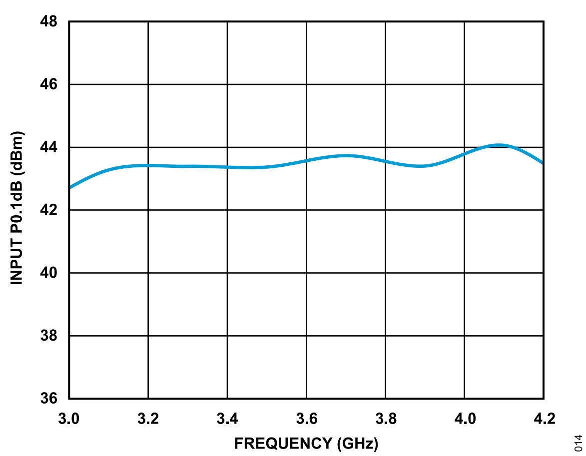


Figure 14. Input P0.1dB vs. Frequency

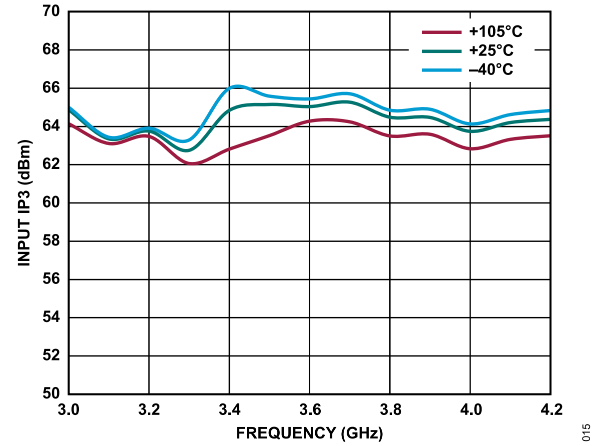


Figure 15. Input IP3 vs. Frequency

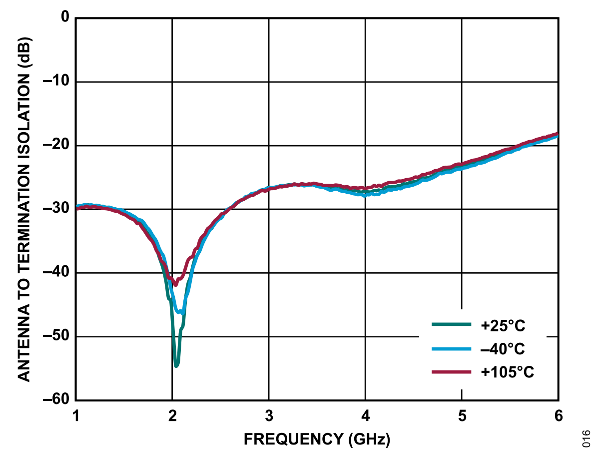


Figure 16. Antenna to Termination Isolation vs. Frequency, LNA On

THEORY OF OPERATION

The ADRF5534 requires a positive supply voltage applied to the VCC. Use the bypass capacitors on the supply lines to filter noise. Refer to the application circuit for the capacitor values and configuration.

SIGNAL PATH SELECTION

The ADRF5534 supports two operational states: transmit operation and receive operation.

The transmit operation is enabled when 0 V is applied to T/R. In the transmit operation, the signal paths are connected from ANT to TERM. Additionally, the ADRF5534 disables the power to the LNA, reducing the current and thermal contributions from the LNA.

The receive operation is enabled when 5 V is applied to T/R. In the receive operation, the signal paths are connected from ANT to RXOUT. During the receive operation, the switch is in an isolation state.

BIASING SEQUENCE

To bias up the ADRF5534, perform the following steps:

1. Connect any GND pin to ground.
2. Power up the supply input VCC.
3. Apply digital control input T/R. Applying the T/R control before applying the VCC supply inadvertently forward biases and damages the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller output is in a high-impedance state after VCC is powered up and the control pins are not driven to a valid logic state.
4. Apply an RF input signal.

To bias down, perform these steps in the reverse order.

Table 6. Truth Table: Signal Path Selection

	Signal Path Selection	
T/R	**Transmit Operation (ANT to TERM)**	**Receive Operation (ANT to RXOUT)**
Low	On	Off, LNA powered down
High	Off, isolation state	On

APPLICATIONS INFORMATION

The ADRF5534 has a single power-supply pin (VCC) and one control pin (T/R). Figure 17 shows the external components and connections for supply and control pins. The VCC pin is decoupled with a 100 pF multilayer ceramic capacitor and a 4.7 uF capacitor. The T/R pin is decoupled with a 100 pF multilayer ceramic capacitor. The device pin-out allows the placement of the decoupling capacitors close to the device. The RF pins (ANT, TERM, RXOUT) do not require external DC blocking capacitors; all pins are pulled down to 0 V DC with high-impedance. Refer to Table 5 for details.

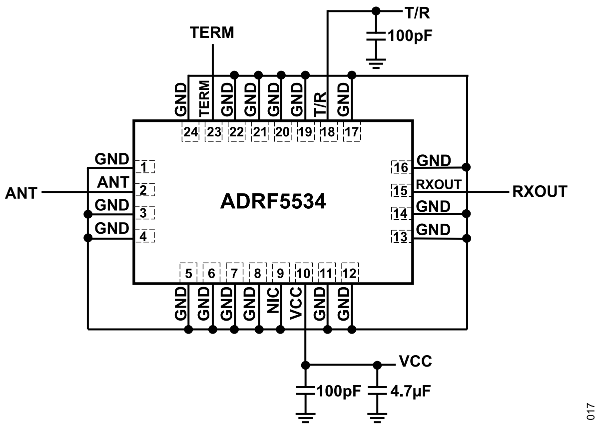


Figure 17. Recommended Schematic

RECOMMENDATIONS FOR PRINTED CIRCUIT BOARD DESIGN

The RF ports are matched to 50 Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with 50 Ω characteristic impedance on the PCB. Figure 18 shows the referenced CPWG RF trace design for an RF substrate with 10 mil thick Rogers RO4350 dielectric material. RF trace with 18 mil width and 13 mil clearance is recommended for the 2.7 mil finished copper thickness.

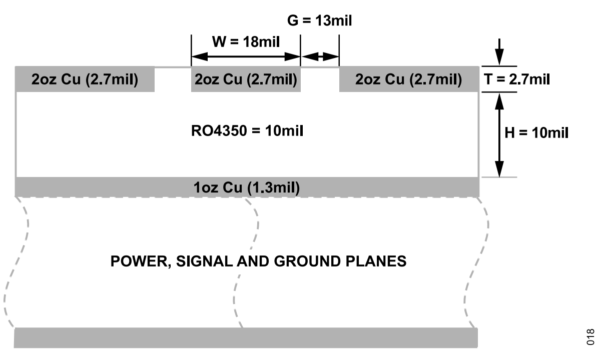


Figure 18. Example PCB Stack-Up

Figure 19 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with as many filled, through vias as allowed for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

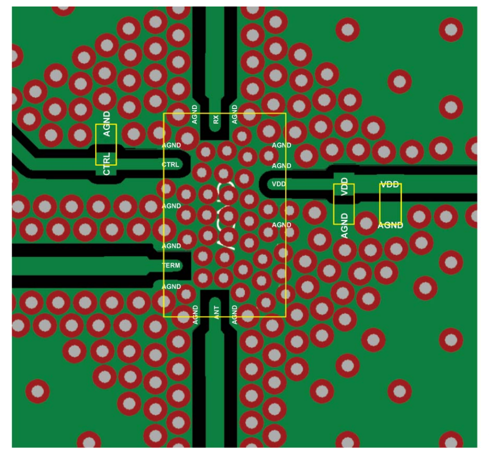


Figure 19. PCB Routings

Figure 20 shows the recommended layout from the device RF pins to the 50 Ω CPWG on the referenced stack-up. The ground pads are drawn as soldermask defined and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width and tapered to the RF trace with a 45° angle. The paste mask is also designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

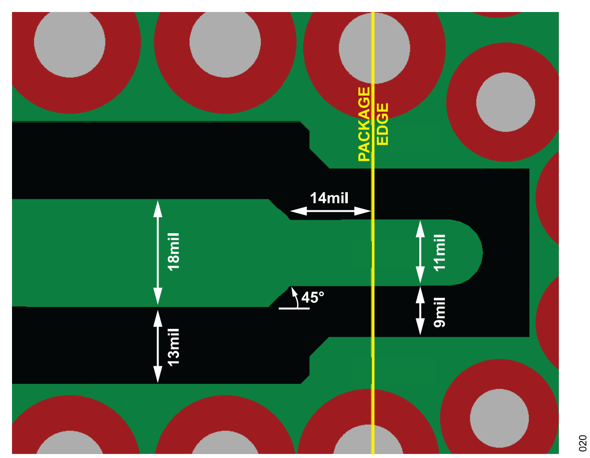


Figure 20. Recommended RF Pin Transitions

For alternate PCB stack-ups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support Request for further recommendations.