46 dB, 2 dB LSB, 5-Bit, Silicon Digital Attenuator, 100 MHz to 22 GHz

FEATURES

- Wideband frequency range: 100 MHz to 22 GHz
- Attenuation range: 46 dB with 2 dB steps
- Low insertion loss
  - 1.6 dB typical up to 10 GHz
  - 2.0 dB typical up to 20 GHz
- Excellent attenuation accuracy
  - +(0.1 + 0.5% of attenuation state) typical up to 10 GHz
  - −(0.1 + 2.0% of attenuation state) typical up to 10 GHz
  - +(0.1 + 0.5% of attenuation state) typical up to 20 GHz
  - −(0.1 + 3.0% of attenuation state) typical up to 20 GHz
- Low step error
  - ±0.2 dB typical up to 10 GHz
  - ±0.3 dB typical up to 20 GHz
- High input linearity
  - P0.1dB: >27 dBm typical at all attenuation states
  - P1dB: >30 dBm typical at all attenuation states
  - IP3: >47 dBm typical at all attenuation states
- High RF power handling
  - 24 dBm steady state average
  - 30 dBm steady state peak
- Excellent return loss at all attenuation states
- Tight distribution in relative phase
- No low frequency spurious signals
- Parallel mode control, CMOS/LVTTL compatible
- RF amplitude settling time (0.1 dB of final RF output): 130 ns
- 20-terminal, 3.0 mm × 3.0 mm LGA package

APPLICATIONS

- Industrial scanners
- Test and instrumentation
- Cellular infrastructure: 5G millimeterwave
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

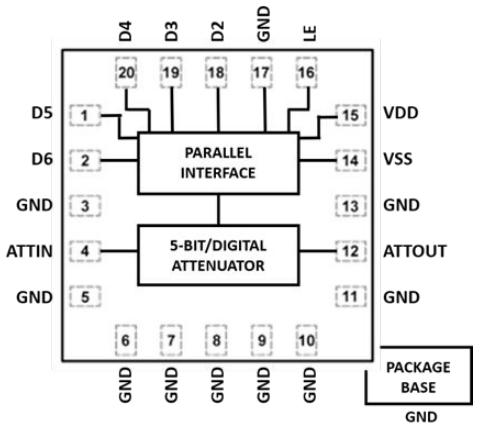

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5700 is a silicon, 5-bit digital attenuator with 46 dB attenuation control range in 2 dB steps.

This device operates from 100 MHz to 22 GHz with better than 2.0 dB of insertion loss and excellent attenuation accuracy. The ADRF5700 supports bidirectional operation and has a RF input power handling capability of 24 dBm average and 30 dBm peak for all attenuation states.

The ADRF5700 requires a dual-supply voltage of +3.3 V and −3.3 V. The device features parallel mode control, and complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5700 can also operate with a single positive supply voltage (VDD) applied while the negative supply voltage (VSS) is tied to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance are derated, see Table 2.

The ADRF5700 RF ports are designed to match a characteristic impedance of 50 Ω. The ADRF5700 comes in a 20-terminal, 3.0 mm × 3.0 mm, RoHS compliant, land grid array (LGA) package and operates from −40°C to +105°C.

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD = 3.3 V, VSS = −3.3 V, V_{CTRL} = 0 V or VDD, T_{CASE} = 25°C, and 50 Ω system, unless otherwise noted. V_{CTRL} refers to the control voltages on the LE, D2, D3, D4, D5 and D6 pins.

Table 1. Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		100		22,000	MHz
INSERTION LOSS	100 MHz to 10 GHz		1.6		dB
	10 GHz to 20 GHz		2.0		dB
RETURN LOSS	ATTIN and ATTOUT, all attenuation states				
	100 MHz to 10 GHz		18		dB
	10 GHz to 20 GHz		18		dB
ATTENUATION					
Range	Between minimum and maximum attenuation states		46		dB
Step Size	Between any successive attenuation states		2		dB
Accuracy	Referenced to insertion loss				
	100 MHz to 10 GHz		+(0.1 + 0.5% of state)		dB
			−(0.1 + 2.0% of state)		dB
	10 GHz to 20 GHz		+(0.1 + 0.5% of state)		dB
			−(0.1 + 3.0% of state)		dB
Step Error	Between any successive state				
	100 MHz to 10 GHz		±0.2		dB
	10 GHz to 20 GHz		±0.3		dB
RELATIVE PHASE	Referenced to insertion loss				
	100 MHz to 10 GHz		40		Degrees
	10 GHz to 20 GHz		85		Degrees
SWITCHING CHARACTERISTICS	All attenuation states at input power (P_{IN}) = 10 dBm				
Rise Time and Fall Time (t_{RISE} and t_{FALL})	10% to 90% of RF output (RF_{OUT})		10		ns
On Time and Off Time (t_{ON} and t_{OFF})	50% triggered control to 90% of RF_{OUT}		50		ns
RF Amplitude Settling Time					
0.1 dB	50% triggered control to 0.1 dB of final RF_{OUT}		130		ns
0.05 dB	50% triggered control to 0.05 dB of final RF_{OUT}		150		ns
Overshoot			1		dB
Undershoot			0.75		dB
RF Phase Settling Time	Frequency = 20 GHz				
5°	50% triggered control to 5° of final RF output		60		ns
1°	50% triggered control to 1° of final RF output		80		ns
INPUT LINEARITY[1]	100 MHz to 20 GHz, all attenuation states				
0.1 dB Power Compression (P0.1dB)			>27		dBm
1 dB Power Compression (P1dB)			>30		dBm
Third-Order Intercept (IP3)	Two-tone P_{IN} = 15 dBm per tone, Δf = 1 MHz		>47		dBm
DIGITAL CONTROL INPUTS	LE, D2, D3, D4, D5, and D6				
Voltage					
Low (V_{INL})		0		0.8	V
High (V_{INH})		1.2		3.3	V
Current					
Low (I_{INL})			−33		µA
High (I_{INH})			<1		µA

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY CURRENT					
Positive Supply Current (I_{DD})					
Bias Low	LE, D2, D3, D4, D5, and D6 = 0 V		350		µA
Bias High	LE, D2, D3, D4, D5, and D6 = 3.3 V		150		µA
Negative Supply Current (I_{SS})			−520		µA
RECOMMENDED OPERATING CONDITIONS					
Supply Voltage					
Positive (VDD)		3.15		3.45	V
Negative (VSS)		−3.45		−3.15	V
Digital Control Voltage		0		VDD	V
RF Power Handling[2,3]	Frequency = 100 MHz to 20 GHz, T_{CASE} = 85°C, all attenuation states				
Input at ATTIN or ATTOUT	Steady state, average			24	dBm
	Steady state, peak			30	dBm
	Hot switching, average			24	dBm
	Hot switching, peak			27	dBm
Case Temperature	T_{CASE}	−40		+105	°C

[1] For input linearity performance over wide frequency range, see Figure 21 and Figure 22.

[2] For power derating over frequency, see Figure 2 to Figure 3. Applicable for all ATTIN and ATTOUT power specifications.

[3] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specifications by 3 dB.

SPECIFICATIONS

SINGLE-SUPPLY OPERATION

VDD = 3.3 V, VSS = 0 V, V_{CTRL} = 0 V or VDD V, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 2. Single-Supply Operational Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		100		22,000	MHz
SWITCHING CHARACTERISTICS					
Rise Time and Fall Time	10% to 90% of RF_{OUT}		95		ns
On Time and Off Time	50% V_{CTRL} to 90% of RF_{OUT}		125		ns
RF Amplitude Settling Time					
0.1 dB	50% V_{CTRL} to 0.1 dB of final RF_{OUT}		160		ns
0.05 dB	50% V_{CTRL} to 0.05 dB of final RF_{OUT}		165		ns
RF Phase Settling Time	Frequency = 20 GHz				
5°	50% triggered control to 5° of final RF_{OUT}		70		ns
1°	50% triggered control to 1° of final RF_{OUT}		150		ns
INPUT LINEARITY	Frequency = 100 MHz to 20 GHz				
0.1 dB Power Compression			17		dBm
Input Third-Order Intercept	Two-tone input power = 5 dBm each tone, Δf = 1 MHz		42		dBm
RECOMMENDED OPERATING CONDITONS					
RF Power Handling[1, 2]	Frequency = 100 MHz to 20 GHz, T_{CASE} = 85°C, all attenuation states				
Input at ATTIN or ATTOUT	Steady state, average			15	dBm
	Steady state, peak			15	dBm
	Hot switching, average			15	dBm
	Hot switching, peak			15	dBm

[1] For power derating over frequency, see Figure 2 to Figure 3. Applicable for all ATTIN and ATTOUT power specifications.

[2] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

TIMING SPECIFICATIONS

See Figure 24 for the timing diagram.

Table 3. Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t_{LEW}	LE pulse width, see Figure 24	10			ns
t_{PH}	Hold time, see Figure 24			10	ns
t_{PS}	Setup time, see Figure 24	2			ns

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
VDD	−0.3 V to +3.6 V
VSS	−3.6 V to +0.3 V
Digital Control Inputs	
Voltage	−0.3 V to VDD + 0.3 V
Current	3 mA
RF Input Power, Dual Supply[1] (VDD = 3.3 V, VSS = −3.3 V, frequency = 100 MHz to 20 GHz, T_{CASE} = 85°C[2])	
Steady State, Average	25 dBm
Steady State, Peak	31 dBm
Hot Switching, Average	25 dBm
Hot Switching, Peak	28 dBm
RF Input Power, Single Supply[1] (VDD = 3.3 V, VSS = 0 V, frequency = 100 MHz to 20 GHz, T_{CASE} = 85°C[2])	
Steady State, Average	16 dBm
Steady State, Peak	16 dBm
Hot Switching, Average	16 dBm
Hot Switching, Peak	16 dBm
RF Power Under Unbiased Condition (VDD and VSS = 0 V)	
Input at ATTIN or ATTOUT	11 dBm
Temperature	
Junction (T_J)	135°C
Storage	−65°C to +150°C
Reflow	260°C

[1] For power derating over frequency, see Figure 2 and Figure 3. Applicable for all ATTIN and ATTOUT power specifications.

[2] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specifications by 3 dB.

Stresses at or above those listed under absolute maximum ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
C-20-9	200	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

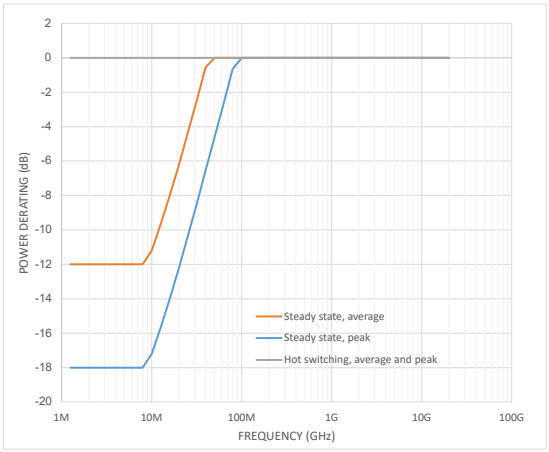

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

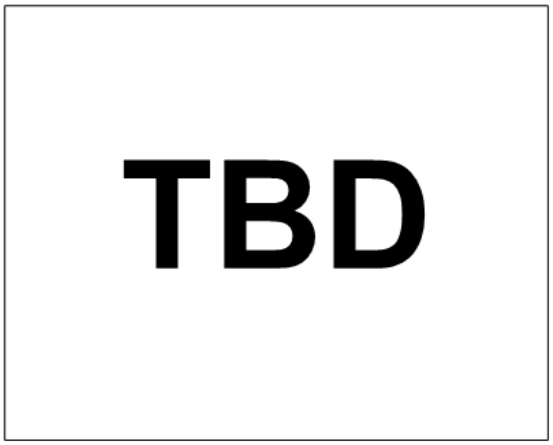

Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{CASE} = 85°C

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5700

Table 6. ADRF5700, 20-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	±1000 for ATTIN and ATTOUT Pins	1C
	±2000 for Supply and Control Pins	2
CDM	±500 for All Pins	C2

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

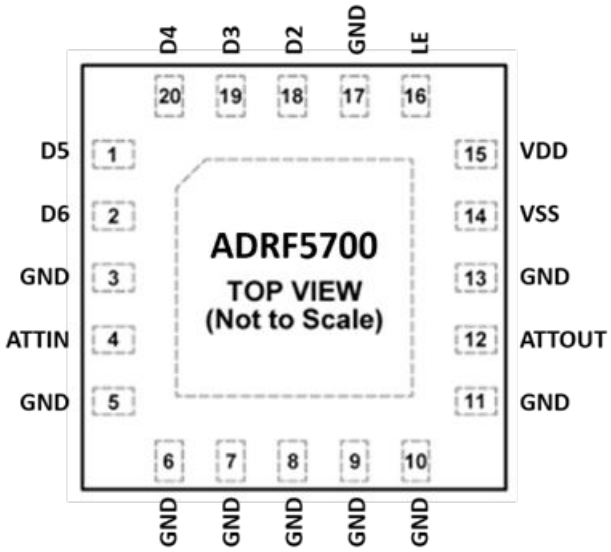

Figure 4. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D5	Parallel Control Input for the First 16 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
2	D6	Parallel Control Input for the Second 16 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
3, 5 to 11, 13, 17	GND	Ground. The GND pins must be connected to the RF and DC ground of the PCB.
4	ATTIN	Attenuator Input. The ATTIN pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 5 for the interface schematic.
12	ATTOUT	Attenuator Output. The ATTOUT pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 5 for the interface schematic.
14	VSS	Negative Supply Input. See Figure 8 for the interface schematic.
15	VDD	Positive Supply Input. See Figure 7 for the interface schematic.
16	LE	Latch Enable Input. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
18	D2	Parallel Control Input for 2 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
19	D3	Parallel Control Input for 4 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
20	D4	Parallel Control Input for 8 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and DC ground of the PCB.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

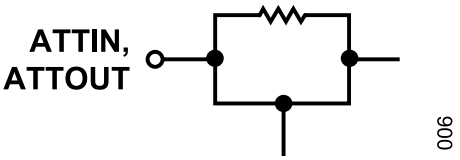

Figure 5. ATTIN and ATTOUT Interface Schematic

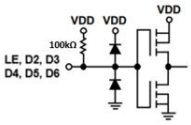

Figure 6. Digital Input Interface Schematic (LE, D2, D3, D4, D5, and D6)

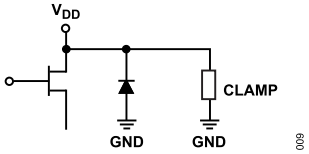

Figure 7. VDD Input Interface Schematic

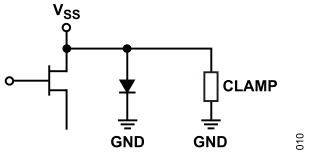

Figure 8. VSS Input Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

VDD = 3.3 V, VSS = −3.3 V, V_{CTRL} = 0 V or VDD, T_{CASE} = 25°C, and a 50 Ω system, unless otherwise noted. Measured on the ADRF5700-EVALZ.

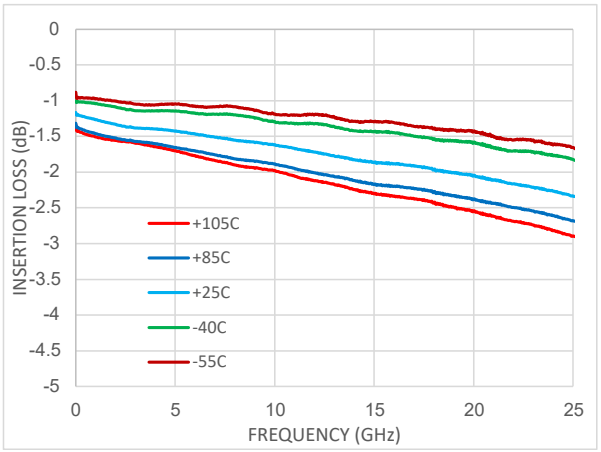

Figure 9. Insertion Loss vs. Frequency over Temperature

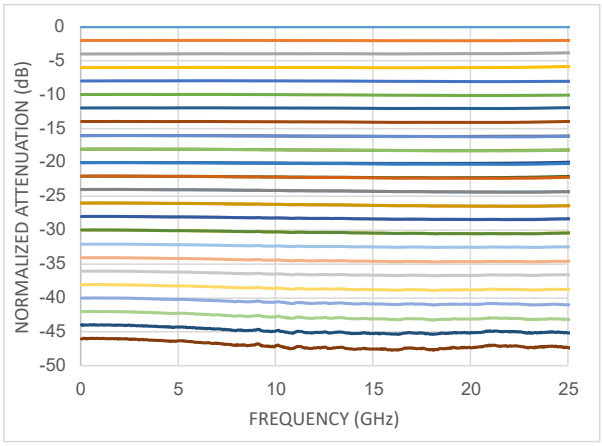

Figure 12. Normalized Attenuation vs. Frequency for All States

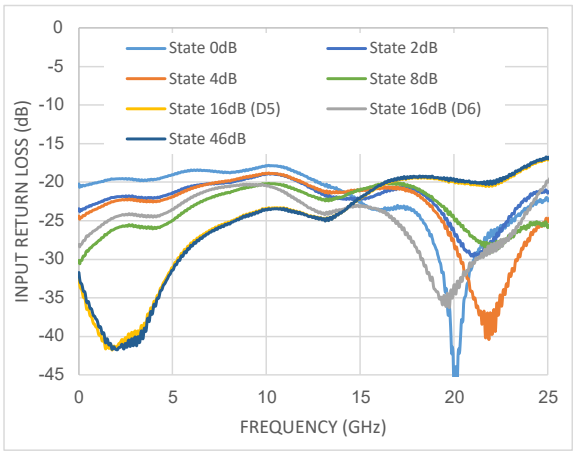

Figure 10. Input Return Loss vs. Frequency (Major States Only)

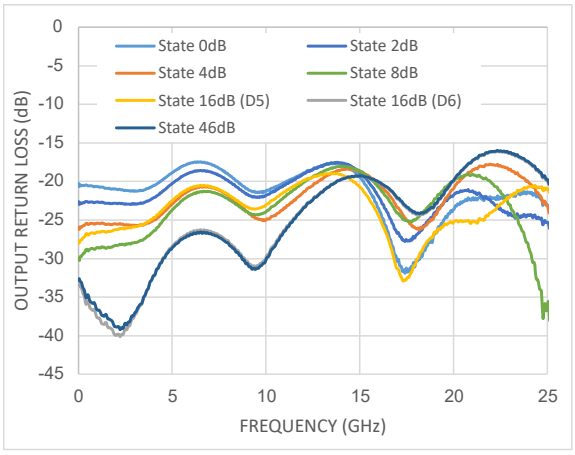

Figure 13. Output Return Loss vs. Frequency (Major States Only)

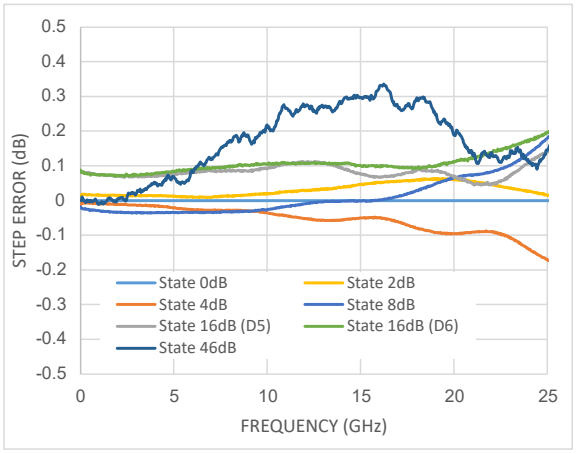

Figure 11. Step Error vs. Frequency

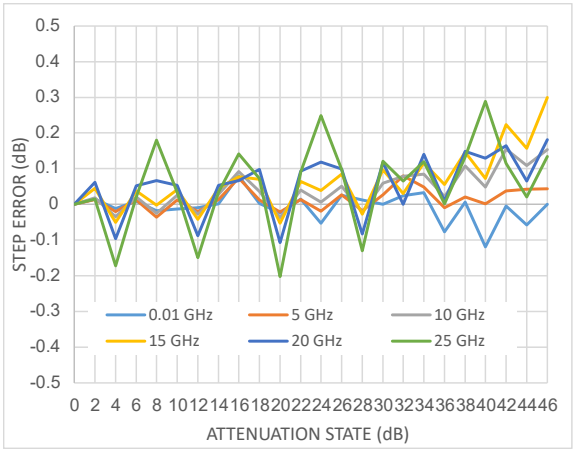

Figure 14. Step Error vs. Attenuation State over Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

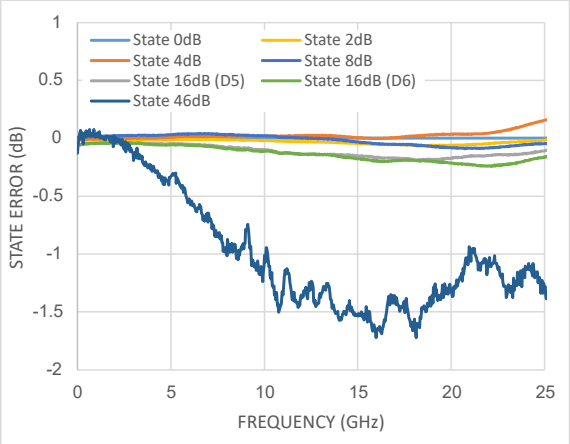

Figure 15. State Error vs. Frequency

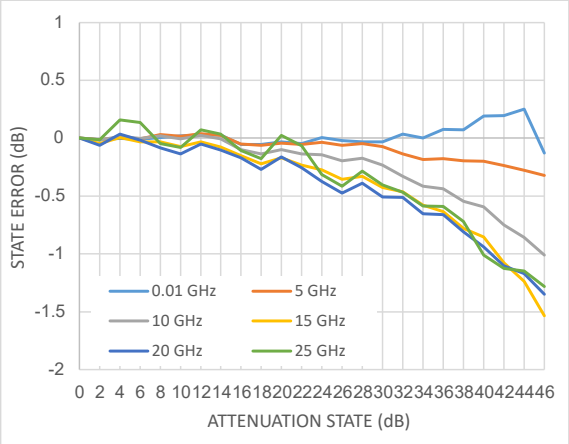

Figure 17. State Error vs. Attenuation State over Frequency

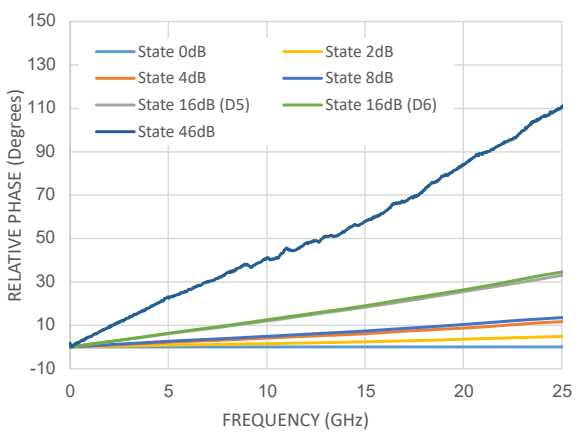

Figure 16. Relative Phase vs. Frequency

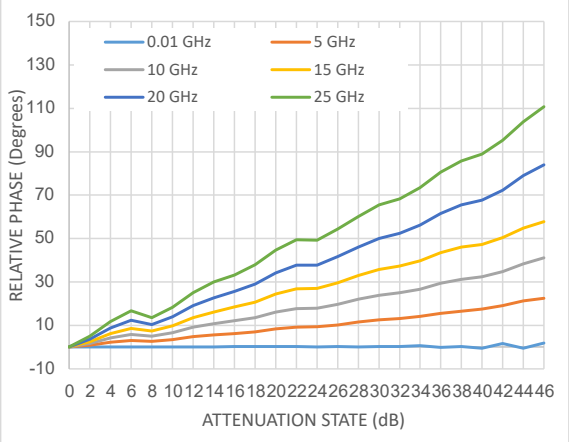

Figure 18. Relative Phase vs. Attenuation State over Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

VDD = 3.3 V, VSS = −3.3 V, V_{CTRL} = 0 V or VDD, T_{CASE} = 25°C, and a 50 Ω system, unless otherwise noted. Measured on the ADRF5700-EVALZ.

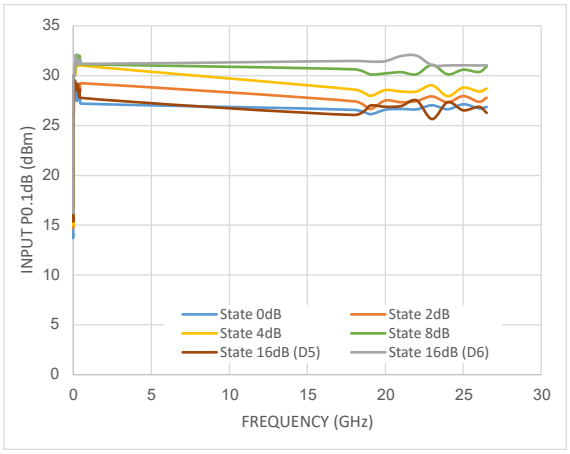

Figure 19. Input P0.1dB vs. Frequency

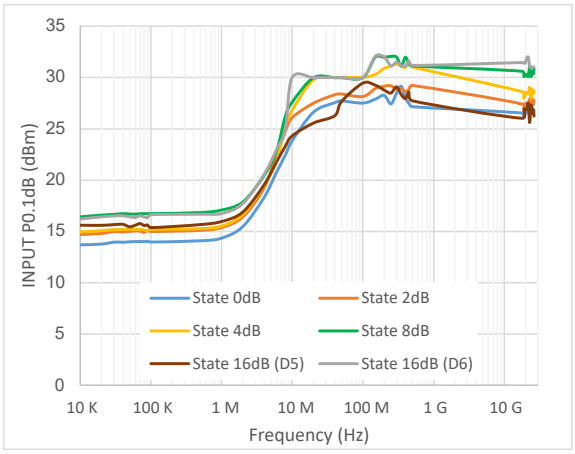

Figure 21. Input P0.1dB vs. Frequency, Low Frequency Detail

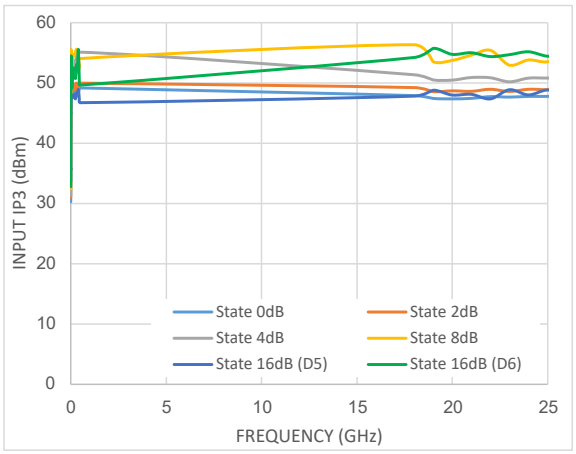

Figure 20. Input IP3 vs. Frequency

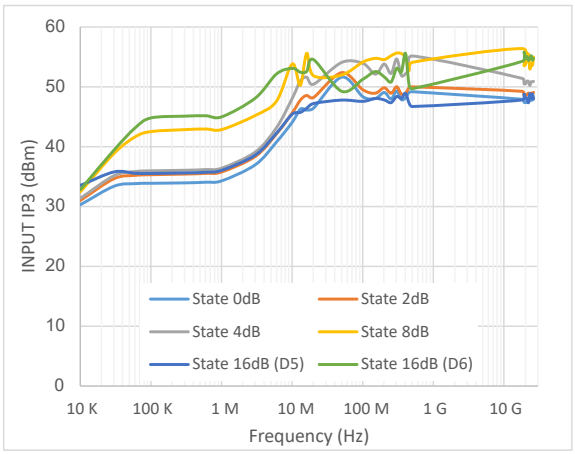

Figure 22. Input IP3 vs. Frequency, Low Frequency Detail

THEORY OF OPERATION

The ADRF5700 incorporates a 5-bit fixed attenuator array that offers an attenuation range of 46 dB in 2 dB steps. An integrated driver provides parallel mode control of the attenuator array.

The ADRF5700 has five digital control inputs, D2 (LSB) to D6 (MSB), to select the desired attenuation state in parallel mode, as shown in Figure 23. Internally, there are two 16 dB stages, and these stages can be controlled by the D5 and D6 pins.

POWER SUPPLY

The ADRF5700 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The power-up sequence is as follows:

1. Connect GND.
2. Power up the VDD and VSS voltages. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Power up the digital control inputs. The order of the digital control inputs is not important. However, powering the digital control inputs before the VDD voltage supply can inadvertently forward bias and damage the internal ESD structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin.
4. Apply an RF input signal to ATTIN or ATTOUT.

The power-down sequence is the reverse order of the power-up sequence.

Power-Up State

The ADRF5700 has an internal pull-up resistor (see Figure 6). The internal pull-up resistor sets the attenuator to the maximum attenuation state (46 dB) when the VDD and VSS voltages are applied if D2 to D6 pins are left floating.

Single-Supply Operation

The ADRF5700 can operate with a single positive supply voltage applied to the VDD pin and VSS pin connected to ground. However, some performance difference can occur in switching characteristics and large signal, see Electrical Specifications for further information.

RF INPUT AND OUTPUT

Both RF ports (ATTIN and ATTOUT) are DC-coupled to 0 V. No DC blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching components are not required.

The ADRF5700 supports bidirectional operation with equal power handling capability. Refer to the RF input power specifications in Table 1.

Table 8. Truth Table

Digital Control Input[1]					
D6[2]	D5[2]	D4	D3	D2	Attenuation State (dB)
Low	Low	Low	Low	Low	0 (reference)
Low	Low	Low	Low	High	2
Low	Low	Low	High	Low	4
Low	Low	High	Low	Low	8
Low	High	Low	Low	Low	16 (D5)
High	Low	Low	Low	Low	16 (D6)
High	High	High	High	High	46

[1] Any combination of the V_{CTRL} input states shown in this table provides an attenuation equal to the sum of the bits selected.

[2] D5 and D6 both correspond to the 16 dB state. D5 has slightly better state accuracy at higher frequencies.

THEORY OF OPERATION

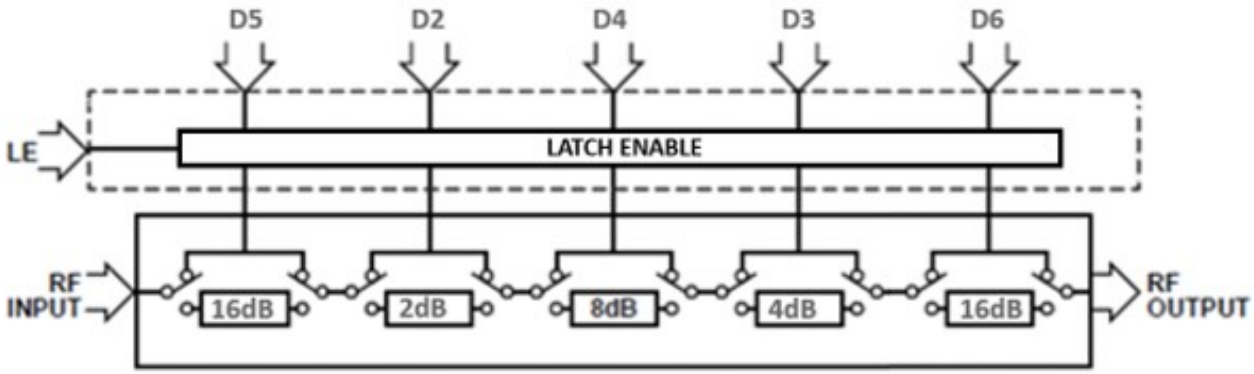

Figure 23. Simplified Circuit Diagram

PARALLEL MODE INTERFACE

The ADRF5700 has five digital control inputs, D2 (LSB) to D6 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 8.

There are two modes of parallel operation: direct and latched.

Direct Parallel Mode

To enable direct parallel mode, keep the LE pin high. To change the attenuation state, use the control voltage inputs (D2 to D6) directly. Direct parallel mode is for manual control of the attenuator.

Latched Parallel Mode

To enable latched parallel mode, the LE pin must be kept low when changing the control voltage inputs (D2 to D6) to set the attenuation state. When the desired state is set, toggle LE high to transfer the 5-bit data to the bypass switches of the attenuator array, and then toggle LE low to latch the change into the device until the next desired attenuation change (see Figure 24 and Timing Specifications for additional information).

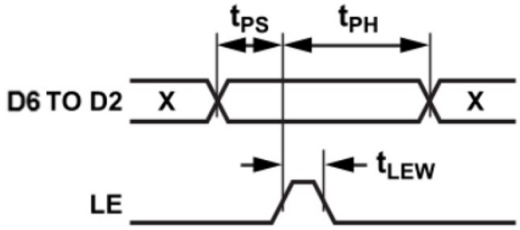

Figure 24. Latched Parallel Mode Timing Diagram

APPLICATIONS INFORMATION

The ADRF5700 has two power supply pins (VDD and VSS) and six control pins (LE, D2, D3, D4, D5, and D6). Figure 25 shows the external components and connections for supply and control pins. The VDD pin and the VSS pin are decoupled with a 100 pF multilayer ceramic capacitor. The device pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RFx pins when the RF lines are biased at a voltage different than 0 V. For more details, see the Pin Configuration and Function Descriptions section.

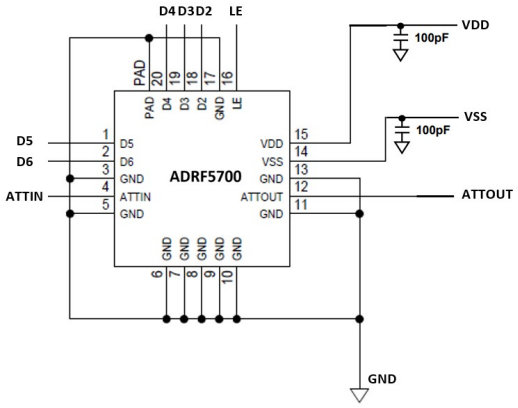

Figure 25. Recommended Schematic

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50 Ω internally, and the pinout is designed to mate a coplanar waveguide (CPWG) with a 50 Ω characteristic impedance on the PCB. Figure 26 shows the referenced CPWG RF trace design for an RF substrate with 12 mil thick Rogers RO4003 dielectric material. The RF trace with a 16 mil width and a 6 mil clearance is recommended for 2.2 mil finished copper thickness.

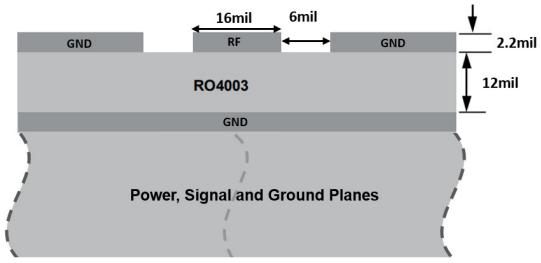

Figure 26. Example PCB Stackup

Figure 27 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with as many filled through vias as allowed for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

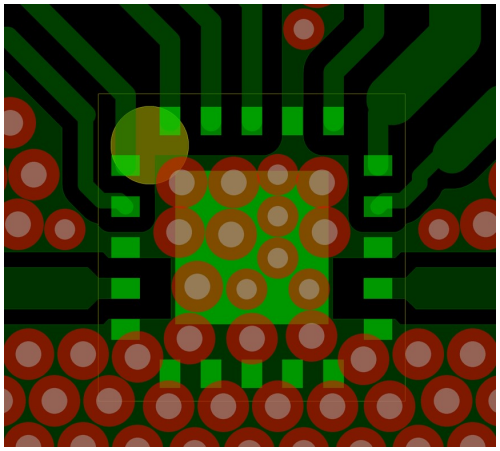

Figure 27. PCB Routings

Figure 28 shows the recommended layout from the device RFx pins to the 50 Ω CPWG on the referenced stackup. PCB pads are drawn 1:1 to device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width till the package edge and tapered to the RF trace with a 45° angle. The paste mask is also designed to match the pad without any aperture reduction and is divided into multiple openings for the paddle.

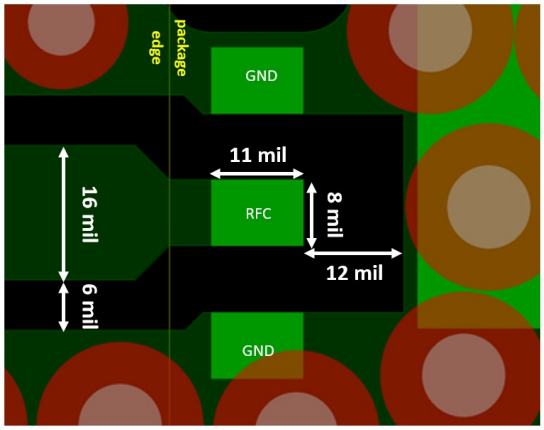

Figure 28. Recommended RF Pin Transitions

For alternate PCB stackups with different dielectric thickness and CPWG design, contact Technical Support for further recommendations for further information.