100 MHz to 2400 MHz I/Q Modulator with Integrated Fractional-N PLL and VCO

Data Sheet

ADRF6755

FEATURES

I/Q modulator with integrated fractional-N PLL and VCO
Gain control span: 47 dB in 1 dB steps
Output frequency range: 100 MHz to 2400 MHz
Output 1 dB compression: 8 dBm at LO = 1800 MHz
Output IP3: 20.5 dBm at LO = 1800 MHz
Noise floor: −161 dBm/Hz at LO = 1800 MHz
Baseband modulation bandwidth: 600 MHz (3 dB)
Output frequency resolution: 1 Hz
SPI and I²C-compatible serial interfaces
Power supply: 5 V/380 mA

GENERAL DESCRIPTION

The ADRF6755 is a highly integrated quadrature modulator, frequency synthesizer, and programmable attenuator. The device covers an operating frequency range from 100 MHz to 2400 MHz for use in satellite, cellular, and broadband communications.

The ADRF6755 modulator includes a high modulus, fractional-N frequency synthesizer with integrated VCO, providing less than 1 Hz frequency resolution, and a 47 dB digitally controlled output attenuator with 1 dB steps.

Control of all the on-chip registers is through a user-selected SPI interface or I²C interface. The device operates from a single power supply ranging from 4.75 V to 5.25 V.

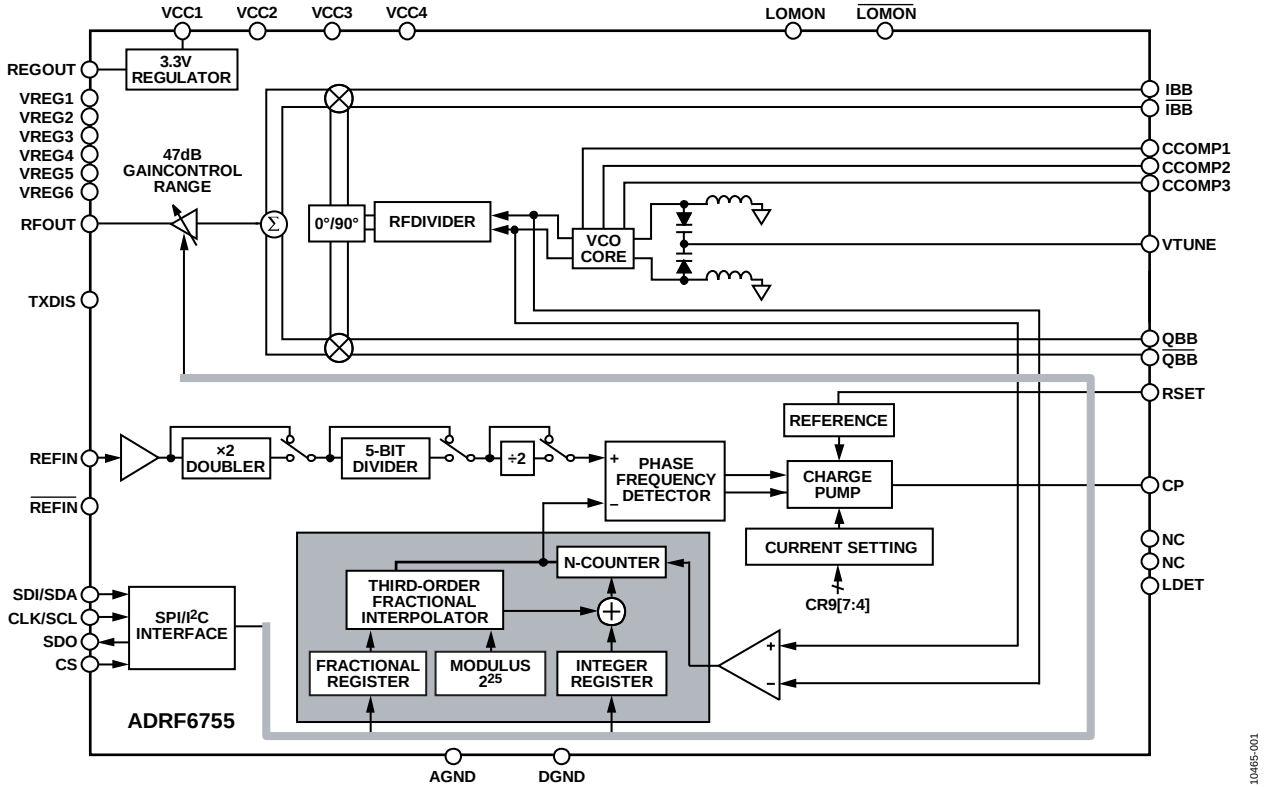

Figure 1.

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7/12—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 5 V ± 5%, operating temperature range = −40°C to +85°C, I/Q inputs = 0.9 V p-p differential sine waves in quadrature on a 500 mV dc bias, REFIN = 80 MHz, PFD = 40 MHz, baseband frequency = 1 MHz, LOMON off, loop bandwidth (LBW) = 100 kHz, I_{CP} = 5 mA, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING FREQUENCY RANGE		100		2400	MHz
RF OUTPUT = 100 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		−0.2		dBm
Gain Flatness	Any 40 MHz		±2.0		dB
Output P1dB			9.0		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		21.0		dBm
Output Return Loss	Attenuator setting = 0 dB		−12		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−55		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−80		dBm
Sideband Suppression			−70		dBc
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−153		dBm/Hz
Baseband Harmonics			−60		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−85		dBc
	>10 MHz offset from carrier		−90		dBc
Phase Noise	100 Hz offset		−106		dBc/Hz
	1 kHz offset		−116		dBc/Hz
	10 kHz offset		−127		dBc/Hz
	100 kHz offset		−131		dBc/Hz
	1 MHz offset		−146		dBc/Hz
	10 MHz offset		−152		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.02		° rms
RF OUTPUT = 300 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		0.2		dBm
Gain Flatness	Any 40 MHz		±0.5		dB
Output P1dB			9.3		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		23.0		dBm
Output Return Loss	Attenuator setting = 0 dB		−20		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−50		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−75		dBm
Sideband Suppression			−70		dBc
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−158		dBm/Hz
Baseband Harmonics			−60		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−85		dBc
	>10 MHz offset from carrier		−85		dBc
Phase Noise	100 Hz offset		−105		dBc/Hz
	1 kHz offset		−113		dBc/Hz
	10 kHz offset		−117		dBc/Hz
	100 kHz offset		−122		dBc/Hz
	1 MHz offset		−145		dBc/Hz
	10 MHz offset		−150		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.04		° rms

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF OUTPUT = 700 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		0.2		dBm
Gain Flatness	Any 40 MHz		±0.5		dB
Output P1dB			9.4		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		23.0		dBm
Output Return Loss	Attenuator setting = 0 dB		−16		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−48		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−70		dBm
Sideband Suppression			−70		dBc
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−158		dBm/Hz
Baseband Harmonics			−60		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−60		dBc
	>10 MHz offset from carrier		−85		dBc
Phase Noise	100 Hz offset		−97		dBc/Hz
	1 kHz offset		−106		dBc/Hz
	10 kHz offset		−112		dBc/Hz
	100 kHz offset		−115		dBc/Hz
	1 MHz offset		−139		dBc/Hz
	10 MHz offset		−154		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.07		° rms
RF OUTPUT = 900 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		0.0		dBm
Gain Flatness	Any 40 MHz		±0.5		dB
Output P1dB			9.2		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		22.8		dBm
Output Return Loss	Attenuator setting = 0 dB		−15		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−48		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−68		dBm
Sideband Suppression			−60		dBc
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−158.5		dBm/Hz
	Attenuator setting = 0 dB to 21 dB, carrier offset = 10 MHz		−152		dBc/Hz
	Attenuator setting = 21 dB to 47 dB, carrier offset = 10 MHz		−171		dBm/Hz
Baseband Harmonics			−60		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−60		dBc
	>10 MHz offset from carrier		−80		dBc
Phase Noise	100 Hz offset		−94		dBc/Hz
	1 kHz offset		−104		dBc/Hz
	10 kHz offset		−109		dBc/Hz
	100 kHz offset		−114		dBc/Hz
	1 MHz offset		−139		dBc/Hz
	10 MHz offset		−154		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.11		° rms
RF OUTPUT = 1800 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		−0.4		dBm
Gain Flatness	Any 40 MHz		±0.5		dB
Output P1dB			8.0		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		20.5		dBm
Output Return Loss	Attenuator setting = 0 dB		−13		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−45		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−53		dBm
Sideband Suppression			−45		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−161		dBm/Hz
	Attenuator setting = 0 dB to 21 dB, carrier offset = 10 MHz		−150		dBc/Hz
	Attenuator setting = 21 dB to 47 dB, carrier offset = 10 MHz		−170		dBm/Hz
Baseband Harmonics			−58		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−60		dBc
	>10 MHz offset from carrier		−75		dBc
Phase Noise	100 Hz offset		−89		dBc/Hz
	1 kHz offset		−99		dBc/Hz
	10 kHz offset		−103		dBc/Hz
	100 kHz offset		−108		dBc/Hz
	1 MHz offset		−133		dBc/Hz
	10 MHz offset		−152		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.17		° rms
RF OUTPUT = 1875 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		−0.6		dBm
Gain Flatness	Any 40 MHz		±0.5		dB
Output P1dB			7.8		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		20.2		dBm
Output Return Loss	Attenuator setting = 0 dB		−13		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−45		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−52		dBm
Sideband Suppression			−50		dBc
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−160		dBm/Hz
	Attenuator setting = 0 dB to 21 dB, carrier offset = 10 MHz		−150		dBc/Hz
	Attenuator setting = 21 dB to 47 dB, carrier offset = 10 MHz		−170		dBm/Hz
Baseband Harmonics			−60		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−60		dBc
	>10 MHz offset from carrier		−73		dBc
Phase Noise	100 Hz offset		−89		dBc/Hz
	1 kHz offset		−97		dBc/Hz
	10 kHz offset		−103		dBc/Hz
	100 kHz offset		−108		dBc/Hz
	1 MHz offset		−133		dBc/Hz
	10 MHz offset		−152		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.18		° rms
RF OUTPUT = 2100 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		−1.0		dBm
Gain Flatness	Any 40 MHz		±0.5		dB
Output P1dB			7.4		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		19.5		dBm
Output Return Loss	Attenuator setting = 0 dB		−12		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−44		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−51		dBm
Sideband Suppression			−45		dBc
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−161		dBm/Hz
	Attenuator setting = 0 dB to 21 dB, carrier offset = 10 MHz		−149		dBc/Hz
	Attenuator setting = 21 dB to 47 dB, carrier offset = 10 MHz		−170		dBm/Hz
Baseband Harmonics			−60		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−60		dBc
	>10 MHz offset from carrier		−67		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Phase Noise	100 Hz offset		−88		dBc/Hz
	1 kHz offset		−98		dBc/Hz
	10 kHz offset		−101		dBc/Hz
	100 kHz offset		−108		dBc/Hz
	1 MHz offset		−134		dBc/Hz
	10 MHz offset		−152		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.25		° rms
RF OUTPUT = 2400 MHz	RFOUT pin				
Nominal Output Power	V_{IQ} = 0.9 V p-p differential		−1.7		dBm
Gain Flatness	Any 40 MHz		±0.5		dB
Output P1dB			6.5		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −6 dBm per tone		18.5		dBm
Output Return Loss	Attenuator setting = 0 dB		−11		dB
LO Carrier Feedthrough[1]	Attenuator setting = 0 dB to 47 dB		−43		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		−60		dBm
Sideband Suppression			−40		dBc
Noise Floor	I/Q inputs = 0 V p-p differential, attenuator setting = 0 dB		−160.5		dBm/Hz
	Attenuator setting = 0 dB to 21 dB, carrier offset = 10 MHz		−148		dBc/Hz
	Attenuator setting = 21 dB to 47 dB, carrier offset = 10 MHz		−170		dBm/Hz
Baseband Harmonics			−55		dBc
Synthesizer Spurs	Integer boundary < loop bandwidth		−55		dBc
	>10 MHz offset from carrier		−64		dBc
Phase Noise	100 Hz offset		−85		dBc/Hz
	1 kHz offset		−96		dBc/Hz
	10 kHz offset		−100		dBc/Hz
	100 kHz offset		−107		dBc/Hz
	1 MHz offset		−132		dBc/Hz
	10 MHz offset		−152		dBc/Hz
Integrated Phase Noise	1 kHz to 8 MHz integration bandwidth		0.25		° rms
REFERENCE CHARACTERISTICS	REFIN pin				
Input Frequency	With reference divide-by-2 enabled	10		300	MHz
	With reference divide-by-2 disabled	10		165	MHz
	With reference doubler enabled	10		80	MHz
Input Sensitivity	AC-coupled	0.4		VREG	V p-p
Input Capacitance				10	pF
Input Current				±100	µA
CHARGE PUMP					
I_{CP} Sink/Source	Programmable, RSET = 4.7 kΩ				
High Value			5		mA
Low Value			312.5		µA
Absolute Accuracy			4.0		%
VCO					
Gain	K_{VCO}		25		MHz/V
SYNTHESIZER	LO = 100 MHz to 2400 MHz				
Frequency Resolution				1	Hz
Frequency Settling	Any step size, maximum frequency error = 100 Hz		0.17		ms
Maximum Frequency Step for No Autocalibration	Frequency step with no autocalibration routine; Register CR24, Bit 0 = 1			$100/2^{RFDIV}$	kHz
Phase Detector Frequency		10		40	MHz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GAIN CONTROL					
Gain Range			47		dB
Step Size			1		dB
Relative Step Accuracy	Fixed frequency, adjacent steps, all attenuation steps, LO > 300 MHz[2]		±0.3		dB
	Over full frequency range, adjacent steps, all attenuation steps, LO > 300 MHz[3]		±1.5		dB
Absolute Step Accuracy[4]	47 dB attenuation step, LO > 300 MHz[5]		−2.0		dB
Output Settling Time	Any step; output power settled to ±0.2 dB		15		µs
OUTPUT DISABLE	TXDIS pin				
Off Isolation	RFOUT, attenuator setting = 0 dB to 47 dB, TXDIS high		−100		dBm
	LO, attenuator setting = 0 dB to 47 dB, TXDIS high		−75		dBm
	2× LO, attenuator setting = 0 dB to 47 dB, TXDIS high		−50		dBm
Turn-On Settling Time	TXDIS high to low: output power to 90% of envelope		180		ns
	Frequency settling to 100 Hz		20		µs
Turn-Off Settling Time	TXDIS low to high (to −55 dBm)		350		ns
MONITOR OUTPUT	LOMON, $\overline{\text{LOMON}}$ pins				
Nominal Output Power			−24		dBm
BASEBAND INPUTS	IBB, $\overline{\text{IBB}}$, QBB, $\overline{\text{QBB}}$ pins				
I and Q Input Bias Level			500		mV
3 dB Bandwidth			600		MHz
LOGIC INPUTS					
Input High Voltage, V_{INH}	CS, TXDIS pins	1.4			V
Input Low Voltage, V_{INL}	CS, TXDIS pins			0.6	V
Input High Voltage, V_{INH}	SDI/SDA, CLK/SCL pins	2.1			V
Input Low Voltage, V_{INL}	SDI/SDA, CLK/SCL pins			1.1	V
Input Current, I_{INH}/I_{INL}	CS, TXDIS, SDI/SDA, CLK/SCL pins			±1	µA
Input Capacitance, C_{IN}	CS, TXDIS, SDI/SDA, CLK/SCL pins			10	pF
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	SDO, LDET pins; I_{OH} = 500 µA	2.8			V
Output Low Voltage, V_{OL}	SDO, LDET pins; I_{OL} = 500 µA			0.4	V
	SDA (SDI/SDA); I_{OL} = 3 mA			0.4	V
POWER SUPPLIES	VCC1, VCC2, VCC3, VCC4, VREG1, VREG2, VREG3, VREG4, VREG5, VREG6, and REGOUT pins; REGOUT normally connected to VREG1, VREG2, VREG3, VREG4, VREG5, and VREG6				
Voltage Range	VCC1, VCC2, VCC3, and VCC4	4.75	5	5.25	V
	REGOUT, VREG1, VREG2, VREG3, VREG4, VREG5, and VREG6		3.3		V
Supply Current	VCC1, VCC2, VCC3, and VCC4 combined; REGOUT connected to VREG1, VREG2, VREG3, VREG4, VREG5, and VREG6		380	420	mA
Power-Down Current	CR29[0] = 0, power down modulator, CR12[2] = 1, power down PLL, CR28[4] = 1, power down RFDIVIDER, CR27[2] = 0, power down LOMON		7		mA
Operating Temperature		−40		+85	°C

[1] LO carrier feedthrough is expressed in dBc relative to the RF output power changing as the attenuator is stepped. LO carrier feedthrough is constant as the RF output is altered due to a change in the I/Q input amplitude.
[2] For relative step accuracy at LO < 300 MHz, refer to Figure 37.
[3] For relative step accuracy over frequency range at LO < 300 MHz, refer to Figure 39.
[4] All other attenuation steps have an absolute error of <±2.0 dB.
[5] For absolute step accuracy at LO < 300 MHz, refer to Figure 40.

TIMING CHARACTERISTICS

I²C Interface Timing

Table 2.

Parameter[1]	Symbol	Limit	Unit
SCL Clock Frequency	f_{SCL}	400	kHz max
SCL Pulse Width High	t_{HIGH}	600	ns min
SCL Pulse Width Low	t_{LOW}	1300	ns min
Start Condition Hold Time	$t_{HD;STA}$	600	ns min
Start Condition Setup Time	$t_{SU;STA}$	600	ns min
Data Setup Time	$t_{SU;DAT}$	100	ns min
Data Hold Time	$t_{HD;DAT}$	300	ns min
Stop Condition Setup Time	$t_{SU;STO}$	600	ns min
Data Valid Time	$t_{VD;DAT}$	900	ns max
Data Valid Acknowledge Time	$t_{VD;ACK}$	900	ns max
Bus Free Time	t_{BUF}	1300	ns min

[1] See Figure 2.

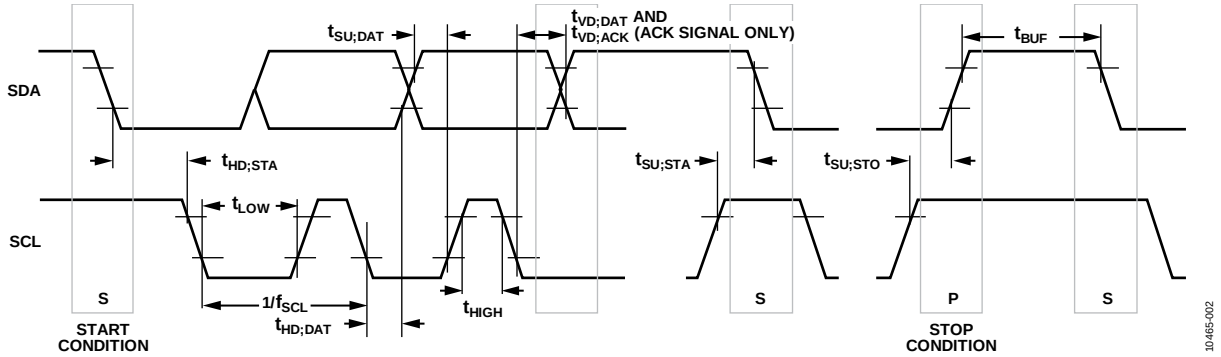

Figure 2. I²C Port Timing Diagram

SPI Interface Timing

Table 3.

Parameter[1]	Symbol	Limit	Unit
CLK Frequency	f_{CLK}	20	MHz max
CLK Pulse Width High	t_1	15	ns min
CLK Pulse Width Low	t_2	15	ns min
Start Condition Hold Time	t_3	5	ns min
Data Setup Time	t_4	10	ns min
Data Hold Time	t_5	5	ns min
Stop Condition Setup Time	t_6	5	ns min
SDO Access Time	t_7	15	ns min
CS to SDO High Impedance	t_8	25	ns max

[1] See Figure 3.

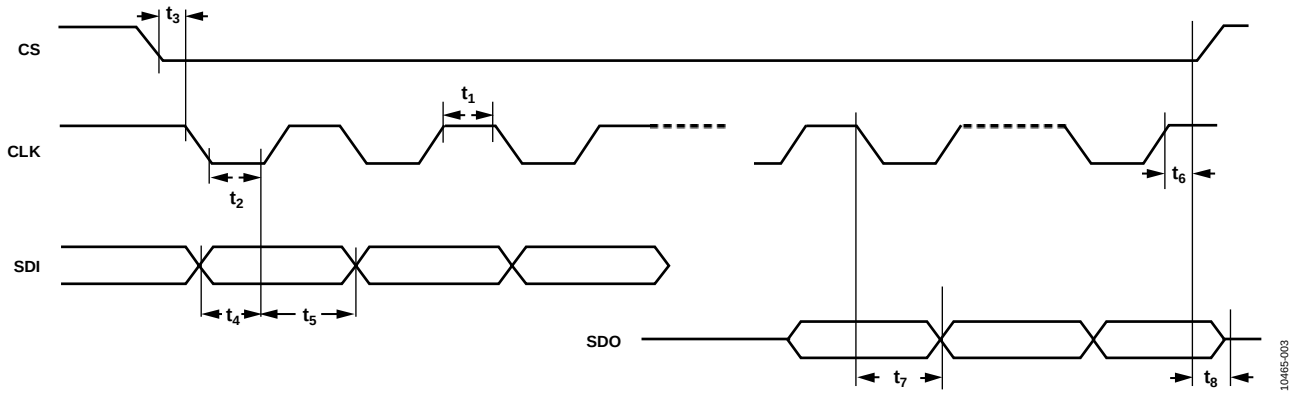

Figure 3. SPI Port Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VCC1, VCC2, VCC3, and VCC4 Supply Voltage	−0.3 V to +6 V
VREG1, VREG2, VREG3, VREG4, VREG5, and VREG6 Supply Voltage	−0.3 V to +4 V
IBB, $\overline{\text{IBB}}$, QBB, and $\overline{\text{QBB}}$	0 V to 2.5 V
Digital I/O	−0.3 V to +4 V
Analog I/O (Other Than IBB, $\overline{\text{IBB}}$, QBB, and $\overline{\text{QBB}}$)	−0.3 V to +4 V
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

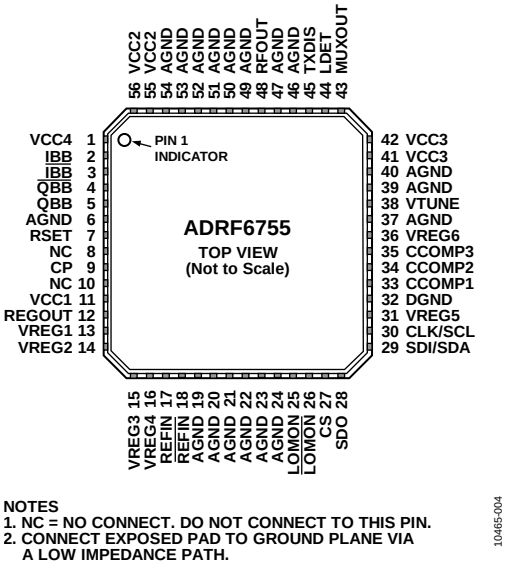

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
11, 55, 56, 41, 42, 1	VCC1 to VCC4	Positive Power Supplies for I/Q Modulator. Apply a 5 V power supply to VCC1, which should be decoupled with power supply decoupling capacitors. Connect VCC2, VCC3, and VCC4 to the same 5 V power supply.
12	REGOUT	3.3 V Output Supply. Drives VREG1, VREG2, VREG3, VREG4, VREG5, and VREG6.
13, 14, 15, 16, 31, 36	VREG1 to VREG6	Positive Power Supplies for PLL Synthesizer, VCO, and Serial Port. Connect these pins to REGOUT (3.3 V) and decouple them separately.
6, 19, 20, 21, 22, 23, 24, 37, 39, 40, 46, 47, 49, 50, 51, 52, 53, 54	AGND	Analog Ground. Connect to a low impedance ground plane.
32	DGND	Digital Ground. Connect to the same low impedance ground plane as the AGND pins.
2, 3	IBB, $\overline{\text{IBB}}$	Differential In-Phase Baseband Inputs. These high impedance inputs must be dc biased to approximately 500 mV dc and should be driven from a low impedance source. Nominal characterized ac signal swing is 450 mV p-p on each pin. These inputs are not self-biased and must be externally biased.
4, 5	$\overline{\text{QBB}}$, QBB	Differential Quadrature Baseband Inputs. These high impedance inputs must be dc-biased to approximately 500 mV dc and should be driven from a low impedance source. Nominal characterized ac signal swing is 450 mV p-p on each pin. These inputs are not self-biased and must be externally biased.
33, 34, 35	CCOMP1 to CCOMP3	Internal Compensation Nodes. These pins must be decoupled to ground with a 100 nF capacitor.
38	VTUNE	Control Input to the VCO. This voltage determines the output frequency and is derived from filtering the CP output voltage.
7	RSET	Charge Pump Current Set. Connecting a resistor between this pin and ground sets the maximum charge pump output current. The relationship between I_{CP} and R_{SET} is as follows: $I_{CPmax} = \frac{23.5}{R_{SET}}$ where R_{SET} = 4.7 kΩ and $I_{CP\,max}$ = 5 mA.
9	CP	Charge Pump Output. When enabled, this output provides ±I_{CP} to the external loop filter, which, in turn, drives the internal VCO.
27	CS	Chip Select, CMOS Input. When CS is high, the data stored in the shift registers is loaded into one of 31 latches. In I^2C mode, when CS is high, the slave address of the device is 0x60, and, when CS is low, the slave address is 0x40.

Pin No.	Mnemonic	Description
29	SDI/SDA	Serial Data Input for SPI Port/Serial Data Input/Output for I²C Port. In SPI mode, this pin is a high impedance CMOS data input, and data is loaded in an 8-bit word. In I²C mode, this pin is a bidirectional port.
30	CLK/SCL	Serial Clock Input for SPI/I²C Port. This serial clock is used to clock in the serial data to the registers. This input is a high impedance CMOS input.
28	SDO	Serial Data Output for SPI Port. Register states can be read back on the SDO data output line.
17	REFIN	Reference Input. This high impedance CMOS input should be ac-coupled.
18	$\overline{\text{REFIN}}$	Reference Input Bar. This pin should be either grounded or ac-coupled to ground.
48	RFOUT	RF Output. Single-ended, 50 Ω, internally biased RF output. This pin must be ac-coupled to the load.
45	TXDIS	Output Disable. This pin can be used to disable the RF output. Connect to a high logic level to disable the output. Connect to a low logic level for normal operation.
25, 26	LOMON, $\overline{\text{LOMON}}$	Differential Monitor Outputs. These pins provide a replica of the internal local oscillator frequency (1× LO) at four different power levels: −6 dBm, −12 dBm, −18 dBm, and −24 dBm, approximately. These open-collector outputs must be terminated with external resistors to REGOUT. These outputs can be disabled through serial port programming and should be tied to REGOUT if not used.
8, 10	NC	No Connect. Do not connect to these pins.
44	LDET	Lock Detect. This output pin indicates the state of the PLL: a high level indicates a locked condition, whereas a low level indicates a loss of lock condition.
43	MUXOUT	Mux Output. This pin is a test output for diagnostic use only. Do not connect to this pin.
Exposed Paddle	EP	Exposed Paddle. Connect to ground plane via a low impedance path.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5 V ± 5%, operating temperature range = −40°C to +85°C, I/Q inputs = 0.9 V p-p differential sine waves in quadrature on a 500 mV dc bias, REFIN = 80 MHz, PFD = 40 MHz, baseband frequency = 1 MHz, LOMON is off, loop bandwidth (LBW) = 100 kHz, I_{CP} = 5 mA, unless otherwise noted. A nominal condition is defined as 25°C, 5.00 V, and an LO frequency of 1800 MHz. A worst-case condition is defined as having the worst-case temperature, supply voltage, and LO frequency.

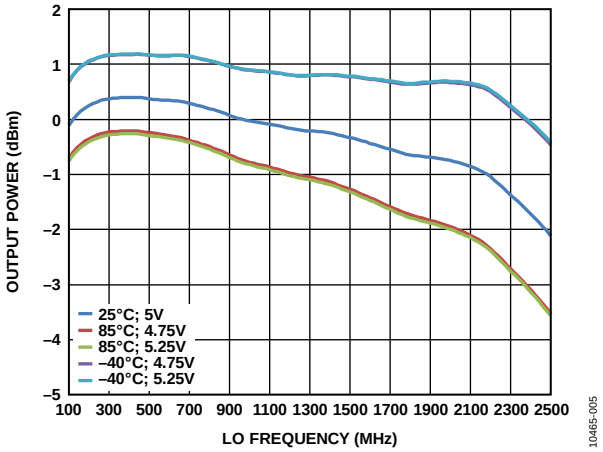

Figure 5. Output Power vs. LO Frequency, Supply, and Temperature

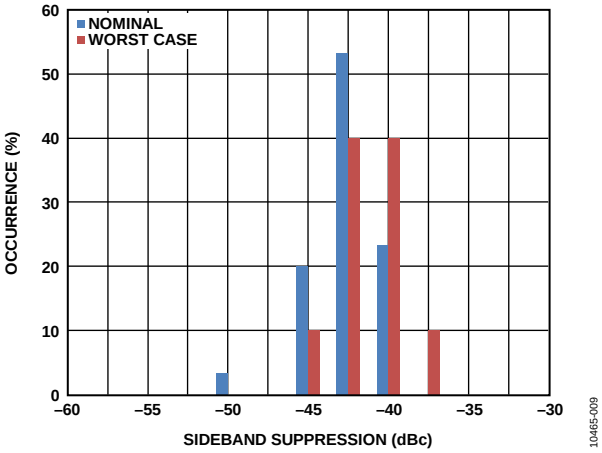

Figure 8. Sideband Suppression Distribution at Nominal and Worst-Case Conditions

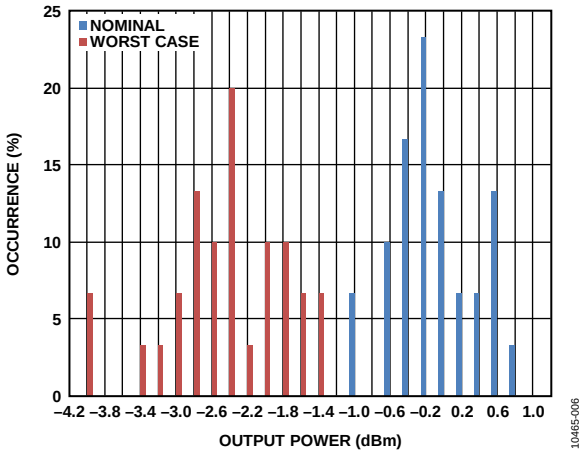

Figure 6. Output Power Distribution at Nominal and Worst-Case Conditions

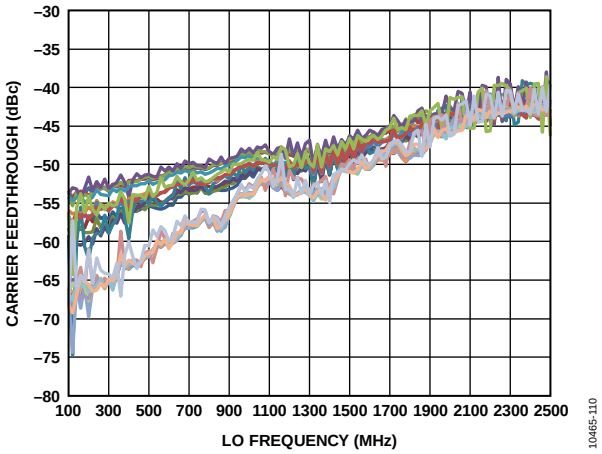

Figure 9. LO Carrier Feedthrough vs. LO Frequency, Attenuation, Supply, and Temperature

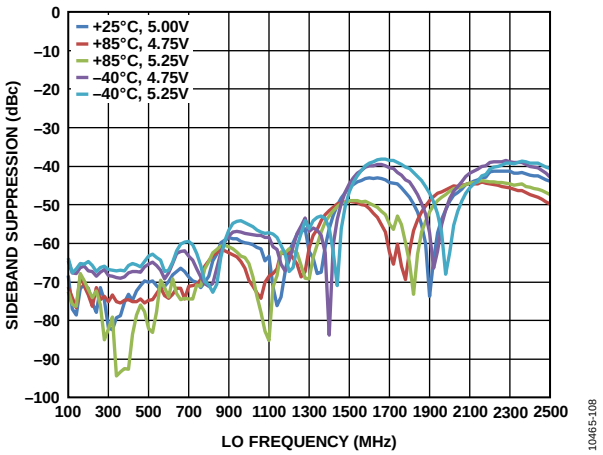

Figure 7. Sideband Suppression vs. LO Frequency, Supply, and Temperature

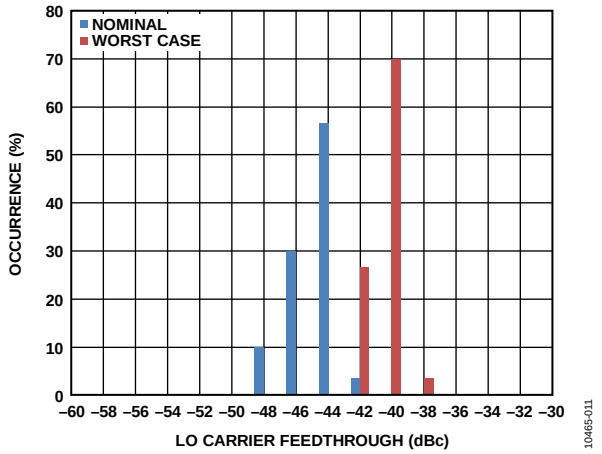

Figure 10. LO Carrier Feedthrough Distribution at Nominal and Worst-Case Conditions and Attenuation Setting

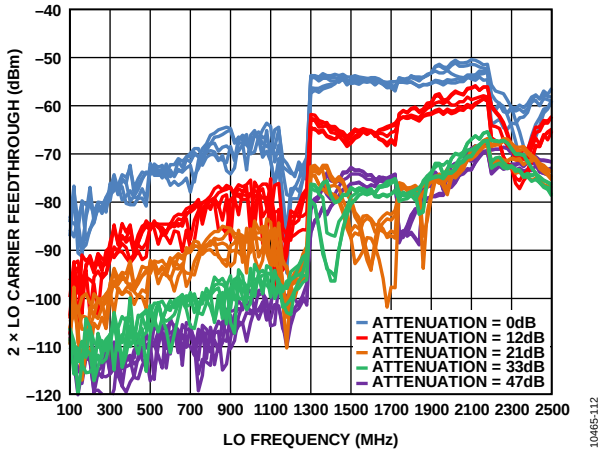

Figure 11. 2× LO Carrier Feedthrough vs. LO Frequency, Attenuation, Supply, and Temperature

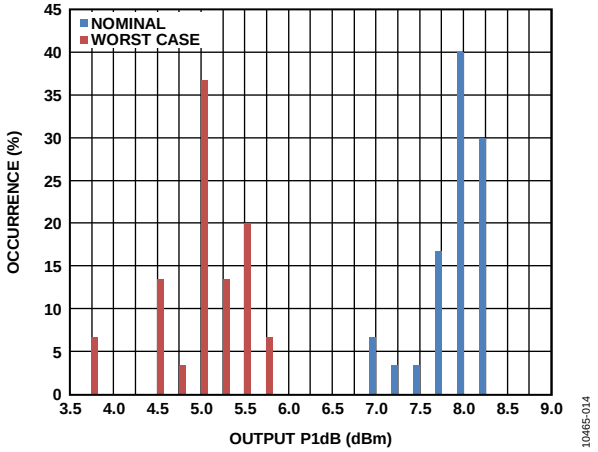

Figure 14. Output P1dB Compression Point Distribution at Nominal and Worst-Case Conditions

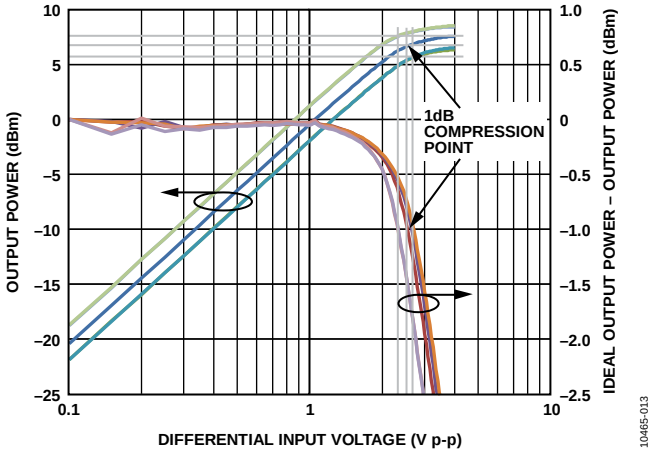

Figure 12. Output P1dB Compression Point at Worst-Case LO Frequency vs. Supply and Temperature

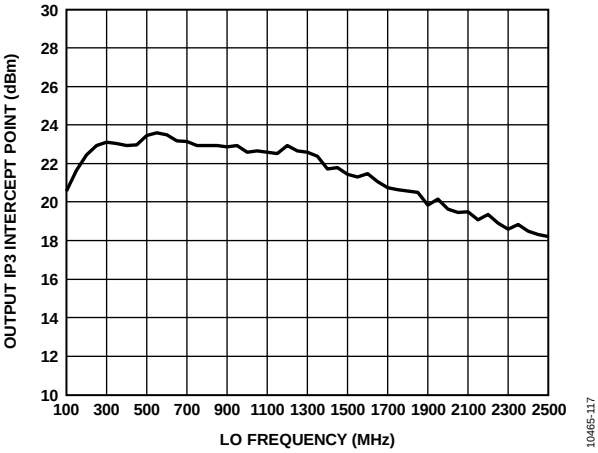

Figure 15. Output IP3 vs. LO Frequency at Nominal Conditions

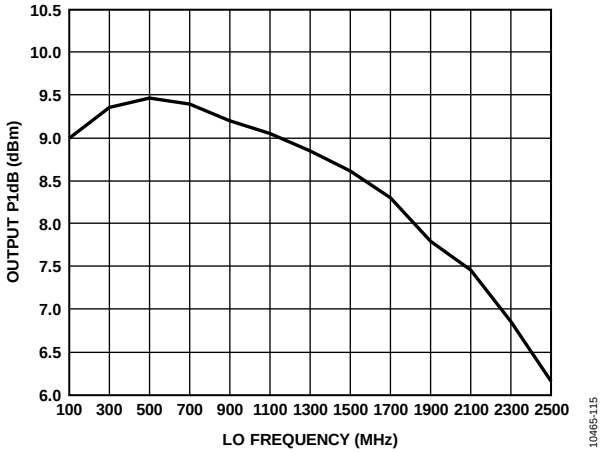

Figure 13. Output P1dB Compression Point vs. LO Frequency at Nominal Conditions

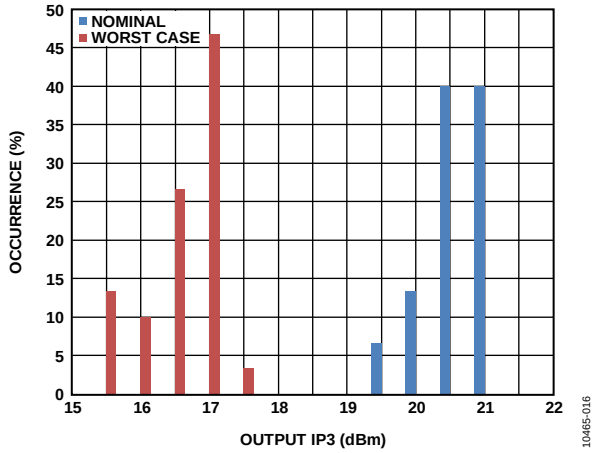

Figure 16. Output IP3 Distribution at Nominal and Worst-Case Conditions

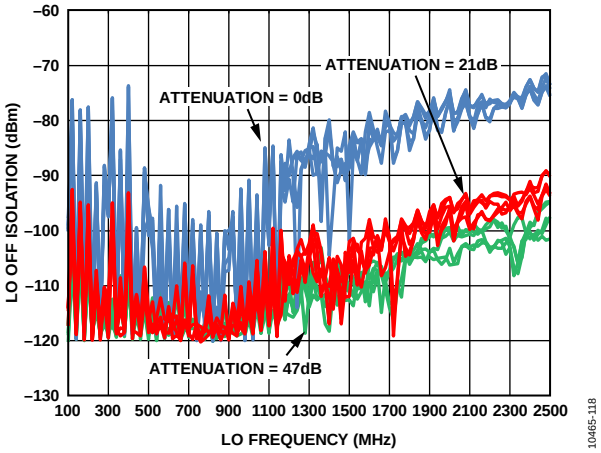

Figure 17. LO Off Isolation vs. LO Frequency, Attenuation, Supply, and Temperature

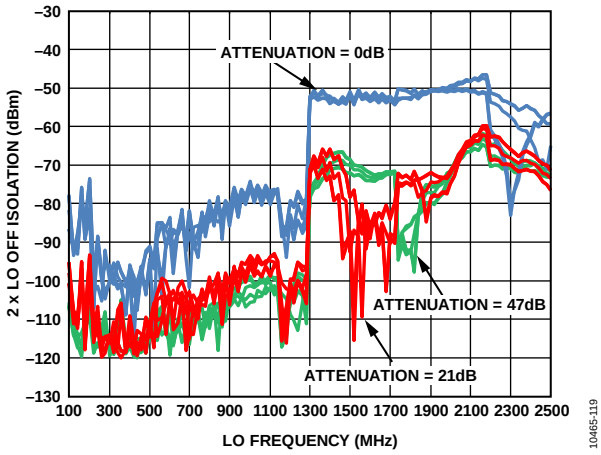

Figure 18. 2 × LO Off Isolation vs. LO Frequency, Attenuation, Supply, and Temperature

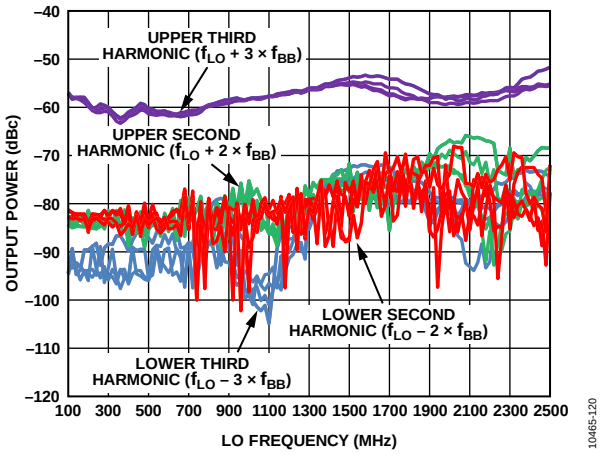

Figure 19. Second-Order and Third-Order Harmonic Distortion vs. LO Frequency, Supply, and Temperature

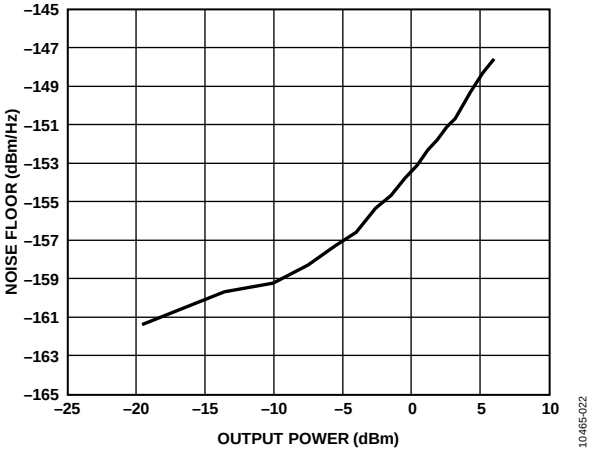

Figure 20. Noise Floor at 0 dB Attenuation vs. Output Power at Nominal Conditions

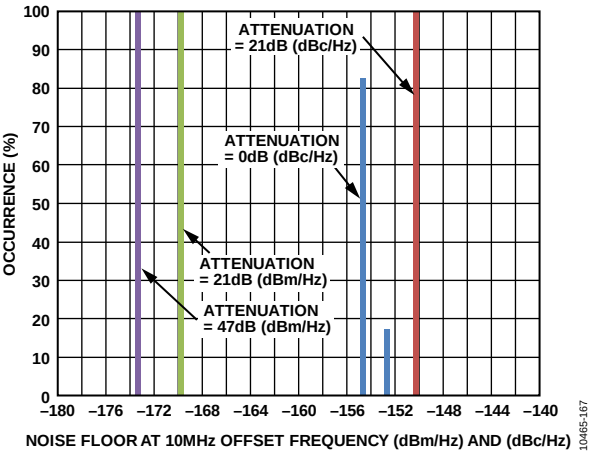

Figure 21. Noise Floor at 10 MHz Offset Frequency Distribution at Worst-Case Conditions and Different Attenuation Settings

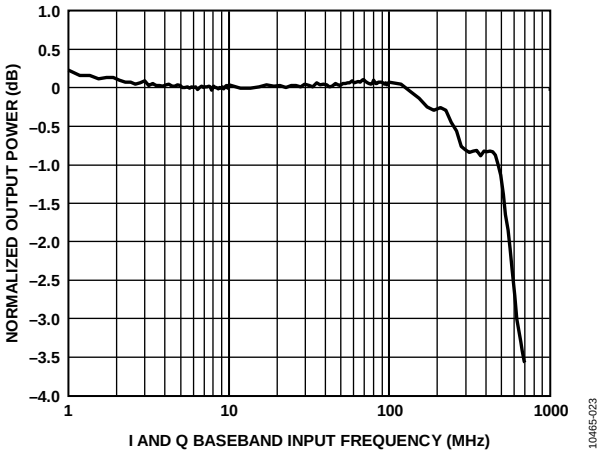

Figure 22. Normalized I and Q Input Bandwidth

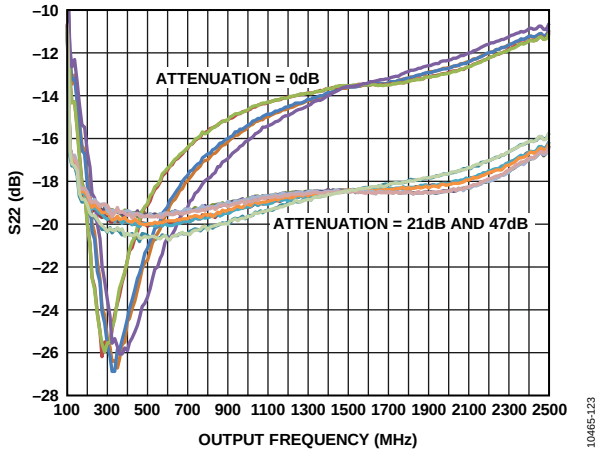

Figure 23. Output Return Loss at Different Attenuation Settings vs. Output Frequency, Supply, and Temperature

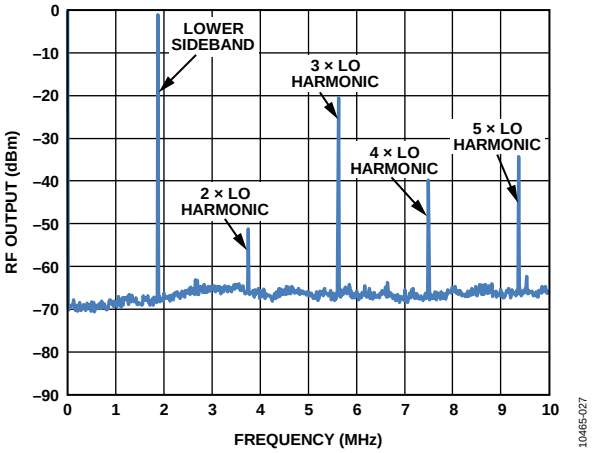

Figure 26. RF Output Spectral Plot over a Wide Span

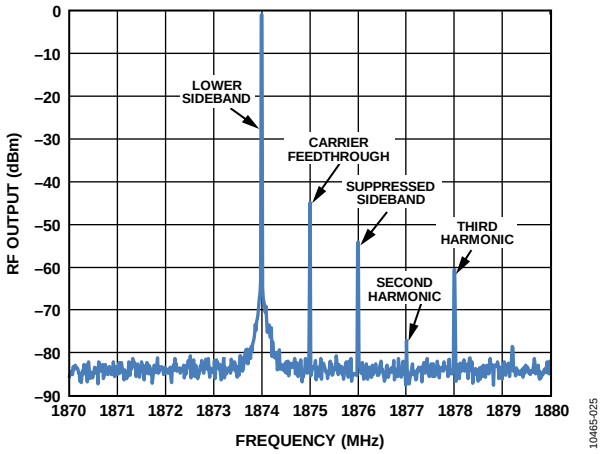

Figure 24. RF Output Spectral Plot over a 10 MHz Span

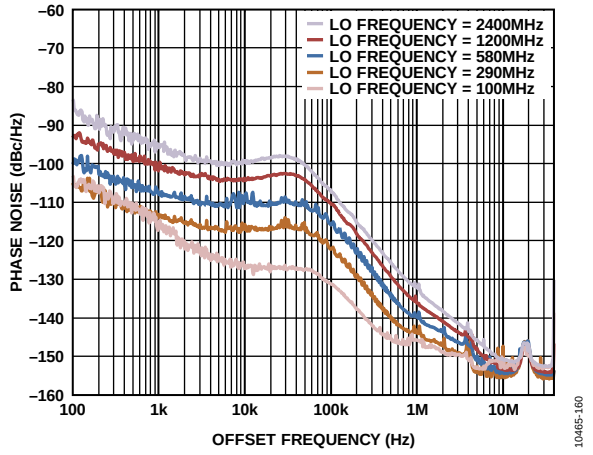

Figure 27. Phase Noise Performance vs. LO Frequency, Nominal Conditions

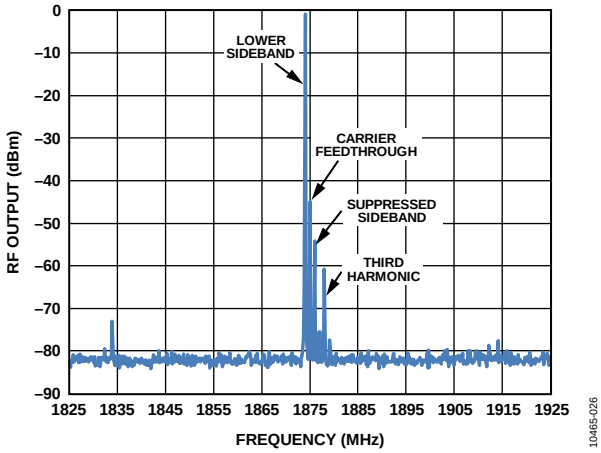

Figure 25. RF Output Spectral Plot over a 100 MHz Span

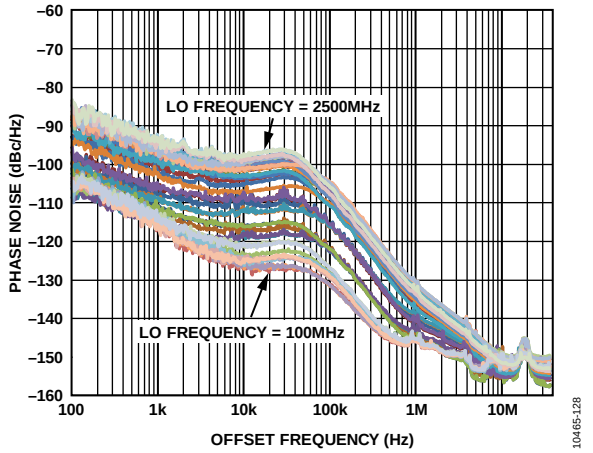

Figure 28. Phase Noise Performance vs. LO Frequency, Supply, and Temperature

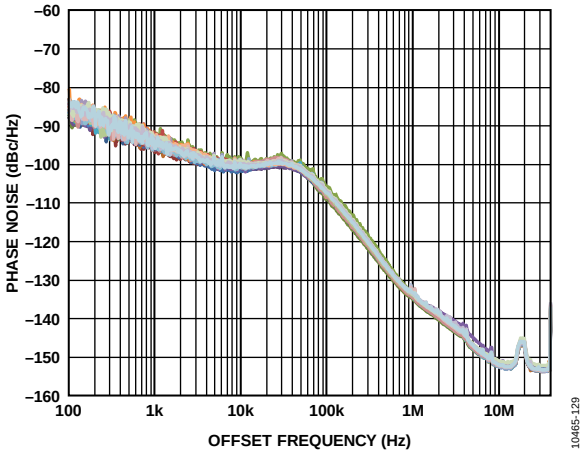

Figure 29. Phase Noise Performance Distribution at Worst-Case Conditions

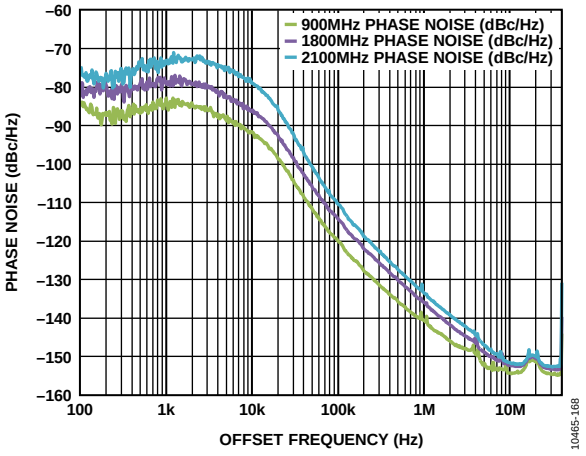

Figure 32. Phase Noise Performance vs. LO Frequency, Nominal Conditions with Narrow Loop Bandwidth

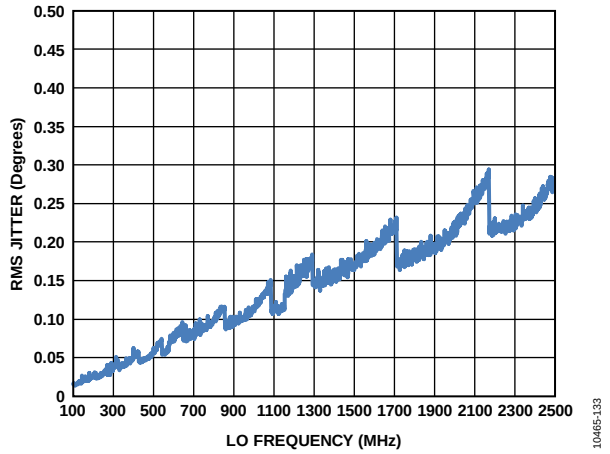

Figure 30. Integrated Phase Noise over an Integration Bandwidth of 1 kHz to 8 MHz vs. LO Frequency at Nominal Conditions

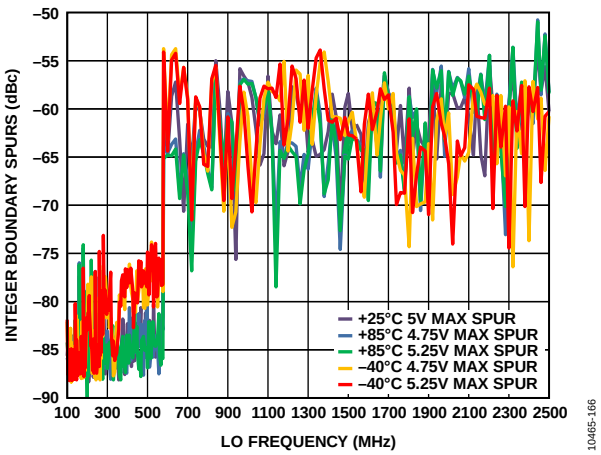

Figure 33. Integer Boundary Spur Performance vs. LO Frequency, Supply, and Temperature

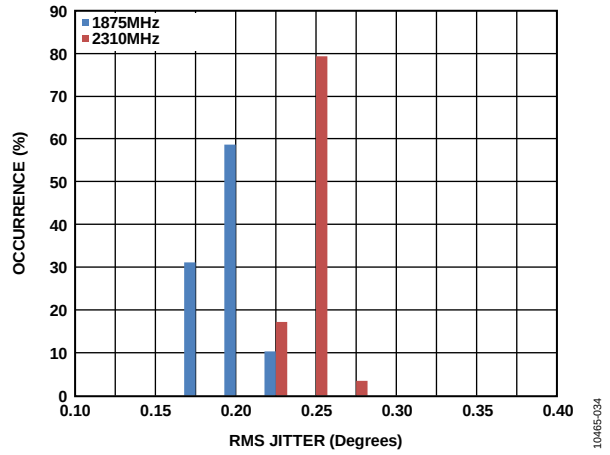

Figure 31. Integrated Phase Noise Distribution over an Integration Bandwidth of 1 kHz to 8 MHz at 1875 MHz and 2310 MHz

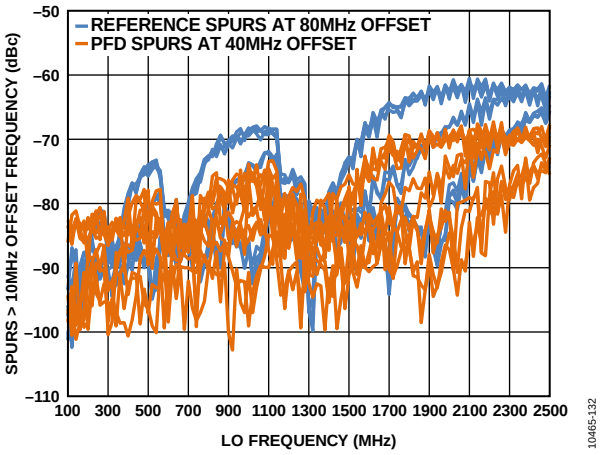

Figure 34. Spurs > 10 MHz from Carrier vs. LO Frequency, Supply, and Temperature

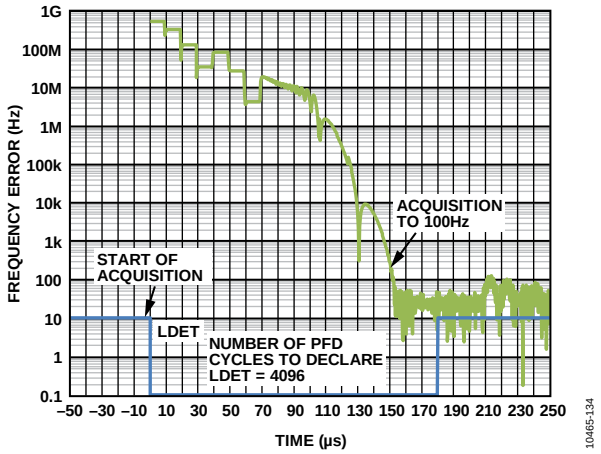

Figure 35. PLL Frequency Settling Time at Worst-Case LO Frequency with Lock Detect Shown

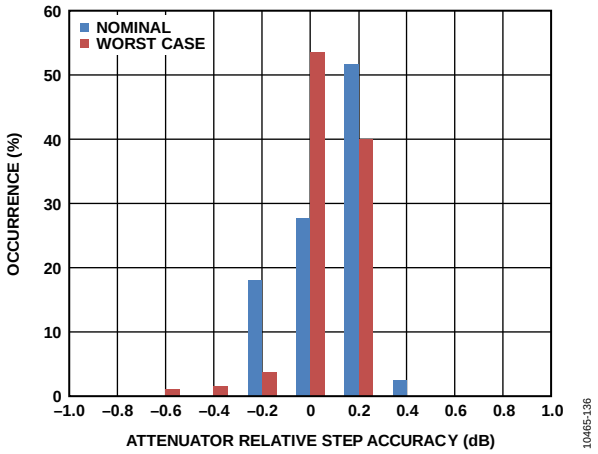

Figure 38. Attenuator Relative Step Accuracy Distribution at Nominal and Worst-Case Conditions, LO > 300 MHz, All Attenuation Steps

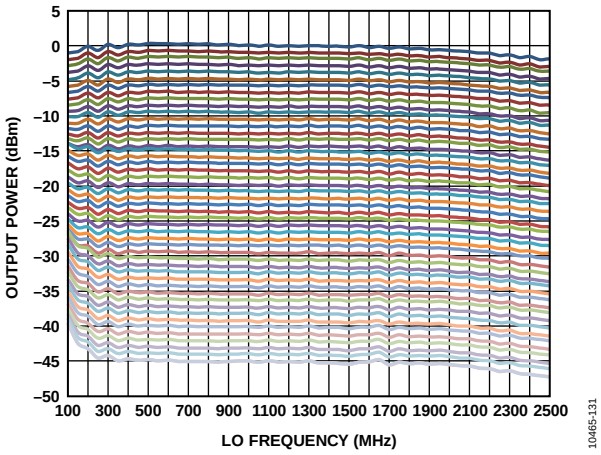

Figure 36. Attenuator Gain vs. LO Frequency by Gain Code, All Attenuator Code Steps

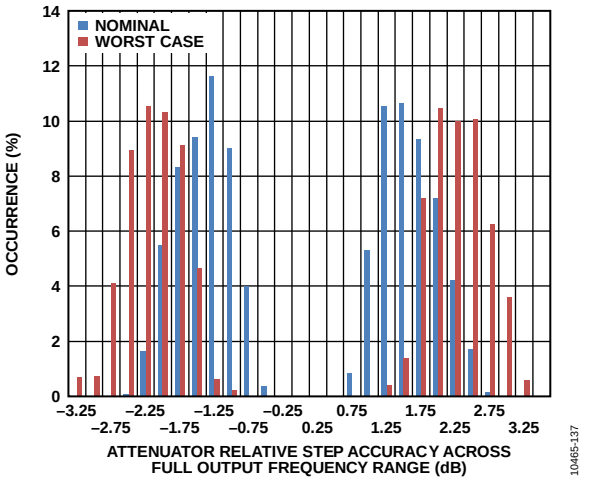

Figure 39. Attenuator Relative Step Accuracy Across Full Output Frequency Range Distribution at Nominal and Worst-Case Conditions, LO > 300 MHz, All Attenuation Steps

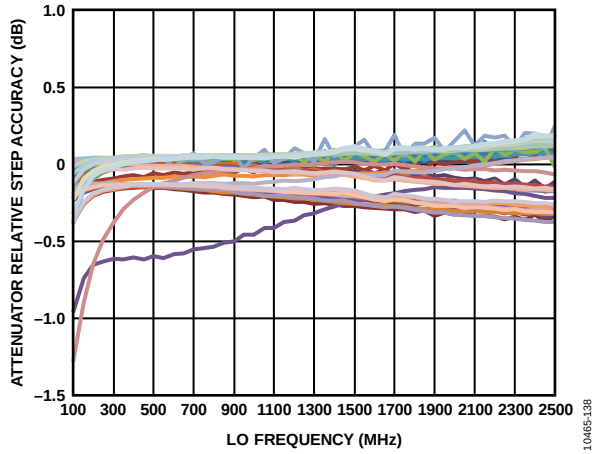

Figure 37. Attenuator Relative Step Accuracy over all Attenuation Steps vs. LO Frequency, Nominal Conditions

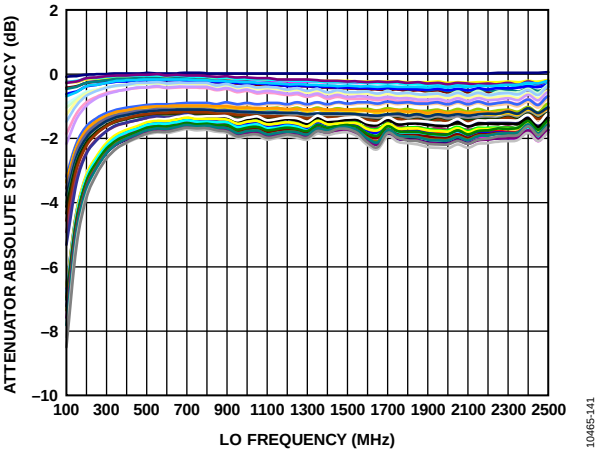

Figure 40. Attenuator Absolute Step Accuracy over all Attenuation Steps vs. LO Frequency, Nominal Conditions

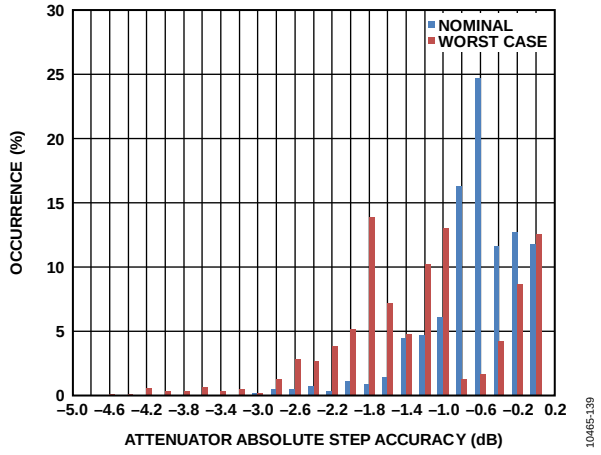

Figure 41. Attenuator Absolute Step Accuracy Distribution at Nominal and Worst-Case Conditions, LO > 300 MHz, All Attenuation Steps

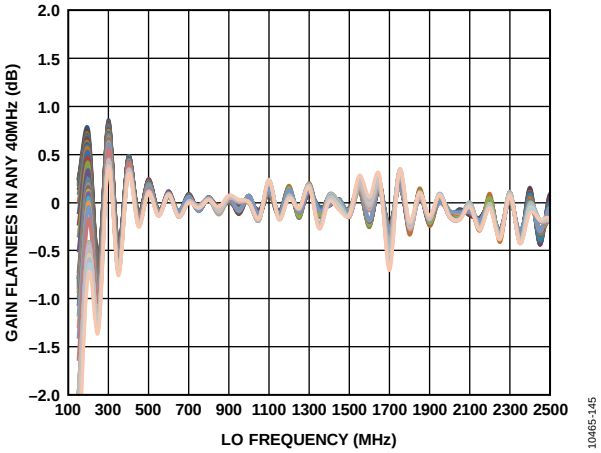

Figure 42. Gain Flatness in any 40 MHz for all Attenuation Steps vs. LO Frequency at Nominal Conditions

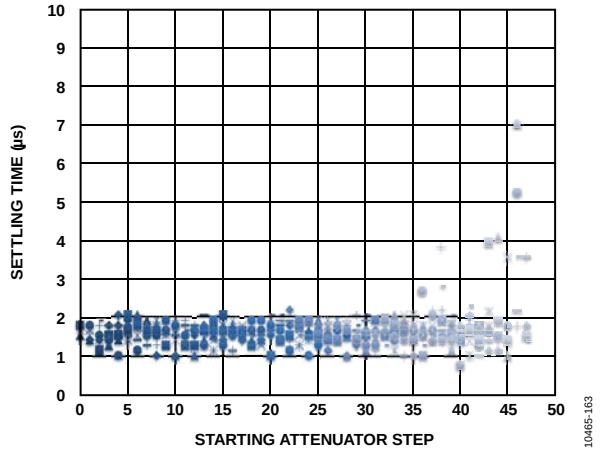

Figure 43. Attenuator Setting Time to 0.2 dB for Small Steps (1 dB to 6 dB) at Nominal Conditions

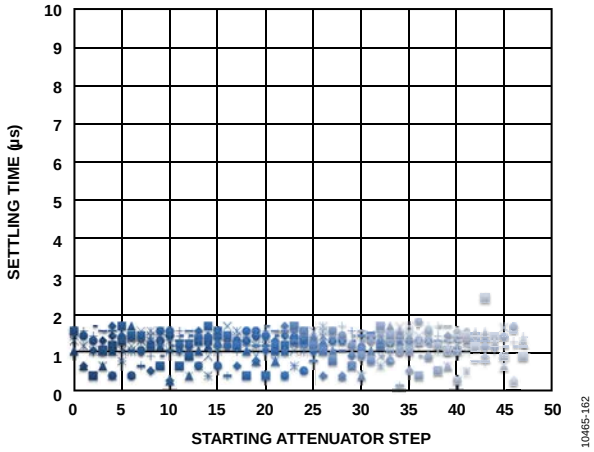

Figure 44. Attenuator Settling Time to 0.5 dB for Small Steps (1 dB to 6 dB) at Nominal Conditions

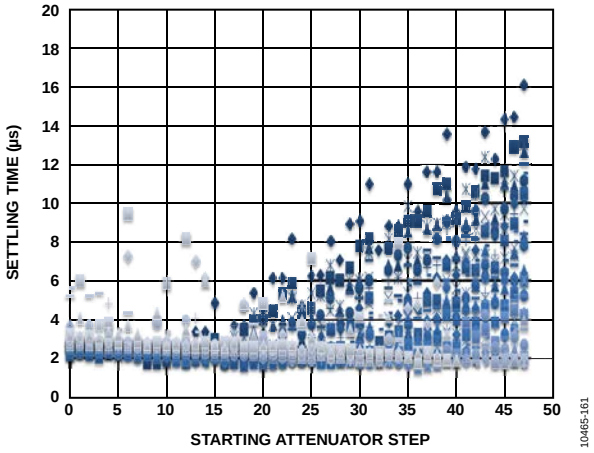

Figure 45. Attenuator Settling Time to 0.2 dB for Large Steps (7 dB to 47 dB) at Nominal Conditions

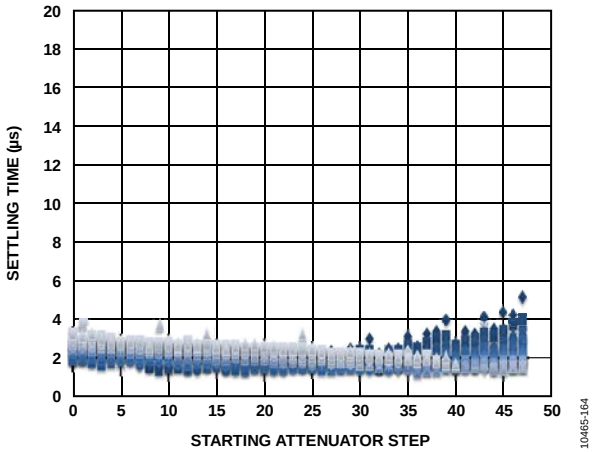

Figure 46. Attenuator Settling Time to 0.5 dB for Large Steps (7 dB to 47 dB) at Nominal Conditions

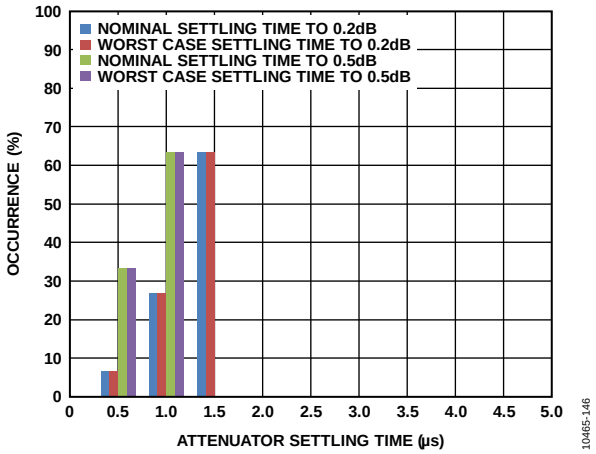

Figure 47. Attenuator Settling Time to 0.2 dB and 0.5 dB Distribution at Nominal and Worst-Case Conditions for Typical Small Step

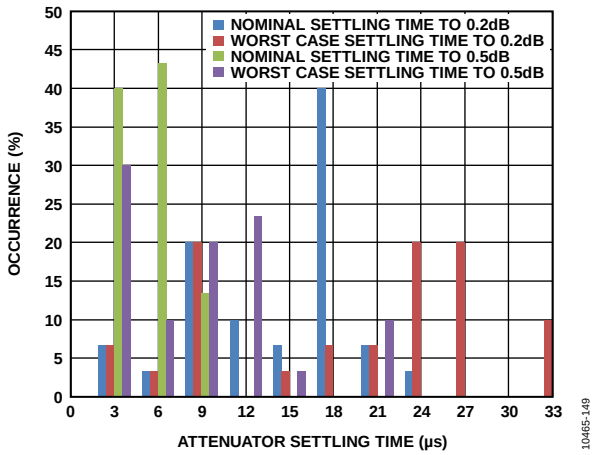

Figure 50. Attenuator Settling Time to 0.2 dB and 0.5 dB Distribution at Nominal and Worst-Case Conditions for Worst-Case Large Step (47 dB to 0 dB)

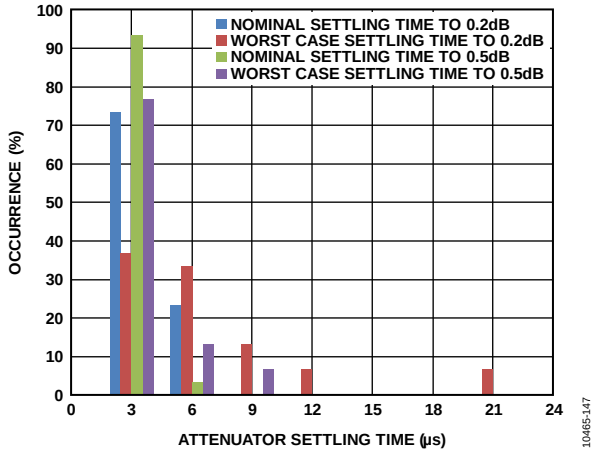

Figure 48. Attenuator Settling Time to 0.2 dB and 0.5 dB Distribution at Nominal and Worst-Case Conditions for Worst-Case Small Step (36 dB to 42 dB)

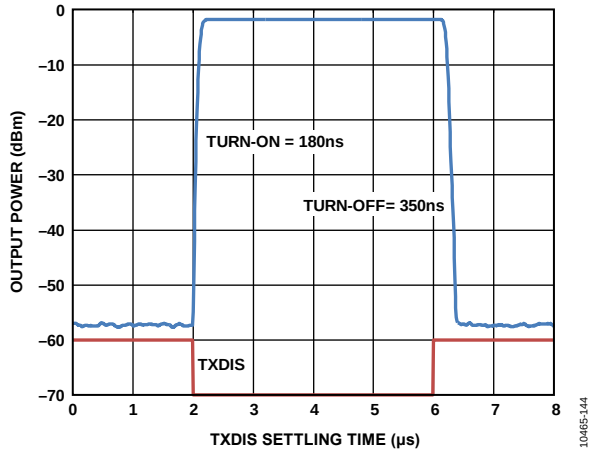

Figure 51. TXDIS Settling Time at Worst-Case Supply and Temperature

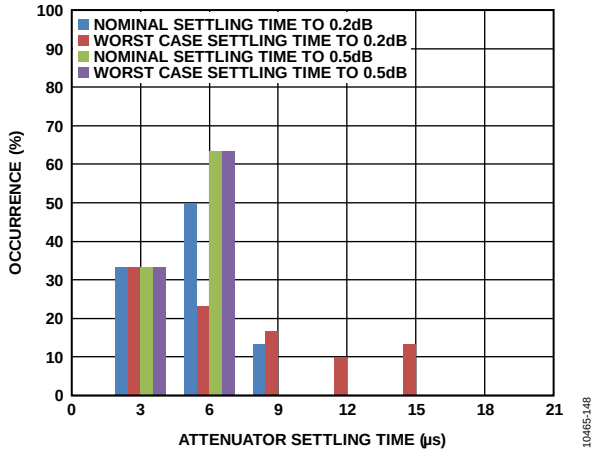

Figure 49. Attenuator Settling Time to 0.2 dB and 0.5 dB Distribution at Nominal and Worst-Case Conditions for Typical Large Step

THEORY OF OPERATION

OVERVIEW

The ADRF6755 device can be divided into the following basic building blocks:

- PLL synthesizer and VCO
- Quadrature modulator
- Attenuator
- Voltage regulator
- I²C/SPI interface

Each of these building blocks is described in detail in the sections that follow.

PLL SYNTHESIZER AND VCO

Overview

The phase-locked loop (PLL) consists of a fractional-N frequency synthesizer with a 25-bit fixed modulus, allowing a frequency resolution of less than 1 Hz over the entire frequency range. It also has an integrated voltage-controlled oscillator (VCO) with a fundamental output frequency ranging from 2310 MHz to 4800 MHz. An RF divider, controlled by Register CR28, Bits[2:0], extends the lower limit of the local oscillator (LO) frequency range to 100 MHz. See Table 6 for more details on Register CR28.

Reference Input Section

The reference input stage is shown Figure 52. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed, and SW1 and SW2 are open. This ensures that there is no loading of the REFIN pin at power-down.

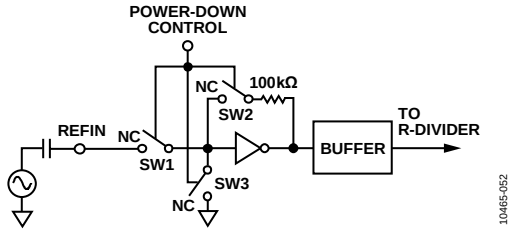

Figure 52. Reference Input Stage

Reference Input Path

The on-chip reference frequency doubler allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually improves the in-band phase noise performance by up to 3 dBc/Hz.

The 5-bit R-divider allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

An additional divide-by-2 (÷2) function in the reference input path allows for a greater division range.

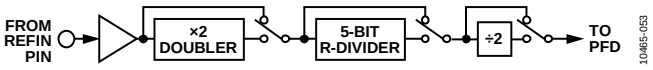

Figure 53. Reference Input Path

The PFD frequency equation is

$$f_{PFD} = f_{REFIN} \times [(1 + D)/(R \times (1 + T))] \quad (1)$$

where:
f_{REFIN} is the reference input frequency.
D is the doubler bit.
R is the programmed divide ratio of the binary 5-bit programmable reference divider (1 to 32).
T is the R/2 divider setting bit (CR10[6] = 0 or 1).

If no division is required, it is recommended that the 5-bit R-divider and the divide-by-2 be disabled by setting CR5[4] = 0. If an even numbered division is required, enable the divide-by-2 by setting CR5[4] = 1 and CR10[6] = 1 and implement the remainder of the division in the 5-bit R-divider. If an odd number division is required, set CR5[4] = 1 and implement all of the division in the 5-bit R-divider.

RF Fractional-N Divider

The RF fractional-N divider allows a division ratio in the PLL feedback path that can range from 23 to 4095. The relationship between the fractional-N divider and the LO frequency is described in the INT and FRAC Relationship section.

INT and FRAC Relationship

The integer (INT) and fractional (FRAC) values make it possible to generate output frequencies that are spaced by fractions of the phase frequency detector (PFD) frequency. See the Example—Changing the LO Frequency section for more information.

The LO frequency equation is

$$LO = f_{PFD} \times (INT + (FRAC/2^{25}))/2^{RFDIV} \quad (2)$$

where:
LO is the local oscillator frequency.
f_{PFD} is the PFD frequency.
INT is the integer component of the required division factor and is controlled by the CR6 and CR7 registers.
$FRAC$ is the fractional component of the required division factor and is controlled by the CR0 to CR3 registers.
$RFDIV$ is set in Register CR28, Bits[2:0], and controls the setting of the divider at the output of the PLL.

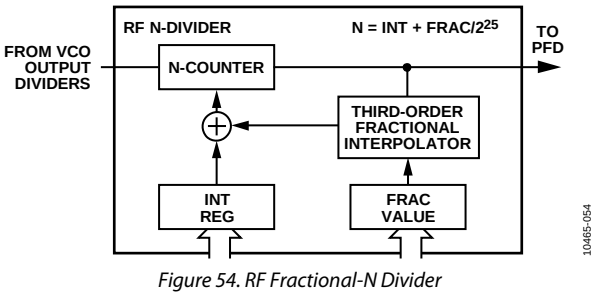

Figure 54. RF Fractional-N Divider

Phase Frequency Detector (PFD) and Charge Pump

The PFD takes inputs from the R-divider and the N-counter and produces an output proportional to the phase and frequency difference between them (see Figure 55 for a simplified schematic). The PFD includes a fixed delay element that sets the width of the antibacklash pulse, ensuring that there is no dead zone in the PFD transfer function.

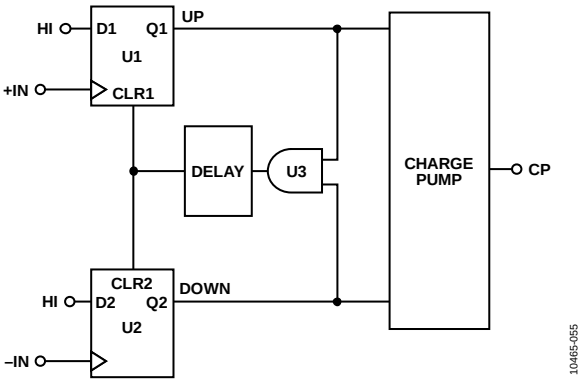

Figure 55. PFD Simplified Schematic

Lock Detect (LDET)

LDET (Pin 44) signals when the PLL has achieved lock to an error frequency of less than 100 Hz. On a write to Register CR0, a new PLL acquisition cycle starts, and the LDET signal goes low. When lock has been achieved, this signal returns high.

Voltage-Controlled Oscillator (VCO)

The VCO core in the ADRF6755 consists of three separate VCOs, each with 16 overlapping bands. This configuration of 48 bands allows the VCO frequency range to extend from 2310 MHz to 4800 MHz. The three VCOs are divided by a programmable divider, RFDIV, controlled by Register CR28, Bits[2:0]. This divider provides divisions of 1, 2, 4, 8, and 16 to ensure that the frequency range is extended from 144.375 MHz (2310 MHz/16) to 4800 MHz (4800 MHz/1). A divide-by-2 quadrature circuit in the path to the modulator then provides the full LO frequency range from 100 MHz to 2400 MHz.

Figure 56 shows a sweep of V_{TUNE} vs. LO frequency demonstrating the three VCOs overlapping and the multiple overlapping bands within each VCO at the LO frequency range of 100 MHz to 2400 MHz. Note that Figure 56 includes the RFDIV being incorporated to provide further divisions of the fundamental VCO frequency; thus, each VCO is used on multiple different occasions throughout the full LO frequency range. The choice of three 16-band VCOs and an RFDIV allows the wide frequency range to be covered without large VCO sensitivity (K_{VCO}) or resultant poor phase noise and spurious performance.

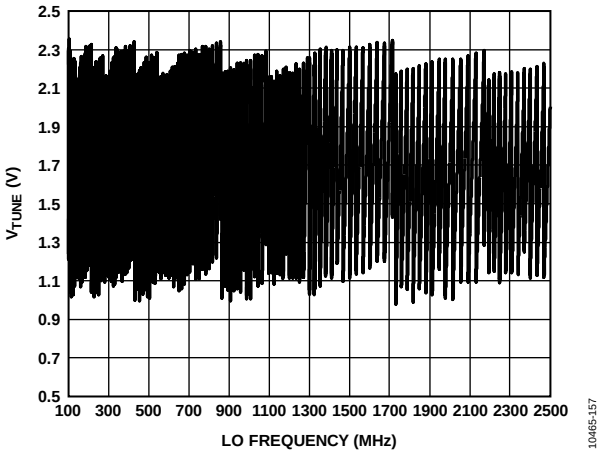

Figure 56. V_{TUNE} vs. LO Frequency

The VCO displays a variation of K_{VCO} as V_{TUNE} varies within the band and from band to band. Figure 57 shows how K_{VCO} varies across the full frequency range. Figure 57 is useful when calculating the loop filter bandwidth and individual loop filter components using ADISimPLL™. ADISimPLL is an Analog Devices, Inc., simulator that aids in PLL design, particularly with respect to the loop filter. It reports parameters such as phase noise, integrated phase noise, and acquisition time for a particular set of input conditions. ADISimPLL can be downloaded from www.analog.com/adisimpll.

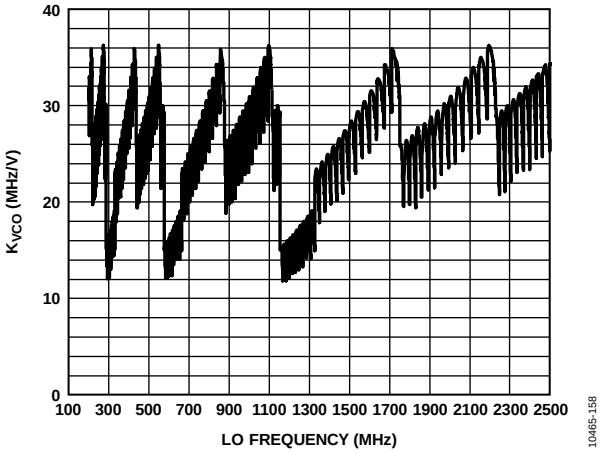

Figure 57. K_{VCO} vs. LO Frequency

Autocalibration

The correct VCO and band are chosen automatically by the VCO and band select circuitry when Register CR0 is updated. This is referred to as autocalibration. The autocalibration time is set by Register CR25.

$$Autocalibration\ Time = (BSCDIV \times 28)/PFD \quad (3)$$

where:
BSCDIV = Register CR25, Bits[7:0].
PFD = PFD frequency.

For a PFD frequency of 40 MHz, set BSCDIV = 100 to set an autocalibration time of 70 µs.

Note that BSCDIV must be recalculated if the PFD frequency is changed. The recommended autocalibration setting is 70 µs. During this time, the VCO V_{TUNE} is disconnected from the output of the loop filter and is connected to an internal reference voltage. A typical frequency acquisition is shown in Figure 58.

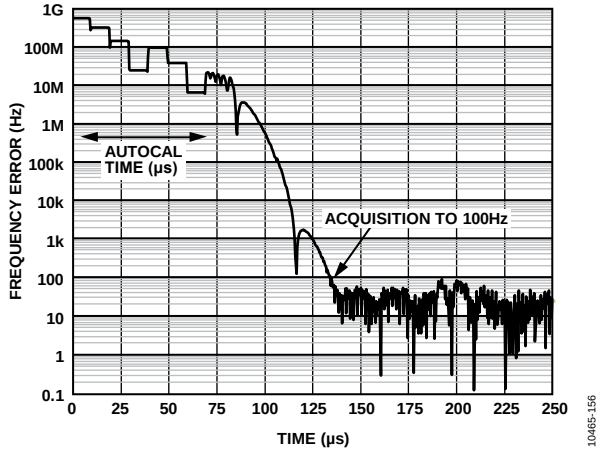

Figure 58. PLL Acquisition

After autocalibration, normal PLL action resumes, and the correct frequency is acquired to within a frequency error of 100 Hz in 170 µs typically. For a maximum cumulative step of 100 kHz/2^{RFDIV}, autocalibration can be turned off by setting Register CR24, Bit 0 = 1. This enables cumulative PLL acquisitions of ≤100 kHz (for RFDIV = ÷1, 50 kHz for RFDIV = ÷2, and so on) to occur without the autocalibration procedure, which improves acquisition times significantly (see Figure 59).

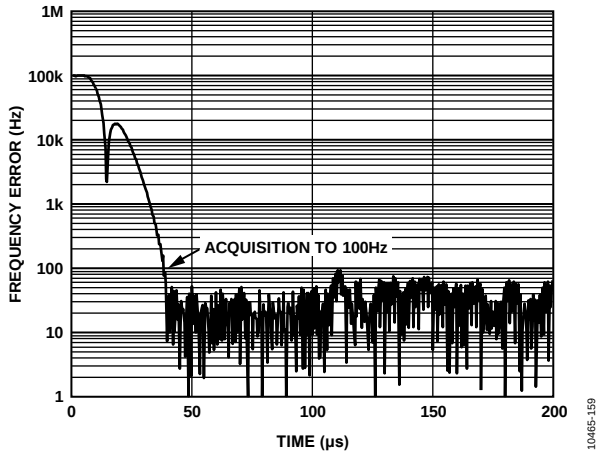

Figure 59. PLL Acquisition Without Autocalibration for a 100 kHz Step

Programming the Correct LO Frequency

There are two steps to programming the correct LO frequency. The user must calculate the RFDIV value based on the required LO frequency and PFD frequency, and the N-divider ratio that is required in the PLL.

1. Calculate the value of RFDIV, which is used to program Register CR28, Bits[2:0] and CR27, Bit 4 from the following lookup table, Table 6.

Table 6. RFDIV Lookup Table

LO Frequency (MHz)	RFDIVIDER	CR28[2:0] = RFDIV	CR27[4]
1155 < LO < 2400	Divide-by-1	000	1
577.5 < LO ≤ 1155	Divide-by-2	001	0
288.75 < LO ≤ 577.5	Divide-by-4	010	0
144.375 < LO ≤ 288.75	Divide-by-8	011	0
100 < LO ≤ 144.375	Divide-by-16	100	0

2. Using the following equation, calculate the value of the N-divider:

$$N = (2^{RFDIV} \times LO)/f_{PFD} \quad (4)$$

where:
N is the N-divider value.
$RFDIV$ is the setting in Register CR28, Bits[2:0].
LO is the local oscillator frequency.
f_{PFD} is the PFD frequency.

This equation is a different representation of Equation 2.

Example to Program the Correct LO Frequency

Assume that the PFD frequency is 40 MHz and that the required LO frequency is 1875 MHz.

From Table 6, $2^{RFDIV} = 1$ (RFDIV = 0)

$$N = (1 \times 1875 \times 10^6)/(40 \times 10^6) = 46.875$$

The N-divider value is composed of integer (INT) and fractional (FRAC) components according to the following equation:

$$N = INT + FRAC/2^{25} \quad (5)$$

INT = 46 and FRAC = 29,360,128

The appropriate registers must then be programmed according to the register map. The order in which the registers are programmed is important. Writing to CR0 initiates a PLL acquisition cycle. If the programmed LO frequency requires a change in the value of CR27[4] (see Table 6), CR27 should be the last register programmed, preceded by CR0. If the programmed LO frequency does not require a change in the value of CR27[4], it is optional to omit the write to CR27 and, in that case, CR0 should be the last register programmed.

QUADRATURE MODULATOR

Overview

A basic block diagram of the ADRF6755 quadrature modulator circuit is shown in Figure 60. The VCO/RFDIVIDER generates a signal at the 2× LO frequency, which is then divided down to give a signal at the LO frequency. This signal is then split into in-phase and quadrature components to provide the LO signals that drive the mixers.

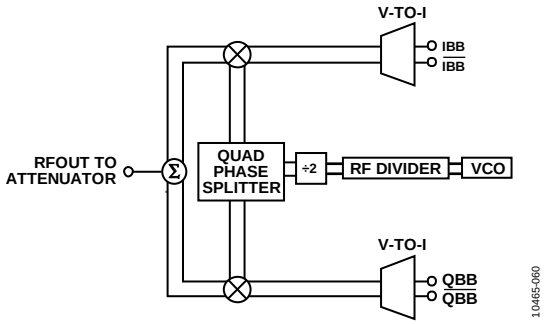

Figure 60. Block Diagram of the Quadrature Modulator

The I and Q baseband input signals are converted to currents by the V-to-I stages, which then drive the two mixers. The outputs of these mixers combine to feed the single-ended output. This single-ended output is then fed to the attenuator and, finally, to the external RFOUT signal pin.

Baseband Inputs

The baseband inputs, QBB, $\overline{\text{QBB}}$, IBB, and $\overline{\text{IBB}}$, must be driven from a differential source. The nominal drive level of 0.9 V p-p differential (450 mV p-p on each pin) should be biased to a common-mode level of 500 mV dc.

To set the dc bias level at the baseband inputs, refer to Figure 61. The average output current on each of the AD9779 outputs is 10 mA. A current of 10 mA flowing through each of the 50 Ω resistors to ground produces the desired dc bias of 500 mV at each of the baseband inputs.

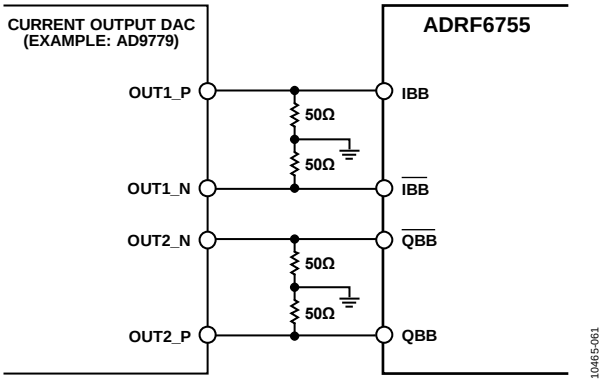

Figure 61. Establishing DC Bias Level on Baseband Inputs

The differential baseband inputs (QBB, $\overline{\text{QBB}}$, $\overline{\text{IBB}}$, and IBB) consist of the bases of PNP transistors, which present a high impedance of about 30 kΩ in parallel with approximately 2 pF of capacitance. The impedance is approximately 30 kΩ below 1 MHz and starts to roll off at higher frequency. A 100 Ω differential termination is recommended at the baseband inputs, and this dominates the input impedance as seen by the input baseband signal. This ensures that the input impedance, as seen by the input circuit, remains flat across the baseband bandwidth. See Figure 62 for a typical configuration.

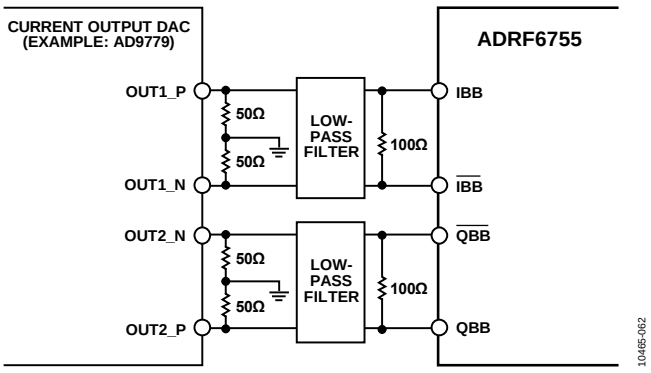

Figure 62. Typical Baseband Input Configuration

The swing of the AD9779 output currents ranges from 0 mA to 20 mA. The ac voltage swing is 1 V p-p single-ended or 2 V p-p differential with the 50 Ω resistors in place. The 100 Ω differential termination resistors at the baseband inputs have the effect of limiting this swing without changing the dc bias condition of 500 mV. The low-pass filter is used to filter the DAC outputs and remove images when driving a modulator.

Another consideration is that the baseband inputs actually source a current of 240 µA out of each of the four inputs. This current must be taken into account when setting up the dc bias of 500 mV. In the initial example based on Figure 61, an error of 12 mV occurs due to the 240 µA current flowing through the 50 Ω resistor. Analog Devices recommends that the accuracy of the dc bias should be 500 mV ± 25 mV. It is also important that this 240 µA current have a dc path to ground.

Optimization

The carrier feedthrough and the sideband suppression performance of the ADRF6755 can be improved over the specifications in Table 1 by using the following optimization techniques.

Carrier Feedthrough Nulling

Carrier feedthrough results from dc offsets that occur between the P and N inputs of each of the differential baseband inputs. Normally these inputs are set to a dc bias of approximately 500 mV.

However, if a dc offset is introduced between the P and N inputs of either or both I and Q inputs, the carrier feedthrough is affected in either a positive or a negative fashion. Note that the dc bias level remains at 500 mV (average P and N level). The I channel offset is often held constant while the Q channel offset is varied until a minimum carrier feedthrough level is obtained. Then, while retaining the new Q channel offset, the I channel offset is adjusted until a new minimum is reached. This is usually performed at a single frequency and, thus, is not optimized over the complete frequency range. Multiple optimizations at different

frequencies must be performed to ensure optimum carrier feed-through across the full frequency range.

Sideband Suppression Nulling

Sideband suppression results from relative gain and relative phase offsets between the I channel and Q channel and can be optimized through adjustments to those two parameters. Adjusting only one parameter improves the sideband suppression only to a point. For optimum sideband suppression, an iterative adjustment between phase and amplitude is required.

ATTENUATOR

The digital attenuator consists of six attenuation blocks: 1 dB, 2 dB, 4 dB, 8 dB, and two 16 dB blocks; each is separately controlled. Each attenuation block consists of field effect transistor (FET) switches and resistors that form either a pi-shaped or a T-shaped attenuator. By controlling the states of the FET switches through the control lines, each attenuation block can be set to the pass state (0 dB) or the attenuation state (1 dB to 47 dB). The various combinations of the six blocks provide the attenuation states from 0 dB to 47 dB in 1 dB increments.

VOLTAGE REGULATOR

The voltage regulator is powered from a 5 V supply that is provided by VCC1 (Pin 11) and produces a 3.3 V nominal regulated output voltage, REGOUT, on Pin 12. This pin must be connected (external to the IC) to the VREG1 through VREG6 package pins.

Decouple the regulator output (REGOUT) with a parallel combination of 10 pF and 220 µF capacitors. The 220 µF capacitor, which is recommended for best performance, decouples broadband noise, leading to better phase noise. Each VREGx pin should have the following decoupling capacitors: 100 nF multilayer ceramic with an additional 10 pF in parallel, both placed as close as possible to the device under test (DUT) power supply pins. X7R or X5R capacitors are recommended. See the Evaluation Board section for more information.

I²C INTERFACE

The ADRF6755 supports a 2-wire, I²C-compatible serial bus that drives multiple peripherals. The serial data (SDA) and serial clock (SCL) inputs carry information between any devices that are connected to the bus. Each slave device is recognized by a unique address. The ADRF6755 has two possible 7-bit slave addresses for both read and write operations. The MSB of the 7-bit slave address is set to 1. Bit A5 of the slave address is set by the CS pin (Pin 27). Bits[4:0] of the slave address are set to all 0s. The slave address consists of the seven MSBs of an 8-bit word. The LSB of the word sets either a read or a write operation (see Figure 63). Logic 1 corresponds to a read operation, whereas Logic 0 corresponds to a write operation.

To control the device on the bus, the following protocol must be followed. The master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address and the R/W bit). The bits are transferred from MSB to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices then withdraw from the bus and maintain an idle condition. During the idle condition, the device monitors the SDA and SCL lines waiting for the start condition and the correct transmitted address. The R/W bit determines the direction of the data. Logic 0 on the LSB of the first byte indicates that the master writes information to the peripheral. Logic 1 on the LSB of the first byte indicates that the master reads information from the peripheral.

The ADRF6755 acts as a standard slave device on the bus. The data on the SDA pin (Pin 29) is eight bits long, supporting the 7-bit addresses plus the R/W bit. The ADRF6755 has 34 subaddresses to enable the user-accessible internal registers. Therefore, it interprets the first byte as the device address and the second byte as the starting subaddress. Auto-increment mode is supported, which allows data to be read from or written to the starting sub-address and each subsequent address without manually addressing the subsequent subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all registers.

Stop and start conditions can be detected at any stage of the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. If an invalid subaddress is issued by the user, the ADRF6755 does not issue an acknowledge and returns to the idle condition. In a no acknowledge condition, the SDA line is not pulled low on the ninth pulse. See Figure 64 and Figure 65 for sample write and read data transfers, Figure 66 for the timing protocol, and Figure 2 for a more detailed timing diagram.

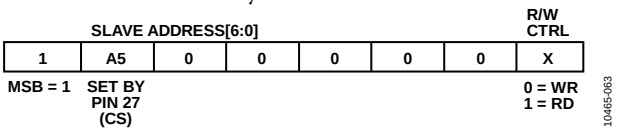

Figure 63. Slave Address Configuration

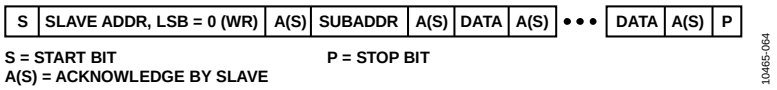

Figure 64. I²C Write Data Transfer

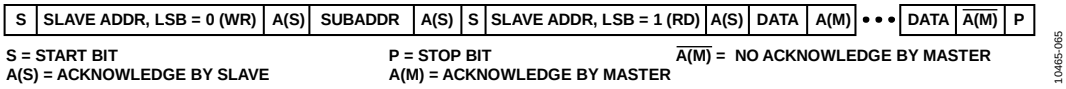

Figure 65. I²C Read Data Transfer

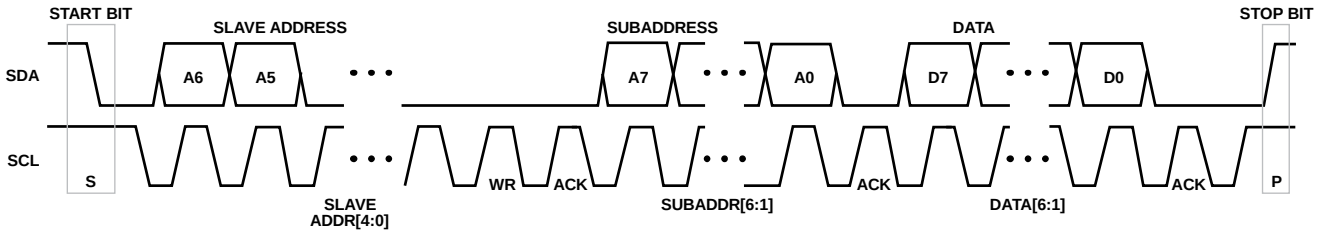

Figure 66. I²C Data Transfer Timing

SPI INTERFACE

The ADRF6755 also supports the SPI protocol. The part powers up in I²C mode but is not locked in this mode. To stay in I²C mode, it is recommended that the user tie the CS line to either 3.3 V or GND, thus disabling SPI mode. It is not possible to lock the I²C mode, but it is possible to select and lock the SPI mode.

To select and lock the SPI mode, three pulses must be sent to the CS pin, as shown in Figure 67. When the SPI protocol is locked in, it cannot be unlocked while the device is still powered up. To reset the serial interface, the part must be powered down and powered up again.

Serial Interface Selection

The CS pin controls selection of the I²C or SPI interface. Figure 67 shows the selection process that is required to lock the SPI mode. To communicate with the part using the SPI protocol, three pulses must be sent to the CS pin. On the third rising edge, the part selects and locks the SPI protocol. Consistent with most SPI standards, the CS pin must be held low during all SPI communication to the part and held high at all other times.

SPI Serial Interface Functionality

The SPI serial interface of the ADRF6755 consists of the CS, SDI (SDI/SDA), CLK (CLK/SCL), and SDO pins. CS is used to select the device when more than one device is connected to the serial clock and data lines. CLK is used to clock data in and out of the part. The SDI pin is used to write to the registers. The SDO pin is a dedicated output for the read mode. The part operates in slave mode and requires an externally applied serial clock to the CLK pin. The serial interface is designed to allow the part to be interfaced to systems that provide a serial clock that is synchronized to the serial data.

Figure 68 shows an example of a write operation to the ADRF6755. Data is clocked into the registers on the rising edge of CLK using a 24-bit write command. The first eight bits represent the write command, 0xD4; the next eight bits are the register address; and the final eight bits are the data to be written to the specific register. Figure 69 shows an example of a read operation. In this example, a shortened 16-bit write command is first used to select the appropriate register for a read operation, the first eight bits representing the write command, 0xD4, and the final eight bits representing the specific register. Then the CS line is pulsed low for a second time to retrieve data from the selected register using a 16-bit read command, the first eight bits representing the read command, 0xD5, and the final eight bits representing the contents of the register being read. Figure 3 shows the timing for both SPI read and SPI write operations.

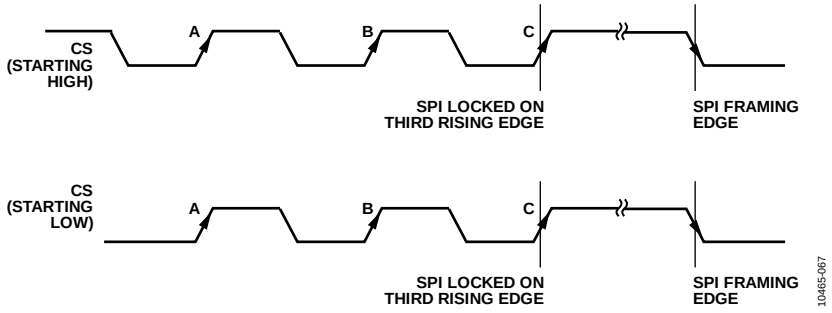

Figure 67. Selecting the SPI Protocol

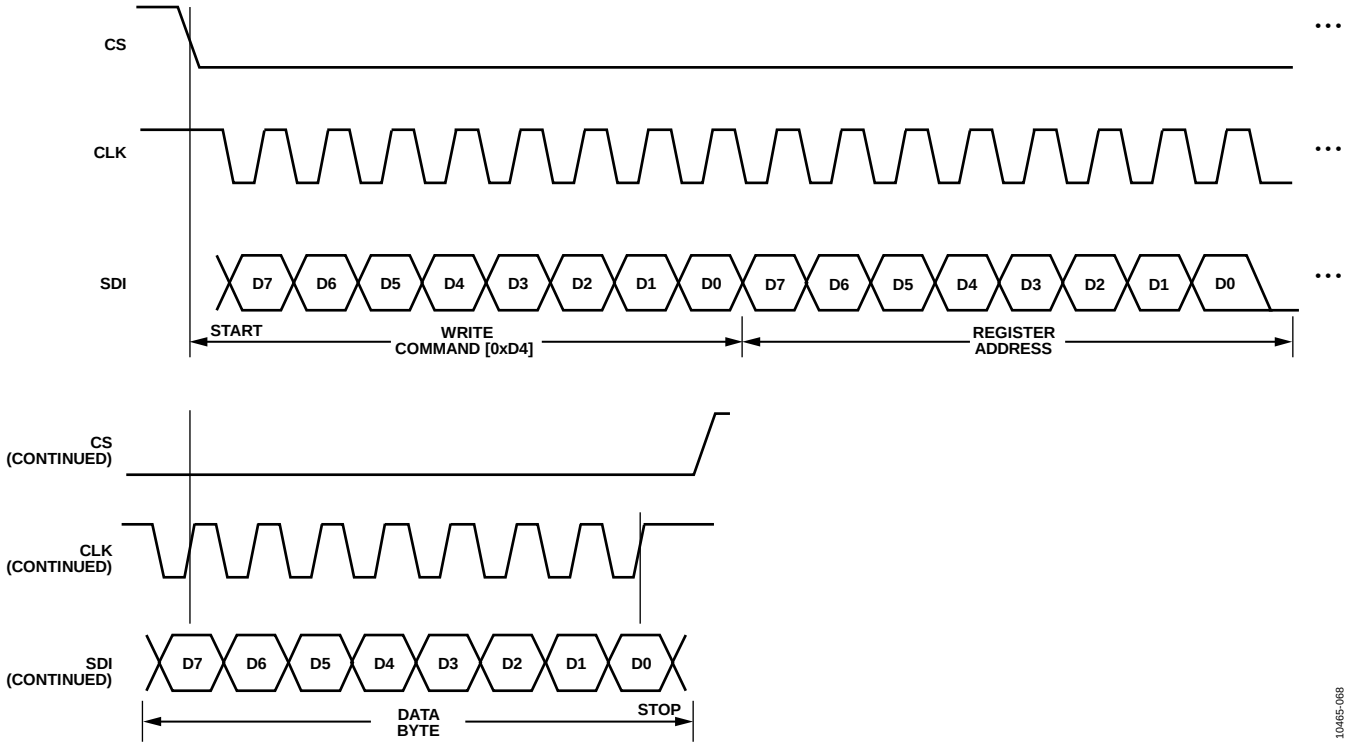

Figure 68. SPI Byte Write Example

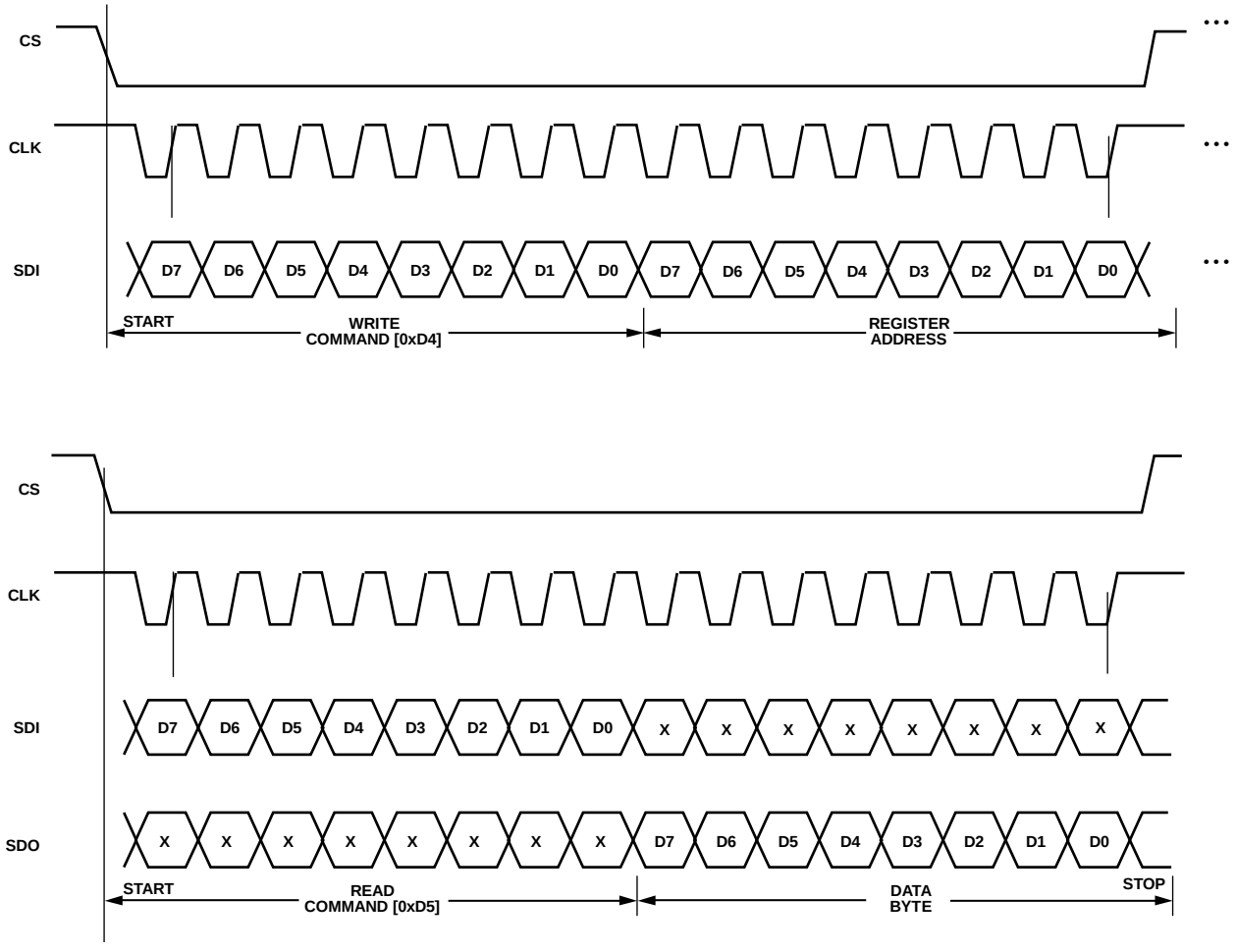

Figure 69. SPI Byte Read Example

PROGRAM MODES

The ADRF6755 has 34 8-bit registers to allow program control of a number of functions. Either an SPI or an I²C interface can be used to program the register set. For details about the interfaces and timing, see Figure 63 to Figure 69. The registers are documented in Table 8 to Table 28.

Several settings in the ADRF6755 are double-buffered. These settings include the FRAC value, the INT value, the 5-bit R-divider value, the reference frequency doubler, the R/2 divider, the RFDIV value, and the charge pump current setting. This means that two events must occur before the part uses a new value for any of the double-buffered settings. First, the new value is latched into the device by writing to the appropriate register. Next, a new write must be performed on Register CR0. When Register CR0 is written, a new PLL acquisition takes place.

For example, updating the fractional value involves a write to Register CR3, Register CR2, Register CR1, and Register CR0. Register CR3 should be written to first, followed by Register CR2 and Register CR1, and, finally, Register CR0. The new acquisition begins after the write to Register CR0. Double buffering ensures that the bits written to do not take effect until after the write to Register CR0.

12-Bit Integer Value

Register CR7 and Register CR6 program the integer value (INT) of the feedback division factor (N); see Equation 5 for details. The INT value is a 12-bit number whose MSBs are programmed through Register CR7, Bits[3:0]. The LSBs are programmed through Register CR6, Bits[7:0]. The LO frequency setting is described by Equation 2. An alternative to this equation is provided by Equation 4, which details how to set the N-divider value. Note that these registers are double buffered.

25-Bit Fractional Value

Register CR3 to Register CR0 program the fractional value (FRAC) of the feedback division factor (N); see Equation 5 for details. The FRAC value is a 25-bit number whose MSB is programmed through Register CR3, Bit 0. The LSB is programmed through Register CR0, Bit 0. The LO frequency setting is described by Equation 2. An alternative to this equation is described by Equation 4, which details how to set the N-divider value. Note that these registers are double buffered.

RFDIV Value

The RFDIV value is dependent on the value of the LO frequency. The RFDIV value can be selected from the list in Table 6. Apply the selected RFDIV value to Equation 4, together with the LO frequency and PFD frequency values, to calculate the correct N-divider value.

Reference Input Path

The reference input path consists of a reference frequency doubler, a 5-bit reference divider, and a divide-by-2 function (see Figure 53). The doubler is programmed through Register CR10, Bit 5. The 5-bit divider and divide-by-2 are enabled by programming Register CR5, Bit 4, and the division ratio is programmed through Register CR10, Bits[4:0]. The R/2 divider is programmed through Register CR10, Bit 6. Note that these registers are double-buffered.

Charge Pump Current

Register CR9, Bits[7:4], specify the charge pump current setting. With an R_{SET} value of 4.7 kΩ, the maximum charge pump current is 5 mA. The following equation applies:

$$I_{CPmax} = 23.5/R_{SET}$$

The charge pump current has 16 settings from 312.5 µA to 5 mA. For the loop filter that is specified in the application solution, a charge pump current of 5 mA (Register CR9[7:4] = 0xF) gives a loop bandwidth of 100 kHz, which is the recommended loop bandwidth setting.

Transmit Disable Control (TXDIS)

The transmit disable control (TXDIS) is used to disable the RF output. TXDIS is normally held low. When asserted (brought high), it disables the RF output. Register CR14 is used to control which circuit blocks are powered down when TXDIS is asserted. To meet both the off isolation power specifications and the turn-on/turn-off settling time specifications, a value of 0x80 should be loaded into Register CR14. This effectively ensures that the attenuator is always enabled when TXDIS is asserted, even if other circuitry is disabled.

Power-Down/Power-Up Control Bits

The four programmable power-up and power-down control bits are as follows:

- Register CR12, Bit 2. Master power control bit for the PLL, including the VCO. This bit is normally set to a default value of 0 to power up the PLL.
- Register CR28, Bit 4. Controls the RFDIVIDER. This bit is normally set to a default value of 0 to power up the RFDIVIDER.
- Register CR27, Bit 2. Controls the LO monitor outputs, LOMON and $\overline{\text{LOMON}}$. The default is 0 when the monitor outputs are powered down. Setting this bit to 1 powers up the monitor outputs to one of four options, −6 dBm, −12 dBm, −18 dBm, or −24 dBm, as controlled by Register CR27, Bits[1:0].
- Register CR29, Bit 0. Controls the quadrature modulator power. The default is 0, which powers down the modulator. Write a 1 to this bit to power up the modulator.

Lock Detect (LDET)

Lock detect is enabled by setting Register CR23, Bit 4, to 1. The lock detect circuit is based on monitoring the up/down pulses from the PFD. As acquisition proceeds, the width of these pulses reduces until they are less than a target width (set by CR23[2]). At this point, a count of the number of successive PFD cycles is initiated, where the width of the up/down pulses remains less that the target width. When this count reaches a target count (set by CR13[6] and CR23[3]), LDET is set. The truth table for declaring LDET is given in Table 7.

Table 7. Declaring LDET

LDCount1 CR13[6]	LDCount0 CR23[3]	Number of PFD Cycles to Declare LDET
0	0	2048
0	1	3072
1	0	4096
1	1	16,384

The appropriate setting to use depends on the PFD frequency as well as the desired accuracy when LDET is declared. The LDET setting does not affect the acquisition time of the PLL. It only affects the time at which LDET goes high.

VCO Autocalibration

The VCO uses an autocalibration technique to select the correct VCO and band, as explained in the Autocalibration section. Register CR24, Bit 0, controls whether the autocalibration is enabled. For normal operation, autocalibration must be enabled. However, if using cumulative frequency steps of 100 kHz/2^{RFDIV} or less, autocalibration can be disabled by setting this bit to 1 and then a new acquisition is initiated by writing to Register CR0.

Attenuator

The attenuator can be programmed from 0 dB to 47 dB in steps of 1 dB. Control is through Register CR30, Bits[5:0].

Revision Readback

The revision of the silicon die can be read back via Register CR33.

REGISTER MAP

REGISTER MAP SUMMARY

Table 8. Register Map Summary

Register Address (Hex)	Register Name	Type	Description
0x00	CR0	Read/write	Fractional Word 4
0x01	CR1	Read/write	Fractional Word 3
0x02	CR2	Read/write	Fractional Word 2
0x03	CR3	Read/write	Fractional Word 1
0x04	CR4	Read/write	Reserved
0x05	CR5	Read/write	5-bit reference dividers enable
0x06	CR6	Read/write	Integer Word 2
0x07	CR7	Read/write	Integer Word 1 and MUXOUT control
0x08	CR8	Read/write	Reserved
0x09	CR9	Read/write	Charge pump current setting
0x0A	CR10	Read/write	Reference frequency control
0x0B	CR11	Read/write	Reserved
0x0C	CR12	Read/write	PLL power-up
0x0D	CR13	Read/write	Lock Detector Control 2
0x0E	CR14	Read/write	TXDIS control
0x0F	CR15	Read/write	Reserved
0x10	CR16	Read/write	Reserved
0x11	CR17	Read/write	Reserved
0x12	CR18	Read/write	Reserved
0x13	CR19	Read/write	Reserved
0x14	CR20	Read/write	Reserved
0x15	CR21	Read/write	Reserved
0x16	CR22	Read/write	Reserved
0x17	CR23	Read/write	Lock Detector Control 1
0x18	CR24	Read/write	Autocalibration
0x19	CR25	Read/write	Autocalibration Timer
0x1A	CR26	Read/write	Reserved
0x1B	CR27	Read/write	LO monitor output and LO selection
0x1C	CR28	Read/write	LO selection
0x1D	CR29	Read/write	Modulator
0x1E	CR30	Read/write	Attenuator
0x1F	CR31	Read only	Reserved
0x20	CR32	Read only	Reserved
0x21	CR33	Read only	Revision code

REGISTER BIT DESCRIPTIONS

Table 9. Register CR0 (Address 0x00), Fractional Word 4

Bit	Description[1]
7	Fractional Word F7
6	Fractional Word F6
5	Fractional Word F5
4	Fractional Word F4
3	Fractional Word F3
2	Fractional Word F2
1	Fractional Word F1
0	Fractional Word F0 (LSB)

[1] Double-buffered. Loaded on a write to Register CR0.

Table 10. Register CR1 (Address 0x01), Fractional Word 3

Bit	Description[1]
7	Fractional Word F15
6	Fractional Word F14
5	Fractional Word F13
4	Fractional Word F12
3	Fractional Word F11
2	Fractional Word F10
1	Fractional Word F9
0	Fractional Word F8

[1] Double-buffered. Loaded on a write to Register CR0.

Table 11. Register CR2 (Address 0x02), Fractional Word 2

Bit	Description[1]
7	Fractional Word F23
6	Fractional Word F22
5	Fractional Word F21
4	Fractional Word F20
3	Fractional Word F19
2	Fractional Word F18
1	Fractional Word F17
0	Fractional Word F16

[1] Double-buffered. Loaded on a write to Register CR0.

Table 12. Register CR3 (Address 0x03), Fractional Word 1

Bit	Description
7	Set to 0
6	Set to 0
5	Set to 0
4	Set to 0
3	Set to 0
2	Set to 1
1	Set to 0
0	Fractional Word F24 (MSB)[1]

[1] Double-buffered. Loaded on a write to Register CR0.

Table 13. Register CR5 (Address 0x05), 5-Bit Reference Divider Enable

Bit	Description
7	Set to 0
6	Set to 0
5	Set to 0
4	5-bit R-divider and divide-by-2 enable[1] 0 = disable 5-bit R-divider and divide-by-2 (default) 1 = enable 5-bit R-divider and divide-by-2
3	Set to 0
2	Set to 0
1	Set to 0
0	Set to 0

[1] Double-buffered. Loaded on a write to Register CR0.

Table 14. Register CR6 (Address 0x06), Integer Word 2

Bit	Description[1]
7	Integer Word N7
6	Integer Word N6
5	Integer Word N5
4	Integer Word N4
3	Integer Word N3
2	Integer Word N2
1	Integer Word N1
0	Integer Word N0

[1] Double-buffered. Loaded on a write to Register CR0.

Table 15. Register CR7 (Address 0x07), Integer Word 1 and MUXOUT Control

Bit	Description
[7:4]	MUXOUT control 0000 = tristate 0001 = logic high 0010 = logic low 1101 = reference clock/2 1110 = RF fractional-N divider clock/2
3	Integer Word N11[1]
2	Integer Word N10[1]
1	Integer Word N9[1]
0	Integer Word N8[1]

[1] Double-buffered. Loaded on a write to Register CR0.

Table 16. Register CR9 (Address 0x09), Charge Pump Current Setting

Bit	Description
[7:4]	Charge pump current[1] 0000 = 0.3125 mA (default) 0001 = 0.63 mA 0010 = 0.94 mA 0011 = 1.25 mA 0100 = 1.57 mA 0101 = 1.88 mA 0110 = 2.19 mA 0111 = 2.50 mA 1000 = 2.81 mA 1001 = 3.13 mA 1010 = 3.44 mA 1011 = 3.75 mA 1100 = 4.06 mA 1101 = 4.38 mA 1110 = 4.69 mA 1111 = 5.00 mA
3	Set to 0
2	Set to 0
1	Set to 0
0	Set to 0

[1] Double-buffered. Loaded on a write to Register CR0.

Table 17. Register CR10 (Address 0x0A), Reference Frequency Control

Bit	Description
7	Set to 0[1]
6	R/2 divider setting[1] 0 = bypass R/2 divider (default) 1 = select R/2 divider
5	Reference frequency doubler (R-doubler) enable[1] 0 = disable doubler (default) 1 = enable doubler
[4:0]	5-bit R-divider setting[1] 00000 = divide by 32 (default) 00001 = divide by 1 00010 = divide by 2 … 11110 = divide by 30 11111 = divide by 31

[1] Double-buffered. Loaded on a write to Register CR0.

Table 18. Register CR12 (Address 0x0C), PLL Power-Up

Bit	Description
7	Set to 0
6	Set to 0
5	Set to 0
4	Set to 1
3	Set to 1
2	Power down PLL 0 = power up PLL (default) 1 = power down PLL
1	Set to 0
0	Set to 0

Table 19. Register CR13 (Address 0x0D), Lock Detector Control 2

Bit	Description
7	Set to 1
6	LDCount1 (see Table 7)
5	Set to 1
4	Set to 0
3	Set to 1
2	Set to 0
1	Set to 0
0	Set to 0

Table 20. Register CR14 (Address 0x0E), TXDIS Control

Bit	Description
7	TXDIS_LOCLK 0 = LO clock always running 1 = stop LO clock when TXDIS = 1
6	Set to 0
5	Set to 0
4	Set to 0
3	Set to 0
2	Set to 0
1	Set to 0
0	Set to 0

Table 21. Register CR23 (Address 0x17), Lock Detector Control 1

Bit	Description
7	Set to 0
6	Set to 1
5	Set to 1
4	Lock detector enable 0 = lock detector disabled (default) 1 = lock detector enabled
3	Lock detector up/down count, LDCount0 (see Table 7)
2	Lock detector precision 0 = low, coarse (10 ns) 1 = high, fine (6 ns)
1	Set to 0
0	Set to 0

Table 22. Register CR24 (Address 0x18), Autocalibration

Bit	Description
7	Set to 0
6	Set to 0
5	Set to 0
4	Set to 1
3	Set to 1
2	Set to 0
1	Set to 0
0	Disable autocalibration 0 = enable autocalibration (default) 1 = disable autocalibration

Table 23. Register CR25 (Address 0x19), Autocalibration Timer

Bit	Description
[7:0]	Autocalibration timer

Table 24. Register CR27 (Address 0x1B), LO Monitor Output and LO Selection

Bit	Description
7	Set to 0
6	Set to 0
5	Set to 0
4	Frequency range; set according to Table 6
3	Set to 0
2	Power up LO monitor output 0 = power down (default) 1 = power up
[1:0]	Monitor output power into 50 Ω 00 = −24 dBm (default) 01 = −18 dBm 10 = −12 dBm 11 = −6 dBm

Table 25. Register CR28 (Address 0x1C), LO Selection

Bit	Description
7	Set to 0
6	Set to 0
5	Set to 0
4	Power down RFDIVIDER 0 = power up (default) 1 = power down
3	Set to 1
[2:0]	RFDIV[1], set according to Table 6

[1] Double-buffered. Loaded on a write to Register CR0.

Table 26. Register CR29 (Address 0x1D), Modulator

Bit	Description
7	Set to 1
6	Set to 0
5	Set to 0
4	Set to 0
3	Set to 0
2	Set to 0
1	Set to 0
0	Power up modulator 0 = power down (default) 1 = power up

Table 27. Register CR30 (Address 0x1E), Attenuator

Bit	Description
7	Set to 0
6	Set to 0
[5:0]	Attenuator A5 to Attenuator A0 000000 = 0 dB 000001 = 1 dB 000010 = 2 dB … 011111 = 31 dB 110000 = 32 dB 110001 = 33 dB … 111101 = 45 dB 111110 = 46 dB 111111 = 47 dB

Table 28. Register CR33 (Address 0x21), Revision Code[1]

Bit	Description
[7:0]	Revision code

[1] Read-only register.

SUGGESTED POWER-UP SEQUENCE

INITIAL REGISTER WRITE SEQUENCE

After applying power to the part, perform the initial register write sequence that follows. Note that Register CR33, Register CR32, and Register CR31 are read-only registers. Also, note that all writable registers should be written to on power-up. Refer to the Register Map section for more details on all registers.

1. Write 0x00 to Register CR30. Set the attenuator to 0 dB gain.
2. Write 0x80 to Register CR29. The modulator is powered down. The modulator is powered down by default to ensure that no spurious signals can occur on the RF output when the PLL is carrying out its first acquisition. The modulator should be powered up only when the PLL is locked.
3. Write 0x0X to Register CR28. RFDIV depends on the value of the LO frequency to be used and is set according to Table 6. Note that Register CR28, Bit 3, is set to 1.
4. Write 0xX0 to Register CR27. Bit 4 depends on the LO frequency to be used and is set according to Table 6.
5. Write 0x00 to Register CR26. Reserved register.
6. Write 0x64 to Register CR25, the autocalibration timer. This setting applies for PFD = 40 MHz. For other PFDs, refer to Equation 3 in the VCO Autocalibration section.
7. Write 0x18 to Register CR24. Enable autocalibration.
8. Write 0x70 to Register CR23. Enable the lock detector and choose the recommended lock detect timing. This setting applies to PFD = 40 MHz. For other PFDs, refer to the Lock Detect (LDET) section in the Program Modes section.
9. Write 0x80 to Register CR22. Reserved register.
10. Write 0x00 to Register CR21. Reserved register.
11. Write 0x00 to Register CR20. Reserved register.
12. Write 0x80 to Register CR19. Reserved register.
13. Write 0x60 to Register CR18. Reserved register.
14. Write 0x00 to Register CR17. Reserved register.
15. Write 0x00 to Register CR16. Reserved register.
16. Write 0x00 to Register CR15. Reserved register.
17. Write 0x80 to Register CR14. Stop LO when TXDIS = 1.
18. Write 0xE8 to Register CR13. This setting applies to PFD = 40 MHz. For other PFDs, refer to the Lock Detect (LDET) section in the Program Modes section.
19. Write 0x18 to Register CR12. Power up the PLL.
20. Write 0x00 to Register CR11. Reserved register.
21. Write to Register CR10. Refer to the Reference Input Path section, in particular Equation 1.
22. Write 0xF0 to Register CR9. With the recommended loop filter component values and R_{SET} = 4.7 kΩ, as shown in Figure 70, the charge pump current is set to 5 mA for a loop bandwidth of 100 kHz.
23. Write 0x00 to Register CR8. Reserved register.
24. Write 0x0X to Register CR7. Set according to Equation 2 in the Theory of Operation section. Also, set the MUXOUT pin to tristate.
25. Write 0xXX to Register CR6. Set according to Equation 2 in the Theory of Operation section.
26. Write to Register CR5. Refer to the Reference Input Path section, in particular Equation 1.
27. Write 0x01 to Register CR4. Reserved register.
28. Write 0000010X binary to Register CR3. Set according to Equation 2 in the Theory of Operation section.
29. Write 0xXX to Register CR2. Set according to Equation 2 in the Theory of Operation section.
30. Write 0xXX to Register CR1. Set according to Equation 2 in the Theory of Operation section.
31. Write 0xXX to Register CR0. Set according to Equation 2 in the Theory of Operation section. Register CR0 must be the last register written for all the double-buffered bit writes to take effect.
32. Write to Register CR27, setting Bit 4 according to Table 6.
33. Monitor the LDET output or wait 170 µs to ensure that the PLL is locked.
34. Write 0x81 to Register CR29. Power up the modulator. The write to Register CR29 does not need to be followed by a write to Register CR0 because this register is not double-buffered.

Example—Changing the LO Frequency

Following is an example of how to change the LO frequency after the initialization sequence. Using an example in which the PLL is locked to 2000 MHz, the following conditions apply:

- f_{PFD} = 40 MHz (assumed)
- Divide ratio N = 50; therefore, INT = 50 decimal and FRAC = 0
- RFDIVIDER = divide-by-1. See Table 6.

Register CR28[2:0] = 000
Register CR27[4] = 1

The INT registers contain the following values:
Register CR7 = 0x00 and Register CR6 = 0x32

The FRAC registers contain the following values:
Register CR3 = 0x04, Register CR2 = 0x00,
Register CR1 = 0x00, and Register CR0 = 0x00

To change the LO frequency to 925 MHz,

- f_{PFD} = 40 MHz (assumed)
- Divide ratio N = 46.25; therefore, INT = 46 decimal and FRAC = 8,388,608
- RFDIVIDER = divide-by-2. See Table 6.

Register CR28[2:0] = 001
Register CR27[4] = 0

The INT registers contain the following values:
Register CR7 = 0x00 and Register CR6 = 0x2E

The FRAC registers contain the following values:
Register CR3 = 0x04, Register CR2 = 0x80,
Register CR1 = 0x00, and Register CR0 = 0x00

Note that Register CR27 should be the last write in this sequence, preceded by CR0. Writing to Register CR0 causes all double-buffered registers to be updated, including the INT, FRAC, and RFDIV registers, and starts a new PLL acquisition.

EVALUATION BOARD

GENERAL DESCRIPTION

The EVAL-ADRF6755SDZ evaluation board is designed to allow the user to evaluate the performance of the ADRF6755. It contains the following:

- I/Q modulator with integrated fractional-N PLL and VCO
- Connector to interface to a standard USB interface board (SPD-S) that must be ordered with the EVAL-ADRF6755SDZ board.
- DC biasing and filter circuitry for the baseband inputs
- Low-pass loop filter circuitry
- An 80 MHz reference clock
- Circuitry to monitor the LOMON outputs
- SMA connectors for power supplies and the RF output

The evaluation board is supplied with the associated driver software to allow easy programming of the ADRF6755.

HARDWARE DESCRIPTION

For more information, refer to the circuit diagram in Figure 70.

Power Supplies

An external 5 V supply, DUT +5 V (J14), drives both an on-chip 3.3 V regulator and the quadrature modulator.

The regulator feeds the VREG1 through VREG6 pins on the chip with 3.3 V. These pins power the PLL circuitry.

The external reference clock generator should be driven by a 3.3 V supply. This supply should be connected via an SMA connector, OSC +V (J15).

Recommended Decoupling for Supplies

The external DUT +5 V supply is decoupled initially by a 10 µF capacitor and then further by a parallel combination of 100 nF and 10 pF capacitors that are placed as close to the DUT as possible for good local decoupling. The regulator output should be decoupled by a parallel combination of 10 pF and 220 µF capacitors. The 220 µF capacitor decouples broadband noise, which leads to better phase noise and is recommended for best performance. Case Size C 220 µF capacitors are used to minimize area. Place a parallel combination of 100 nF and 10 pF capacitors on each VREGx pin, as close to the pins as possible. The impedance of these capacitors should be low and constant across a broad frequency range. Surface-mount multilayered ceramic chip (MLCC) Class II capacitors provide very low ESL and ESR, which assist in decoupling supply noise effectively. They also provide good temperature stability and good aging characteristics.

Capacitance also changes vs. applied bias voltage. Larger case sizes have less capacitance change vs. applied bias voltage and have lower ESR but higher ESL. The 0603 size capacitors provide a good compromise. X5R and X7R capacitors are examples of these types of capacitors and are recommended for decoupling.

SPI Interface

The SPI interface is provided by an additional SPD-S board. This must be ordered with the ADRF6755 evaluation board. The system demonstration platform (SDP) is a hardware and software platform that provides a means to communicate from the PC to Analog Devices products and systems that require digital control and/or readback (see Figure 71).

The SDP-S controller board connects to the PC via USB 2.0 and to the ADRF6755 evaluation board via a small footprint, 120-pin connector. The SDP-S (serial only interface) is a low cost, small form factor, SDP controller board.

Baseband Inputs

The pair of I and Q baseband inputs are served by SMA inputs (J2 to J5) so that they can be driven directly from an external generator or a DAC board, both of which can also provide the dc bias required. There is also an option to filter the baseband inputs, although filtering may not be required, depending on the quality of the baseband source.

Loop Filter

A fourth-order loop filter is provided at the output of the charge pump and is required to adequately filter noise from the Σ-Δ modulator used in the N-divider. With the charge pump current set to a value of 5 mA and using the on-chip VCO, the loop bandwidth is approximately 100 kHz, and the phase margin is 55°. C0G capacitors are recommended for use in the loop filter because they have low dielectric absorption, which is required for fast and accurate settling time. The use of non-C0G capacitors may result in a long tail being introduced into the settling time transient.

Reference Input

The reference input can be supplied by an 80 MHz Jauch clock generator or by an external clock through the use of Connector REFIN (J7). The frequency range of the PFD input is from 10 MHz to 40 MHz; if the 80 MHz clock generator is used, the on-chip 5-bit reference frequency divider or the divide-by-2 divider should be used to set the PFD frequency to 40 MHz to optimize phase noise performance.

LOMON Outputs

These pins are differential LO monitor outputs that provide a replica of the internal LO frequency at 1× LO. The single-ended power in a 50 Ω load can be programmed to −24 dBm, −18 dBm, −12 dBm, or −6 dBm. These open-collector outputs must be terminated to 3.3 V. Because both outputs must be terminated to 50 Ω, options are provided to terminate to 3.3 V using on-board 50 Ω resistors or by series inductors (or a ferrite bead), in which case the 50 Ω termination is provided by the measuring instrument. If not used, these outputs should be tied to REGOUT.

CCOMPx Pins

The CCOMPx pins are internal compensation nodes that must be decoupled to ground with a 100 nF capacitor.

MUXOUT

MUXOUT is a test output that allows different internal nodes to be monitored. It is a CMOS output stage that requires no termination.

Lock Detect (LDET)

Lock detect is a CMOS output that indicates the state of the PLL. A high level indicates a locked condition, and a low level indicates a loss of lock condition.

TXDIS

This input disables the RF output. It can be driven from an external stimulus or simply connected high or low by Jumper J18.

RF Output (RFOUT)

RFOUT (J12) is the RF output of the ADRF6755.

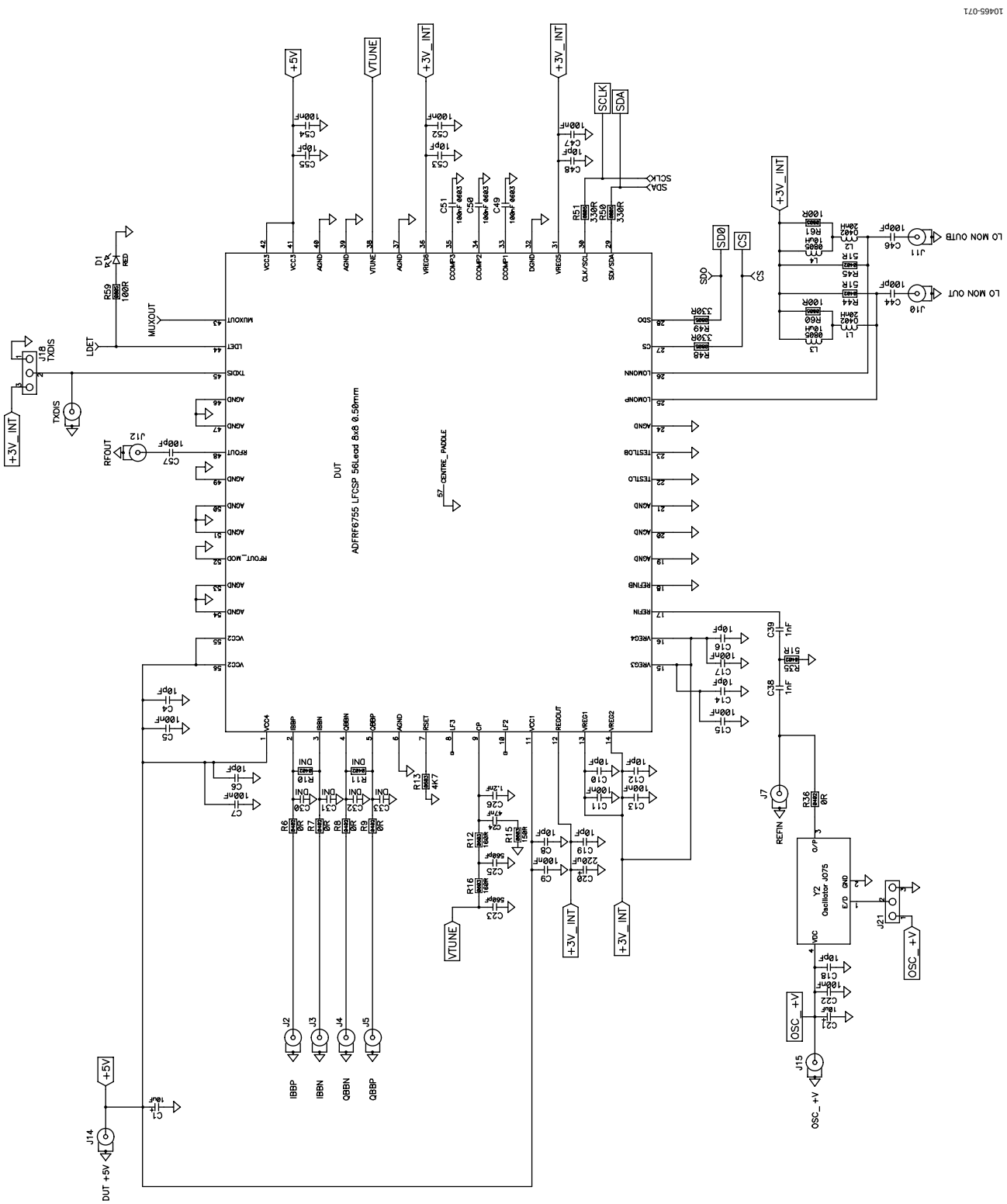

Figure 70. Applications Circuit Schematic

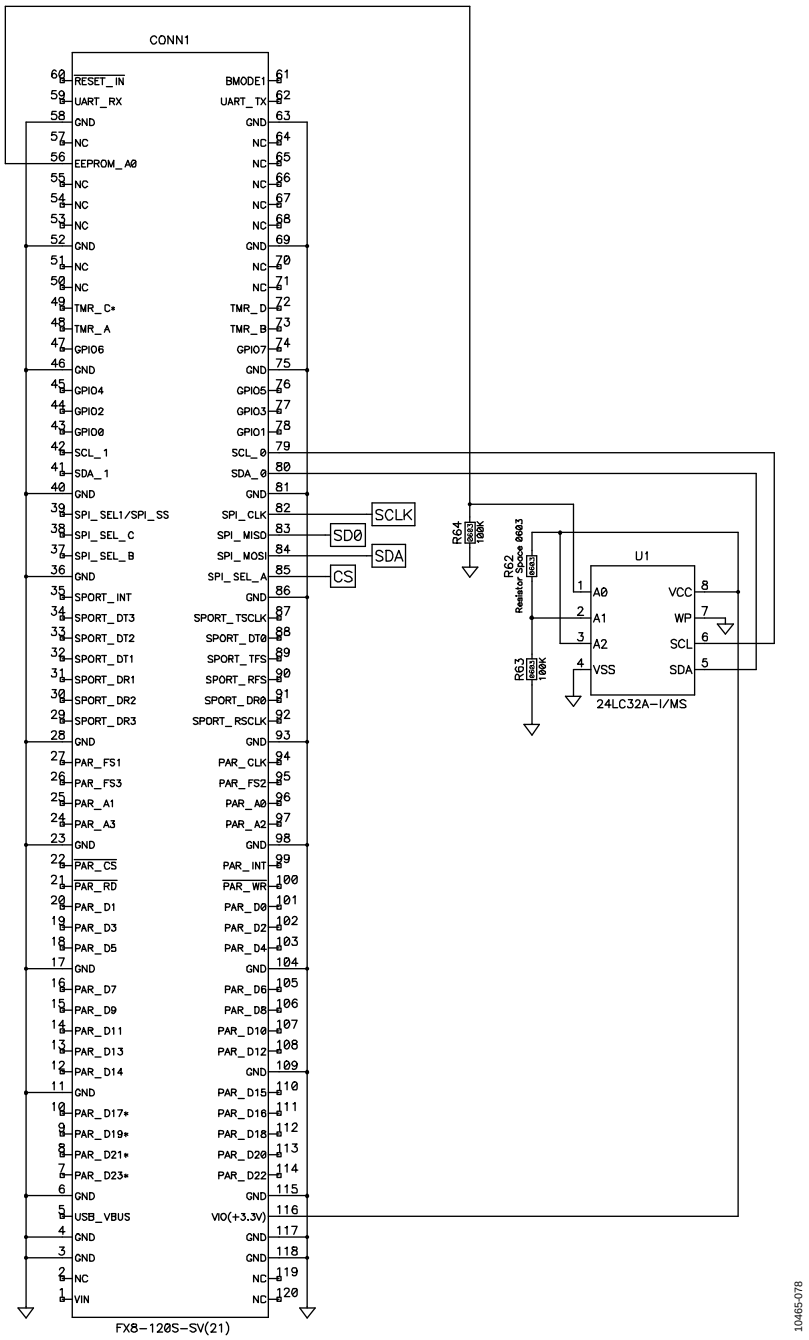

Figure 71. Applications Circuit Schematic—SDP-S

PCB ARTWORK

Component Placement

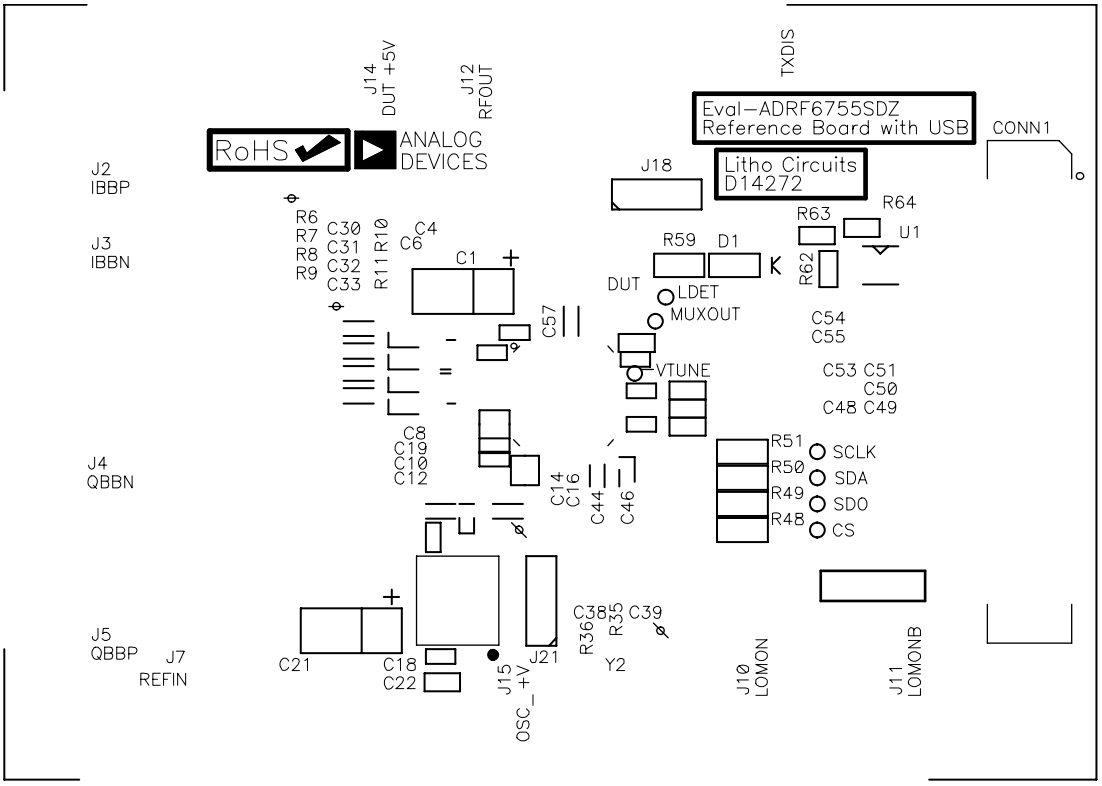

Figure 72. Evaluation Board, Top Side Component Placement

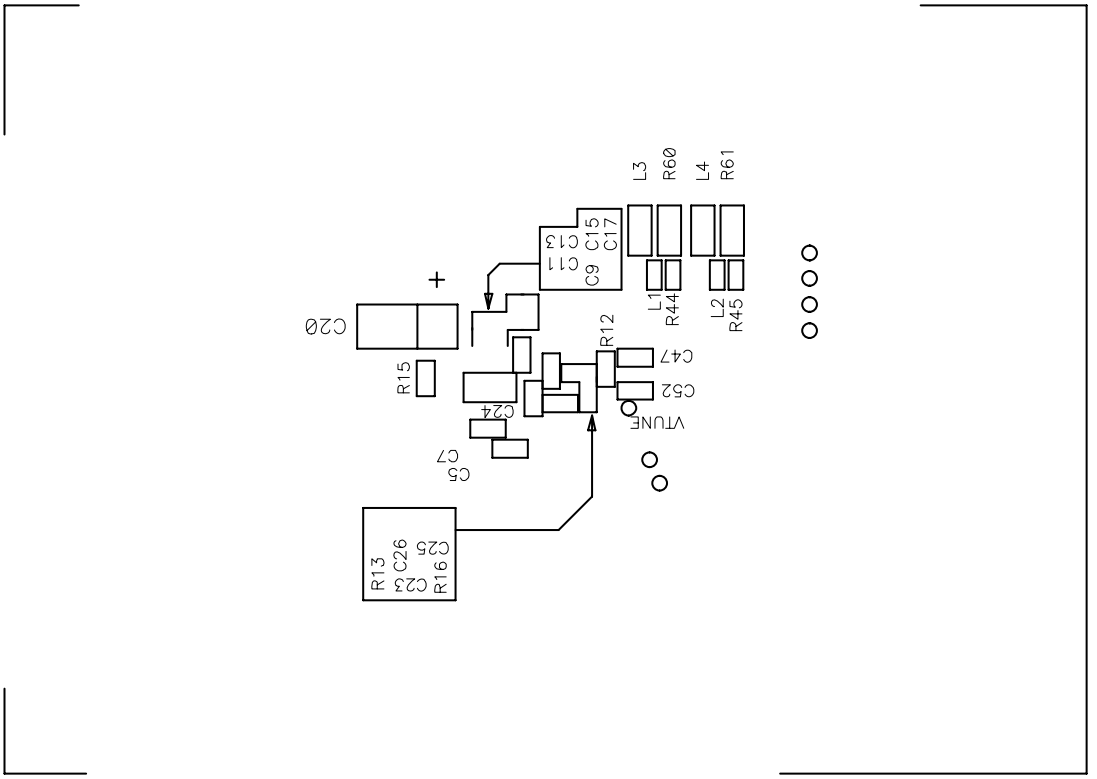

Figure 73. Evaluation Board, Bottom Side Component Placement

PCB Layer Information

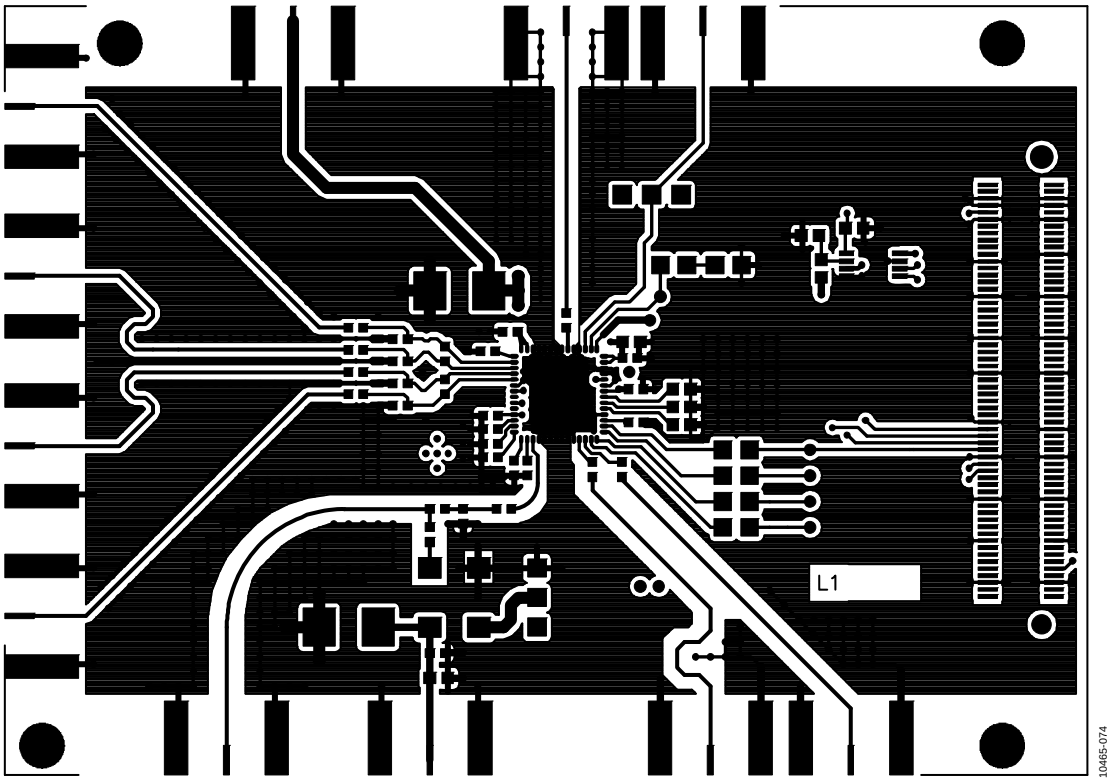

Figure 74. Evaluation Board, Top Side—Layer 1

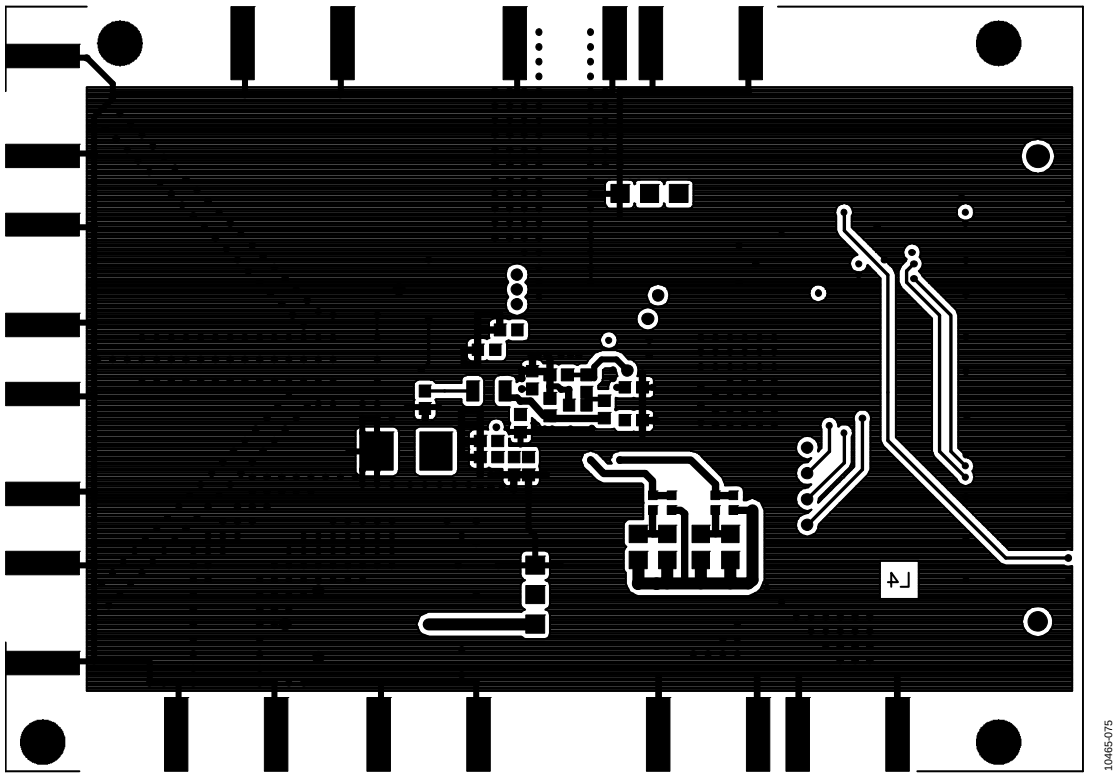

Figure 75. Evaluation Board, Bottom Side—Layer 4

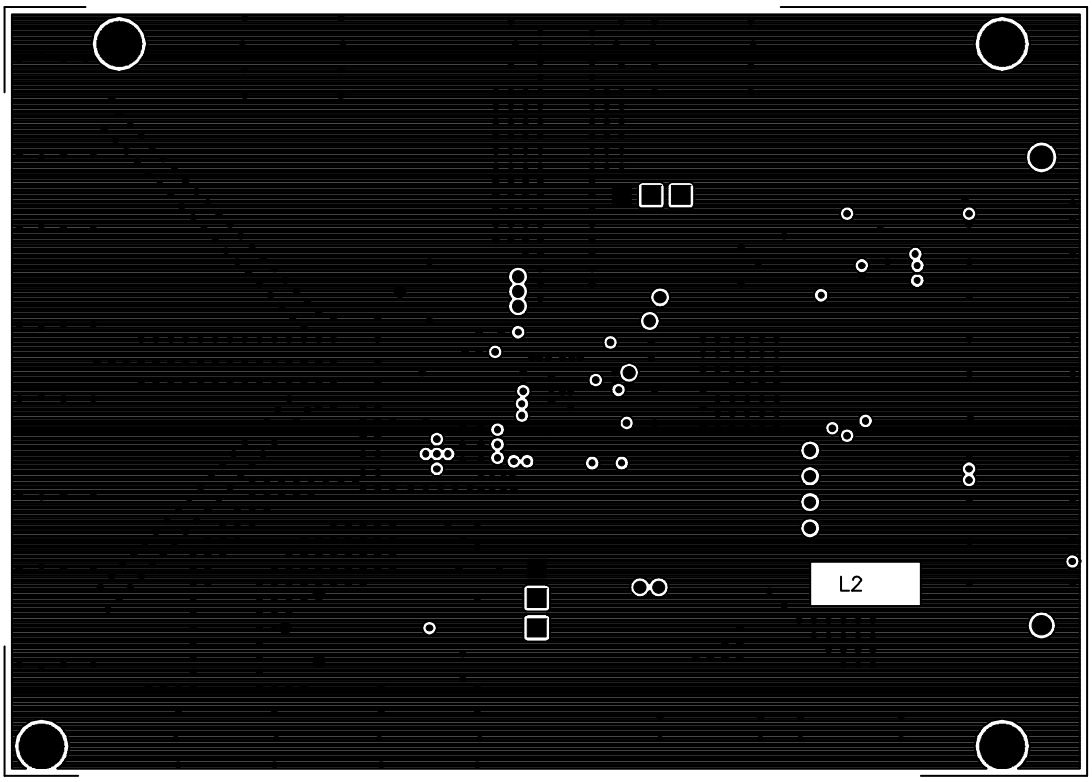

Figure 76. Evaluation Board, Ground—Layer 2

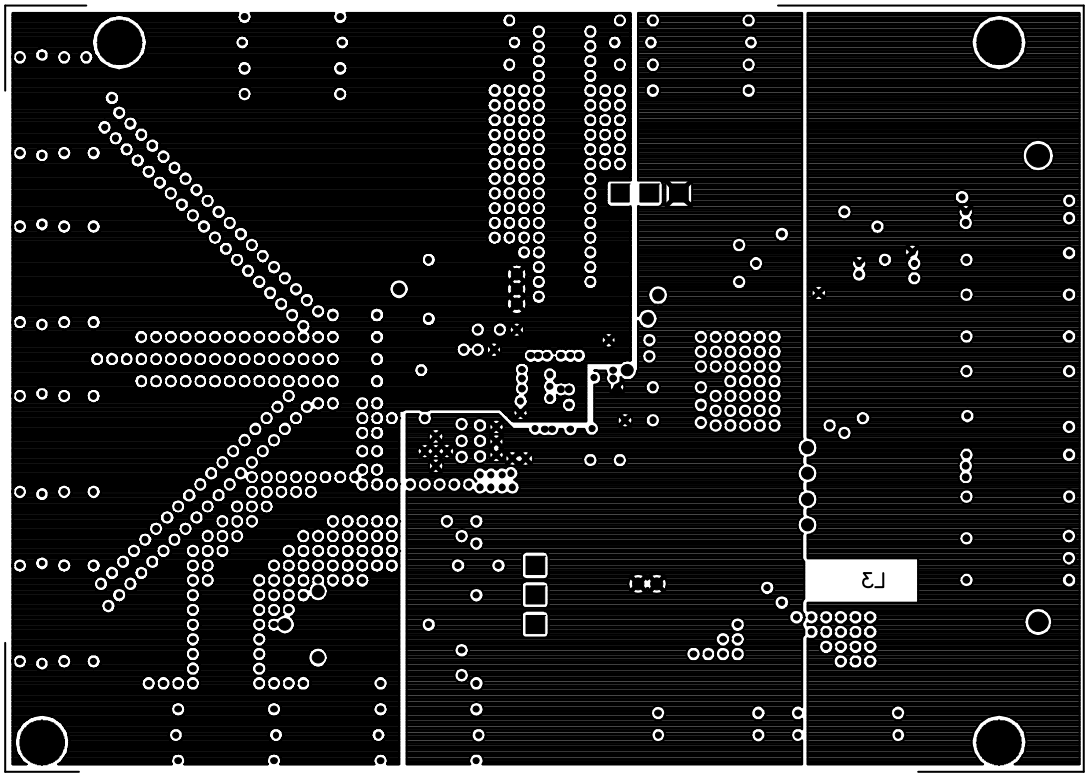

Figure 77. Evaluation Board Power—Layer 3

BILL OF MATERIALS

Table 29. Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Part Number
1	DUT	ADRF6755, 56-lead 8 mm × 8 mm LFCSP	Analog Devices	ADRF6755ACPZ
1	Y2	Crystal Oscillator, 80 MHz	Jauch	O 80.0-JO75-B-3.3-2-T1
1	CONN1	Connector, FX8-120S-SV(21)	Hirose	FEC 1324660
2	C1, C21	Capacitor, 10 µF, 25 V, tantalum, TAJ-C	AVX	FEC 197518
12	C4, C6, C8, C10, C12, C14, C16, C18, C19, C48, C53, C55	Capacitor, 10 pF, 50 V, ceramic, C0G, 0402	Murata	FEC 8819564
14	C5, C7, C9, C11, C13, C15, C17, C22, C47, C49 to C52, C54	Capacitor, 100 nF, 25 V, X7R, ceramic, 0603	AVX	FEC 317287
1	C20	Capacitor, 220 µF, 6.3 V, tantalum, Case Size C	AVX	FEC 197087
4	C30 to C33	Capacitor spacing, 0402 (do not install)		
1	C26	Capacitor, 1.2 nF, 50 V, C0G, ceramic, 0603	Kemet	FEC 1813421
1	C24	Capacitor, 47 nF, 50 V, C0G, ceramic, 1206	Murata	FEC 8820201
2	C23, C25	Capacitor, 560 pF, 50 V, NP0, ceramic, 0603	Murata	FEC 1828912
2	C38, C39	Capacitor, 1 nF, 50 V, C0G, ceramic, 0402	Murata	FEC 8819556
3	C44, C46, C57	Capacitor, 100 pF, 50 V, C0G, ceramic, 0402	Murata	FEC 8819572
11	J2 to J5, J7, J10 to J12, J14, J15, TXDIS	SMA end launch connector	Johnson/Emerson	142-0701-851
2	J18, J21	Jumper, 3-pin + shunt	Harwin	FEC 148533 and FEC 150411
2	L1, L2	Inductor, 20 nH, 0402, 5%	TE Connectivity	FEC 1265424
2	L3, L4	Inductor, 10 µH, 0805, LQM series	Vishay	FEC 1653752
5	R6 to R9, R36	Resistor, 0 Ω, 1/16 W, 1%, 0402	Multicomp	FEC 1357983
2	R10, R11	Resistor, 0402, spacing (do not install)		
1	R13	Resistor, 4.7 kΩ, 1/10 W, 1%, 0603	Bourns	FEC 2008358
2	R12, R16	Resistor, 160 Ω, 1/16 W, 1%, 0603	Multicomp	FEC 9330658
1	R15	Resistor, 150 Ω, 1/16 W, 1%, 0603	Multicomp	FEC 9330593
2	R62	Resistor, 0603, spacing (do not install)		
3	R35, R44, R45	Resistor, 51 Ω, 1/16 W, 5%, 0402	Bourns	FEC 2008358
4	R48 to R51	Resistor, 330 Ω, 1/10 W, 5%, 0805	Vishay	FEC 1739223
3	R59 to R61	Resistor, 100 Ω, 1/10 W, 5%, 0805	Vishay	FEC 1652907
2	R63, R64	Resistor, 100 kΩ, 1/16 W, 1%, 0603	Multicomp	FEC 9330402
1	D1	LED, red, 0805, 1.8 V, low current	Rohm	FEC 1685056
1	U1	IC 24LC32A-I/MS EEPROM MSOP-8	Microchip	FEC 133-4660

OUTLINE DIMENSIONS

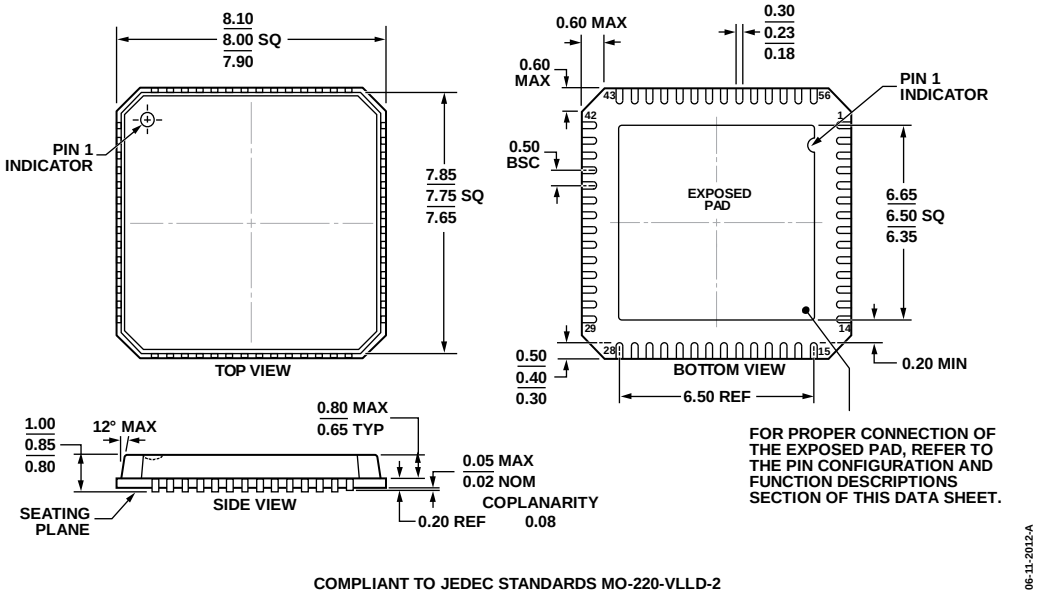

Figure 78. 56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
8 mm × 8 mm Body, Very Thin Quad
(CP-56-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADRF6755ACPZ	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ], Tray	CP-56-4
ADRF6755ACPZ-R7	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 7" Tape and Reel	CP-56-4
EVAL-ADRF6755SDZ		Evaluation Board	
EVAL-SDP-CS1Z		SDP-S Controller Board; Interface to EVAL-ADRF6755SDZ (also required)	
EVAL-SDP-CB1Z		SDP-B Controller Board; Interface to EVAL-ADRF6755SDZ (alternative solution)	

[1] Z = RoHS Compliant Part.
[2] Choose either EVAL-SDP-CS1Z or EVAL-SDP-CB1Z as EVAL-ADRF6755SDZ interface solution.

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