SHARC Processor

ADSP-21371/ADSP-21375

SUMMARY

High performance 32-bit/40-bit floating point processor optimized for high performance audio processing

Single-instruction, multiple-data (SIMD) computational architecture

On-chip memory, ADSP-21371—1M bits of on-chip SRAM and 4M bits of on-chip mask-programmable ROM

On-chip memory, ADSP-21375—0.5M bits of on-chip SRAM and 2M bits of on-chip mask-programmable ROM

Code compatible with all other members of the SHARC family

The ADSP-21371/ADSP-21375 processors are available with a 200/266 MHz core instruction rate with unique audiocentric peripherals such as the digital applications interface, S/PDIF transceiver, serial ports, precision clock generators, and more. For complete ordering information, see Ordering Guide on Page 56.

DEDICATED AUDIO COMPONENTS

ADSP-21371—S/PDIF-compatible digital audio receiver/transmitter

ADSP-21371—8 dual data line serial ports that operate at up to 33 Mbps on each data line — each has a clock, frame sync, and two data lines that can be configured as either a receiver or transmitter pair

16 PWM outputs configured as four groups of four outputs

ROM-based security features include

- **JTAG access to memory permitted with a 64-bit key**
- **Protected memory regions that can be assigned to limit access under program control to sensitive code**

PLL has a wide variety of software and hardware multiplier/divider ratios

Available in a 208-lead LQFP_EP package

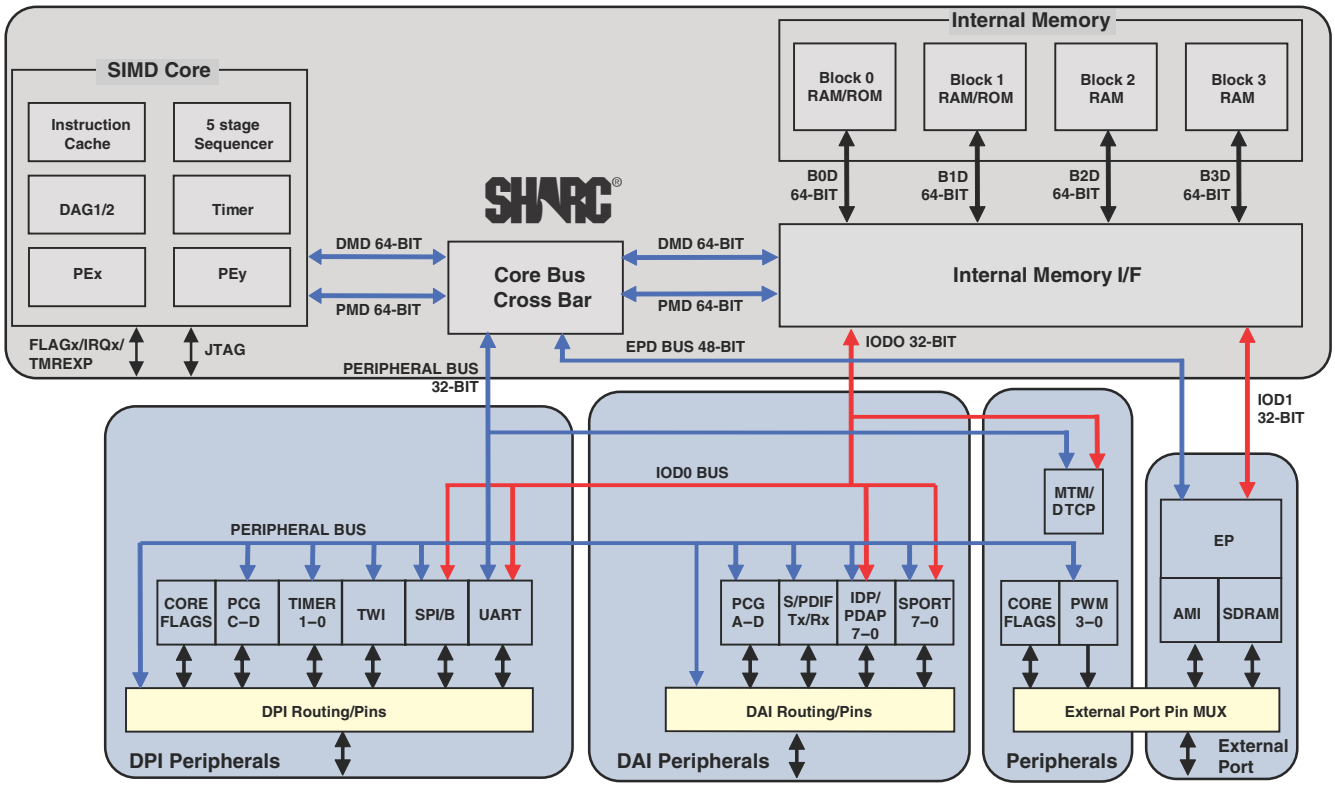

Figure 1. Functional Block Diagram

Rev. D **Document Feedback**

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GENERAL DESCRIPTION

The ADSP-21371/ADSP-21375 SHARC® processors are members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. The processors are source code compatible with the ADSP-2126x, ADSP-2136x, and ADSP-2116x DSPs, as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The processors are 32-bit/40-bit floating-point processors optimized for high performance automotive audio applications with their large on-chip SRAM and mask-programmable ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

As shown in the functional block diagram on Page 1, the processors use two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the processors achieve an instruction cycle time of 3.75 ns at 266 MHz. With its SIMD computational hardware, the processors can perform 1.596 GFLOPS running at 266 MHz.

Table 1 shows performance benchmarks for these devices. Table 2 shows the features of the individual product offerings.

Table 1. Processor Benchmarks (at 266 MHz)

Benchmark Algorithm	Speed (at 266 MHz)
1024 Point Complex FFT (Radix 4, With Reversal)	34.5 µs
FIR Filter (per Tap)[1]	1.88 ns
IIR Filter (per Biquad)[1]	7.5 ns
Matrix Multiply (Pipelined)	
[3 × 3] × [3 × 1]	16.91 ns
[4 × 4] × [4 × 1]	30.07 ns
Divide (y/x)	13.1 ns
Inverse Square Root	20.4 ns

[1] Assumes two files in multichannel SIMD mode

Table 2. ADSP-21371/ADSP-21375 Features

Feature	ADSP-21371	ADSP-21375
Frequency	266 MHz (3.75 ns)	266 MHz (3.75 ns)
RAM	1M bit	0.5M bit
ROM	4M bits	2M bits
Pulse-Width Modulation	Yes	No
Serial Ports	8	4
UART	1	
Digital Application Interface (DAI)	Yes	
Digital Peripheral Interface (DPI)	Yes	
S/PDIF Transceiver	Yes	No
SPI	2	
TWI	Yes	
Package	208-Lead LQFP_EP	

The diagram on Page 1 shows the two clock domains that make up the ADSP-2137x processors. The core clock domain contains the following features:

- Two processing elements, each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (1M bit, ADSP-21371; 0.5M bit, ADSP-21375)
- On-chip mask-programmable ROM (4M bit, ADSP-21371; 2M bit, ADSP-21375)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints which allow flexible exception handling.

The diagram on Page 1 also shows the peripheral clock domains (also known as the I/O processor) and contains the following features:

- IOD0 (peripheral DMA) and IOD1 (external port DMA) buses for 32-bit data transfers
- Peripheral and external port bus for core connection
- Digital applications interface that includes four precision clock generators (PCG), an S/PDIF-compatible digital audio receiver/transmitter, an input data port (IDP), eight serial ports, eight serial interfaces, a 20-bit parallel input port (PDAP), and a flexible signal routing unit (DAI SRU).
- Digital peripheral interface that includes two timers, one UART, two serial peripheral interfaces (SPI), a 2-wire interface (TWI), and a flexible signal routing unit (DPI SRU).
- External port with AMI and SDRAM controller
- Four units for PWM control
- One MTM for internal to internal memory transfers

SHARC FAMILY CORE ARCHITECTURE

The ADSP-21371/ADSP-21375 processors are code compatible at the assembly level with the ADSP-2136x, ADSP-2126x, ADSP-21160x, and ADSP-21161N, and with the first generation ADSP-2106x SHARC processors. The ADSP-21371/ADSP-21375 processors share architectural features with the ADSP-2126x, ADSP-2136x, and ADSP-2116x SIMD SHARC processors, as shown in Figure 2 and detailed in the following sections.

SIMD Computational Engine

The processors contain two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY, and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

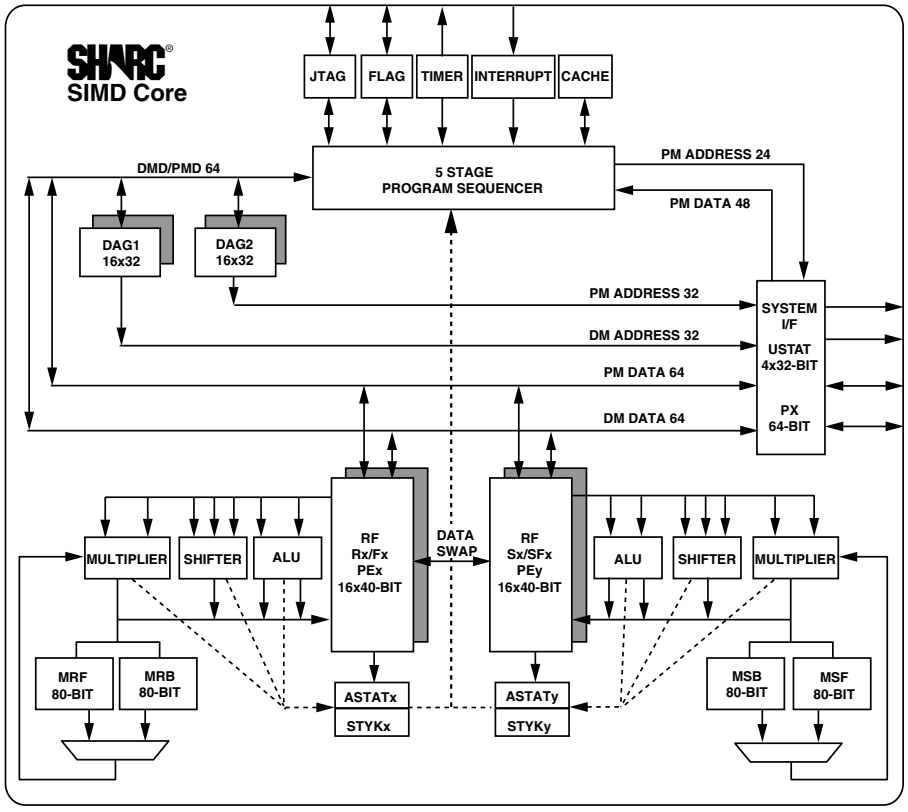


Figure 2. SHARC Core Block Diagram

Data Register File

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the SHARC's enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Context Switch

Many of the processor's registers have secondary registers that can be activated during interrupt servicing for a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result register all have secondary registers. The primary registers are active at reset, while the secondary registers are activated by control bits in a mode control register.

Universal Registers

Universal registers can be used for general purpose tasks. The USTAT (4) registers allow easy bit manipulations (Set, Clear, Toggle, Test, XOR) for all system registers (control/status) of the core.

The data bus exchange register PX permits data to be passed between the 64-bit PM data bus and the 64-bit DM data bus, or between the 40-bit register file and the PM data bus. These registers contain hardware to handle the data width difference.

Timer

The processors contain a core timer that can generate periodic software interrupts. The core timer can be configured to use FLAG3 as a timer expired signal.

Single-Cycle Fetch of an Instruction and Four Operands

The processors feature an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 2). With the processor's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The processors include an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators with Zero-Overhead Hardware Circular Buffer Support

The processors's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the processors can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

On-Chip Memory

The ADSP-21371 processor contains 1 megabit of internal RAM and four megabits of internal mask-programmable ROM (see Table 3 on Page 6) and the ADSP-21375 processor contains 0.5 megabits of internal RAM and two megabits of internal mask-programmable ROM (see Table 4 on Page 7). Each block can be configured for different combinations of code and data storage. Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The processor's memory architecture, in combination with its separate on-chip buses, allow two data transfers from the core and one from the I/O processor, in a single cycle.

The ADSP-21371 processor's SRAM can be configured as a maximum of 32k words of 32-bit data, 64k words of 16-bit data, 21.3k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 1 megabit. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

On-Chip Memory Bandwidth

The internal memory architecture allows four accesses at the same time to any of the four blocks, assuming no block conflicts. The total bandwidth is gained with DMD and PMD buses (2 × 64-bits, core CLK) and the IOD0/1 buses (2 × 32-bit, PCLK).

ROM-Based Security

The processors have a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the processor does not boot-load any

Table 3. ADSP-21371 Internal Memory Space

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 bits)	**Extended Precision Normal or Instruction Word (48 bits)**	**Normal Word (32 bits)**	**Short Word (16 bits)**
BLOCK 0 ROM 0x0004 0000–0x0004 7FFF	BLOCK 0 ROM 0x0008 0000–0x0008 AAA9	BLOCK 0 ROM 0x0008 0000–0x0008 FFFF	BLOCK 0 ROM 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 BFFF	Reserved 0x0008 AAAA–0x0008 FFFF	Reserved 0x0009 0000–0x0009 7FFF	Reserved 0x0012 0000–0x0012 FFFF
BLOCK 0 RAM 0x0004 C000–0x0004 CFFF	BLOCK 0 RAM 0x0009 0000–0x0009 1554	BLOCK 0 RAM 0x0009 8000–0x0009 9FFF	BLOCK 0 RAM 0x0013 0000–0x0013 3FFF
Reserved 0x0004 D000–0x0004 FFFF	Reserved 0x0009 1555–0x0009 FFFF	Reserved 0x0009 A000–0x0009 FFFF	Reserved 0x0013 4000–0x0013 FFFF
BLOCK 1 ROM 0x0005 0000–0x0005 7FFF	BLOCK 1 ROM 0x000A 0000–0x000A AAA9	BLOCK 1 ROM 0x000A 0000–0x000A FFFF	BLOCK 1 ROM 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 BFFF	Reserved 0x000A AAAA–0x000A FFFF	Reserved 0x000B 0000–0x000B 7FFF	Reserved 0x0016 0000–0x0016 FFFF
BLOCK 1 RAM 0x0005 C000–0x0005 CFFF	BLOCK 1 RAM 0x000B 0000–0x000B 1554	BLOCK 1 RAM 0x000B 8000–0x000B 9FFF	BLOCK 1 RAM 0x0017 0000–0x0017 3FFF
Reserved 0x0005 D000–0x0005 FFFF	Reserved 0x000B 1555–0x000B FFFF	Reserved 0x000B A000–0x000B FFFF	Reserved 0x0017 4000–0x0017 FFFF
BLOCK 2 RAM 0x0006 0000–0x0006 0FFF	BLOCK 2 RAM 0x000C 0000–0x000C 1554	BLOCK 2 RAM 0x000C 0000–0x000C 1FFF	BLOCK 2 RAM 0x0018 0000–0x0018 3FFF
Reserved 0x0006 1000–0x0006 FFFF	Reserved 0x000C 1555–0x000D FFFF	Reserved 0x000C 2000–0x000D FFFF	Reserved 0x0018 4000–0x001B FFFF
BLOCK 3 RAM 0x0007 0000–0x0007 0FFF	BLOCK 3 RAM 0x000E 0000–0x000E 1554	BLOCK 3 RAM 0x000E 0000–0x000E 1FFF	BLOCK 3 RAM 0x001C 0000–0x001C 3FFF
Reserved 0x0007 1000–0x0007 FFFF	Reserved 0x000E 1555–0x000F FFFF	Reserved 0x000E 2000–0x000F FFFF	Reserved 0x001C 4000–0x001F FFFF

external code, executing exclusively from internal ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or Test Access Port will be assigned to each customer. The device will ignore a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

FAMILY PERIPHERAL ARCHITECTURE

The ADSP-21371/ADSP-21375 family contains a rich set of peripherals that support a wide variety of applications, including high quality audio, medical imaging, communications, military, test equipment, 3D graphics, speech recognition, monitor control, imaging, and other applications.

External Port

The external port on the ADSP-21371/ADSP-21375 SHARC processors provide a high performance, glueless interface to a wide variety of industry-standard memory devices. The 32-bit wide bus (ADSP-21371) may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers: the first is an SDRAM controller for connection of industry-standard synchronous DRAM devices and DIMMs (dual inline memory module), while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types.

Table 4. ADSP-21375 Internal Memory Space

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 bits)	**Extended Precision Normal or Instruction Word (48 bits)**	**Normal Word (32 bits)**	**Short Word (16 bits)**
BLOCK 0 ROM 0x0004 0000–0x0004 3FFF	BLOCK 0 ROM 0x0008 0000–0x0008 5554	BLOCK 0 ROM 0x0008 0000–0x0008 7FFF	BLOCK 0 ROM 0x0010 0000–0x0010 FFFF
Reserved 0x0004 4000–0x0004 BFFF	Reserved 0x0008 5555–0x0008 FFFF	Reserved 0x0008 8000–0x0009 7FFF	Reserved 0x0011 0000–0x0012 FFFF
BLOCK 0 RAM 0x0004 C000–0x0004 C7FF	BLOCK 0 RAM 0x0009 0000–0x0009 0AA9	BLOCK 0 RAM 0x0009 8000–0x0009 8FFF	BLOCK 0 RAM 0x0013 0000–0x0013 1FFF
Reserved 0x0004 C800–0x0004 FFFF	Reserved 0x0009 0AAA–0x0009 FFFF	Reserved 0x0009 9000–0x0009 FFFF	Reserved 0x0013 2000–0x0013 FFFF
BLOCK 1 ROM 0x0005 0000–0x0005 3FFF	BLOCK 1 ROM 0x000A 0000–0x000A 5554	BLOCK 1 ROM 0x000A 0000–0x000A 7FFF	BLOCK 1 ROM 0x0014 0000–0x0014 FFFF
Reserved 0x0005 4000–0x0005 BFFF	Reserved 0x000A 5555–0x000A FFFF	Reserved 0x000A 8000–0x000B 7FFF	Reserved 0x0015 0000–0x0016 FFFF
BLOCK 1 RAM 0x0005 C000–0x0005 C7FF	BLOCK 1 RAM 0x000B 0000–0x000B 0AA9	BLOCK 1 RAM 0x000B 8000–0x000B 8FFF	BLOCK 1 RAM 0x0017 0000–0x0017 1FFF
Reserved 0x0005 C800–0x0005 FFFF	Reserved 0x000B 0AAA–0x000B FFFF	Reserved 0x000B 9000–0x000B FFFF	Reserved 0x0017 2000–0x0017 FFFF
BLOCK 2 RAM 0x0006 0000–0x0006 07FF	BLOCK 2 RAM 0x000C 0000–0x000C 0AA9	BLOCK 2 RAM 0x000C 0000–0x000C 0FFF	BLOCK 2 RAM 0x0018 0000–0x0018 1FFF
Reserved 0x0006 0800–0x0006 FFFF	Reserved 0x000C 0AAA–0x000D FFFF	Reserved 0x000C 1000–0x000D FFFF	Reserved 0x0018 2000–0x001B FFFF
BLOCK 3 RAM 0x0007 0000–0x0007 07FF	BLOCK 3 RAM 0x000E 0000–0x000E 0AA9	BLOCK 3 RAM 0x000E 0000–0x000E 0FFF	BLOCK 3 RAM 0x001C 0000–0x001C 1FFF
Reserved 0x0007 0800–0x0007 FFFF	Reserved 0x000E 0AAA–0x000F FFFF	Reserved 0x000E 1000–0x000F FFFF	Reserved 0x001C 2000–0x001F FFFF

SDRAM Controller

The SDRAM controller provides an interface to up to four separate banks of industry-standard SDRAM devices or DIMMs. Fully compliant with the SDRAM standard, each bank has its own memory select line ($\overline{MS0}$–$\overline{MS3}$), and can be configured to contain between 16M bytes and 256M bytes of memory. SDRAM external memory address space is shown in Table 5.

The controller maintains all of the banks as a contiguous address space so that the processor sees this as a single address space, even if different size devices are used in the different banks.

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. The memory banks can be configured as 16 bits wide or as 32 bits wide. The SDRAM controller address, data, clock, and command pins can drive loads up to 30 pF. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

Table 5. External Memory for SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000–0x03FF FFFF
Bank 1	64M	0x0400 0000–0x07FF FFFF
Bank 2	64M	0x0800 0000–0x0BFF FFFF
Bank 3	64M	0x0C00 0000–0x0FFF FFFF

Note that the external memory bank addresses shown in Table 5 are for normal word accesses. If 48-bit instructions are placed in any such bank (with two instructions packed into three 32-bit locations), then care must be taken to map data buffers in the same bank. For example, if 2k instructions are placed starting at the bank 0 base address (0x0020 0000), then the data buffers can be placed starting at an address that is offset by 3k words (0x0020 0C00).

External Memory Code Execution

The program sequencer can execute code directly from external memory bank 0 (SRAM, SDRAM) over the 48-bit external port data bus (EPD). This allows a reduction in internal memory size, thereby reducing the die area. Because instructions on the

SHARC processor are 48 bits wide, instruction throughput when executing code from external SDRAM memory is 2 instructions every 3 SDCLK (peripheral) clock cycles over a 32-bit wide external port, and 2 instructions every 6 SDCLK clock cycles over a 16-bit external port. Non SDRAM external memory address space is shown in Table 6.

Table 6. External Memory for Non SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	14M	0x0020 0000–0x00FF FFFF
Bank 1	16M	0x0400 0000–0x04FF FFFF
Bank 2	16M	0x0800 0000–0x08FF FFFF
Bank 3	16M	0x0C00 0000–0x0CFF FFFF

External Port Throughput

The throughput for the external port, based on 133 MHz clock and 32-bit data bus, is 177M bytes/s for the AMI and 532M bytes/s for SDRAM.

Asynchronous Memory Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, ROM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 14.7M word window and banks 1, 2, and 3 occupy a 16M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic. The banks can also be configured as 8-bit or 16-bit wide buses for ease of interfacing to a range of memories and I/O devices tailored either to high performance or to low cost and power.

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs each. Therefore, this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the mid-point of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the mid-point of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

Digital Applications Interface (DAI)

The digital applications interface (DAI) provides the ability to connect various peripherals to any of the processor's DAI pins (DAI_P1 to DAI_P20).

Programs make these connections using the signal routing unit (SRU), shown in Figure 1.

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

In the ADSP-21371, the DAI includes eight serial ports, four precision clock generators (PCG), and an input data port (IDP). For the ADSP-21375, the DAI includes four serial ports, four precision clock generators (PCG) and an input data port (IDP).

The IDP provides an additional input path to the core of the processor, configurable as either eight channels of I^2S serial data, or a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

Serial Ports

The processors feature eight synchronous serial ports on the ADSP-21371 and four on the ADSP-21375. The SPORTs provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

For the ADSP-21371, serial ports are enabled via 16 programmable pins and simultaneous receive or transmit pins that support up to 32 transmit or 32 receive channels of audio data when all eight SPORTs are enabled, or eight duplex TDM streams of 128 channels per frame.

For the ADSP-21375, serial ports are enabled via eight programmable pins and simultaneous receive or transmit pins that support up to 16 transmit or 16 receive channels of audio data when all four SPORTs are enabled, or four duplex TDM streams of 128 channels per frame.

The serial ports operate at a maximum data rate of $f_{PCLK}/4$. Serial port data can be automatically transferred to and from on-chip memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode with support for packed I²S mode
- I²S mode
- Packed I²S mode
- Left-justified sample pair mode

Left-justified sample pair mode is a mode where in each frame sync cycle two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified sample pair and I²S protocols (I²S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs such as the Analog Devices AD183x family), with two data pins, allowing four left-justified sample pair or I²S channels (using two stereo devices) per serial port, with a maximum of up to 32 I²S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified sample pair and I²S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

The serial ports also contain frame sync error detection logic where the serial ports detect frame syncs that arrive early (for example frame syncs that arrive while the transmission/reception of the previous word is occurring). All the serial ports also share one dedicated error interrupt.

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The ADSP-21371 S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left justified, I²S or right justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), and are controlled by the SRU control registers.

The ADSP-21375 does not have an S/PDIF-compatible digital receiver/transmitter.

Input Data Port (IDP)

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I²S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processor supports 24- and 32-bit I²S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

Precision Clock Generator (PCG)

The precision clock generators (PCG) consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A B, C, and D, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface (SPI) ports, one universal asynchronous receiver-transmitter (UART), 12 flags, a 2-wire interface (TWI), and two general-purpose timers.

Serial Peripheral (Compatible) Interface

The ADSP-21371/ADSP-21375 SHARC processors contain two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible ports of the processors to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device.

The SPI-compatible peripheral implementation also features programmable baud rates and clock phases and polarities. The SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

UART Port

The processors provide a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated

DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable. The port:

- Supports bit rates ranging from (f_{PCLK}/1,048,576) to (f_{PCLK}/16) bits per second.
- Supports data formats from 7 to 12 bits per frame.
- Can be configured to generate maskable interrupts for both transmit and receive operations.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

Peripheral Timers

Two general-purpose timers can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

Each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables the general-purpose timers independently.

2-Wire Interface Port (TWI)

The TWI is a bidirectional 2-wire serial bus used to move 8-bit data while maintaining compliance with the I^2C bus protocol. The TWI master incorporates the following features:

- Simultaneous master and slave operation on multiple device systems with support for multi master data arbitration
- Digital filtering and timed event processing
- 7-bit addressing
- 100 kbps and 400 kbps data rates
- Low interrupt rate

I/O PROCESSOR FEATURES

The I/O processor provides many channels of DMA and controls the extensive set of peripherals described in the previous sections.

DMA Controller

The processor's on-chip DMA controller allows data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-2137x processor's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP), or the UART (see Table 7).

Table 7. DMA Channels

Peripheral	ADSP-21371	ADSP-21375
SPORT	16	8
PDAP	8	8
SPI	2	2
UART	2	2
EP	2	2
MTM/DTCP	2	2
Total DMA Channels	32	24

Delay Line DMA

The processors provide delay line DMA functionality. This allows processor reads and writes to external delay line buffers (and hence to external memory) with limited core interaction.

Scatter/Gather DMA

The ADSP-2137x processor provides scatter/gather DMA functionality. This allows processor DMA reads/writes to/from noncontiguous memory blocks.

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues. For complete system design information, see the *ADSP-2137x SHARC Processor Hardware Reference*.

Program Booting

The internal memory of the processor boots at system power-up from an 8-bit EPROM via the external port, an SPI master, or an SPI slave. Booting is determined by the boot configuration (BOOT_CFG1–0) pins in Table 8. Selection of the boot source is controlled via the SPI as either a master or slave device, or it can immediately begin executing from ROM.

Table 8. Boot Mode Selection

BOOT_CFG1–0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	EPROM/FLASH Boot
11	No boot (processor executes from internal ROM after reset)

The "Running Reset" feature allows programs to perform a reset of the processor core and peripherals, but without resetting the PLL and SDRAM controller, or performing a boot. The $\overline{\text{RESET-OUT}}$ pin acts as the input for initiating a running reset.

Power Supplies

The processors have separate power supply connections for the internal (V_{DDINT}), and external (V_{DDEXT}) power supplies. The internal supplies must meet the 1.2 V requirement. The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same power supply.

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the processor to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading
or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate "Emulator Hardware User's Guide".

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *"Analog Devices JTAG Emulation Technical Reference"* (EE-68) on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the processor's architecture and functionality. For detailed information on the core architecture and instruction set, refer to the *ADSP-2137x SHARC Processor Hardware Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Circuits from the Lab™ site (www.analog.com/signal chains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

The following symbols appear in the Type column of Table 9:
A = asynchronous, I = input, O = output, S = synchronous,
(A/D) = active drive, (O/D) = open drain, and T = three-state,
(pd) = pull-down resistor, (pu) = pull-up resistor.

Table 9. Pin Descriptions

Name	Type	State During and After Reset	Description
$ADDR_{23-0}$	O/T (pu)	Pulled high/ driven low	**External Address.** The processor outputs addresses for external memory and peripherals on these pins.
$DATA_{31-0}$	I/O (pu)	Pulled high/ pulled high	**External Data.** The data pins can be multiplexed to support the external memory interface data (I/O), the PDAP (I) (PDAP for ADSP-21371), FLAGS (I/O) and PWM (O). After reset, all DATA pins are in EMIF mode and FLAG(0–3) pins are in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the external port data pins for parallel input data. PDAP over 16-bit external port DATA is not supported on the ADSP-21375 processor.
DAI $_P_{20-1}$	I/O with programmable (pu)[1]	Pulled high/ pulled high	**Digital Applications Interface Pins**. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audio-centric peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determine the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins. The DAI SRU provides the connection from the serial ports, the S/PDIF module (ADSP-21371), IDP (2), and the PCGs (4), to the DAI_P20–1 pins. Pullups can be disabled via the DAI_PIN_PULLUP register.
DPI $_P_{14-1}$	I/O with programmable (pu)[1]	Pulled high/ pulled high	**Digital Peripheral Interface.** These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins. The DPI SRU provides the connection from the timers (2), SPIs (2), UART (1), flags (12), and general-purpose I/O (9) to the DPI_P14–1 pins. Pull-ups can be disabled via the DPI_PIN_PULLUP register.
ACK	I (pu)		**Memory Acknowledge.** External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{RD}$	O/T (pu)	Pulled high/ driven high	**External Port Read Enable.** $\overline{RD}$ is asserted whenever the processor reads a word from external memory. $\overline{RD}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{WR}$	O/T (pu)	Pulled high/ driven high	**External Port Write Enable.** $\overline{WR}$ is asserted when the processor writes a word to external memory. $\overline{WR}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{SDRAS}$	O/T (pu)	Pulled high/ driven high	**SDRAM Row Address Strobe.** Connect to SDRAM's RAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{SDCAS}$	O/T (pu)	Pulled high/ driven high	**SDRAM Column Address Select.** Connect to SDRAM's CAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{SDWE}$	O/T (pu)	Pulled high/ driven high	**SDRAM Write Enable.** Connect to SDRAM's WE or W buffer pin.

Table 9. Pin Descriptions (Continued)

Name	Type	State During and After Reset	Description
SDCKE	O/T (pu)	Pulled high/ driven high	**SDRAM Clock Enable.** Connect to SDRAM's CKE pin. Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	O/T (pu)	Pulled high/ driven low	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with a non-SDRAM accesses. This pin replaces the DSP's A10 pin only during SDRAM accesses.
SDCLK	O/T	High-Z/driving	**SDRAM Clock.**
$\overline{MS}_{0-1}$	O/T (pu)	Pulled high/ driven high	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. The $\overline{MS1}$ pin can be used in EPORT/FLASH boot mode. For more information, see the *ADSP-2137x SHARC Processor Hardware Reference*.
FLAG[0]/$\overline{IRQ0}$	I/O	FLAG[0] INPUT	**FLAG0/Interrupt Request0.**
FLAG[1]/$\overline{IRQ1}$	I/O	FLAG[1] INPUT	**FLAG1/Interrupt Request1.**
FLAG[2]/$\overline{IRQ2}$/ $\overline{MS2}$	I/O with programmable pu (for MS mode)	FLAG[2] INPUT	**FLAG2/Interrupt Request/Memory Select2.**
FLAG[3]/ TMREXP/ $\overline{MS3}$	I/O with programmable pu (for MS mode)	FLAG[3] INPUT	**FLAG3/Timer Expired/Memory Select3.**
TDI	I (pu)		**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 22.5 kΩ internal pull-up resistor.
TDO	O/T		**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
TMS	I (pu)		**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 22.5 kΩ internal pull-up resistor.
TCK	I		**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the processor.
$\overline{TRST}$	I (pu)		**Test Reset (JTAG).** Resets the test state machine. $\overline{TRST}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor. $\overline{TRST}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{EMU}$	O (O/D) (pu)		**Emulation Status.** Must be connected to the processor. Analog Devices DSP Tools product line of JTAG emulators target board connector only. $\overline{EMU}$ has a 22.5 kΩ internal pull-up resistor.
CLK_CFG_{1-0}	I		**Core to CLKIN Ratio Control.** These pins set the start up clock frequency. See the *ADSP-2137x SHARC Processor Hardware Reference* for a description of the clock configuration modes. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset.
$BOOT\_CFG_{1-0}$	I		**Boot Configuration Select.** These pins select the boot mode for the processor. The BOOT_CFG pins must be valid before reset is asserted. See the *ADSP-2137x SHARC Processor Hardware Reference* for information about boot modes.

Table 9. Pin Descriptions (Continued)

Name	Type	State During and After Reset	Description
$\overline{\text{RESET}}$	I		**Processor Reset.** Resets the processor to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
XTAL	O		**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal.
CLKIN	I		**Local Clock In.** Used in conjunction with XTAL. CLKIN is the processor clock input. It configures the processor to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processor to use the external clock source such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency.
$\overline{\text{RESETOUT}}$/ $\overline{\text{RUNRSTIN}}$	I/O (pu)		**Reset Out/Running Reset In.** The default setting is reset out. This pin also has a second function as $\overline{\text{RUNRSTIN}}$, which is enabled by setting bit 0 of the RUNRSTCTL register. For more information, see the *ADSP-2137x SHARC Processor Hardware Reference*.

[1] Pull-up can be enabled/disabled, value of pull-up cannot be programmed.

ADSP-21371/ADSP-21375 SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	0.95	1.05	1.14	1.26	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	3.13	3.47	V
V_{IH}[2]	High Level Input Voltage @ V_{DDEXT} = Max	2.0	V_{DDEXT} + 0.5	2.0	V_{DDEXT} + 0.5	V
V_{IL}[2]	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+0.8	–0.5	+0.8	V
V_{IH_CLKIN}[3]	High Level Input Voltage @ V_{DDEXT} = Max	1.74	V_{DDEXT} + 0.5	1.74	V_{DDEXT} + 0.5	V
V_{IL_CLKIN}[3]	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+1.10	–0.5	+1.10	V
$T_{JUNCTION}$	Junction Temperature 208-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C	N/A	N/A	0	95	°C
$T_{JUNCTION}$	Junction Temperature 208-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	N/A	N/A	–40	+110	°C
$T_{JUNCTION}$	Junction Temperature 208-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +105°C	–40	+120	N/A	N/A	°C

[1] Specifications subject to change without notice.

[2] Applies to input and bidirectional pins: ADDR23–0, DATA31–0 (DATA15–0 on ADSP-21375), FLAG3–0, DAI_Px, DPI_Px, $\overline{SPIDS}$, BOOT_CFGx, CLK_CFGx, $\overline{RUNRSTIN}$, $\overline{RESET}$, TCK, TMS, TDI, $\overline{TRST}$.

[3] Applies to input pin CLKIN.

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	1.0 V, 200 MHz			1.2 V, 266 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OH}[2]	High Level Output Voltage	@ V_{DDEXT} = Min, I_{OH} = –1.0 mA[3]	2.4			2.4			V
V_{OL}[2]	Low Level Output Voltage	@ V_{DDEXT} = Min, I_{OL} = 1.0 mA[3]			0.4			0.4	V
I_{IH}[4, 5]	High Level Input Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} max			10			10	µA
I_{IL}[4]	Low Level Input Current	@ V_{DDEXT} = Max, V_{IN} = 0 V			10			10	µA
I_{ILPU}[5]	Low Level Input Current Pull-up	@ V_{DDEXT} = Max, V_{IN} = 0 V			200			200	µA
I_{OZH}[6, 7]	Three-State Leakage Current	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max			10			10	µA
I_{OZL}[6]	Three-State Leakage Current	@ V_{DDEXT}= Max, V_{IN} = 0 V			10			10	µA
I_{OZLPU}[7]	Three-State Leakage Current Pull-up	@ V_{DDEXT}= Max, V_{IN} = 0 V			200			200	µA
$I_{DD-INTYP}$[8, 9]	Supply Current (Internal)	1.0V, 200 MHz: t_{CCLK} = 5.00 ns, V_{DDINT} = 1.0 V, 25ºC		400					mA
		1.2V, 266 MHz: t_{CCLK} = 3.75 ns, V_{DDINT} = 1.2 V, 25ºC					600		mA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN}= 1.2 V			4.7			4.7	pF

[1] Specifications subject to change without notice.

[2] Applies to output and bidirectional pins: ADDR23–0, DATA31–0 (DATA15–0 on ADSP-21375), $\overline{RD}$, $\overline{WR}$, FLAG3–0, DAI_Px, DPI_Px, $\overline{EMU}$, TDO, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, and SDCLK.

[3] See Output Drive Currents on Page 49 for typical drive current capabilities.

[4] Applies to input pins: BOOT_CFGx, CLKCFGx, TCK, $\overline{RESET}$, CLKIN.

[5] Applies to input pins with 22.5 kΩ internal pull-ups: $\overline{TRST}$, TMS, TDI.

[6] Applies to three-statable pins: FLAG3–0.

[7] Applies to three-statable pins with 22.5 kΩ pull-ups: DAI_Px, DPI_Px, $\overline{EMU}$.

[8] Typical internal current data reflects nominal operating conditions.

[9] See Engineer-to-Engineer Note *"Estimating Power Dissipation for ADSP-2137x SHARC Processors"* (EE-318) for further information.

[10] Applies to all signal pins.

[11] Guaranteed, but not tested.

PACKAGE INFORMATION

The information presented in Figure 3 provides details about the package branding for the ADSP-21371/ADSP-21375 processor. For a complete listing of product availability, see Ordering Guide on Page 56.

Figure 3. Typical Package Brand

Table 10. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

MAXIMUM POWER DISSIPATION

See Engineer-to-Engineer Note *"Estimating Power Dissipation for ADSP-2137x SHARC Processors"* (EE-318) for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 50.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 11 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 11. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.5 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage –0.5 V to V_{DDEXT}	+0.5 V
Output Voltage Swing –0.5 V to V_{DDEXT}	+0.5 V

Table 11. Absolute Maximum Ratings (Continued)

Parameter	Rating
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature under Bias	125°C

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See Figure 38 on Page 49 under Test Conditions for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see Figure 4). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Voltage Controlled Oscillator

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in Table 14.

- The product of CLKIN and PLLM must never exceed 1/2 f_{VCO} (max) in Table 14 if the input divider is not enabled (INDIV = 0).
- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in Table 14 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$f_{VCO} = 2 \times PLLM \times f_{INPUT}$
$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div (2 \times PLLD)$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLD = 1, 2, 4, 8 based on the PLLD value programmed on the PMCTL register. During reset this value is 1.

f_{INPUT} = Input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled or

f_{INPUT} = CLKIN ÷ 2 when the input divider is enabled

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in Table 12. All of the timing specifications for the ADSP-2137x peripherals are defined in relation to t_{PCLK}. See the peripheral specific section for each peripheral's timing information.

Table 12. Clock Periods

Timing Requirements	Description
t_{CK}	CLKIN Clock Period
t_{CCLK}	Processor Core Clock Period
t_{PCLK}	Peripheral Clock Period = 2 × t_{CCLK}

Figure 4 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the *ADSP-2137x SHARC Processor Hardware Reference*.

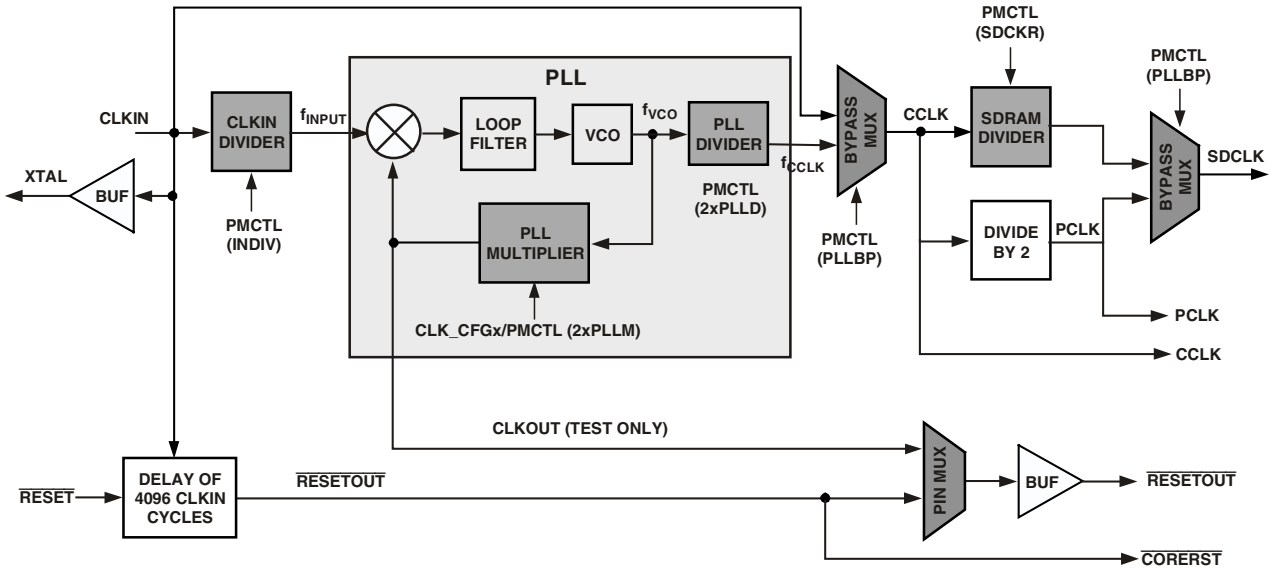


Figure 4. Core Clock and System Clock Relationship to CLKIN

Power-Up Sequencing

The timing requirements for processor startup are given in Table 13.

Note that during power-up, a leakage current of approximately 200 µA may be observed on the $\overline{\text{RESET}}$ pin. This leakage current results from the weak internal pull-up resistor on this pin being enabled during power-up.

Table 13. Power Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} On	0		ns
$t_{IVDDEVDD}$	V_{DDINT} on Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD} [1]	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10 [2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20 [3]		µs
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096 \times t_{CK} + 2 \times t_{CCLK}$ [4, 5]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.2 and 3.3 volt rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's datasheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4096 cycle count depends on t_{SRST} specification in Table 15. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

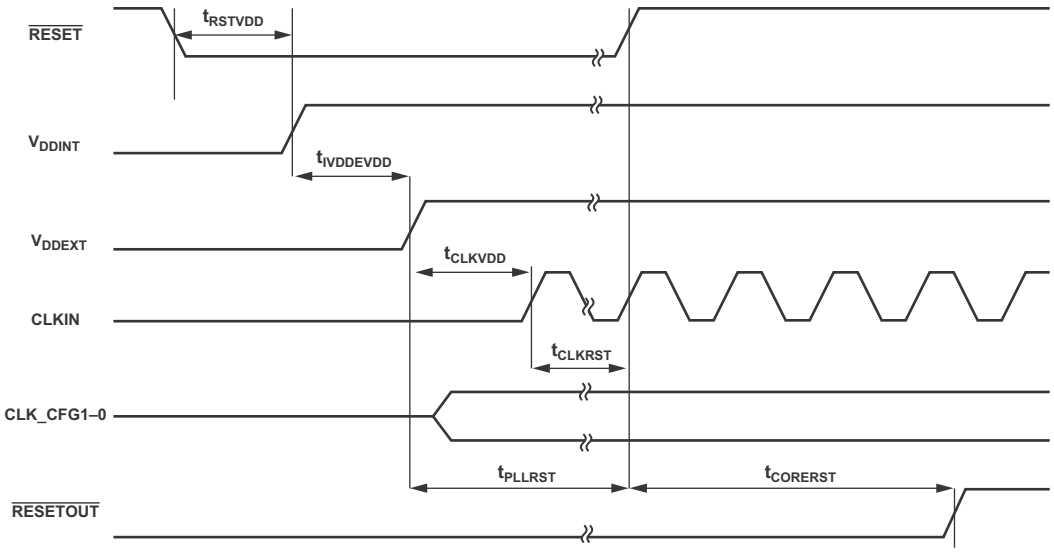


Figure 5. Power-Up Sequencing

Clock Input

Table 14. Clock Input

Parameter		200 MHz Min	200 MHz Max	266 MHz Min	266 MHz Max	Unit
Timing Requirements						
t_{CK}	CLKIN Period	30[1]	100	22.5[1]	100	ns
t_{CKL}	CLKIN Width Low	15[1]	45	11.25[1]	45	ns
t_{CKH}	CLKIN Width High	15[1]	45	11.25[1]	45	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		6		6	ns
t_{CCLK}[2]	CCLK Period	5	10	3.75	10	ns
f_{VCO}	VCO Frequency	200	800	200	800	MHz

[1] Applies only for CLKCFG1–0 = 00 and default values for PLL control bits in the PMCTL register.
[2] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.

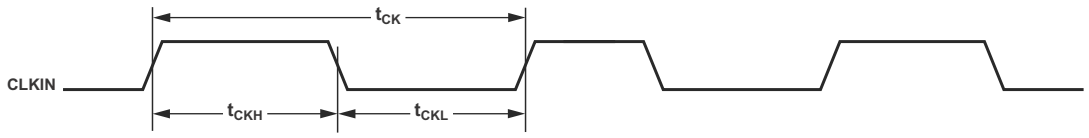


Figure 6. Clock Input

Clock Signals

The processor can use an external clock or a crystal. See the CLKIN pin description in Table 9. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 7 shows the component connections used for a crystal operating in fundamental mode. Note that the clock rate is achieved using a 16.67 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 266 MHz). To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

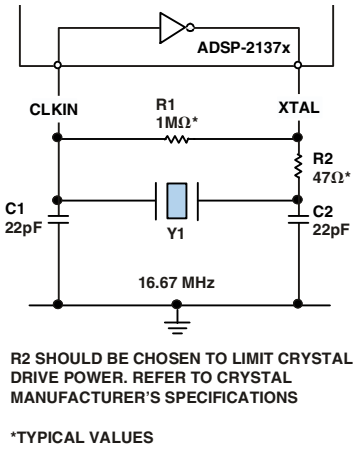


Figure 7. 266 MHz Operation (Fundamental Mode Crystal)

Reset

Table 15. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}[1]	$\overline{\text{RESET}}$ Pulse Width Low	$4 \times t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

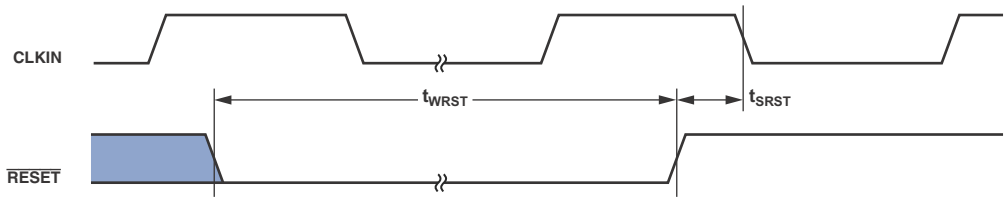


Figure 8. Reset

Running Reset

The following timing specification applies to the $\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$ pin when it is configured as $\overline{\text{RUNRSTIN}}$.

Table 16. Running Reset

Parameter		Min	Max	Unit
Timing Requirements				
$t_{WRUNRST}$	Running $\overline{\text{RESET}}$ Pulse Width Low	$4 \times t_{CK}$		ns
$t_{SRUNRST}$	Running $\overline{\text{RESET}}$ Setup Before CLKIN High	8		ns

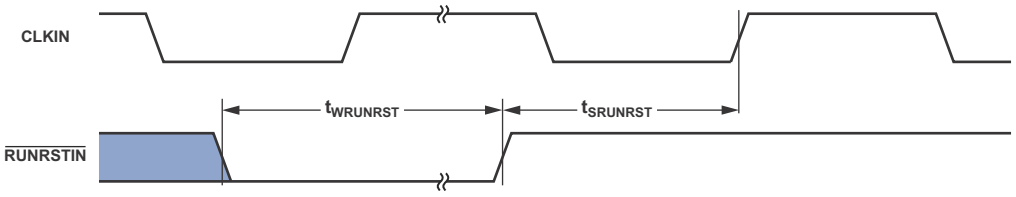


Figure 9. Running Reset

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP pin).

Table 17. Core Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{WCTIM}	TMREXP Pulse Width	$4 \times t_{PCLK} - 1$		ns

Figure 10. Core Timer

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$ interrupts as well as the DAI_P20–1 and DPI_P14–1 pins when they are configured as interrupts.

Table 18. Interrupts

Parameter		Min	Max	Unit
Timing Requirement				
t_{IPW}	$\overline{IRQx}$ Pulse Width	$2 \times t_{PCLK} + 2$		ns

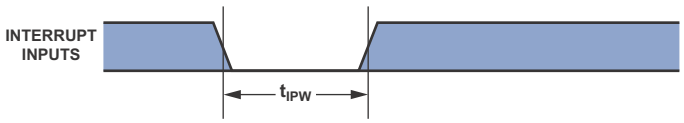


Figure 11. Interrupts

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer0 and Timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the specifications provided below are valid at the DPI_P14–1 pins.

Table 19. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

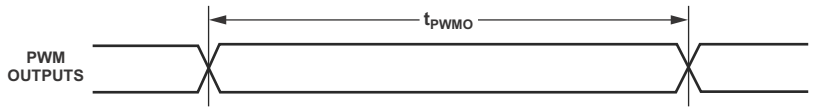


Figure 12. Timer PWM_OUT Timing

Timer WDTH_CAP Timing

The following timing specification applies to Timer0 and Timer1 in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the specifications provided below are valid at the DPI_P14–1 pins.

Table 20. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

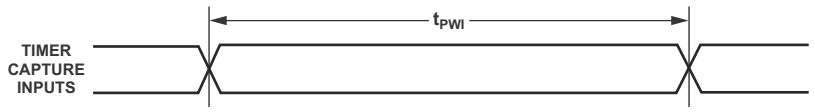


Figure 13. Timer Width Capture Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 21. DAI/DPI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid	1.5	10	ns

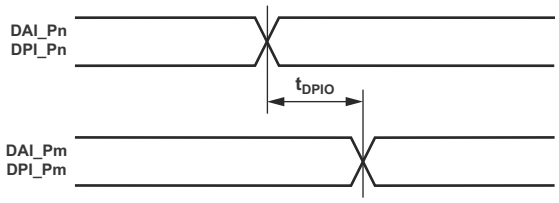


Figure 14. DAI/DPI Pin to Pin Direct Routing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 through DAI_P20).

Table 22. Precision Clock Generator (Direct Pin Routing)

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Timing Requirements						
t_{PCGIP}	Input Clock Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		3		ns
Switching Characteristics						
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	12.8	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + ((2.5) \times t_{PCGIW})$	$12.8 + ((2.5) \times t_{PCGIW})$	$2.5 + ((2.5) \times t_{PCGIW})$	$10 + ((2.5) \times t_{PCGIW})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIW})$	$12.8 + ((2.5 + D - PH) \times t_{PCGIW})$	$2.5 + ((2.5 + D - PH) \times t_{PCGIW})$	$10 + ((2.5 + D - PH) \times t_{PCGIW})$	ns
t_{PCGOW}[1]	Output Clock Period	$2 \times t_{PCGIW} - 1$		$2 \times t_{PCGIW} - 1$		ns

D = FSxDIV, PH = FSxPHASE. For more information, see the *ADSP-2137x SHARC Processor Hardware Reference*, "Precision Clock Generators" chapter.

[1] Normal mode of operation.

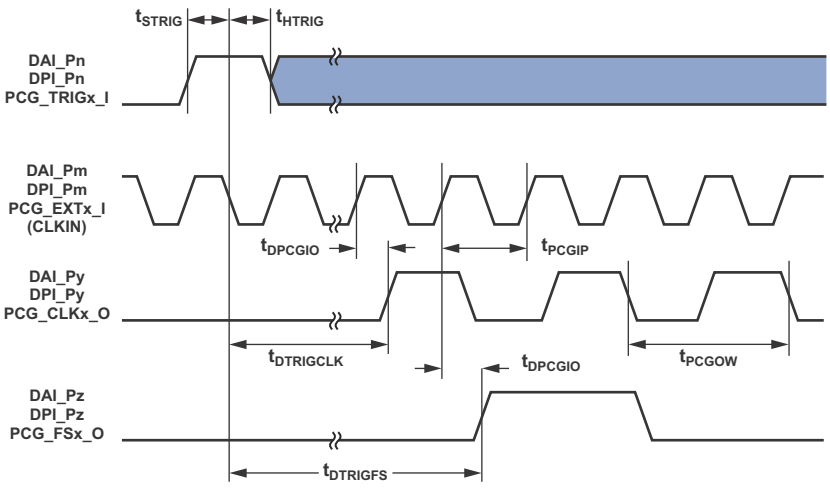


Figure 15. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications provided below apply to the FLAG3–0 and DPI_P14–1 pins, and the DATA31–0 pins. See Table 9 on Page 13 for more information on flag use.

Table 23. Flags

Parameter		Min	Max	Unit
Timing Requirement				
t_{FIPW}	DPI_P14–1, DATA31–0, FLAG3–0 $_{IN}$ Pulse Width	$2 \times t_{PCLK} + 3$		ns
Switching Characteristic				
t_{FOPW}	DPI_P14–1, DATA31–0, FLAG3–0 $_{OUT}$ Pulse Width	$2 \times t_{PCLK} - 2$		ns

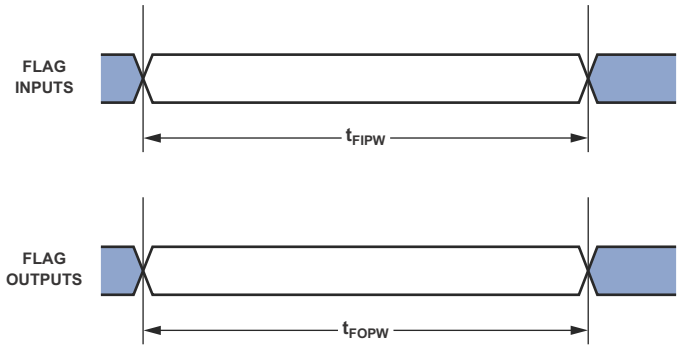


Figure 16. Flags

SDRAM Interface Timing

Maximum SDRAM frequency for 1.2 V is 133 MHz SDCLK.

Table 24. SDRAM Interface Timing[1]

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Timing Requirements						
t_{SSDAT}	DATA Setup Before SDCLK	0.58		0.58		ns
t_{HSDAT}	DATA Hold After SDCLK	2.2		2.2		ns
Switching Characteristics						
t_{SDCLK}	SDCLK Period	10		7.5		ns
t_{SDCLKH}	SDCLK Width High	4		3		ns
t_{SDCLKL}	SDCLK Width Low	4		3		ns
t_{DCAD}	Command, ADDR, Data Delay After SDCLK[2]		6.4		5.3	ns
t_{HCAD}	Command, ADDR, Data Hold After SDCLK[2]	1.3		1.3		ns
t_{DSDAT}	Data Disable After SDCLK		5.3		5.3	ns
t_{ENSDAT}	Data Enable After SDCLK	1.6		1.6		ns

[1] For F_{CCLK} = 133 MHz (SDCLK ratio = 1:2).
[2] Command pins include: $\overline{SDCAS}$, $\overline{SDRAS}$, $\overline{SDWE}$, $\overline{MSx}$, SDA10, and SDCKE.

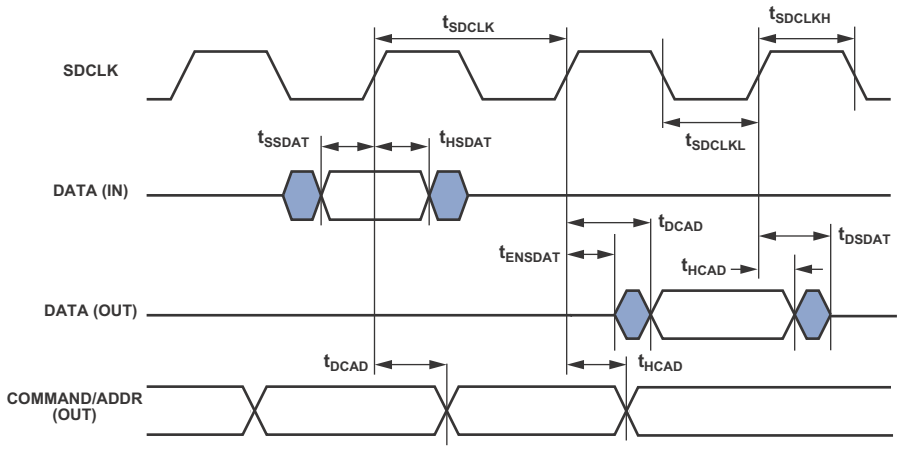


Figure 17. SDRAM Interface Timing for 133 MHz SDCLK

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.

Table 25. Memory Read—Bus Master

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Timing Requirements						
t_{DAD}	Address, Selects Delay to Data Valid[1, 2, 3]		W + t_{SDCLK} – 5.12		W + t_{SDCLK} – 5.12	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1, 3]		W – 3		W – 3	ns
t_{SDS}	Data Setup to $\overline{RD}$ High	2.2		2.2		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[4, 5]	0		0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 6]		t_{SCDCLK} – 11.4 + W		t_{SCDCLK} – 10.1 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[5]		W – 7.25		W – 7.0	ns
Switching Characteristics						
t_{DRHA}	Address Selects Hold After $\overline{RD}$ High	RHC + 0.38		RHC + 0.38		ns
t_{DARL}	Address Selects to $\overline{RD}$ Low[2]	t_{SDCLK} – 3.8		t_{SDCLK} – 3.3		ns
t_{RW}	$\overline{RD}$ Pulse Width	W – 1.4		W – 1.4		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, Low	HI + t_{SDCLK} – 0.8		HI + t_{SDCLK} – 0.8		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}
HI = RHC + IC (RHC = (number of Read Hold Cycles specified in AMICTLx register) × t_{SDCLK}
IC = (number of idle cycles specified in AMICTLx register) × t_{SDCLK})
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}

[1] Data delay/setup: System must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{MS}$x, is referenced.
[3] The maximum limit of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.
[4] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.
[5] Data hold: User must meet t_{HDRH} in asynchronous access mode. See Test Conditions on Page 49 for the calculation of hold times given capacitive and dc loads.
[6] ACK delay/setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (low). For asynchronous assertion of ACK (high) user must meet t_{DAAK} or t_{DSAK}.

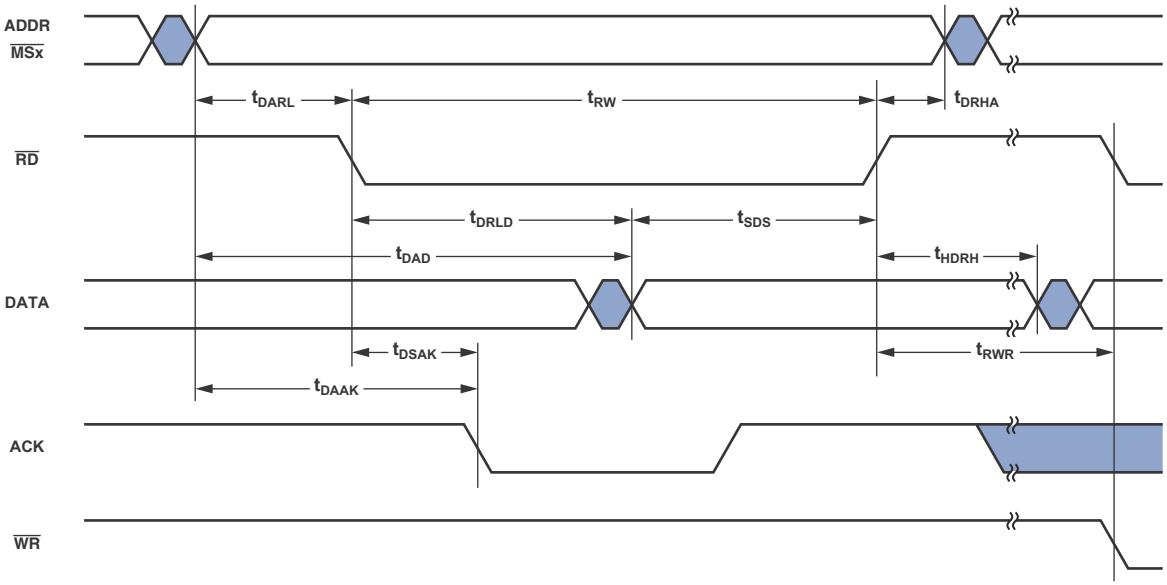


Figure 18. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.

Table 26. Memory Write—Bus Master

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Timing Requirements						
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		t_{SDCLK} – 11 + W		t_{SDCLK} – 10.1 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low [1, 3]		W – 7.35		W – 7.1	ns
Switching Characteristics						
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	t_{SDCLK} – 4.3 + W		t_{SDCLK} – 3.6 + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	t_{SDCLK} – 2.7		t_{SDCLK} – 2.7		ns
t_{WW}	$\overline{WR}$ Pulse Width	W – 1.3		W – 1.3		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	t_{SDCLK} – 3.0 + W		t_{SDCLK} – 3.0 + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	H + 0.15		H + 0.15		ns
t_{DWHD}	Data Hold After $\overline{WR}$ Deasserted	H + 0.02		H + 0.02		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[4]	t_{SDCLK} – 1.37 + H	t_{SDCLK} + 10.7+ H	t_{SDCLK} – 1.37 + H	t_{SDCLK} + 4.9+ H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$ Low	t_{SDCLK} – 1.5+ H		t_{SDCLK} – 1.5+ H		ns
t_{DDWR}	Data Disable Before $\overline{RD}$ Low	$2t_{SDCLK}$ – 12		$2t_{SDCLK}$ – 5.1		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	t_{SDCLK} – 4.1		t_{SDCLK} – 4.1		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}, H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}

[1] ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (low). For asynchronous assertion of ACK (high) user must meet t_{DAAK} or t_{DSAK}.
[2] The falling edge of $\overline{MSx}$ is referenced.
[3] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only applies to asynchronous access mode.
[4] See Test Conditions on Page 49 for calculation of hold times given capacitive and dc loads.

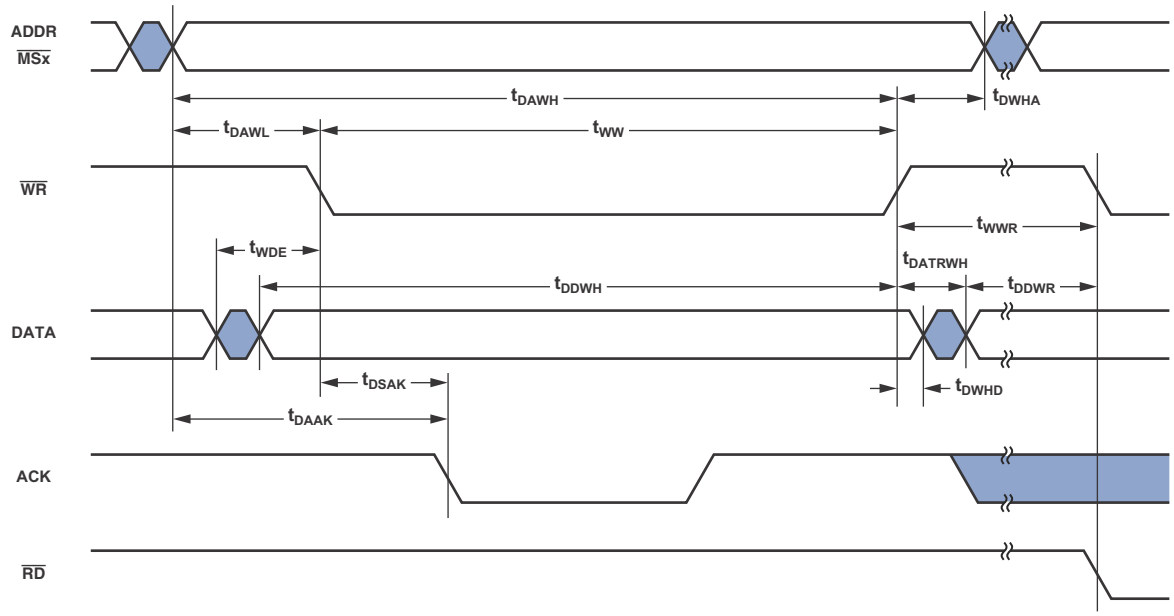


Figure 19. Memory Write—Bus Master

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) serial clock (SCLK) width.

Serial port signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 27. Serial Ports—External Clock

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Timing Requirements						
t_{SFSE}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.8		2.5		ns
t_{HFSE}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	3.1		2.5		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		2.5		ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 1.5$		$(t_{PCLK} \times 4) \div 2 - 1.5$		ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns
Switching Characteristics						
t_{DFSE}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)		13.5		10.5	ns
t_{HOFSE}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)	2		2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		13.9		11	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 28. Serial Ports—Internal Clock

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Timing Requirements						
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	7		7		ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7		7		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		2.5		ns
Switching Characteristics						
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		4		4	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1.0		–1.0		ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		13.5		10.7	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1.0		–1.0		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		4.6		3.6	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0		–1.0		ns
t_{SCKLIW}[3]	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.
[3] Minimum SPORT divisor register value.

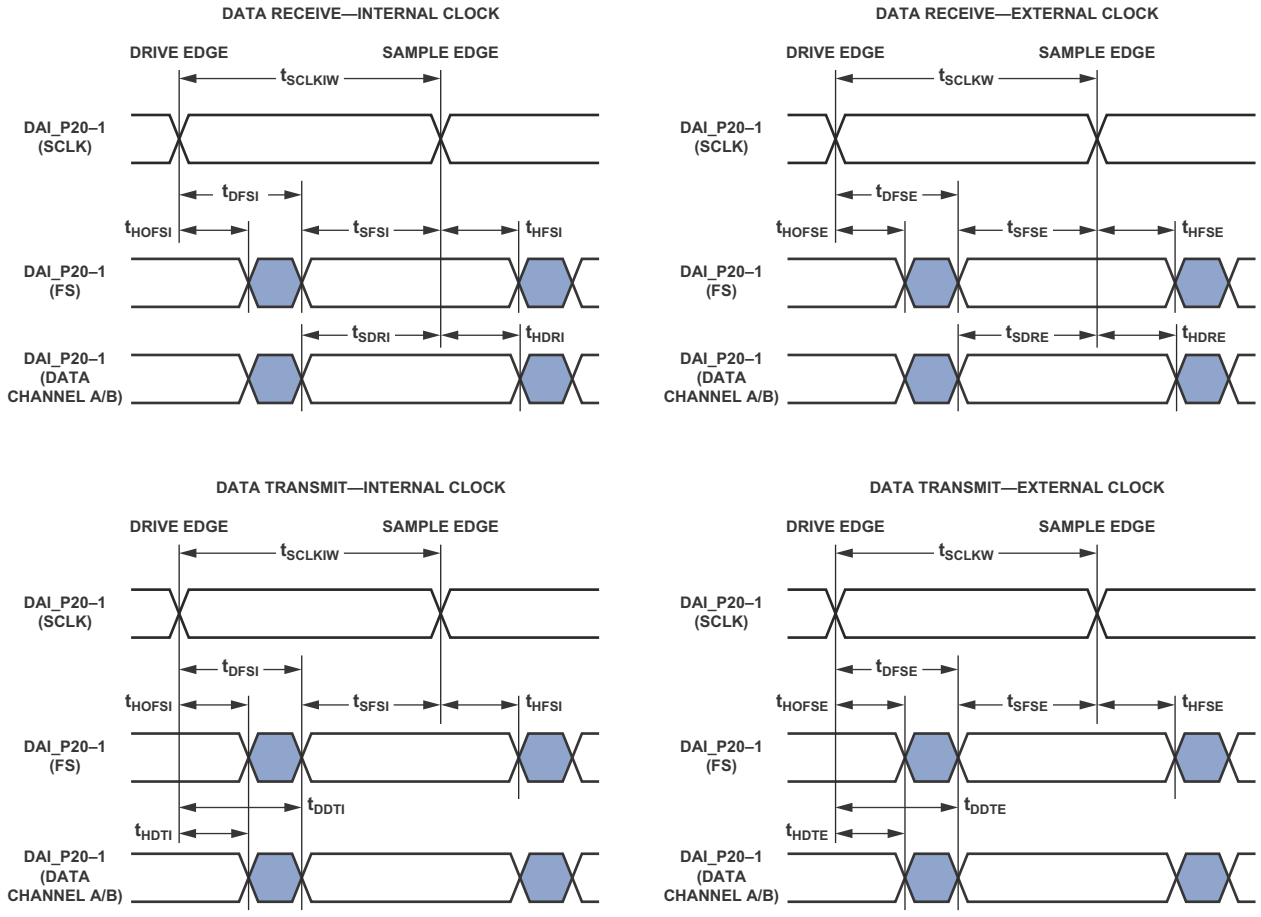


Figure 20. Serial Ports

Table 29. Serial Ports—Enable and Three-State

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Switching Characteristics						
t_{DDTEN}[1]	Data Enable from External Transmit SCLK	2		2		ns
t_{DDTTE}[1]	Data Disable from External Transmit SCLK		11.3		10	ns
t_{DDTIN}[1]	Data Enable from Internal Transmit SCLK	–1		–1		ns

[1] Referenced to drive edge.

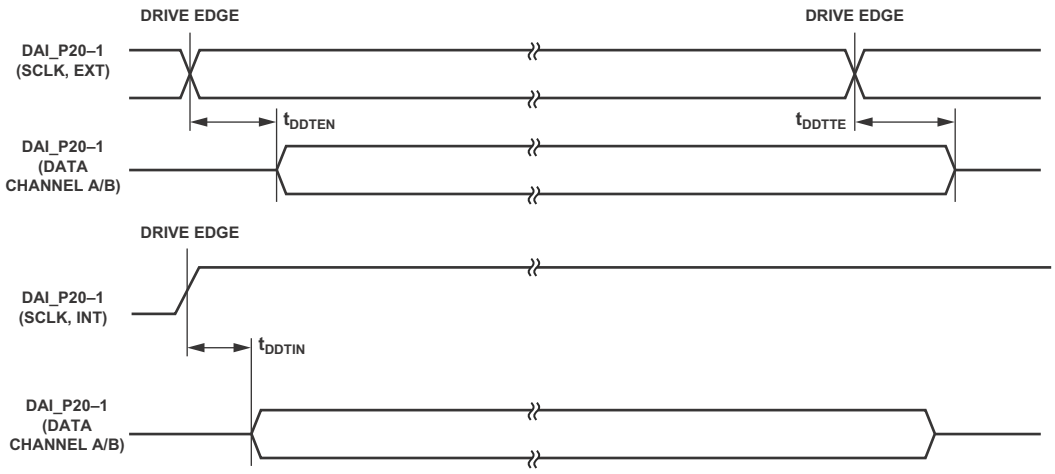


Figure 21. Enable and Three-State

Table 30. Serial Ports—External Late Frame Sync

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Switching Characteristics						
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0		12.7		10	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5		0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified sample pair as well as DSP serial mode, and MCE = 1, MFD = 0.

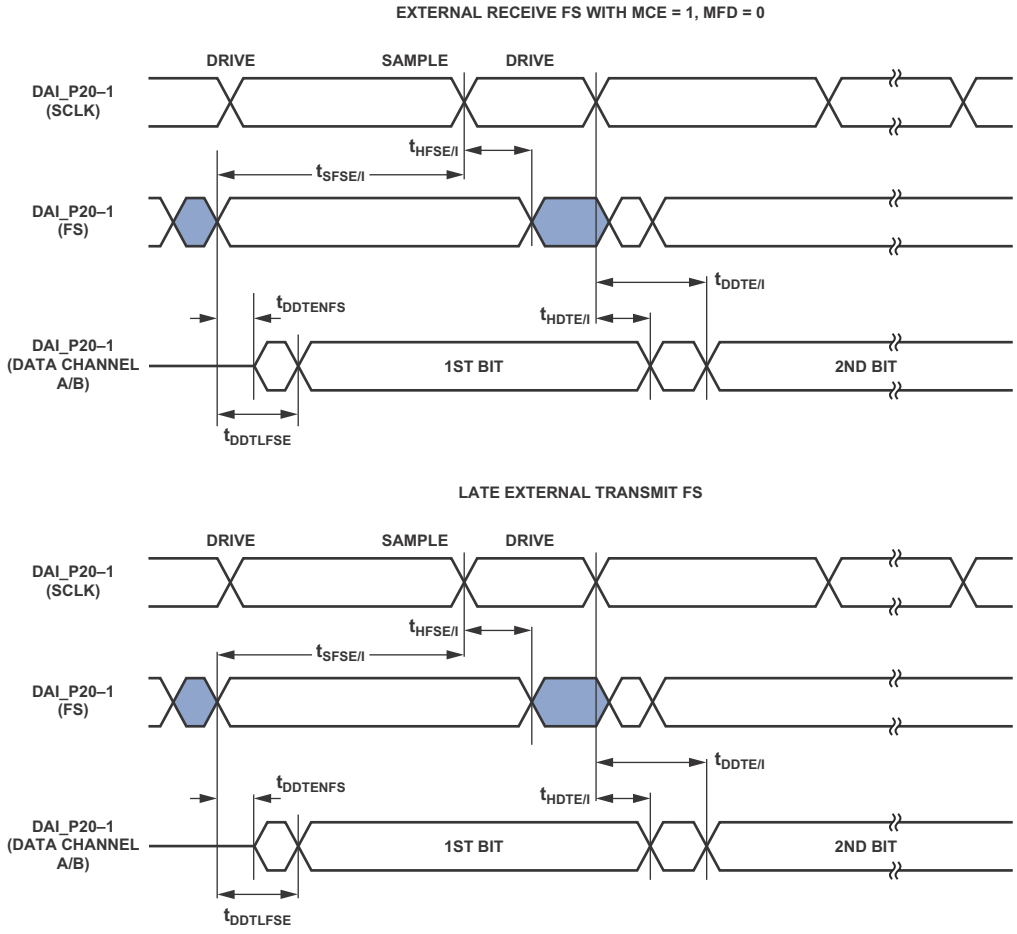


Figure 22. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified sample pair mode.

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 31. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 31. Input Data Port (IDP)

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Timing Requirements						
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4.95		3.8		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	2.5		2.5		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	3.35		2.5		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	2.5		2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns

[1] The data, serial clock, and frame sync signals can come from any of the DAI pins. Serial clock and frame sync can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

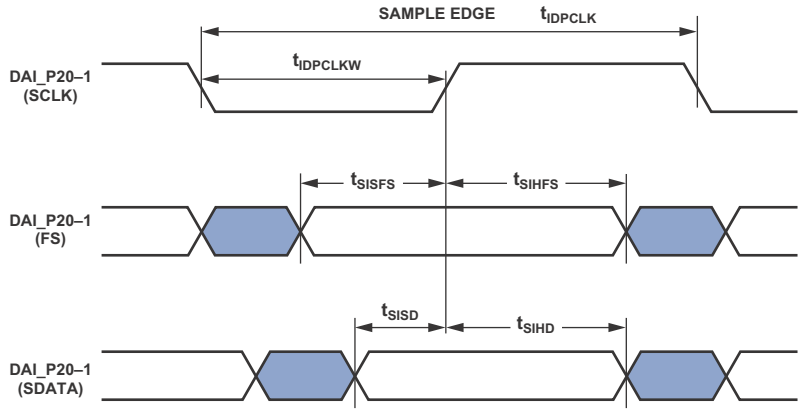


Figure 23. IDP Master Timing

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 32. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the *ADSP-2137x SHARC Processor Hardware Reference*.

Note that the 20-bits of external PDAP data can be provided through the external port DATA31–12 pins. On the ADSP-21375 processors, PDAP can not be multiplexed on the external port (since only DATA15–0). Use the SRU DAI instead.

Table 32. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPCLKEN}$[1]	PDAP_CLKEN Setup Before PDAP_CLK Sample Edge	2.5		ns
$t_{HPCLKEN}$[1]	PDAP_CLKEN Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDSD}[1]	PDAP_DAT Setup Before Serial Clock PDAP_CLK Sample Edge	3.85		ns
t_{PDHD}[1]	PDAP_DAT Hold After Serial Clock PDAP_CLK Sample Edge	2.5		ns
t_{PDCLKW}	Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$		ns
t_{PDCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} + 3$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1$		ns

[1] Data source pins are DATA31–12 or DAI pins. Source pins for serial clock and frame sync are: 1) DATA11–10 pins, 2) DAI pins.

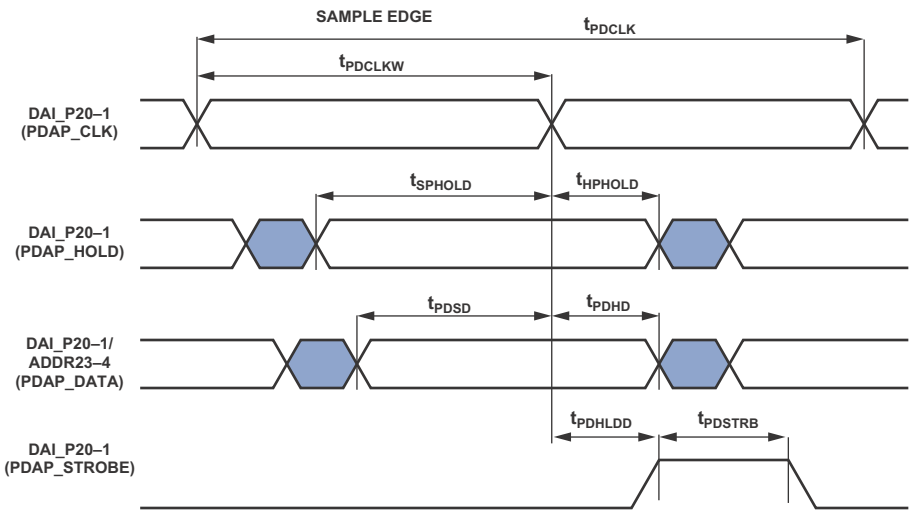


Figure 24. PDAP Timing

Pulse-Width Modulation Generators (PWM)

For the ADSP-21371, the following timing specifications apply when the DATA31–16 pins are configured as PWM.

Pulse-width modulation generator information does not apply to the ADSP-21375.

Table 33. Pulse-Width Modulation (PWM) Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2.5$	$(2^{16} - 2) \times t_{PCLK}$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 2.5$	$(2^{16} - 1) \times t_{PCLK}$	ns

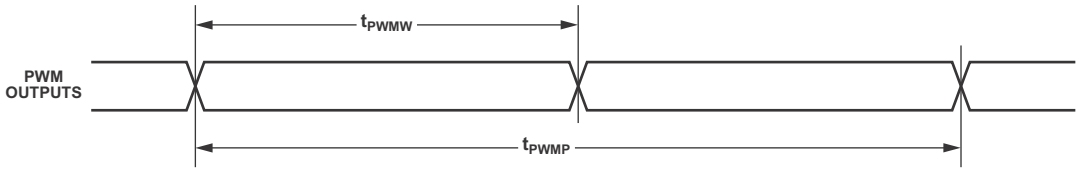


Figure 25. PWM Timing

S/PDIF Transmitter

For the ADSP-21371, serial data input to the S/PDIF transmitter can be formatted as left-justified, I²S, or right-justified with word widths of 16-, 18-, 20-, or 24-bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 26 shows the right-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed 12-bit clock periods (in 20-bit output mode) or 16-bit clock periods (in 16-bit output mode) from an LRCLK transition, so that when there are 64 serial clock periods per LRCLK period, the LSB of the data will be right-justified to the next LRCLK transition.

S/PDIF transmitter information does not apply to the ADSP-21375.

Figure 27 shows the default I²S-justified mode. LRCLK is low for the left channel and high for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to an LRCLK transition but with a single serial clock period delay.

Figure 28 shows the left-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to an LRCLK transition with no MSB delay.

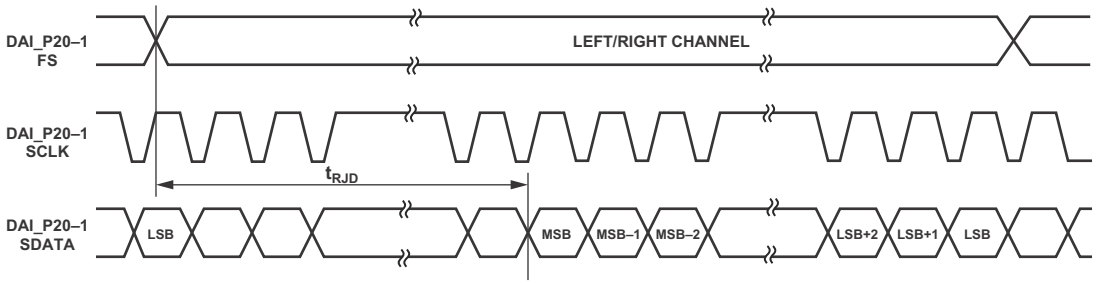


Figure 26. Right-Justified Mode

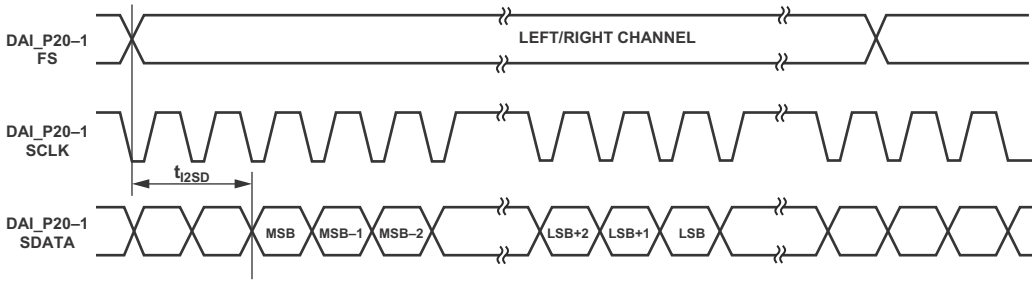


Figure 27. I²S-Justified Mode

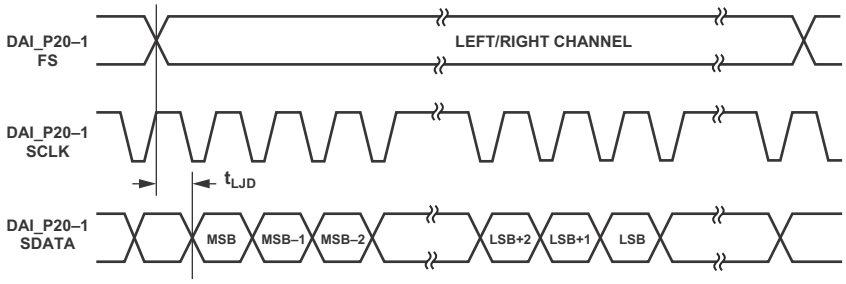


Figure 28. Left-Justified Mode

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 34. Input signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 34. S/PDIF Transmitter Input Data Timing

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Timing Requirements						
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3		3		ns
t_{SIHRS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		3		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	3.2		3		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		3		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		9		ns
$t_{SITXCLK}$	Transmit Clock Period	20		20		ns
$t_{SISCLKW}$	Clock Width	36		36		ns
t_{SISCLK}	Clock Period	80		80		ns

[1] The data, serial clock, and frame sync can come from any of the DAI pins. Serial clock and frame sync can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

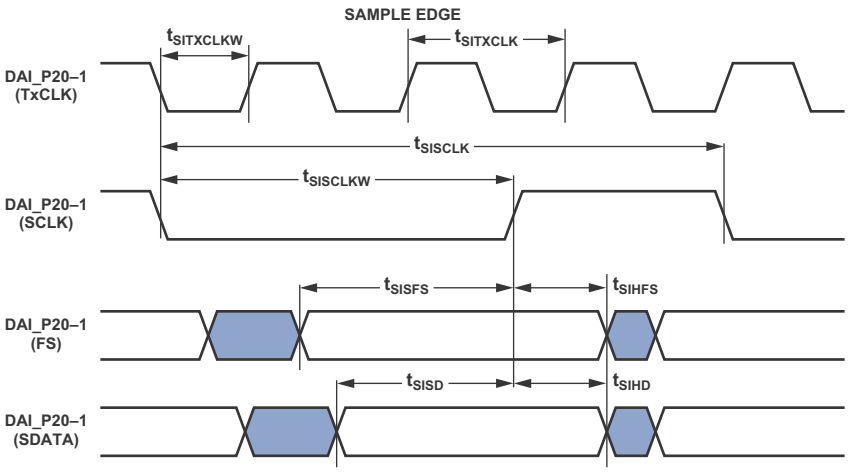


Figure 29. S/PDIF Transmitter Input Timing

Oversampling Clock (HFCLK) Switching Characteristics

The S/PDIF transmitter has an oversampling clock. This HFCLK input is divided down to generate the biphase clock.

Table 35. Oversampling Clock HFxCLK) Switching Characteristics

Parameter	Max	Unit
HFCLK Frequency for HFCLK = 384 × Frame Sync	Oversampling Ratio × Frame Sync <= $1/t_{SITXCLK}$	MHz
HFCLK Frequency for HFCLK = 256 × Frame Sync	49.2	MHz
Frame Rate (FS)	192.0	kHz

S/PDIF Receiver

For the ADSP-21371, the following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the 512 × Frame Sync clock. The S/PDIF receiver information does not apply to the ADSP-21375.

Table 36. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter		1.0 V, 200 MHz		1.2 V, 266 MHz		Unit
		Min	Max	Min	Max	
Switching Characteristics						
t_{DFSI}	LRCLK Delay After Serial Clock		5		5	ns
t_{HOFSI}	LRCLK Hold After Serial Clock	–2		–2		ns
t_{DDTI}	Transmit Data Delay After Serial Clock		5		5	ns
t_{HDTI}	Transmit Data Hold After Serial Clock	–2		–2		ns
t_{SCLKIW}[1]	Transmit Serial Clock Width	52		38.5		ns

[1] Serial lock frequency is 64 × Frame Sync where FS = the frequency of LRCLK.

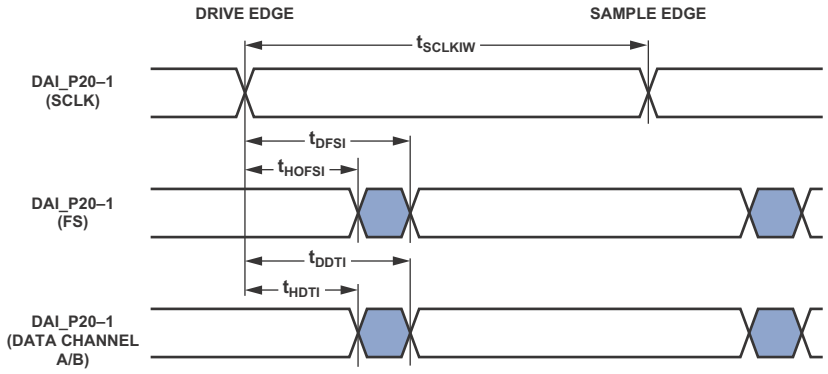


Figure 30. S/PDIF Receiver Internal Digital PLL Mode Timing

SPI Interface—Master

The processor contains two SPI ports. Both primary and secondary are available through DPI only. The timing provided in Table 37 and Table 38 applies to both.

Table 37. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid To SPICLK Edge (Data Input Setup Time)	8.2		ns
t_{HSPIDM}	SPICLK Last Sampling Edge To Data Input Not Valid	2		ns
Switching Characteristics				
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		2.5	ns
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	DPI Pin (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK Edge to DPI Pin (SPI Device Select) High	$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1$		ns

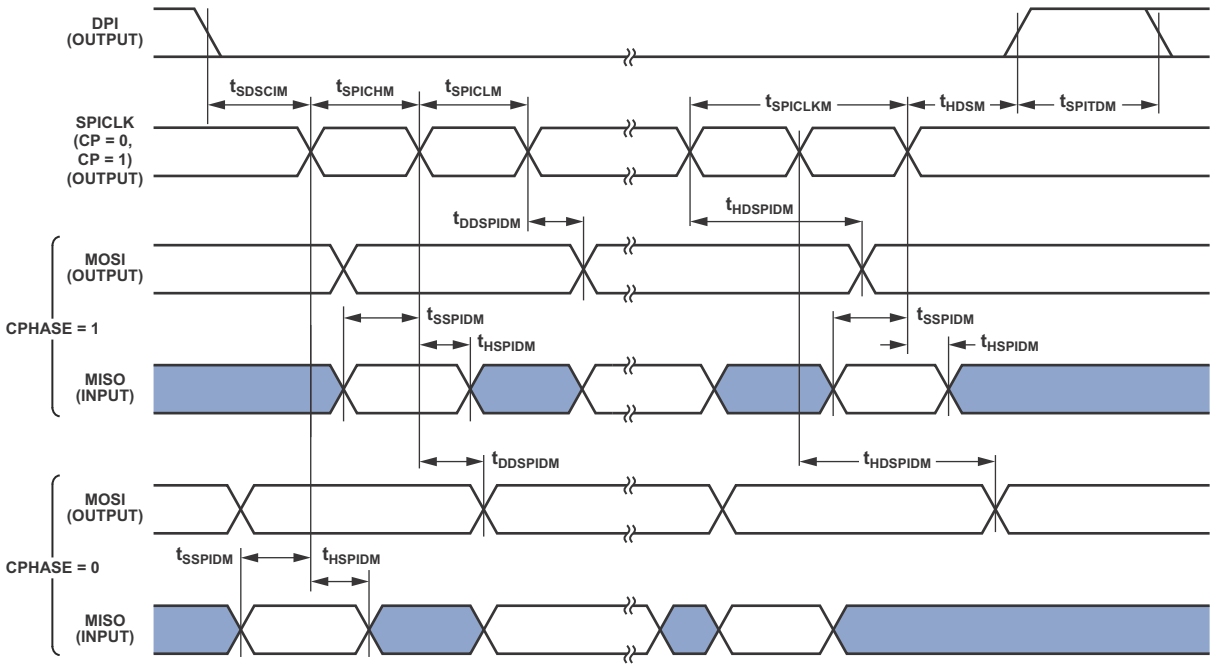


Figure 31. SPI Master Timing

SPI Interface—Slave

Table 38. SPI Interface Protocol—Slave Switching and Timing Specifications

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Timing Requirements						
$t_{SPICLKS}$	Serial Clock Cycle	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SPICHS}	Serial Clock High Period	$2 \times t_{PCLK} - 2$		$2 \times t_{PCLK} - 2$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{PCLK} - 2$		$2 \times t_{PCLK} - 2$		ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge					ns
	CPHASE = 0	$2 \times t_{PCLK}$		$2 \times t_{PCLK}$		
	CPHASE = 1	$2 \times t_{PCLK}$		$2 \times t_{PCLK}$		
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted (CPHASE=0)	$2 \times t_{PCLK}$		$2 \times t_{PCLK}$		ns
t_{SSPIDS}	Data Input Valid to SPICLK edge (Data Input Set-up Time)	2		2		ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2		2		ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE=0)	$2 \times t_{PCLK}$		$2 \times t_{PCLK}$		ns
Switching Characteristics						
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	0	6.8	0	6.8	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	0	9.9	0	6.8	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		9.5		9.5	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$2 \times t_{PCLK}$		$2 \times t_{PCLK}$		ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$5 \times t_{PCLK}$		$5 \times t_{PCLK}$	ns

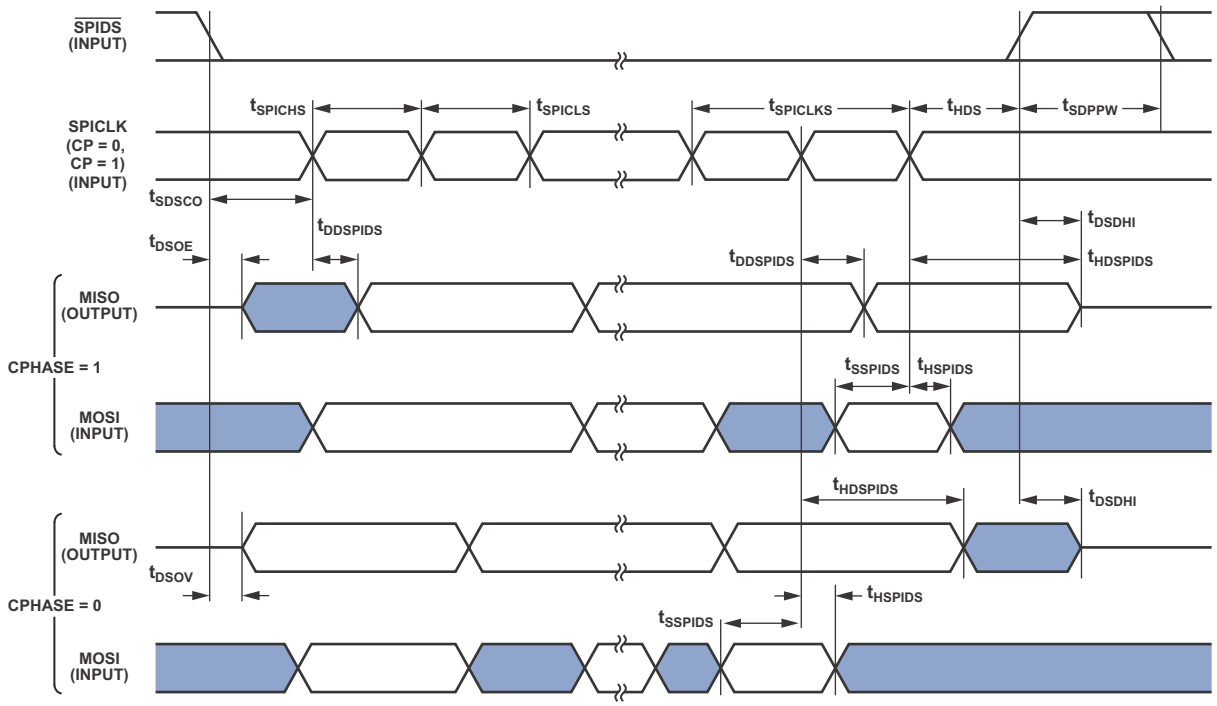


Figure 32. SPI Slave Timing

Universal Asynchronous Receiver-Transmitter (UART) Port—Receive and Transmit Timing

Figure 33 describes UART port receive and transmit operations. The maximum baud rate is PCLK/16 where PCLK = $1/t_{PCLK}$. As shown in Figure 33 there is some latency between the generation of internal UART interrupts and the external data operations. These latencies are negligible at the data transmission rates for the UART.

Table 39. UART Port

Parameter		Min	Max	Unit
Timing Requirement				
t_{TXD}[1]	Incoming Data Pulse Width	$16t_{PCLK}-1$		ns
Switching Characteristic				
t_{RXD}[1]	Incoming Data Pulse Width	$16t_{PCLK}-1$		ns

[1] UART signals TXD and RXD are routed through DPI P14-1 pins using the SRU.

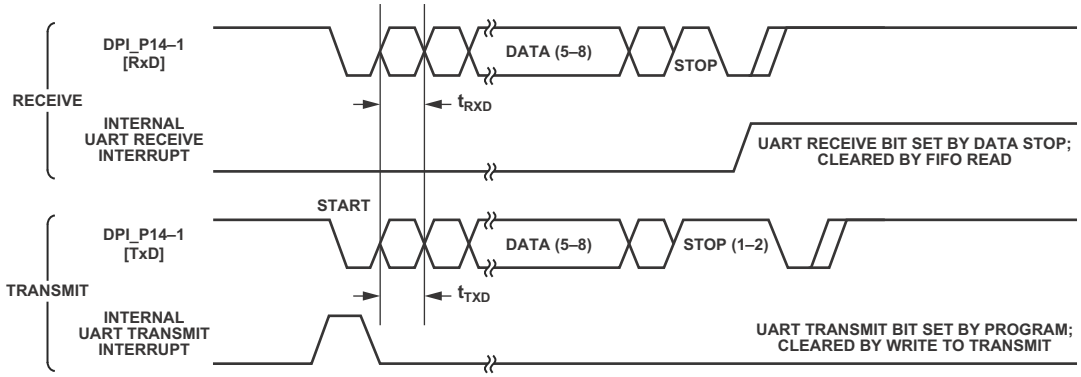


Figure 33. UART Port—Receive and Transmit Timing

TWI Controller Timing

Table 40 and Figure 34 provide timing information for the TWI interface. Input signals (SCL, SDA) are routed to the DPI_P14–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 40. Characteristics of the SDA and SCL Bus Lines for F/S-Mode TWI Bus Devices[1]

Parameter		Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	0	100	0	400	kHz
t_{HDSTA}	Hold Time (repeated) Start Condition. After This Period, the First Clock Pulse is Generated.	4.0		0.6		µs
t_{LOW}	Low Period of the SCL Clock	4.7		1.3		µs
t_{HIGH}	High Period of the SCL Clock	4.0		0.6		µs
t_{SUSTA}	Setup Time for a Repeated Start Condition	4.7		0.6		µs
t_{HDDAT}	Data Hold Time for TWI-Bus Devices	0		0		µs
t_{SUDAT}	Data Setup Time	250		100		ns
t_{SUSTO}	Setup Time for Stop Condition	4.0		0.6		µs
t_{BUF}	Bus Free Time Between a Stop and Start Condition	4.7		1.3		µs
t_{SP}	Pulse Width of Spikes Suppressed By the Input Filter	N/A	N/A	0	50	ns

[1] All values referred to V_{IHmin} and V_{ILmax} levels. For more information, see Electrical Characteristics on page 17.

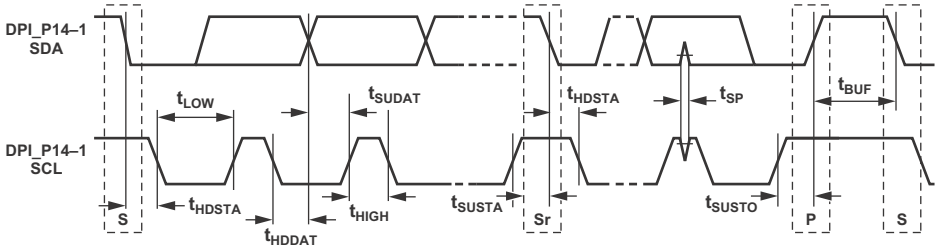


Figure 34. Fast and Standard Mode Timing on the TWI Bus

JTAG Test Access Port and Emulation

Table 41. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = ADDR15–0, CLKCFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, DAI_Px, and FLAG3–0.
[2] System Outputs = DAI_Px, ADDR15–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, FLAG3–0, $\overline{\text{EMU}}$, and ALE.

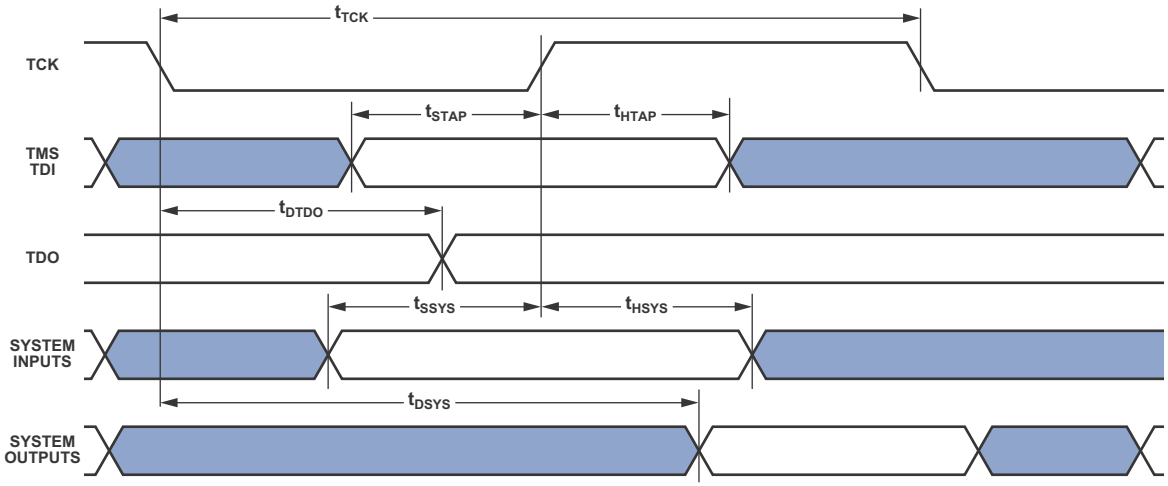


Figure 35. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 36 shows typical I-V characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

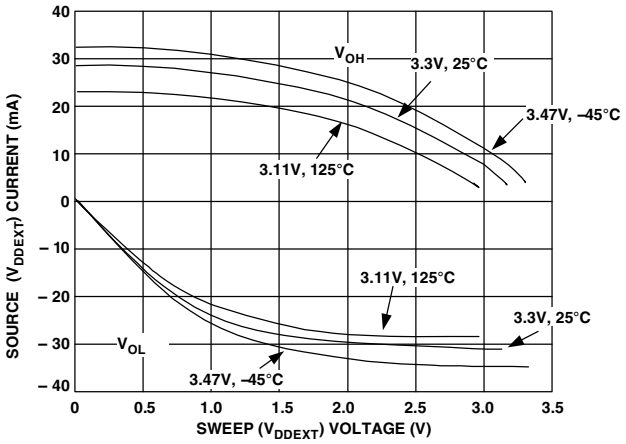


Figure 36. Typical Drive at Junction Temperature

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 15 on Page 22 through Table 41 on Page 48. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 37.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 38. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

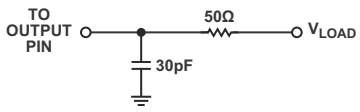


Figure 37. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

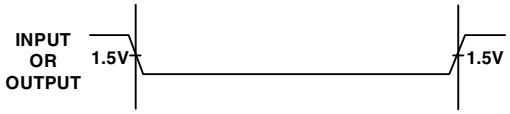


Figure 38. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 37). Figure 41 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 39, Figure 40, and Figure 41 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

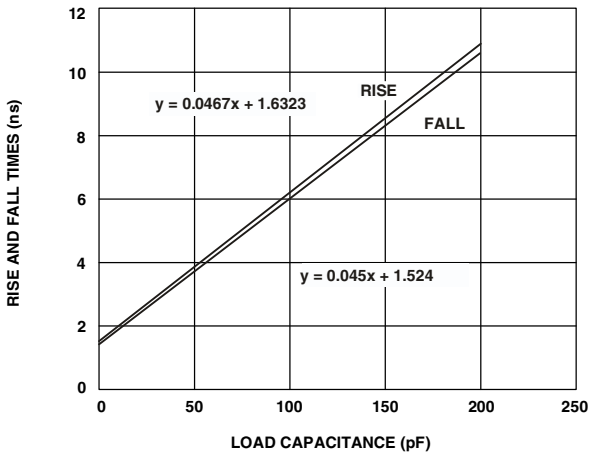


Figure 39. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

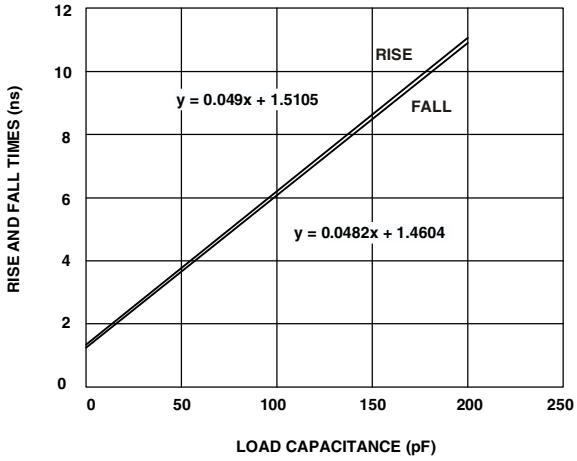


Figure 40. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

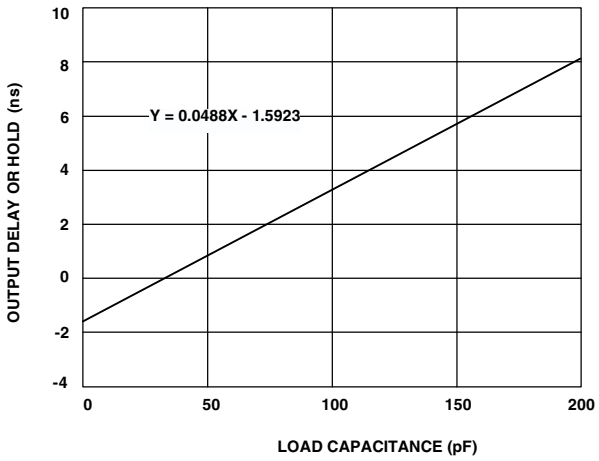


Figure 41. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

THERMAL CHARACTERISTICS

The processor is rated for performance over the temperature range specified in Operating Conditions on Page 16.

Table 42 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standard JESD51-7 (LQFP_EP). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature °C

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the Typical value from Table 42.

P_D = power dissipation

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations. Note that the thermal characteristics values provided in Table 42 are modeled values.

Table 42. Thermal Characteristics for 208-Lead LQFP E_PAD (With Exposed Pad Soldered to PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	17.1	°C/W
θ_{JMA}	Airflow = 1 m/s	14.7	°C/W
θ_{JMA}	Airflow = 2 m/s	14.0	°C/W
θ_{JC}		9.6	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.23	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.39	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.45	°C/W
Ψ_{JB}	Airflow = 0 m/s	11.5	°C/W
Ψ_{JMB}	Airflow = 1 m/s	11.2	°C/W
Ψ_{JMB}	Airflow = 2 m/s	11.0	°C/W

208-LEAD LQFP_EP PINOUT

Table 43. ADSP-21371, 208-Lead LQFP_EP Pin Assignment (Numerical by Lead Number)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	V_{DDINT}	53	V_{DDINT}	105	V_{DDINT}	157	V_{DDINT}
2	DATA28	54	GND	106	GND	158	V_{DDINT}
3	DATA27	55	V_{DDEXT}	107	V_{DDEXT}	159	GND
4	GND	56	ADDR0	108	$\overline{SDCAS}$	160	V_{DDINT}
5	V_{DDEXT}	57	ADDR2	109	$\overline{SDRAS}$	161	V_{DDINT}
6	DATA26	58	ADDR1	110	SDCKE	162	V_{DDINT}
7	DATA25	59	ADDR4	111	$\overline{SDWE}$	163	TDI
8	DATA24	60	ADDR3	112	$\overline{WR}$	164	$\overline{TRST}$
9	DATA23	61	ADDR5	113	SDA10	165	TCK
10	GND	62	GND	114	GND	166	GND
11	V_{DDINT}	63	V_{DDINT}	115	V_{DDEXT}	167	V_{DDINT}
12	DATA22	64	GND	116	SDCLK	168	TMS
13	DATA21	65	V_{DDEXT}	117	GND	169	CLK_CFG0
14	DATA20	66	ADDR6	118	V_{DDINT}	170	BOOT_CFG0
15	V_{DDEXT}	67	ADDR7	119	$\overline{RD}$	171	CLK_CFG1
16	GND	68	ADDR8	120	ACK	172	$\overline{EMU}$
17	DATA19	69	ADDR9	121	FLAG3	173	BOOT_CFG1
18	DATA18	70	ADDR10	122	FLAG2	174	TDO
19	V_{DDINT}	71	GND	123	FLAG1	175	DAI_P4 (SFS0)
20	GND	72	V_{DDINT}	124	FLAG0	176	DAI_P2 (SD0B)
21	DATA17	73	GND	125	DAI_P20 (SFS5)	177	DAI_P3 (SCLK0)
22	V_{DDINT}	74	V_{DDEXT}	126	GND	178	DAI_P1 (SD0A)
23	GND	75	ADDR11	127	V_{DDINT}	179	V_{DDEXT}
24	V_{DDINT}	76	ADDR12	128	GND	180	GND
25	GND	77	ADDR13	129	V_{DDEXT}	181	V_{DDINT}
26	DATA16	78	GND	130	DAI_P19 (SCLK5)	182	GND
27	DATA15	79	V_{DDINT}	131	DAI_P18 (SD5B)	183	DPI_P14 (TIMER1)
28	DATA14	80	NC	132	DAI_P17 (SD5A)	184	DPI_P13 (TIMER0)
29	DATA13	81	NC	133	DAI_P16 (SD4B)	185	DPI_P12 (TWI_CLK)
30	DATA12	82	GND	134	DAI_P15 (SD4A)	186	DPI_P11 (TWI_DATA)
31	V_{DDEXT}	83	CLKIN	135	DAI_P14 (SFS3)	187	DPI_P10 (UART0RX)
32	GND	84	XTAL	136	DAI_P13 (SCLK3)	188	DPI_P09 (UART0TX)
33	V_{DDINT}	85	V_{DDEXT}	137	DAI_P12 (SD3B)	189	DPI_P08 (SPIFLG3)
34	GND	86	GND	138	V_{DDINT}	190	DPI_P07 (SPIFLG2)
35	DATA11	87	V_{DDINT}	139	V_{DDEXT}	191	V_{DDEXT}
36	DATA10	88	ADDR14	140	GND	192	GND
37	DATA9	89	GND	141	V_{DDINT}	193	V_{DDINT}
38	DATA8	90	V_{DDEXT}	142	GND	194	GND
39	DATA7	91	ADDR15	143	DAI_P11 (SD3A)	195	DPI_P06 (SPIFLG1)
40	DATA6	92	ADDR16	144	DAI_P10 (SD2B)	196	DPI_P05 (SPIFLG0)
41	V_{DDEXT}	93	ADDR17	145	DAI_P8 (SFS1)	197	DPI_P04 (SPIDS)
42	GND	94	ADDR18	146	DAI_P9 (SD2A)	198	DPI_P03 (SPICLK)
43	V_{DDINT}	95	GND	147	DAI_P6 (SD1B)	199	DPI_P01 (SPIMOSI)
44	DATA4	96	V_{DDEXT}	148	DAI_P7 (SCLK1)	200	DPI_P02 (SPIMISO)

Table 43. ADSP-21371, 208-Lead LQFP_EP Pin Assignment (Numerical by Lead Number) (Continued)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
45	DATA5	97	ADDR19	149	DAI_P5 (SD1A)	201	$\overline{\text{RESETOUT}}$/ $\overline{\text{RUNRSTIN}}$
46	DATA2	98	ADDR20	150	V_{DDEXT}	202	$\overline{\text{RESET}}$
47	DATA3	99	ADDR21	151	GND	203	V_{DDEXT}
48	DATA0	100	ADDR23	152	V_{DDINT}	204	GND
49	DATA1	101	ADDR22	153	GND	205	DATA30
50	V_{DDEXT}	102	$\overline{\text{MS1}}$	154	V_{DDINT}	206	DATA31
51	GND	103	$\overline{\text{MS0}}$	155	GND	207	DATA29
52	V_{DDINT}	104	V_{DDINT}	156	V_{DDINT}	208	V_{DDINT}

Table 44. ADSP-21375, 208-Lead LQFP_EP Pin Assignment (Numerical by Lead Number)

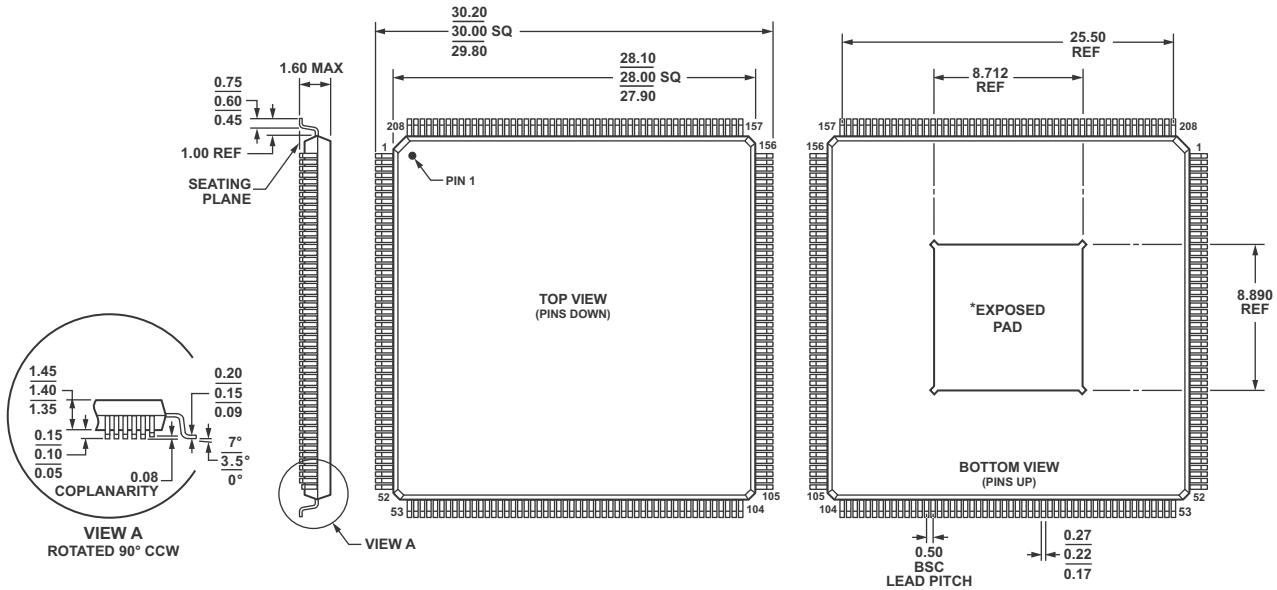
Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	V_{DDINT}	53	V_{DDINT}	105	V_{DDINT}	157	V_{DDINT}
2	NC	54	GND	106	GND	158	V_{DDINT}
3	NC	55	V_{DDEXT}	107	V_{DDEXT}	159	GND
4	GND	56	ADDR0	108	$\overline{SDCAS}$	160	V_{DDINT}
5	V_{DDEXT}	57	ADDR2	109	$\overline{SDRAS}$	161	V_{DDINT}
6	NC	58	ADDR1	110	SDCKE	162	V_{DDINT}
7	NC	59	ADDR4	111	$\overline{SDWE}$	163	TDI
8	NC	60	ADDR3	112	$\overline{WR}$	164	$\overline{TRST}$
9	NC	61	ADDR5	113	SDA10	165	TCK
10	GND	62	GND	114	GND	166	GND
11	V_{DDINT}	63	V_{DDINT}	115	V_{DDEXT}	167	V_{DDINT}
12	NC	64	GND	116	SDCLK	168	TMS
13	NC	65	V_{DDEXT}	117	GND	169	CLK_CFG0
14	NC	66	ADDR6	118	V_{DDINT}	170	BOOT_CFG0
15	NC	67	ADDR7	119	$\overline{RD}$	171	CLK_CFG1
16	NC	68	ADDR8	120	ACK	172	$\overline{EMU}$
17	NC	69	ADDR9	121	FLAG3	173	BOOT_CFG1
18	NC	70	ADDR10	122	FLAG2	174	TDO
19	NC	71	GND	123	FLAG1	175	DAI_P4 (SFS0)
20	NC	72	V_{DDINT}	124	FLAG0	176	DAI_P2 (SD0B)
21	NC	73	GND	125	DAI_P20 (SFS5)	177	DAI_P3 (SCLK0)
22	V_{DDINT}	74	V_{DDEXT}	126	GND	178	DAI_P1 (SD0A)
23	GND	75	ADDR11	127	V_{DDINT}	179	V_{DDEXT}
24	V_{DDINT}	76	ADDR12	128	GND	180	GND
25	GND	77	ADDR13	129	V_{DDEXT}	181	V_{DDINT}
26	NC	78	GND	130	DAI_P19 (SCLK5)	182	GND
27	DATA15	79	V_{DDINT}	131	DAI_P18 (SD5B)	183	DPI_P14 (TIMER1)
28	DATA14	80	NC	132	DAI_P17 (SD5A)	184	DPI_P13 (TIMER0)
29	DATA13	81	NC	133	DAI_P16 (SD4B)	185	DPI_P12 (TWI_CLK)
30	DATA12	82	GND	134	DAI_P15 (SD4A)	186	DPI_P11 (TWI_DATA)
31	V_{DDEXT}	83	CLKIN	135	DAI_P14 (SFS3)	187	DPI_P10 (UART0RX)
32	GND	84	XTAL	136	DAI_P13 (SCLK3)	188	DPI_P09 (UART0TX)
33	V_{DDINT}	85	V_{DDEXT}	137	DAI_P12 (SD3B)	189	DPI_P08 (SPIFLG3)
34	GND	86	GND	138	V_{DDINT}	190	DPI_P07 (SPIFLG2)
35	DATA11	87	V_{DDINT}	139	V_{DDEXT}	191	V_{DDEXT}
36	DATA10	88	ADDR14	140	GND	192	GND
37	DATA9	89	GND	141	V_{DDINT}	193	V_{DDINT}
38	DATA8	90	V_{DDEXT}	142	GND	194	GND
39	DATA7	91	ADDR15	143	DAI_P11 (SD3A)	195	DPI_P06 (SPIFLG1)
40	DATA6	92	ADDR16	144	DAI_P10 (SD2B)	196	DPI_P05 (SPIFLG0)
41	V_{DDEXT}	93	ADDR17	145	DAI_P8 (SFS1)	197	DPI_P04 (SPIDS)
42	GND	94	ADDR18	146	DAI_P9 (SD2A)	198	DPI_P03 (SPICLK)
43	V_{DDINT}	95	GND	147	DAI_P6 (SD1B)	199	DPI_P01 (SPIMOSI)
44	DATA4	96	V_{DDEXT}	148	DAI_P7 (SCLK1)	200	DPI_P02 (SPIMISO)

Table 44. ADSP-21375, 208-Lead LQFP_EP Pin Assignment (Numerical by Lead Number) (Continued)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
45	DATA5	97	ADDR19	149	DAI_P5 (SD1A)	201	$\overline{\text{RESETOUT}}$/ $\overline{\text{RUNRSTIN}}$
46	DATA2	98	ADDR20	150	V_{DDEXT}	202	$\overline{\text{RESET}}$
47	DATA3	99	ADDR21	151	GND	203	V_{DDEXT}
48	DATA0	100	ADDR23	152	V_{DDINT}	204	GND
49	DATA1	101	ADDR22	153	GND	205	DATA30
50	V_{DDEXT}	102	$\overline{\text{MS1}}$	154	V_{DDINT}	206	DATA31
51	GND	103	$\overline{\text{MS0}}$	155	GND	207	DATA29
52	V_{DDINT}	104	V_{DDINT}	156	V_{DDINT}	208	V_{DDINT}

PACKAGE DIMENSIONS

The processors are available in a 208-lead RoHS compliant LQFP_EP package.



COMPLIANT TO JEDEC STANDARDS MS-026-BJB-HD

*NOTE:
THE EXPOSED PAD IS REQUIRED TO BE ELECTRICALLY AND THERMALLY CONNECTED TO GND. THIS SHOULD BE IMPLEMENTED BY SOLDERING THE EXPOSED PAD TO A GND PCB LAND THAT IS THE SAME SIZE AS THE EXPOSED PAD. THE GND PCB LAND SHOULD BE ROBUSTLY CONNECTED TO THE GND PLANE IN THE PCB WITH AN ARRAY OF THERMAL VIAS FOR BEST PERFORMANCE.

Figure 42. 208-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP]
(SW-208-1)
Dimensions shown in millimeters