3.0 kV RMS, Single-Channel Digital Isolator

Data Sheet **ADuM110N**

FEATURES

- High common-mode transient immunity: 100 kV/μs
- High robustness to radiated and conducted noise
- Low propagation delay
  - 13 ns maximum for 5 V operation
  - 15 ns maximum for 1.8 V operation
- 150 Mbps maximum data rate
- Safety and regulatory approvals
  - UL recognition
    - 3000 V rms for 1 minute per UL 1577
  - CSA component acceptance notice 5A
  - VDE certificate of conformity
    - DIN VDE V 0884-11:2017-01
    - V_{IORM} = 565 V peak
  - CQC Certification per GB4943.1-2011
- Backward compatibility
  - Pin compatible with the ADuM1100
- Low dynamic power consumption
- 1.8 V to 5 V level translation
- High temperature operation: 125°C
- Fail-safe high or low options
- 8-lead, RoHS-compliant, SOIC package

APPLICATIONS

- General-purpose single-channel isolation
- Industrial field bus isolation

GENERAL DESCRIPTION

The ADuM110N is a single-channel digital isolator based on Analog Devices, Inc., iCoupler® technology. Combining high speed, complementary metal-oxide semiconductor (CMOS) and monolithic air core transformer technology, this isolation component provides outstanding performance characteristics, superior to alternatives such as optocoupler devices and other integrated couplers. The maximum propagation delay is 13 ns with a pulse width distortion of less than 3 ns at 5 V operation.

The ADuM110N supports data rates as high as 150 Mbps with a withstand voltage rating of 3.0 kV rms (see the Ordering Guide). The device operates with the supply voltage on either side ranging from 1.8 V to 5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier.

Unlike other optocoupler alternatives, dc correctness is ensured in the absence of input logic transitions. Two different fail-safe options are available, in which the outputs transition to a pre-determined state when the input power supply is not applied or the inputs are disabled. The ADuM110N is pin compatible with the ADuM1100.

FUNCTIONAL BLOCK DIAGRAM

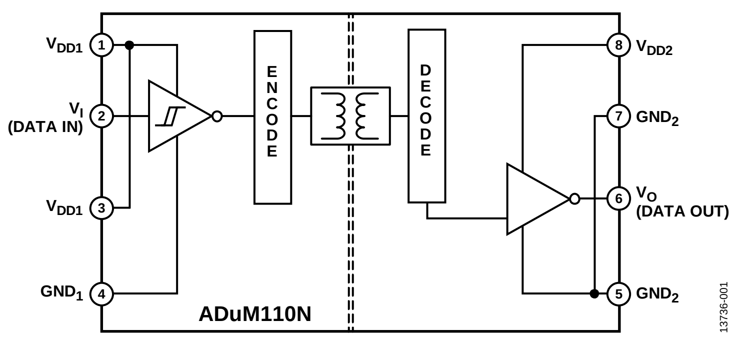

Figure 1.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

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REVISION HISTORY

11/2021—Rev. A to Rev. B

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Changed DIN V VDE V 0884-10 (VDE V 0884-10) Insulation Characteristics Section to DIN VDE V 0884-11:2017-01 Insulation Characteristics Section ... 8
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6/2019—Rev. 0 to Rev. A

Changes to Table 11 ... 8

10/2015—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within pulse width distortion (PWD) limit
Data Rate		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	4.8	7.2	13	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.5	3	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			6.0	ns	Between any two units at the same temperature, voltage, and load
Jitter			380		ps p-p	See the Jitter Measurement section
			55		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DD1}			V	
Logic Low	V_{IL}			0.3 × V_{DD1}	V	
Output Voltage						
Logic High	V_{OH}	V_{DD2} − 0.1	V_{DD2}		V	Output current (I_O) = −20 µA, input voltage (V_I) = V_{IH}
		V_{DD2} − 0.4	V_{DD2} − 0.2		V	I_O = −4 mA, V_I = V_{IH}
Logic Low	V_{OL}		0.0	0.1	V	I_O = 20 µA, V_I = V_{IL}
			0.2	0.4	V	I_O = 4 mA, V_I = V_{IL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_I ≤ V_{DD1}
Quiescent Supply Current						
	$I_{DD1 (Q)}$		0.9	1.4	mA	V_I = 0 (N0), 1 (N1)[1]
	$I_{DD2 (Q)}$		1.0	1.3	mA	V_I = 0 (N0), 1 (N1)[1]
	$I_{DD1 (Q)}$		3.6	6.0	mA	V_I = 1 (N0), 0 (N1)[1]
	$I_{DD2 (Q)}$		1.0	1.4	mA	V_I = 1 (N0), 0 (N1)[1]
Dynamic Supply Current						
Dynamic Output	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Input	$I_{DDO (D)}$		0.02		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[2]	$\|CM_H\|$	75	100		kV/µs	V_I = V_{DD1}, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_I = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] N0 indicates the ADuM110N0 models and N1 indicates the ADuM110N1 models. See the Ordering Guide section.
[2] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DD2}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both the rising and falling common-mode voltage edges.

Table 2. Total Supply Current vs. Data Throughput—5 V Operation

Parameter	Symbol	1 Mbps Min	1 Mbps Typ	1 Mbps Max	25 Mbps Min	25 Mbps Typ	25 Mbps Max	100 Mbps Min	100 Mbps Typ	100 Mbps Max	Unit
SUPPLY CURRENT											
Supply Current Side 1	I_{DD1}		2.2	3.7		2.5	3.9		3.6	4.9	mA
Supply Current Side 2	I_{DD2}		1.1	1.6		1.6	2.3		3.1	4.6	mA

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	4.8	6.8	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.0	ns	Between any two units at the same temperature, voltage, and load
Jitter			290		ps p-p	See the Jitter Measurement section
			45		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DD1}			V	
Logic Low	V_{IL}			0.3 × V_{DD1}	V	
Output Voltage						
Logic High	V_{OH}	V_{DD2} − 0.1	V_{DD2}		V	I_O = −20 µA, V_I = V_{IH}
		V_{DD2} − 0.4	V_{DD2} − 0.2		V	I_O = −2 mA, V_I = V_{IH}
Logic Low	V_{OL}		0.0	0.1	V	I_O = 20 µA, V_I = V_{IL}
			0.2	0.4	V	I_O = 2 mA, V_I = V_{IL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_I ≤ V_{DD1}
Quiescent Supply Current						
	$I_{DD1 (Q)}$		0.8	1.3	mA	V_I = 0 (N0), 1 (N1)[1]
	$I_{DD2 (Q)}$		0.9	1.4	mA	V_I = 0 (N0), 1 (N1)[1]
	$I_{DD1 (Q)}$		3.6	5.8	mA	V_I = 1 (N0), 0 (N1)[1]
	$I_{DD2 (Q)}$		0.9	1.4	mA	V_I = 1 (N0), 0 (N1)[1]
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[2]	$\|CM_H\|$	75	100		kV/µs	$V_I = V_{DD1}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_I = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] N0 indicates the ADuM110N0 models and N1 indicates the ADuM110N1 models. See the Ordering Guide section.
[2] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DD2}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 4. Total Supply Current vs. Data Throughput—3.3 V Operation

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
Supply Current Side 1	I_{DD1}		2.2	3.5		2.4	3.6		3.2	4.6	mA
Supply Current Side 2	I_{DD2}		0.9	1.5		1.4	2.0		2.8	4.3	mA

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

All typical specifications are at T_A = 25°C, $V_{DD1} = V_{DD2}$ = 2.5 V. Minimum/maximum specifications apply over the entire recommended operation range: 2.25 V ≤ V_{DD1} ≤ 2.75 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	5.0	7.0	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.0	ns	Between any two units at the same temperature, voltage, load
Jitter			320		ps p-p	See the Jitter Measurement section
			65		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DD1}			V	
Logic Low	V_{IL}			0.3 × V_{DD1}	V	
Output Voltage						
Logic High	V_{OH}	V_{DD2} − 0.1	V_{DD2}		V	I_O = −20 µA, $V_I = V_{IH}$
		V_{DD2} − 0.4	V_{DD2} − 0.2		V	I_O = −2 mA, $V_I = V_{IH}$
Logic Low	V_{OL}		0.0	0.1	V	I_O = 20 µA, $V_I = V_{IL}$
			0.2	0.4	V	I_O = 2 mA, $V_I = V_{IL}$
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_I ≤ V_{DD1}
Quiescent Supply Current						
	$I_{DD1 (Q)}$		0.8	1.1	mA	V_I = 0 (N0), 1 (N1)[1]
	$I_{DD2 (Q)}$		0.9	1.2	mA	V_I = 0 (N0), 1 (N1)[1]
	$I_{DD1 (Q)}$		3.5	5.6	mA	V_I = 1 (N0), 0 (N1)[1]
	$I_{DD2 (Q)}$		1.0	1.2	mA	V_I = 1 (N0), 0 (N1)[1]
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Undervoltage Lockout						
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[2]	$\|CM_H\|$	75	100		kV/µs	$V_I = V_{DD1}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_I = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] N0 indicates the ADuM110N0 models and N1 indicates the ADuM110N1 models. See the Ordering Guide section.
[2] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DD2}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 6. Total Supply Current vs. Data Throughput—2.5 V Operation

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
Supply Current Side 1	I_{DD1}		2.2	3.4		2.4	3.6		3.2	4.3	mA
Supply Current Side 2	I_{DD2}		0.9	1.4		1.3	1.8		2.3	3.5	mA

ELECTRICAL CHARACTERISTICS—1.8 V OPERATION

All typical specifications are at T_A = 25°C, $V_{DD1} = V_{DD2}$ = 1.8 V. Minimum/maximum specifications apply over the entire recommended operation range: 1.7 V ≤ V_{DD1} ≤ 1.9 V, 1.7 V ≤ V_{DD2} ≤ 1.9 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	5.8	8.7	15	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.0	ns	Between any two units at the same temperature, voltage, and load
Jitter			630		ps p-p	See the Jitter Measurement section
			190		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DD1}			V	
Logic Low	V_{IL}			0.3 × V_{DD1}	V	
Output Voltage						
Logic High	V_{OH}	V_{DD2} − 0.1	V_{DD2}		V	I_O = −20 µA, $V_I = V_{IH}$
		V_{DD2} − 0.4	V_{DD2} − 0.2		V	I_O = −2 mA, $V_I = V_{IH}$
Logic Low	V_{OL}		0.0	0.1	V	I_O = 20 µA, $V_I = V_{IL}$
			0.2	0.4	V	I_O = 2 mA, $V_I = V_{IL}$
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_I ≤ V_{DD1}
Quiescent Supply Current						
	$I_{DD1 (Q)}$		0.7	1.1	mA	V_I = 0 (N0), 1 (N1)[1]
	$I_{DD2 (Q)}$		0.9	1.2	mA	V_I = 0 (N0), 1 (N1)[1]
	$I_{DD1 (Q)}$		3.4	5.4	mA	V_I = 1 (N0), 0 (N1)[1]
	$I_{DD2 (Q)}$		0.9	1.2	mA	V_I = 1 (N0), 0 (N1)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[2]	$\|CM_H\|$	75	100		kV/µs	$V_I = V_{DD1}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_I = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] N0 indicates the ADuM110N0 models and N1 indicates the ADuM110N1 models. See the Ordering Guide section.
[2] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DD2}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 8. Total Supply Current vs. Data Throughput—1.8 V Operation

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
Supply Current Side 1	I_{DD1}		2.1	3.1		2.3	3.4		3.0	4.2	mA
Supply Current Side 2	I_{DD2}		0.9	1.2		1.2	1.6		2.2	3.2	mA

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 9.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	4.0	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	4.0	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	4.5	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

PACKAGE CHARACTERISTICS

Table 10.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		80		°C/W	Thermocouple located at center of package underside

[1] The ADuM110N is considered a 2-terminal device: Pin 1 through Pin 4 are shorted together, and Pin 5 through Pin 8 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

See Table 15 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 11.

UL	CSA(Pending)	VDE	CQC
Recognized Under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN VDE V 0884-11:2017-01[2]	Certified by CQC11-471543-2015
Single Protection, 3000 V rms Isolation Voltage	IEC 62368-1:2014 Edition 2 and CSA 62368-1-14 (Pending)	Reinforced insulation, 565 V peak, V_{IOSM} = 6250 V peak	GB4943.1-2011
	Basic insulation at 400 V rms		
	Reinforced insulation at 200 V rms		Basic insulation at 400 V rms (565 V peak), tropical climate, altitude ≤5000 meters
	IEC 60601-1 Edition 3.1		
	Basic insulation (1 MOPP), 250 V rms		
	CSA 61010-1-12 and IEC 61010-1 Third Edition		
	Basic insulation at 300 V rms mains, 400 V rms		
	Reinforced insulation at 300 V rms mains, 200 V secondary		
File E214100	File 205078	File 2471900-4880-0003	File CQC18001192422

[1] In accordance with UL 1577, each ADuM110N is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec.
[2] In accordance with DIN VDE V 0884-11, each ADuM110N is proof tested by applying an insulation test voltage ≥ 1059 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11 approval.

DIN VDE V 0884-11:2017-01 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The * marking on packages denotes DIN VDE V 0884-11 approval.

Table 12.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	565	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd\,(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd\,(m)}$	1059	V peak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd\,(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd\,(m)}$	848	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd\,(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		678	V peak
Highest Allowable Overvoltage		V_{IOTM}	4200	V peak
Surge Isolation Voltage Reinforced	V peak = 10.0 kV, 1.2 μs rise time, 50 μs, 50% fall time	V_{IOSM}	6250	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		PS	1.56	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	>10^9	Ω

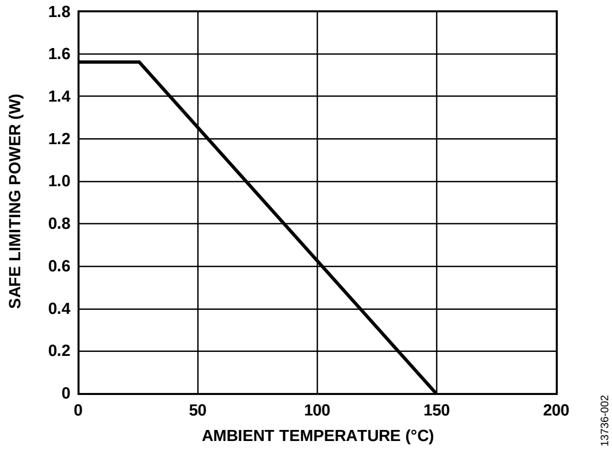

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN VDE V 0884-11

RECOMMENDED OPERATING CONDITIONS

Table 13.

Parameter	Symbol	Rating
Operating Temperature	T_A	−40°C to +125°C
Supply Voltages		
V_{DD1}		1.7 V to 5.5 V
V_{DD2}		1.7 V to 5.5 V
Input Signal Rise and Fall Times		1.0 ms

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 14.

Parameter	Rating
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C
Supply Voltages	
V_{DD1} to GND_1	−0.5 V to +7.0 V
V_{DD2} to GND_2	−0.5 V to +7.0 V
Input Voltages (V_I)	−0.5 V to V_{DDI}[1] + 0.5 V
Output Voltages (V_O)	−0.5 V to V_{DDO}[2] + 0.5 V
Average Output Current per Pin[3]	
Side 2 Output Current (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[4]	−150 kV/μs to +150 kV/μs

[1] V_{DDI} is the input side supply voltage.
[2] V_{DDO} is the output side supply voltage.
[3] See Figure 2 for the maximum rated current values for various temperatures.
[4] Refers to the common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 15. Maximum Continuous Working Voltage[1]

Parameter	Rating	Constraint
AC Voltage		Lifetime limited by package creepage maximum approved working voltage per IEC 60664-1
Bipolar Waveform		
Basic Insulation	789 V peak	
Reinforced Insulation	403 V peak	
Unipolar Waveform		
Basic Insulation	909 V peak	
Reinforced Insulation	469 V peak	
DC Voltage		Lifetime limited by package creepage maximum approved working voltage per IEC 60664-1
Basic Insulation	558 V peak	
Reinforced Insulation	285 V peak	

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Truth Table

Table 16. Truth Table (Positive Logic)

V_I Input[1]	V_{DDI} State	V_{DD2} State	Default Low (N0),[2] V_O Output[1]	Default High (N1),[2] V_O Output[1]	Test Conditions/ Comments
L	Powered	Powered	L	L	Normal operation
H	Powered	Powered	H	H	Normal operation
X[3]	Unpowered	Powered	L	H	Fail-safe output
X[3]	Powered	Unpowered	Indeterminate	Indeterminate	

[1] H means high, L means low, and X means don't care.
[2] N0 indicates the ADuM110N0 models and N1 indicates the ADuM110N1 models. See the Ordering Guide section.
[3] The input pin (V_I) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

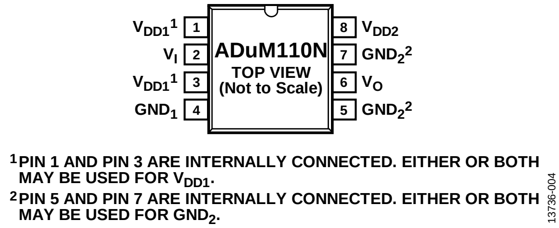

Figure 3. Pin Configuration

Table 17. Pin Function Descriptions

Pin No.	Mnemonic	Description[1]
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_I	Logic Input.
3	V_{DD1}	Supply Voltage for Isolator Side 1.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Ground reference for Isolator Side 2.
6	V_O	Logic Output.
7	GND_2	Ground 2. Ground reference for Isolator Side 2.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

[1] Refer to the AN-1109 Application Note for specific layout guidelines.

TYPICAL PERFORMANCE CHARACTERISTICS

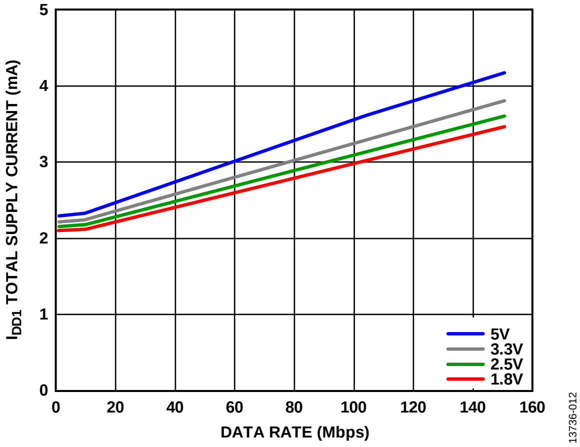

Figure 4. I_{DD1} Total Supply Current vs. Data Rate at Various Voltages

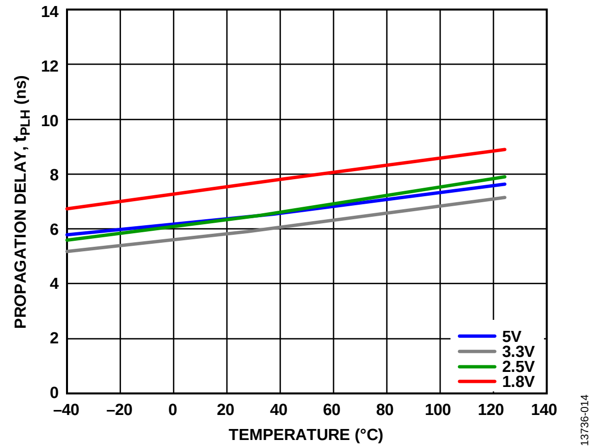

Figure 6. Propagation Delay, t_{PLH} vs. Temperature at Various Voltages

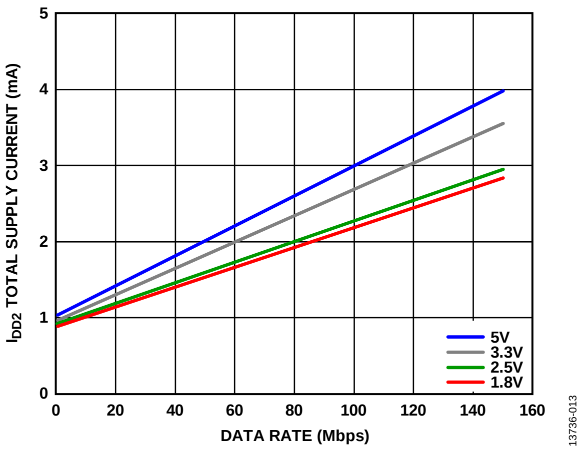

Figure 5. I_{DD2} Total Supply Current vs. Data Rate at Various Voltages

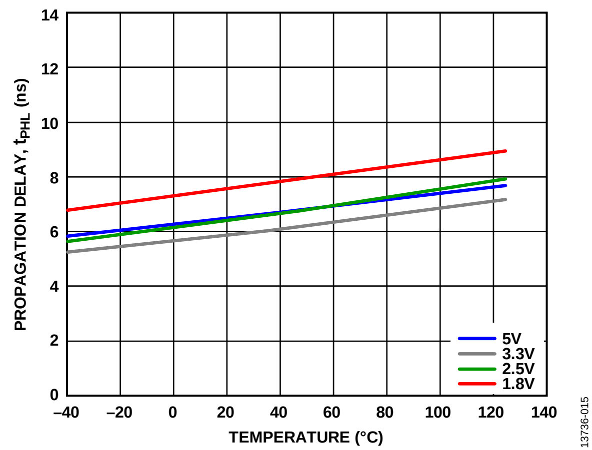

Figure 7. Propagation Delay, t_{PHL} vs. Temperature at Various Voltages

APPLICATIONS INFORMATION

OVERVIEW

The ADuM110N uses a high frequency carrier to transmit data across the isolation barrier using *i*Coupler chip scale transformer coils separated by layers of polyimide isolation. Using an on-off keying (OOK) technique and the differential architecture shown in Figure 9 and Figure 10, the ADuM110N has very low propagation delay and high speed. Internal regulators and input/output design techniques allow logic and supply voltages over a wide range from 1.7 V to 5.5 V, offering voltage translation of 1.8 V, 2.5 V, 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques.

Figure 9 shows the waveforms for the ADuM110N0 models, which have the condition of the fail-safe output state equal to low, where the carrier waveform is off when the input state is low. If the input side is off or not operating, the fail-safe output state of low (noted by a 0 in the model number) sets the output to low. For the ADuM110N1 models, which have a fail-safe output state of high, Figure 10 shows the conditions where the carrier waveform is off when the input state is high. When the input side is off or not operating, the fail-safe output state of high (noted by a 1 in the model number) sets the output to high. See the Ordering Guide for the model numbers that have the fail-safe output state of low or the fail-safe output state of high.

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM110N digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 8). Bypass capacitors are most conveniently connected between Pin 1 and Pin 4 for V_{DD1} and between Pin 5 and Pin 8 for V_{DD2}. The recommended bypass capacitor value is between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm.

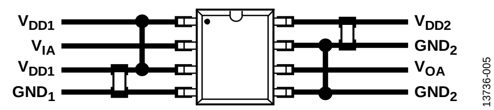

Figure 8. Recommended PCB Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, thereby leading to latch-up or permanent damage.

See the AN-1109 Application Note for board layout guidelines.

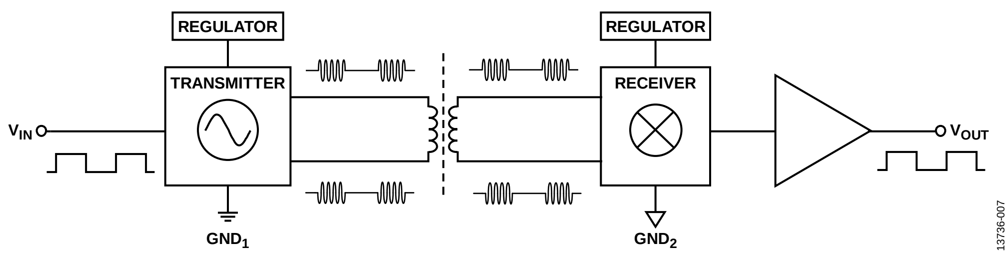

Figure 9. Operational Block Diagram of a Single Channel with a Low Fail-Safe Output State

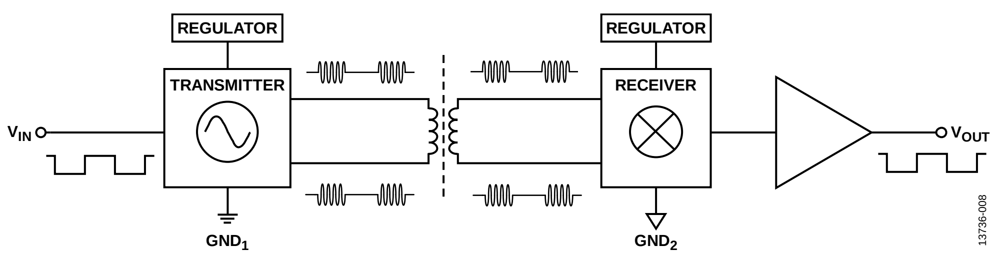

Figure 10. Operational Block Diagram of a Single Channel with a High Fail-Safe Output State

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a Logic 0 output may differ from the propagation delay to a Logic 1 output.

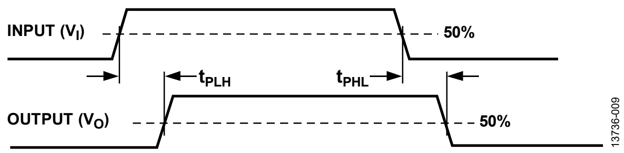

Figure 11. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Propagation delay skew is the maximum amount the propagation delay differs between multiple ADuM110N components operating under the same conditions

JITTER MEASUREMENT

Figure 12 shows the eye diagram for the ADuM110N. The measurement was taken using an Agilent 81110A pulse pattern generator at 150 Mbps with pseudorandom bit sequences (PRBS) 2(n − 1), n = 14, for 5 V supplies. Jitter was measured with the Tektronix Model 5104B oscilloscope, 1 GHz, 10 GS/sec with the DPOJET jitter and eye diagram analysis tools. The result shows a typical measurement on the ADuM110N with 380 ps p-p jitter.

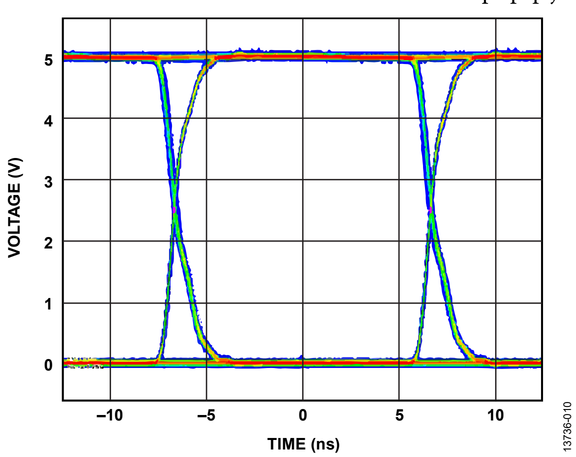

Figure 12. Eye Diagram

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking, and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the ADuM110N isolators are presented in Table 9.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. It is the working voltage applicable to tracking that is specified in most standards.

Testing and modeling have shown that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as: dc stress, which causes very little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as is shown in Equation 2. For insulation wear out with the polyimide materials used in these products, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\,RMS}^{2} + V_{DC}^{2}} \quad (1)$$

or

$$V_{ACRMS} = \sqrt{V_{RMS}^{2} - V_{DC}^{2}} \quad (2)$$

where:
$V_{AC\,RMS}$ is the time varying portion of the working voltage.
V_{DC} is the dc offset of the working voltage.
V_{RMS} is the total rms working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 $V_{AC\ RMS}$ and a 400 V_{DC} bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance and lifetime of a device, see Figure 13 and the following equations.

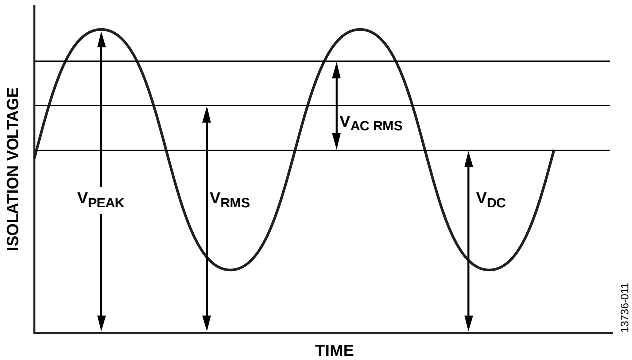

Figure 13. Critical Voltage Example

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{{V_{AC\ RMS}}^2 + {V_{DC}}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

$$V_{RMS} = 466\ \text{V}$$

This is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 2.

$$V_{ACRMS} = \sqrt{{V_{RMS}}^2 - {V_{DC}}^2}$$

$$V_{ACRMS} = \sqrt{466^2 - 400^2}$$

$$V_{ACRMS} = 240\ \text{V rms}$$

In this case, the ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage in Table 15 for the expected lifetime, less than a 60 Hz sine wave, and it is well within the limit for a 50-year service life.

Note that the dc working voltage limit in Table 15 is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.