# Quad-Channel Digital Isolators

Data Sheet

# ADuM1410/ADuM1411/ADuM1412

## FEATURES

- Low power operation
  - 5 V operation
    - 1.3 mA per channel maximum at 0 Mbps to 2 Mbps
    - 4.0 mA per channel maximum at 10 Mbps
  - 3 V operation
    - 0.8 mA per channel maximum at 0 Mbps to 2 Mbps
    - 1.8 mA per channel maximum at 10 Mbps
- Bidirectional communication
- 3 V/5 V level translation
- High temperature operation: 105°C
- Up to 10 Mbps data rate (NRZ)
- Programmable default output state
- High common-mode transient immunity: >25 kV/µs
- 16-lead, RoHS compliant, SOIC wide body package
- Safety and regulatory approvals
  - UL recognition: 3750 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A
  - VDE certificate of conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
    - $V_{IORM}$ = 560 V peak
  - TÜV approval: IEC/EN 60950-1

## APPLICATIONS

- General-purpose multichannel isolation
- SPI interface/data converter isolation
- RS-232/RS-422/RS-485 transceivers
- Industrial field bus isolation

## FUNCTIONAL BLOCK DIAGRAMS

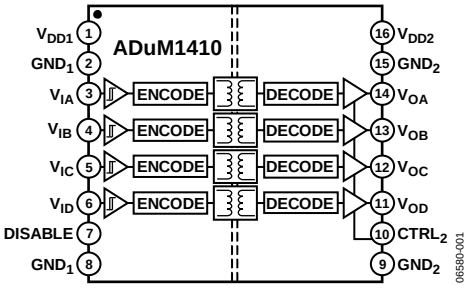



Figure 1. ADuM1410

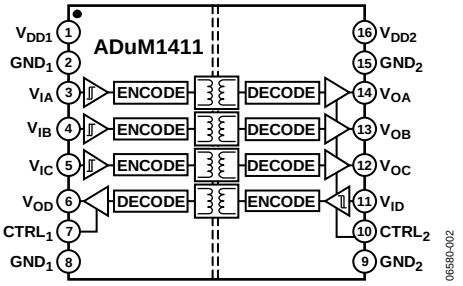



Figure 2. ADuM1411

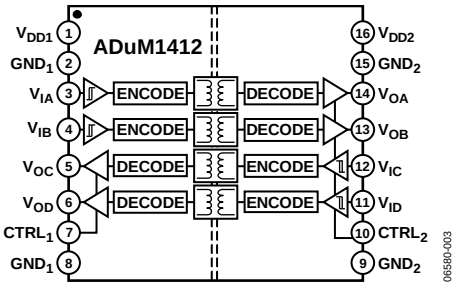



Figure 3. ADuM1412

## GENERAL DESCRIPTION

The ADuM1410/ADuM1411/ADuM1412[1] are four-channel digital isolators based on Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic air core transformer technologies, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. The usual concerns that arise with optocouplers, such as uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects, are eliminated with the simple *i*Coupler digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these *i*Coupler products. Furthermore, *i*Coupler devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM1410/ADuM1411/ADuM1412 isolators provide four independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide) up to 10 Mbps. All models operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. All products also have a default output control pin. This allows the user to define the logic state the outputs are to adopt in the absence of the input power. Unlike other optocoupler alternatives, the ADuM1410/ADuM1411/ADuM1412 isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329.

Rev. M Document Feedback



One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 
Technical Support www.analog.com

# TABLE OF CONTENTS



## REVISION HISTORY

**8/15—Rev. L to Rev. M**
Changes to Table 5 and Table 6 ... 10

**7/15—Rev. K to Rev. L**
Changes to Table 5 and Table 6 ... 10

**4/15—Rev. J to Rev. K**
Changed ADuM141x to ADuM1410/ADuM1411/ADuM1412 ... Throughout
Change to Features Section ... 1
Changes to Table 5 and Table 6 ... 10

**4/14—Rev. I to Rev. J**
Change to Table 5 ... 10

**3/12—Rev. H to Rev. I**
Created Hyperlink for Safety and Regulatory Approvals Entry in Features Section ... 1
Change to PC Board Layout Section ... 19

**11/10—Rev. G to Rev. H**
Added TÜV Approval to Features Section ... 1
Added TÜV Column, Table 5 ... 10

**6/07—Rev. F to Rev. G**
Updated VDE Certification Throughout ... 1
Changes to Features and Applications ... 1
Changes to DC Specifications in Table 1 ... 3
Changes to DC Specifications in Table 2 ... 5
Changes to DC Specifications in Table 3 ... 7
Changes to Regulatory Information Section ... 10
Added Table 10 ... 12
Added Insulation Lifetime Section ... 21

**2/07—Rev. E to Rev. F**
Added ADuM1410ARWZ ... Universal
Updated Pin Name CTRL to $CTRL_2$ Throughout ... 1
Changes to Ordering Guide ... 21

**10/06—Rev. D to Rev. E**
Added ADuM1411 and ADuM1412 ... Universal
Deleted ADuM1310 ... Universal
Changes to Features ... 1
Changes to Specifications Section ... 3
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 20

**3/06—Rev. C to Rev. D**
Added Note 1 and Changes to Figure 2 ... 1
Changes to Absolute Maximum Ratings ... 11

**11/05—Revision C: Initial Version**

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—5 V OPERATION

4.5 V ≤ $V_{DD1}$ ≤ 5.5 V, 4.5 V ≤ $V_{DD2}$ ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = $V_{DD2}$ = 5 V. All voltages are relative to their respective ground.

**Table 1.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Input Supply Current per Channel, Quiescent | $I_{DDI (Q)}$ | | 0.50 | 0.73 | mA | |
| Output Supply Current per Channel, Quiescent | $I_{DDO (Q)}$ | | 0.38 | 0.53 | mA | |
| ADuM1410, Total Supply Current, Four Channels[1] | | | | | | |
| DC to 2 Mbps | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1 (Q)}$ | | 2.4 | 3.2 | mA | DC to 1 MHz logic signal frequency |
| $V_{DD2}$ Supply Current | $I_{DD2 (Q)}$ | | 1.2 | 1.6 | mA | DC to 1 MHz logic signal frequency |
| 10 Mbps (BRWZ Version Only) | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1 (10)}$ | | 8.8 | 12 | mA | 5 MHz logic signal frequency |
| $V_{DD2}$ Supply Current | $I_{DD2 (10)}$ | | 2.8 | 4.0 | mA | 5 MHz logic signal frequency |
| ADuM1411, Total Supply Current, Four Channels[1] | | | | | | |
| DC to 2 Mbps | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1 (Q)}$ | | 2.2 | 2.8 | mA | DC to 1 MHz logic signal frequency |
| $V_{DD2}$ Supply Current | $I_{DD2 (Q)}$ | | 1.8 | 2.4 | mA | DC to 1 MHz logic signal frequency |
| 10 Mbps (BRWZ Version Only) | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1 (10)}$ | | 5.4 | 7.6 | mA | 5 MHz logic signal frequency |
| $V_{DD2}$ Supply Current | $I_{DD2 (10)}$ | | 3.8 | 5.3 | mA | 5 MHz logic signal frequency |
| ADuM1412, Total Supply Current, Four Channels[1] | | | | | | |
| DC to 2 Mbps | | | | | | |
| $V_{DD1}$ or $V_{DD2}$ Supply Current | $I_{DD1 (Q)}$, $I_{DD2 (Q)}$ | | 2.0 | 2.6 | mA | DC to 1 MHz logic signal frequency |
| 10 Mbps (BRWZ Version Only) | | | | | | |
| $V_{DD1}$ or $V_{DD2}$ Supply Current | $I_{DD1 (10)}$, $I_{DD2 (10)}$ | | 4.6 | 6.5 | mA | 5 MHz logic signal frequency |
| All Models | | | | | | |
| Input Currents | $I_{IA}$, $I_{IB}$, $I_{IC}$, $I_{ID}$, $I_{CTRL1}$, $I_{CTRL2}$, $I_{DISABLE}$ | −10 | +0.01 | +10 | µA | 0 V ≤ $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$ ≤ $V_{DD1}$ or $V_{DD2}$, 0 V ≤ $V_{CTRL1}$, $V_{CTRL2}$ ≤ $V_{DD1}$ or $V_{DD2}$, 0 V ≤ $V_{DISABLE}$ ≤ $V_{DD1}$ |
| Logic High Input Threshold | $V_{IH}$ | 2.0 | | | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | 0.8 | V | |
| Logic High Output Voltages | $V_{OAH}$, $V_{OBH}$, $V_{OCH}$, $V_{ODH}$ | ($V_{DD1}$ or $V_{DD2}$) − 0.1 | 5.0 | | V | $I_{Ox}$ = −20 µA, $V_{Ix}$ = $V_{IxH}$ |
| | | ($V_{DD1}$ or $V_{DD2}$) − 0.4 | 4.8 | | V | $I_{Ox}$ = −4 mA, $V_{Ix}$ = $V_{IxH}$ |
| Logic Low Output Voltages | $V_{OAL}$, $V_{OBL}$, $V_{OCL}$, $V_{ODL}$ | | 0.0 | 0.1 | V | $I_{Ox}$ = 20 µA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.04 | 0.1 | V | $I_{Ox}$ = 400 µA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}$ = 4 mA, $V_{Ix}$ = $V_{IxL}$ |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| SWITCHING SPECIFICATIONS | | | | | | |
| ADuM1410ARWZ/ADuM1411ARWZ/ ADuM1412ARWZ | | | | | | |
| Minimum Pulse Width[2] | PW | | | 1000 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Maximum Data Rate[3] | | 1 | | | Mbps | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay[4] | $t_{PHL}$, $t_{PLH}$ | 20 | 65 | 100 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4] | PWD | | | 40 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay Skew[5] | $t_{PSK}$ | | | 50 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching[6] | $t_{PSKCD/OD}$ | | | 50 | ns | $C_L$ = 15 pF, CMOS signal levels |
| ADuM1410BRWZ/ADuM1411BRWZ/ ADuM1412BRWZ | | | | | | |
| Minimum Pulse Width[2] | PW | | | 100 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Maximum Data Rate[3] | | 10 | | | Mbps | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay[4] | $t_{PHL}$, $t_{PLH}$ | 20 | 30 | 50 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4] | PWD | | | 5 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Change vs. Temperature | | | 5 | | ps/°C | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay Skew[5] | $t_{PSK}$ | | | 30 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching, Codirectional Channels[6] | $t_{PSKCD}$ | | | 5 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching, Opposing-Directional Channels[6] | $t_{PSKOD}$ | | | 6 | ns | $C_L$ = 15 pF, CMOS signal levels |
| All Models | | | | | | |
| Output Rise/Fall Time (10% to 90%) | $t_R/t_F$ | | 2.5 | | ns | $C_L$ = 15 pF, CMOS signal levels |
| Common-Mode Transient Immunity at Logic High Output[7] | $\|CM_H\|$ | 25 | 35 | | kV/µs | $V_{Ix} = V_{DD1}$ or $V_{DD2}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output[7] | $\|CM_L\|$ | 25 | 35 | | kV/µs | $V_{Ix}$ = 0 V, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Refresh Rate | $f_r$ | | 1.2 | | Mbps | |
| Input Enable Time[8] | $t_{ENABLE}$ | | | 2.0 | µs | $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$ = 0 V or $V_{DD1}$ |
| Input Disable Time[8] | $t_{DISABLE}$ | | | 5.0 | µs | $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$ = 0 V or $V_{DD1}$ |
| Input Dynamic Supply Current per Channel[9] | $I_{DDI (D)}$ | | 0.12 | | mA/ Mbps | |
| Output Dynamic Supply Current per Channel[9] | $I_{DDO (D)}$ | | 0.04 | | mA/ Mbps | |

[1] The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total $V_{DD1}$ and $V_{DD2}$ supply currents as a function of data rate for ADuM1410/ADuM1411/ADuM1412 channel configurations.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[4] $t_{PHL}$ propagation delay is measured from the 50% level of the falling edge of the $V_{Ix}$ signal to the 50% level of the falling edge of the $V_{Ox}$ signal. $t_{PLH}$ propagation delay is measured from the 50% level of the rising edge of the $V_{Ix}$ signal to the 50% level of the rising edge of the $V_{Ox}$ signal.

[5] $t_{PSK}$ is the magnitude of the worst-case difference in $t_{PHL}$ or $t_{PLH}$ that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

[7] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[8] Input enable time is the duration from when $V_{DISABLE}$ is set low until the output states are guaranteed to match the input states in the absence of any input data logic transitions. If an input data logic transition within a given channel does occur within this time interval, the output of that channel reaches the correct state within the much shorter duration as determined by the propagation delay specifications within this data sheet. Input disable time is the duration from when $V_{DISABLE}$ is set high until the output states are guaranteed to reach their programmed output levels, as determined by the $CTRL_2$ logic state (see Table 14).

[9] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

## ELECTRICAL CHARACTERISTICS—3 V OPERATION

2.7 V ≤ $V_{DD1}$ ≤ 3.6 V, 2.7 V ≤ $V_{DD2}$ ≤ 3.6 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = $V_{DD2}$ = 3.0 V. All voltages are relative to their respective ground.

**Table 2.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Input Supply Current per Channel, Quiescent | $I_{DDI (Q)}$ | | 0.25 | 0.38 | mA | |
| Output Supply Current per Channel, Quiescent | $I_{DDO (Q)}$ | | 0.19 | 0.33 | mA | |
| ADuM1410, Total Supply Current, Four Channels[1] | | | | | | |
| DC to 2 Mbps | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1 (Q)}$ | | 1.2 | 1.6 | mA | DC to 1 MHz logic signal frequency |
| $V_{DD2}$ Supply Current | $I_{DD2 (Q)}$ | | 0.8 | 1.0 | mA | DC to 1 MHz logic signal frequency |
| 10 Mbps (BRWZ Version Only) | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1 (10)}$ | | 4.5 | 6.5 | mA | 5 MHz logic signal frequency |
| $V_{DD2}$ Supply Current | $I_{DD2 (10)}$ | | 1.4 | 1.8 | mA | 5 MHz logic signal frequency |
| ADuM1411, Total Supply Current, Four Channels[1] | | | | | | |
| DC to 2 Mbps | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1 (Q)}$ | | 1.0 | 1.9 | mA | DC to 1 MHz logic signal frequency |
| $V_{DD2}$ Supply Current | $I_{DD2 (Q)}$ | | 0.9 | 1.7 | mA | DC to 1 MHz logic signal frequency |
| 10 Mbps (BRWZ Version Only) | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1 (10)}$ | | 3.1 | 4.5 | mA | 5 MHz logic signal frequency |
| $V_{DD2}$ Supply Current | $I_{DD2 (10)}$ | | 2.1 | 3.0 | mA | 5 MHz logic signal frequency |
| ADuM1412, Total Supply Current, Four Channels[1] | | | | | | |
| DC to 2 Mbps | | | | | | |
| $V_{DD1}$ or $V_{DD2}$ Supply Current | $I_{DD1 (Q)}$, $I_{DD2 (Q)}$ | | 1.0 | 1.8 | mA | DC to 1 MHz logic signal frequency |
| 10 Mbps (BRWZ Version Only) | | | | | | |
| $V_{DD1}$ or $V_{DD2}$ Supply Current | $I_{DD1 (10)}$, $I_{DD2 (10)}$ | | 2.6 | 3.8 | mA | 5 MHz logic signal frequency |
| All Models | | | | | | |
| Input Currents | $I_{IA}$, $I_{IB}$, $I_{IC}$, $I_{ID}$, $I_{CTRL1}$, $I_{CTRL2}$, $I_{DISABLE}$ | −10 | +0.01 | +10 | µA | 0 V ≤ $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$ ≤ $V_{DD1}$ or $V_{DD2}$, 0 V ≤ $V_{CTRL1}$, $V_{CTRL2}$ ≤ $V_{DD1}$ or $V_{DD2}$, 0 V ≤ $V_{DISABLE}$ ≤ $V_{DD1}$ |
| Logic High Input Threshold | $V_{IH}$ | 1.6 | | | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | 0.4 | V | |
| Logic High Output Voltages | $V_{OAH}$, $V_{OBH}$, $V_{OCH}$, $V_{ODH}$ | ($V_{DD1}$ or $V_{DD2}$) − 0.1 | 3.0 | | V | $I_{Ox}$ = −20 µA, $V_{Ix}$ = $V_{IxH}$ |
| | | ($V_{DD1}$ or $V_{DD2}$) − 0.4 | 2.8 | | V | $I_{Ox}$ = −4 mA, $V_{Ix}$ = $V_{IxH}$ |
| Logic Low Output Voltages | $V_{OAL}$, $V_{OBL}$, $V_{OCL}$, $V_{ODL}$ | | 0.0 | 0.1 | V | $I_{Ox}$ = 20 µA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.04 | 0.1 | V | $I_{Ox}$ = 400 µA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}$ = 4 mA, $V_{Ix}$ = $V_{IxL}$ |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| SWITCHING SPECIFICATIONS | | | | | | |
| ADuM1410ARWZ/ADuM1411ARWZ/ ADuM1412ARWZ | | | | | | |
| Minimum Pulse Width[2] | PW | | | 1000 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Maximum Data Rate[3] | | 1 | | | Mbps | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay[4] | $t_{PHL}$, $t_{PLH}$ | 20 | 75 | 100 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4] | PWD | | | 40 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay Skew[5] | $t_{PSK}$ | | | 50 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching[6] | $t_{PSKCD/OD}$ | | | 50 | ns | $C_L$ = 15 pF, CMOS signal levels |
| ADuM1410BRWZ/ADuM1411BRWZ/ ADuM1412BRWZ | | | | | | |
| Minimum Pulse Width[2] | PW | | | 100 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Maximum Data Rate[3] | | 10 | | | Mbps | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay[4] | $t_{PHL}$, $t_{PLH}$ | 20 | 40 | 60 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4] | PWD | | | 5 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Change vs. Temperature | | | 5 | | ps/°C | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay Skew[5] | $t_{PSK}$ | | | 30 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching, Codirectional Channels[6] | $t_{PSKCD}$ | | | 5 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching, Opposing-Directional Channels[6] | $t_{PSKOD}$ | | | 6 | ns | $C_L$ = 15 pF, CMOS signal levels |
| All Models | | | | | | |
| Output Rise/Fall Time (10% to 90%) | $t_R/t_F$ | | 2.5 | | ns | $C_L$ = 15 pF, CMOS signal levels |
| Common-Mode Transient Immunity at Logic High Output[7] | $\|CM_H\|$ | 25 | 35 | | kV/µs | $V_{Ix} = V_{DD1}$ or $V_{DD2}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output[7] | $\|CM_L\|$ | 25 | 35 | | kV/µs | $V_{Ix}$ = 0 V, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Refresh Rate | $f_r$ | | 1.1 | | Mbps | |
| Input Enable Time[8] | $t_{ENABLE}$ | | 2.0 | | µs | $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$ = 0 V or $V_{DD1}$ |
| Input Disable Time[8] | $t_{DISABLE}$ | | 5.0 | | µs | $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$ = 0 V or $V_{DD1}$ |
| Input Dynamic Supply Current per Channel[9] | $I_{DDI (D)}$ | | 0.07 | | mA/ Mbps | |
| Output Dynamic Supply Current per Channel[9] | $I_{DDO (D)}$ | | 0.02 | | mA/ Mbps | |

[1] The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total $V_{DD1}$ and $V_{DD2}$ supply currents as a function of data rate for ADuM1410/ADuM1411/ADuM1412 channel configurations.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[4] $t_{PHL}$ propagation delay is measured from the 50% level of the falling edge of the $V_{Ix}$ signal to the 50% level of the falling edge of the $V_{Ox}$ signal. $t_{PLH}$ propagation delay is measured from the 50% level of the rising edge of the $V_{Ix}$ signal to the 50% level of the rising edge of the $V_{Ox}$ signal.

[5] $t_{PSK}$ is the magnitude of the worst-case difference in $t_{PHL}$ or $t_{PLH}$ that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

[7] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[8] Input enable time is the duration from when $V_{DISABLE}$ is set low until the output states are guaranteed to match the input states in the absence of any input data logic transitions. If an input data logic transition within a given channel does occur within this time interval, the output of that channel reaches the correct state within the much shorter duration as determined by the propagation delay specifications within this data sheet. Input disable time is the duration from when $V_{DISABLE}$ is set high until the output states are guaranteed to reach their programmed output levels, as determined by the $CTRL_2$ logic state (see Table 14).

[9] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

## ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V OPERATION

5 V/3 V operation: 4.5 V ≤ $V_{DD1}$ ≤ 5.5 V, 2.7 V ≤ $V_{DD2}$ ≤ 3.6 V; 3 V/5 V operation: 2.7 V ≤ $V_{DD1}$ ≤ 3.6 V, 4.5 V ≤ $V_{DD2}$ ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A$ = 25°C; $V_{DD1}$ = 3.0 V, $V_{DD2}$ = 5 V; or $V_{DD1}$ = 5 V, $V_{DD2}$ = 3.0 V. All voltages are relative to their respective ground.

**Table 3.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Input Supply Current per Channel, Quiescent | $I_{DDI (Q)}$ | | | | | |
| 5 V/3 V Operation | | | 0.50 | 0.73 | mA | |
| 3 V/5 V Operation | | | 0.25 | 0.38 | mA | |
| Output Supply Current per Channel, Quiescent | $I_{DDO (Q)}$ | | | | | |
| 5 V/3 V Operation | | | 0.19 | 0.33 | mA | |
| 3 V/5 V Operation | | | 0.38 | 0.53 | mA | |
| ADuM1410, Total Supply Current, Four Channels[1] | | | | | | |
| DC to 2 Mbps | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1 (Q)}$ | | | | | |
| 5 V/3 V Operation | | | | | | DC to 1 MHz logic signal frequency |
| | | | 2.4 | 3.2 | mA | |
| 3 V/5 V Operation | | | | | | DC to 1 MHz logic signal frequency |
| | | | 1.2 | 1.6 | mA | |
| $V_{DD2}$ Supply Current | $I_{DD2 (Q)}$ | | | | | |
| 5 V/3 V Operation | | | | | | DC to 1 MHz logic signal frequency |
| | | | 0.8 | 1.0 | mA | |
| 3 V/5 V Operation | | | | | | DC to 1 MHz logic signal frequency |
| | | | 1.2 | 1.6 | mA | |
| 10 Mbps (BRWZ Version Only) | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1 (10)}$ | | | | | |
| 5 V/3 V Operation | | | 8.6 | 11 | mA | 5 MHz logic signal frequency |
| 3 V/5 V Operation | | | 3.4 | 6.5 | mA | 5 MHz logic signal frequency |
| $V_{DD2}$ Supply Current | $I_{DD2 (10)}$ | | | | | |
| 5 V/3 V Operation | | | 1.4 | 1.8 | mA | 5 MHz logic signal frequency |
| 3 V/5 V Operation | | | 2.6 | 3.0 | mA | 5 MHz logic signal frequency |
| ADuM1411, Total Supply Current, Four Channels[1] | | | | | | |
| DC to 2 Mbps | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1 (Q)}$ | | | | | |
| 5 V/3 V Operation | | | | | | DC to 1 MHz logic signal frequency |
| | | | 2.2 | 2.8 | mA | |
| 3 V/5 V Operation | | | | | | DC to 1 MHz logic signal frequency |
| | | | 1.0 | 1.9 | mA | |
| $V_{DD2}$ Supply Current | $I_{DD2 (Q)}$ | | | | | |
| 5 V/3 V Operation | | | | | | DC to 1 MHz logic signal frequency |
| | | | 0.9 | 1.7 | mA | |
| 3 V/5 V Operation | | | | | | DC to 1 MHz logic signal frequency |
| | | | 1.7 | 2.4 | mA | |
| 10 Mbps (BRWZ Version Only) | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1 (10)}$ | | | | | |
| 5 V/3 V Operation | | | 5.4 | 7.6 | mA | 5 MHz logic signal frequency |
| 3 V/5 V Operation | | | 3.1 | 4.5 | mA | 5 MHz logic signal frequency |
| $V_{DD2}$ Supply Current | $I_{DD2 (10)}$ | | | | | |
| 5 V/3 V Operation | | | 2.1 | 3.0 | mA | 5 MHz logic signal frequency |
| 3 V/5 V Operation | | | 3.8 | 5.3 | mA | 5 MHz logic signal frequency |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| ADuM1412, Total Supply Current, Four Channels[1] | | | | | | |
| DC to 2 Mbps | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1 (Q)}$ | | | | | |
| 5 V/3 V Operation | | | | | | DC to 1 MHz logic signal frequency |
| | | | 2.0 | 2.6 | mA | |
| 3 V/5 V Operation | | | | | | DC to 1 MHz logic signal frequency |
| | | | 1.0 | 1.8 | mA | |
| $V_{DD2}$ Supply Current | $I_{DD2 (Q)}$ | | | | | |
| 5 V/3 V Operation | | | | | | DC to 1 MHz logic signal frequency |
| | | | 1.0 | 1.8 | mA | |
| 3 V/5 V Operation | | | | | | DC to 1 MHz logic signal frequency |
| | | | 2.0 | 2.6 | mA | |
| 10 Mbps (BRWZ Version Only) | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1 (10)}$ | | | | | |
| 5 V/3 V Operation | | | 4.6 | 6.5 | mA | 5 MHz logic signal frequency |
| 3 V/5 V Operation | | | 2.6 | 3.8 | mA | 5 MHz logic signal frequency |
| $V_{DD2}$ Supply Current | $I_{DD2 (10)}$ | | | | | |
| 5 V/3 V Operation | | | 2.6 | 3.8 | mA | 5 MHz logic signal frequency |
| 3 V/5 V Operation | | | 4.6 | 6.5 | mA | 5 MHz logic signal frequency |
| All Models | | | | | | |
| Input Currents | $I_{IA}$, $I_{IB}$, $I_{IC}$, $I_{ID}$, $I_{CTRL1}$, $I_{CTRL2}$, $I_{DISABLE}$ | −10 | +0.01 | +10 | µA | 0 V ≤ $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$ ≤ $V_{DD1}$ or $V_{DD2}$, 0 V ≤ $V_{CTRL1}$, $V_{CTRL2}$ ≤ $V_{DD1}$ or $V_{DD2}$, 0 V ≤ $V_{DISABLE}$ ≤ $V_{DD1}$ |
| Logic High Input Threshold | $V_{IH}$ | | | | | |
| 5 V/3 V Operation | | 2.0 | | | V | |
| 3 V/5 V Operation | | 1.6 | | | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | | | |
| 5 V/3 V Operation | | | | 0.8 | V | |
| 3 V/5 V Operation | | | | 0.4 | V | |
| Logic High Output Voltages | | ($V_{DD1}$ or $V_{DD2}$) − 0.1 | ($V_{DD1}$ or $V_{DD2}$) | | V | $I_{Ox}$ = −20 µA, $V_{Ix}$ = $V_{IxH}$ |
| | $V_{OAH}$, $V_{OBH}$, $V_{OCH}$, $V_{ODH}$ | ($V_{DD1}$ or $V_{DD2}$) − 0.4 | ($V_{DD1}$ or $V_{DD2}$) − 0.2 | | V | $I_{Ox}$ = −4 mA, $V_{Ix}$ = $V_{IxH}$ |
| Logic Low Output Voltages | | | 0.0 | 0.1 | V | $I_{Ox}$ = 20 µA, $V_{Ix}$ = $V_{IxL}$ |
| | $V_{OAL}$, $V_{OBL}$, $V_{OCL}$, $V_{ODL}$ | | 0.04 | 0.1 | V | $I_{Ox}$ = 400 µA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}$ = 4 mA, $V_{Ix}$ = $V_{IxL}$ |
| SWITCHING SPECIFICATIONS | | | | | | |
| ADuM1410ARWZ/ADuM1411ARWZ/ ADuM1412ARWZ | | | | | | |
| Minimum Pulse Width[2] | PW | | | 1000 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Maximum Data Rate[3] | | 1 | | | Mbps | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay[4] | $t_{PHL}$, $t_{PLH}$ | 25 | 70 | 100 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4] | PWD | | | 40 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay Skew[5] | $t_{PSK}$ | | | 50 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching[6] | $t_{PSKCD/OD}$ | | | 50 | ns | $C_L$ = 15 pF, CMOS signal levels |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| ADuM1410BRWZ/ADuM1411BRWZ/ ADuM1412BRWZ | | | | | | |
| Minimum Pulse Width[2] | PW | | | 100 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Maximum Data Rate[3] | | 10 | | | Mbps | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay[4] | $t_{PHL}$, $t_{PLH}$ | 25 | 35 | 60 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4] | PWD | | | 5 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Change vs. Temperature | | | 5 | | ps/°C | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay Skew[5] | $t_{PSK}$ | | | 30 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching, Codirectional Channels[6] | $t_{PSKCD}$ | | | 5 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching, Opposing-Directional Channels[6] | $t_{PSKOD}$ | | | 6 | ns | $C_L$ = 15 pF, CMOS signal levels |
| All Models | | | | | | |
| Output Rise/Fall Time (10% to 90%) | $t_R/t_F$ | | | | | $C_L$ = 15 pF, CMOS signal levels |
| 5 V/3 V Operation | | | 2.5 | | ns | |
| 3 V/5 V Operation | | | 2.5 | | ns | |
| Common-Mode Transient Immunity at Logic High Output[7] | $\|CM_H\|$ | 25 | 35 | | kV/µs | $V_{Ix} = V_{DD1}$ or $V_{DD2}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output[7] | $\|CM_L\|$ | 25 | 35 | | kV/µs | $V_{Ix}$ = 0 V, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Refresh Rate | $f_r$ | | | | | |
| 5 V/3 V Operation | | | 1.2 | | Mbps | |
| 3 V/5 V Operation | | | 1.1 | | Mbps | |
| Input Enable Time[8] | $t_{ENABLE}$ | | 2.0 | | µs | $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$ = 0 V or $V_{DD1}$ |
| Input Disable Time[8] | $t_{DISABLE}$ | | 5.0 | | µs | $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$ = 0 V or $V_{DD1}$ |
| Input Dynamic Supply Current per Channel[9] | $I_{DDI (D)}$ | | | | | |
| 5 V Operation | | | 0.12 | | mA/ Mbps | |
| 3 V Operation | | | 0.07 | | mA/ Mbps | |
| Output Dynamic Supply Current per Channel[9] | $I_{DDO (D)}$ | | | | | |
| 5 V Operation | | | 0.04 | | mA/ Mbps | |
| 3 V Operation | | | 0.02 | | mA/ Mbps | |

[1] The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total $V_{DD1}$ and $V_{DD2}$ supply currents as a function of data rate for ADuM1410/ADuM1411/ADuM1412 channel configurations.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[4] $t_{PHL}$ propagation delay is measured from the 50% level of the falling edge of the $V_{Ix}$ signal to the 50% level of the falling edge of the $V_{Ox}$ signal. $t_{PLH}$ propagation delay is measured from the 50% level of the rising edge of the $V_{Ix}$ signal to the 50% level of the rising edge of the $V_{Ox}$ signal.

[5] $t_{PSK}$ is the magnitude of the worst-case difference in $t_{PHL}$ or $t_{PLH}$ that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

[7] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[8] Input enable time is the duration from when $V_{DISABLE}$ is set low until the output states are guaranteed to match the input states in the absence of any input data logic transitions. If an input data logic transition within a given channel does occur within this time interval, the output of that channel reaches the correct state within the much shorter duration as determined by the propagation delay specifications within this data sheet. Input disable time is the duration from when $V_{DISABLE}$ is set high until the output states are guaranteed to reach their programmed output levels, as determined by the $CTRL_2$ logic state (see Table 14).

[9] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

## PACKAGE CHARACTERISTICS

**Table 4.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| Resistance (Input to Output)[1] | $R_{I-O}$ | | $10^{12}$ | | Ω | |
| Capacitance (Input to Output)[1] | $C_{I-O}$ | | 2.2 | | pF | f = 1 MHz |
| Input Capacitance[2] | $C_I$ | | 4.0 | | pF | |
| IC Junction to Case Thermal Resistance | | | | | | |
| Side 1 | $\theta_{JCI}$ | | 33 | | °C/W | Thermocouple located at center of package underside |
| Side 2 | $\theta_{JCO}$ | | 28 | | °C/W | |

[1] The device is considered a 2-terminal device; Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

## REGULATORY INFORMATION

The ADuM1410/ADuM1411/ADuM1412 have been approved by the organizations listed in Table 5. See Table 10 and the Insulation Lifetime section for recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

**Table 5.**

| UL | CSA | CQC | VDE | TÜV |
|---|---|---|---|---|
| Recognized Under 1577 Component Recognition Program[1] | Approved under CSA Component Acceptance Notice 5A | Approved under CQC11-471543-2012 | Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2] | Approved according to IEC 60950-1:2005 and EN 60950-1:2006 |
| Single Protection, 3750 V rms Isolation Voltage | Basic insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage | Basic insulation per GB4943.1-2011, 600 V rms (848 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 m | Reinforced insulation, 560 V peak | 3000 V rms reinforced isolation at a 400 V rms working voltage, 3000 V rms basic isolation at a 600 V rms working voltage |
| | Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage | Reinforced insulation per GB4943.1-2011, 380 V rms (537 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 m | | |
| File E214100 | File 205078 | File CQC14001108689 | File 2471900-4880-0001 | Certificate B 10 03 56232 006 |

[1] In accordance with UL 1577, each ADuM1410/ADuM1411/ADuM1412 is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec (current leakage detection limit = 5 μA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM1410/ADuM1411/ADuM1412 is proof tested by applying an insulation test voltage ≥1050 V peak for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marked on the component designates DIN V VDE V 0884-10 approval.

## INSULATION AND SAFETY RELATED SPECIFICATIONS

**Table 6.**

| Parameter | Symbol | Value | Unit | Conditions |
|---|---|---|---|---|
| Rated Dielectric Insulation Voltage | | 3750 | V rms | 1-minute duration |
| Minimum External Tracking (Creepage) | L(I02) | 7.7[1] | mm min | Measured from input terminals to output terminals, shortest distance path along package body |
| Minimum External Air Gap (Clearance) | L(I01) | 7.7 | mm min | Measured from input terminals to output terminals, shortest distance through air |
| Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance) | L(PCB) | 8.1[2] | mm min | Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane |
| Minimum Internal Gap (Internal Clearance) | | 0.017 | mm min | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >400 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | II | | Material Group (DIN VDE 0110, 1/89, Table 1) |

[1] Clearance and creepage measured by VDE is >8 mm for SOIC wide packages.
[2] This value is for information only, to aid in PCB design. Package clearance is identical to creepage as specified in L(I02).

## DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation within the safety limit data only. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marked on packages denotes DIN V VDE V 0884-10 approval.

**Table 7.**

| Description | Conditions | Symbol | Characteristic | Unit |
|---|---|---|---|---|
| Installation Classification per DIN VDE 0110 | | | | |
| For Rated Mains Voltage ≤ 150 V rms | | | I to IV | |
| For Rated Mains Voltage ≤ 300 V rms | | | I to III | |
| For Rated Mains Voltage ≤ 400 V rms | | | I to II | |
| Climatic Classification | | | 40/105/21 | |
| Pollution Degree per DIN VDE 0110, Table 1 | | | 2 | |
| Maximum Working Insulation Voltage | | $V_{IORM}$ | 560 | V peak |
| Input-to-Output Test Voltage, Method B1 | $V_{IORM} \times 1.875 = V_{PR}$, 100% production test, $t_m = 1$ sec, partial discharge < 5 pC | $V_{PR}$ | 1050 | V peak |
| Input-to-Output Test Voltage, Method A | $V_{IORM} \times 1.6 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC | $V_{PR}$ | | |
| After Environmental Tests Subgroup 1 | | | 896 | V peak |
| After Input and/or Safety Test Subgroup 2 and Subgroup 3 | $V_{IORM} \times 1.2 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC | | 672 | V peak |
| Highest Allowable Overvoltage | Transient overvoltage, $t_{TR} = 10$ seconds | $V_{TR}$ | 4000 | V peak |
| Safety Limiting Values | Maximum value allowed in the event of a failure; see Figure 4 | | | |
| Case Temperature | | $T_S$ | 150 | °C |
| Side 1 Current | | $I_{S1}$ | 265 | mA |
| Side 2 Current | | $I_{S2}$ | 335 | mA |
| Insulation Resistance at $T_S$ | $V_{IO} = 500$ V | $R_S$ | $>10^9$ | Ω |

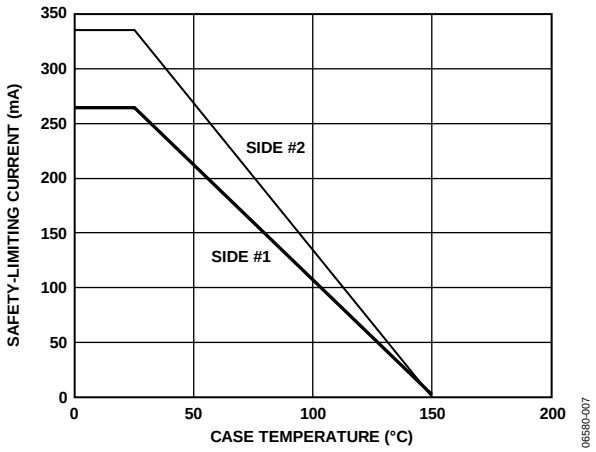



*Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10*

## RECOMMENDED OPERATING CONDITIONS

**Table 8.**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_A$ | −40 | +105 | °C |
| Supply Voltages[1] | $V_{DD1}$, $V_{DD2}$ | 2.7 | 5.5 | V |
| Input Signal Rise and Fall Times | | | 1.0 | ms |

[1] All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 9.**

| Parameter | Rating |
|---|---|
| Storage Temperature ($T_{ST}$) Range | −65°C to +150°C |
| Ambient Operating Temperature ($T_A$) Range | −40°C to +105°C |
| Supply Voltages ($V_{DD1}$, $V_{DD2}$)[1] | −0.5 V to +7.0 V |
| Input Voltages ($V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$, $V_{CTRL1}$, $V_{CTRL2}$, $V_{DISABLE}$)[1, 2] | −0.5 V to $V_{DDI}$ + 0.5 V |
| Output Voltages ($V_{OA}$, $V_{OB}$, $V_{OC}$, $V_{OD}$)[1, 2] | −0.5 V to $V_{DDO}$ + 0.5 V |
| Average Output Current per Pin[3] | |
| Side 1 ($I_{O1}$) | −18 mA to +18 mA |
| Side 2 ($I_{O2}$) | −22 mA to +22 mA |
| Common-Mode Transients[4] | −100 kV/µs to +100 kV/µs |

[1] All voltages are relative to their respective ground.
[2] $V_{DDI}$ and $V_{DDO}$ refer to the supply voltages on the input and output sides of a given channel, respectively. See the PC Board Layout section.
[3] See Figure 4 for maximum rated current values for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

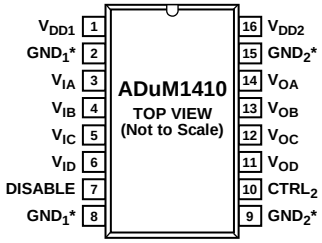
**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**Table 10. Maximum Continuous Working Voltage[1]**

| Parameter | Max | Unit | Constraint |
|---|---|---|---|
| AC Voltage, Bipolar Waveform | 565 | V peak | 50-year minimum lifetime |
| AC Voltage, Unipolar Waveform | | | |
| Basic Insulation | 1131 | V peak | Maximum approved working voltage per IEC 60950-1 |
| Reinforced Insulation | 560 | V peak | Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10 |
| DC Voltage | | | |
| Basic Insulation | 1131 | V peak | Maximum approved working voltage per IEC 60950-1 |
| Reinforced Insulation | 560 | V peak | Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10 |

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS




*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO $GND_1$ IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO $GND_2$ IS RECOMMENDED.

06580-004

*Figure 5. ADuM1410 Pin Configuration*

**Table 11. ADuM1410 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{DD1}$ | Supply Voltage for Isolator Side 1 (2.7 V to 5.5 V). |
| 2 | $GND_1$ | Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to $GND_1$ is recommended. |
| 3 | $V_{IA}$ | Logic Input A. |
| 4 | $V_{IB}$ | Logic Input B. |
| 5 | $V_{IC}$ | Logic Input C. |
| 6 | $V_{ID}$ | Logic Input D. |
| 7 | DISABLE | Input Disable. Disables the isolator inputs and halts the dc refresh circuits. Outputs take on the logic state determined by $CTRL_2$. |
| 8 | $GND_1$ | Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to $GND_1$ is recommended. |
| 9 | $GND_2$ | Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to $GND_2$ is recommended. |
| 10 | $CTRL_2$ | Default Output Control. Controls the logic state the outputs assume when the input power is off. $V_{OA}$, $V_{OB}$, $V_{OC}$, and $V_{OD}$ outputs are high when $CTRL_2$ is high or disconnected and $V_{DD1}$ is off. $V_{OA}$, $V_{OB}$, $V_{OC}$, and $V_{OD}$ outputs are low when $CTRL_2$ is low and $V_{DD1}$ is off. When $V_{DD1}$ power is on, this pin has no effect. |
| 11 | $V_{OD}$ | Logic Output D. |
| 12 | $V_{OC}$ | Logic Output C. |
| 13 | $V_{OB}$ | Logic Output B. |
| 14 | $V_{OA}$ | Logic Output A. |
| 15 | $GND_2$ | Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to $GND_2$ is recommended. |
| 16 | $V_{DD2}$ | Supply Voltage for Isolator Side 2 (2.7 V to 5.5 V). |

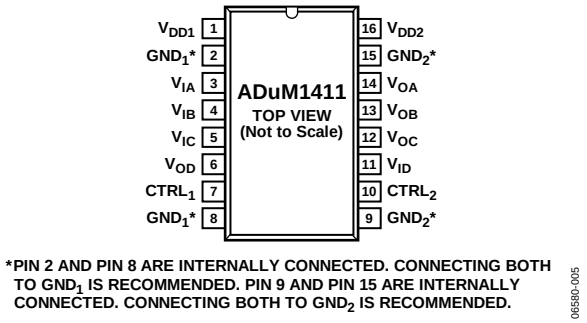



*Figure 6. ADuM1411 Pin Configuration*

**Table 12. ADuM1411 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{DD1}$ | Supply Voltage for Isolator Side 1 (2.7 V to 5.5 V). |
| 2 | $GND_1$ | Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to $GND_1$ is recommended. |
| 3 | $V_{IA}$ | Logic Input A. |
| 4 | $V_{IB}$ | Logic Input B. |
| 5 | $V_{IC}$ | Logic Input C. |
| 6 | $V_{OD}$ | Logic Output D. |
| 7 | $CTRL_1$ | Default Output Control. Controls the logic state the outputs assume when the input power is off. $V_{OD}$ output is high when $CTRL_1$ is high or disconnected and $V_{DD2}$ is off. $V_{OD}$ output is low when $CTRL_1$ is low and $V_{DD2}$ is off. When $V_{DD2}$ power is on, this pin has no effect. |
| 8 | $GND_1$ | Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to $GND_1$ is recommended. |
| 9 | $GND_2$ | Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to $GND_2$ is recommended. |
| 10 | $CTRL_2$ | Default Output Control. Controls the logic state the outputs assume when the input power is off. $V_{OA}$, $V_{OB}$, and $V_{OC}$ outputs are high when $CTRL_2$ is high or disconnected and $V_{DD1}$ is off. $V_{OA}$, $V_{OB}$, and $V_{OC}$ outputs are low when $CTRL_2$ is low and $V_{DD1}$ is off. When $V_{DD1}$ power is on, this pin has no effect. |
| 11 | $V_{ID}$ | Logic Input D. |
| 12 | $V_{OC}$ | Logic Output C. |
| 13 | $V_{OB}$ | Logic Output B. |
| 14 | $V_{OA}$ | Logic Output A. |
| 15 | $GND_2$ | Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to $GND_2$ is recommended. |
| 16 | $V_{DD2}$ | Supply Voltage for Isolator Side 2 (2.7 V to 5.5 V). |

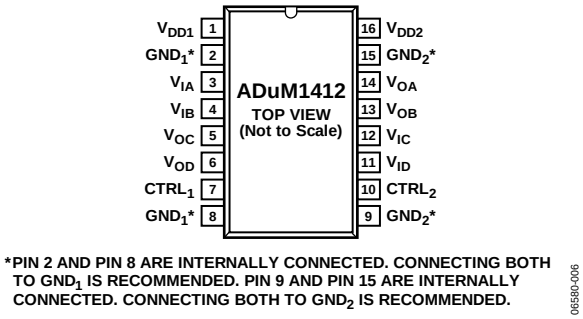



*Figure 7. ADuM1412 Pin Configuration*

**Table 13. ADuM1412 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{DD1}$ | Supply Voltage for Isolator Side 1 (2.7 V to 5.5 V). |
| 2 | $GND_1$ | Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to $GND_1$ is recommended. |
| 3 | $V_{IA}$ | Logic Input A. |
| 4 | $V_{IB}$ | Logic Input B. |
| 5 | $V_{OC}$ | Logic Output C. |
| 6 | $V_{OD}$ | Logic Output D. |
| 7 | $CTRL_1$ | Default Output Control. Controls the logic state the outputs assume when the input power is off. $V_{OC}$ and $V_{OD}$ outputs are high when $CTRL_1$ is high or disconnected and $V_{DD2}$ is off. $V_{OC}$ and $V_{OD}$ outputs are low when $CTRL_1$ is low and $V_{DD2}$ is off. When $V_{DD2}$ power is on, this pin has no effect. |
| 8 | $GND_1$ | Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to $GND_1$ is recommended. |
| 9 | $GND_2$ | Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to $GND_2$ is recommended. |
| 10 | $CTRL_2$ | Default Output Control. Controls the logic state the outputs assume when the input power is off. $V_{OA}$ and $V_{OB}$ outputs are high when $CTRL_2$ is high or disconnected and $V_{DD1}$ is off. $V_{OA}$ and $V_{OB}$ outputs are low when $CTRL_2$ is low and $V_{DD1}$ is off. When $V_{DD1}$ power is on, this pin has no effect. |
| 11 | $V_{ID}$ | Logic Input D. |
| 12 | $V_{IC}$ | Logic Input C. |
| 13 | $V_{OB}$ | Logic Output B. |
| 14 | $V_{OA}$ | Logic Output A. |
| 15 | $GND_2$ | Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to $GND_2$ is recommended. |
| 16 | $V_{DD2}$ | Supply Voltage for Isolator Side 2 (2.7 V to 5.5 V). |

**Table 14. Truth Table (Positive Logic)**

| $V_{Ix}$ Input[1] | $CTRL_X$ Input[2] | $V_{DISABLE}$ State[3] | $V_{DDI}$ State[4] | $V_{DDO}$ State[5] | $V_{Ox}$ Output[1] | Description |
|---|---|---|---|---|---|---|
| H | X | L or NC | Powered | Powered | H | Normal operation, data is high. |
| L | X | L or NC | Powered | Powered | L | Normal operation, data is low. |
| X | H or NC | H | X | Powered | H | Inputs disabled. Outputs are in the default state as determined by $CTRL_X$. |
| X | L | H | X | Powered | L | Inputs disabled. Outputs are in the default state as determined by $CTRL_X$. |
| X | H or NC | X | Unpowered | Powered | H | Input unpowered. Outputs are in the default state as determined by $CTRL_X$. Outputs return to input state within 1 µs of $V_{DDI}$ power restoration. See the pin function descriptions (Table 11, Table 12, and Table 13) for more details. |
| X | L | X | Unpowered | Powered | L | Input unpowered. Outputs are in the default state as determined by $CTRL_X$. Outputs return to input state within 1 µs of $V_{DDI}$ power restoration. See the pin function descriptions (Table 11, Table 12, and Table 13) for more details. |
| X | X | X | Powered | Unpowered | Z | Output unpowered. Output pins are in high impedance state. Outputs return to input state within 1 µs of $V_{DDO}$ power restoration. See the pin function descriptions (Table 11, Table 12, and Table 13) for more details. |

[1] $V_{Ix}$ and $V_{Ox}$ refer to the input and output signals of a given channel (A, B, C, or D).
[2] $CTRL_X$ refers to the default output control signal on the input side of a given channel (A, B, C, or D).
[3] Available only on the ADuM1410.
[4] $V_{DDI}$ refers to the power supply on the input side of a given channel (A, B, C, or D).
[5] $V_{DDO}$ refers to the power supply on the output side of a given channel (A, B, C, or D).

# TYPICAL PERFORMANCE CHARACTERISTICS

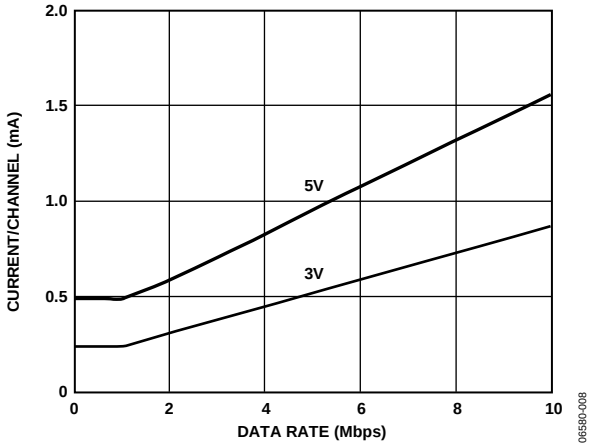



Figure 8. Typical Supply Current per Input Channel vs. Data Rate for 5 V and 3 V Operation

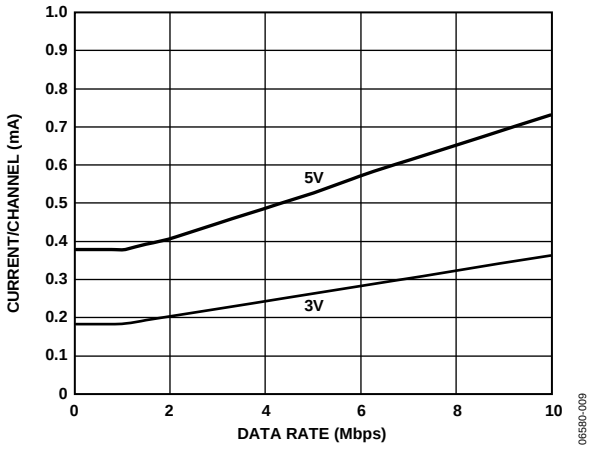



Figure 9. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

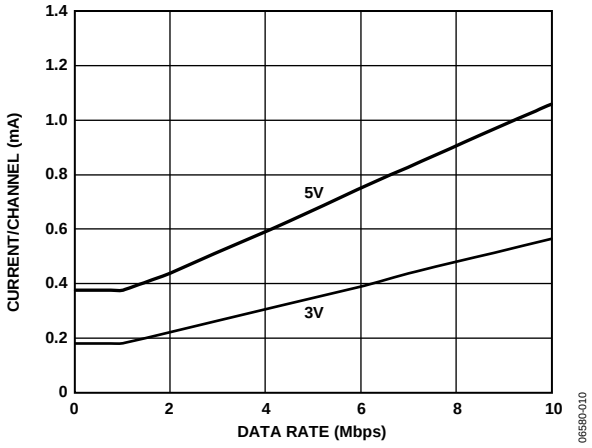



Figure 10. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

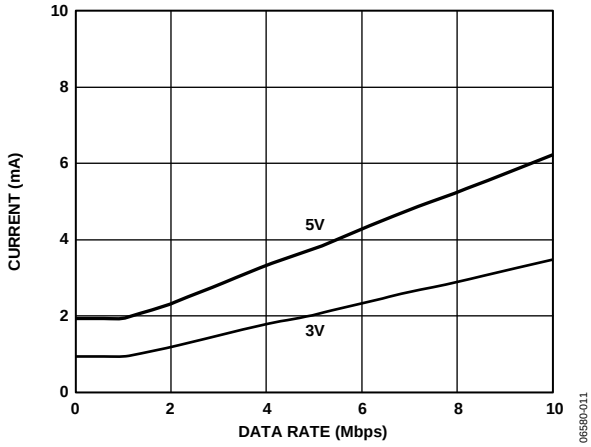



Figure 11. Typical ADuM1410 $V_{DD1}$ Supply Current vs. Data Rate for 5 V and 3 V Operation

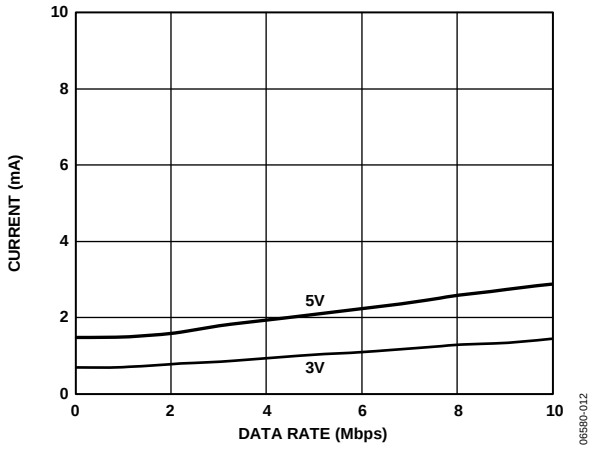



Figure 12. Typical ADuM1410 $V_{DD2}$ Supply Current vs. Data Rate for 5 V and 3 V Operation

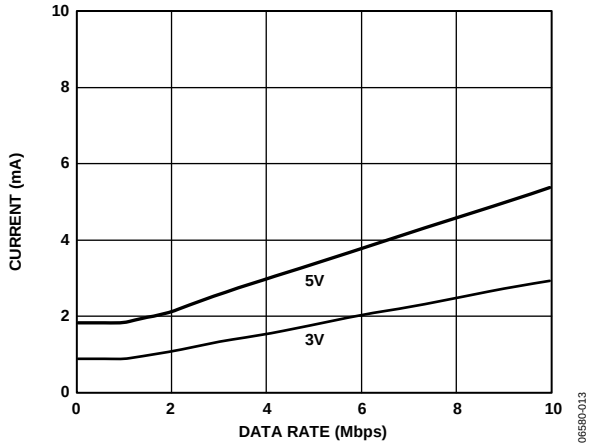



Figure 13. Typical ADuM1411 $V_{DD1}$ Supply Current vs. Data Rate for 5 V and 3 V Operation

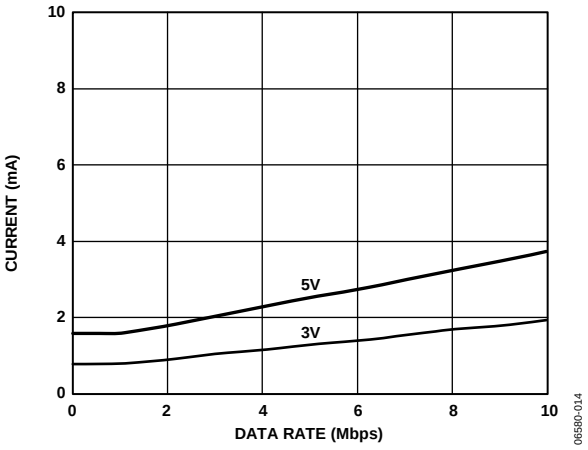



*Figure 14. Typical ADuM1411 $V_{DD2}$ Supply Current vs. Data Rate for 5 V and 3 V Operation*

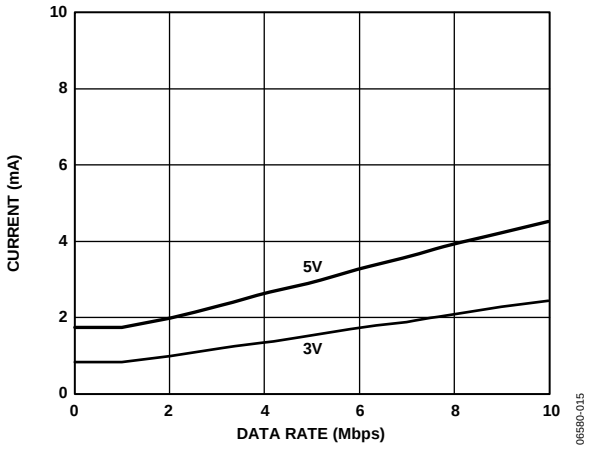



*Figure 15. Typical ADuM1412 $V_{DD1}$ or $V_{DD2}$ Supply Current vs. Data Rate for 5 V and 3 V Operation*

# APPLICATIONS INFORMATION

## PC BOARD LAYOUT

The ADuM1410/ADuM1411/ADuM1412 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 16). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for $V_{DD1}$, and between Pin 15 and Pin 16 for $V_{DD2}$. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered unless both ground pins on each package are connected together close to the package.

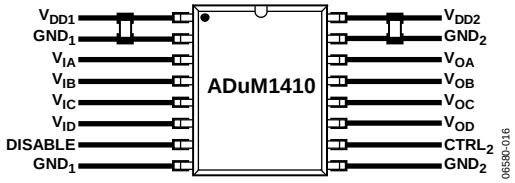



*Figure 16. Recommended Printed Circuit Board Layout*

In applications involving high common-mode transients, it is important to minimize board coupling across the isolation barrier. Furthermore, users should design the board layout so that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage. See the AN-1109 Application Note for board layout guidelines.

## PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The input-to-output propagation delay time for a high-to-low transition may differ from the propagation delay time of a low-to-high transition.

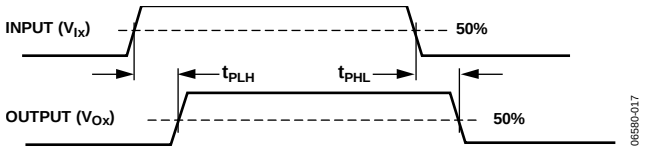



*Figure 17. Propagation Delay Parameters*

Pulse width distortion is the maximum difference between these two propagation delay values and an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM1410/ADuM1411/ADuM1412 component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM1410/ADuM1411/ADuM1412 components operating under the same conditions.

## DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder using the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than approximately 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 14) by the watchdog timer circuit.

The magnetic field immunity of the ADuM1410/ADuM1411/ADuM1412 is determined by the changing magnetic field, which induces a voltage in the transformer's receiving coil large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM1410/ADuM1411/ADuM1412 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2; n = 1, 2, \ldots, N$$

where:
$\beta$ is magnetic flux density (gauss).
$r_n$ is the radius of the n$^{th}$ turn in the receiving coil (cm).
$N$ is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM1410/ADuM1411/ADuM1412 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field at a given frequency can be calculated. The result is shown in Figure 18.

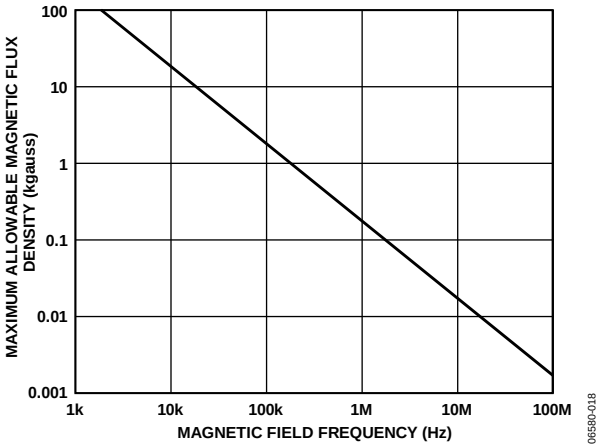



*Figure 18. Maximum Allowable External Magnetic Flux Density*

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurred during a transmitted pulse (and had the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM1410/ADuM1411/ADuM1412 transformers. Figure 19 shows these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM1410/ADuM1411/ADuM1412 is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted previously, a 0.5 kA current would have to be placed 5 mm away from the ADuM1410/ADuM1411/ADuM1412 to affect the operation of the component.

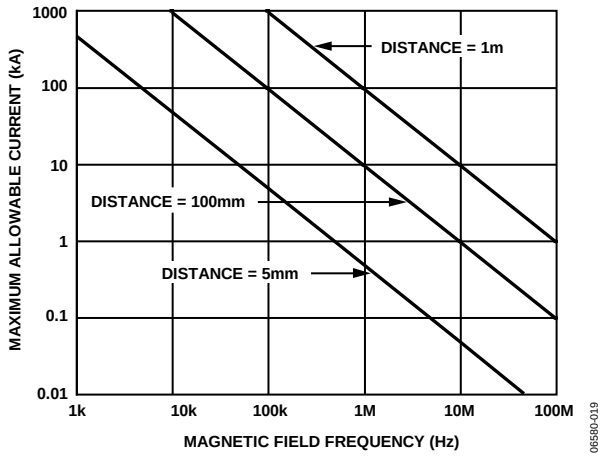



*Figure 19. Maximum Allowable Current for Various Current-to-ADuM1410/ADuM1411/ADuM1412 Spacings*

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces can induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

## POWER CONSUMPTION

The supply current at a given channel of the ADuM1410/ADuM1411/ADuM1412 isolators is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \le 0.5\,f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5\,f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \le 0.5\,f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f > 0.5\,f_r$$

where:
$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
$C_L$ is the output load capacitance (pF).
$V_{DDO}$ is the output supply voltage (V).
$f$ is the input logic signal frequency (MHz); it is half the input data rate, expressed in units of Mbps.
$f_r$ is the input stage refresh rate (Mbps).
$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total $V_{DD1}$ and $V_{DD2}$ supply current, the supply currents for each input and output channel corresponding to $V_{DD1}$ and $V_{DD2}$ are calculated and totaled. Figure 8 and Figure 9 show per-channel supply currents as a function of data rate for an unloaded output condition. Figure 10 shows the per-channel supply current as a function of data rate for a 15 pF output condition. Figure 11 through Figure 15 show the total $V_{DD1}$ and $V_{DD2}$ supply current as a function of data rate for ADuM1410/ADuM1411/ADuM1412 channel configurations.

## INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM1410/ADuM1411/ADuM1412.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 10 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM1410/ADuM1411/ADuM1412 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 20, Figure 21, and Figure 22 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 10 can be applied while maintaining the 50-year minimum lifetime provided the voltage conforms to either the unipolar ac or dc voltage case. Any cross-insulation voltage waveform that does not conform to Figure 21 or Figure 22 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 10.

Note that the voltage presented in Figure 21 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

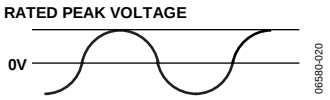



*Figure 20. Bipolar AC Waveform*

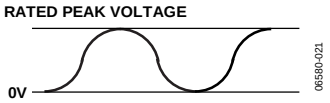



*Figure 21. Unipolar AC Waveform*

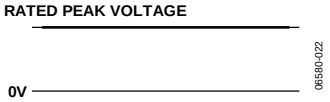



*Figure 22. DC Waveform*