

## FEATURES

Enhanced system-level ESD performance per IEC 61000-4-x

High temperature operation: 125°C

Default low output

Narrow body, RoHS-compliant, 8-lead SOIC

Low power operation

5 V operation

1.7 mA per channel maximum at 0 Mbps to 2 Mbps

3.8 mA per channel maximum at 10 Mbps

7.5 mA per channel maximum at 25 Mbps

3.3 V operation

1.5 mA per channel maximum at 0 Mbps to 2 Mbps

2.5 mA per channel maximum at 10 Mbps

4.7 mA per channel maximum at 25 Mbps

3.3 V/5 V level translation

High data rate: dc to 25 Mbps (NRZ)

Precise timing characteristics

3 ns maximum pulse width distortion at 5 V operation

3 ns maximum channel-to-channel matching

High common-mode transient immunity: >25 kV/μs

**Safety and regulatory approvals**

UL recognition: 2500 V rms for 1 minute per UL 1577

CSA Component Acceptance Notice #5A

VDE certificate of conformity

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12

$V_{IORM} = 560$  V peak

Qualified for automotive applications

## APPLICATIONS

Size-critical multichannel isolation

SPI interface/data converter isolation

RS-232/RS-422/RS-485 transceiver isolation

Digital field bus isolation

Gate drive interfaces

Hybrid electric vehicles, battery monitor, and motor drive

## GENERAL DESCRIPTION

The ADuM3210/ADuM3211<sup>1</sup> are dual-channel digital isolators based on Analog Devices, Inc., *iCoupler*<sup>®</sup> technology. Combining high speed CMOS and monolithic transformer technology, this isolation component provides outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *iCoupler* devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *iCoupler* digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these *iCoupler* products. Furthermore, *iCoupler* devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM3210/ADuM3211 isolators provide two independent isolation channels in two channel configurations with data rates up to 25 Mbps (see the Ordering Guide). They operate with 3.3 V or 5 V supply voltages on either side, providing compatibility with lower voltage systems, as well as enabling voltage translation functionality across the isolation barrier. The ADuM3210/ADuM3211 isolators have a default output low characteristic in comparison to the ADuM3200/ADuM3201 models, which have a default output high characteristic. The ADuM3210W and ADuM3211W models are automotive grade versions qualified for 125°C operation.

In comparison to the ADuM1200/ADuM1201 isolator, the ADuM3210/ADuM3211 isolators contain various circuit and layout changes providing increased capability relative to system-level IEC 61000-4-x testing (ESD, burst, and surge). The precise capability in these tests for either the ADuM1200/ADuM1201 or ADuM3210/ADuM3211 products is strongly determined by the design and layout of the user's board or module. For more information, see the AN-793 *Application Note, ESD/Latch-Up Considerations with iCoupler Isolation Products*.

## FUNCTIONAL BLOCK DIAGRAMS

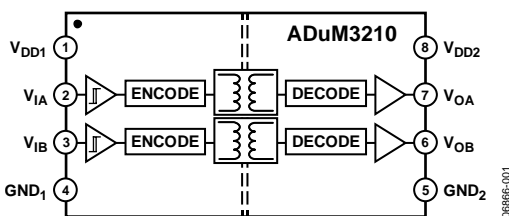


Figure 1. ADuM3210

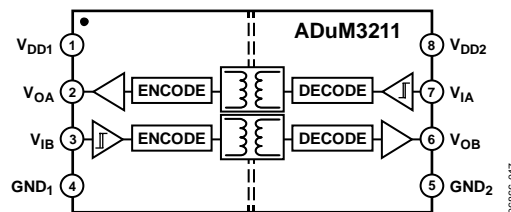


Figure 2. ADuM3211

<sup>1</sup> Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,239.

Rev. K

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### 3/14—Rev. G to Rev. H

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Changed Electrical Characteristics—Mixed 5 V/3 V, 105°C Section to Electrical Characteristics—Mixed 5 V/3.3 V, 105°C Section; Changes to Table Summary Statement and Table 8.....	6
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**11/12—Rev. F to Rev. G**

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**7/09—Rev. A to Rev. B**

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**9/08—Revision A: Initial Version**

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—5 V, 105°C OPERATION

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 5\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

Table 1.

Parameter	Symbol	A Grade			B Grade			Unit	Test Conditions/ Comments
		Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{PLH}$	20		50	20		50	ns	50% input to 50% output
Pulse Width Distortion	PWD			5			3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			6			5		ps/°C	
Pulse Width	PW								Within PWD limit
ADuM3210		1000			22			ns	
ADuM3211		1000			33			ns	
Propagation Delay Skew	$t_{PSK}$			20			18	ns	Between any two units
Channel Matching									
Codirectional	$t_{PSKCD}$			5			3	ns	
Opposing Directional	$t_{PSKOD}$			20			18	ns	
Output Rise/Fall Time	$t_R/t_F$		2.5			2.5		ns	10% to 90%

Table 2.

Parameter	Symbol	1 Mbps—A Grade, B Grade			10 Mbps—B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT								
ADuM3210	$I_{DD1}$		1.3	1.7		3.5	4.8	mA
	$I_{DD2}$		1.0	1.6		2.0	2.8	mA
ADuM3211	$I_{DD1}$		1.1	1.5		3.0	4.0	mA
	$I_{DD2}$		1.3	1.8		3.1	4.1	mA

Table 3. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	$V_{IH}$	$0.7 V_{DDx}$			V	
Logic Low Input Threshold	$V_{IL}$				V	
Logic High Output Voltages	$V_{OH}$	$V_{DDx} - 0.1$	5.0	$0.3 V_{DDx}$	V	$I_{Ox} = -20\text{ }\mu\text{A}$ , $V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.5$	4.8		V	$I_{Ox} = -3.2\text{ mA}$ , $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	$V_{OL}$	0.0			V	$I_{Ox} = 20\text{ }\mu\text{A}$ , $V_{Ix} = V_{IxL}$
		0.2			V	$I_{Ox} = 3.2\text{ mA}$ , $V_{Ix} = V_{IxL}$
Input Current per Channel	$I_i$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$	0.4			mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$	0.4			mA	
Dynamic Input Supply Current	$I_{DDI(D)}$	0.19			mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$	0.05			mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity <sup>1</sup>	$ CM $	25	35		kV/ $\mu\text{s}$	$V_{Ix} = V_{DDx}$ , $V_{CM} = 1000\text{ V}$ , transient magnitude = 800 V
Refresh Rate	$f_r$	1.2			Mbps	

<sup>1</sup>  $|CM|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

**ELECTRICAL CHARACTERISTICS—3.3 V, 105°C OPERATION**

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 3.3\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

**Table 4.**

Parameter	Symbol	A Grade			B Grade			Unit	Test Conditions/ Comments
		Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{PLH}$	20		60	20		60	ns	50% input to 50% output
Pulse Width Distortion	PWD								
ADuM3210				5			3	ns	$ t_{PLH} - t_{PHL} $
ADuM3211				6			4	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			6			5		ps/°C	
Pulse Width	PW								Within PWD limit
ADuM3210		1000			22			ns	
ADuM3211		1000			33			ns	
Propagation Delay Skew	$t_{PSK}$			29			22	ns	Between any two units
Channel Matching									
Codirectional	$t_{PSKCD}$			5			3	ns	
Opposing Directional	$t_{PSKOD}$			29			20	ns	
Output Rise/Fall Time	$t_R/t_F$		3.0			3.0		ns	10% to 90%

**Table 5.**

Parameter	Symbol	1 Mbps—A Grade, B Grade			10 Mbps—B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT								
ADuM3210	$I_{DD1}$		0.8	1.3		2.1	3.2	mA
	$I_{DD2}$		0.7	1.0		1.3	1.9	mA
ADuM3211	$I_{DD1}$		0.7	1.3		1.8	2.6	mA
	$I_{DD2}$		0.8	1.6		1.9	2.5	mA

**Table 6. For All Models**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	$V_{IH}$	$0.7 V_{DDx}$			V	
Logic Low Input Threshold	$V_{IL}$				$0.3 V_{DDx}$	
Logic High Output Voltages	$V_{OH}$	$V_{DDx} - 0.1$	3.0		V	$I_{Ox} = -20\ \mu\text{A}, V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.5$	2.8		V	$I_{Ox} = -3.2\ \text{mA}, V_{Ix} = V_{IxH}$
Logic Low Output Voltages	$V_{OL}$		0.0	0.1	V	$I_{Ox} = 20\ \mu\text{A}, V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{Ox} = 3.2\ \text{mA}, V_{Ix} = V_{IxL}$
Input Current per Channel	$I_i$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity <sup>1</sup>	$ CM $	25	35		kV/ $\mu\text{s}$	$V_{Ix} = V_{DDx}, V_{CM} = 1000\text{ V}$ , transient magnitude = 800 V
Refresh Rate	$f_r$		1.1		Mbps	

<sup>1</sup>  $|CM|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

**ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V, 105°C OPERATION**

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

Table 7.

Parameter	Symbol	A Grade			B Grade			Unit	Test Conditions/ Comments
		Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{PLH}$	15		55	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD			5			3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			6			5		ps/°C	
Pulse Width	PW								Within PWD limit
ADuM3210		1000			22			ns	
ADuM3211		1000			33			ns	
Propagation Delay Skew	$t_{PSK}$			29			22	ns	Between any two units
Channel Matching									
Codirectional	$t_{PSKCD}$			5			3	ns	
Opposing Directional	$t_{PSKOD}$			29			20	ns	
Output Rise/Fall Time	$t_R/t_F$		3.0			3.0		ns	10% to 90%

Table 8.

Parameter	Symbol	1 Mbps—A Grade, B Grade			10 Mbps—B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT								
ADuM3210	$I_{DD1}$		1.3	1.7		3.5	4.8	mA
	$I_{DD2}$		0.7	1.0		1.3	1.9	mA
ADuM3211	$I_{DD1}$		1.1	1.5		2.9	4.0	mA
	$I_{DD2}$		0.8	1.6		1.9	2.5	mA

Table 9. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	$V_{IH}$	$0.7 V_{DDx}$			V	
Logic Low Input Threshold	$V_{IL}$				V	
Logic High Output Voltages	$V_{OH}$	$V_{DDx} - 0.1$	$V_{DDx}$	$0.3 V_{DDx}$	V	$I_{Ox} = -20\text{ }\mu\text{A}$ , $V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.5$	$V_{DDx} - 0.2$		V	$I_{Ox} = -3.2\text{ mA}$ , $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	$V_{OL}$	0.0			V	$I_{Ox} = 20\text{ }\mu\text{A}$ , $V_{Ix} = V_{IxL}$
		0.2			V	$I_{Ox} = 3.2\text{ mA}$ , $V_{Ix} = V_{IxL}$
		0.4			V	
Input Current per Channel	$I_i$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$	0.4			mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$	0.3			mA	
Dynamic Input Supply Current	$I_{DDI(D)}$	0.19			mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$	0.03			mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity <sup>1</sup>	$ CM $	25	35		kV/ $\mu\text{s}$	$V_{Ix} = V_{DDx}$ , $V_{CM} = 1000\text{ V}$ , transient magnitude = 800 V
Refresh Rate	$f_r$	1.2			Mbps	

<sup>1</sup>  $|CM|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

**ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V, 105°C OPERATION**

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 3.3\text{ V}$ ,  $V_{DD2} = 5.0\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

**Table 10.**

Parameter	Symbol	A Grade			B Grade			Unit	Test Conditions/ Comments
		Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{PLH}$	15		55	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD								
ADuM3210				5			3	ns	$ t_{PLH} - t_{PHL} $
ADuM3211				6			4	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			6			5		ps/°C	
Pulse Width	PW								Within PWD limit
ADuM3210		1000			22			ns	
ADuM3211		1000			33			ns	
Propagation Delay Skew	$t_{PSK}$			29			20	ns	Between any two units
Channel Matching									
Codirectional	$t_{PSKCD}$			15			3	ns	
Opposing Directional	$t_{PSKOD}$			29			22	ns	
Output Rise/Fall Time	$t_R/t_F$		2.5			2.5		ns	10% to 90%

**Table 11.**

Parameter	Symbol	1 Mbps—A Grade, B Grade			10 Mbps—B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT								
ADuM3210	$I_{DD1}$		0.8	1.3		2.1	3.2	mA
	$I_{DD2}$		1.0	1.6		2.0	2.8	mA
ADuM3211	$I_{DD1}$		0.7	1.3		1.8	2.6	mA
	$I_{DD2}$		1.3	1.8		3.1	4.1	mA

**Table 12. For All Models**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	$V_{IH}$	0.7 $V_{DDx}$			V	
Logic Low Input Threshold	$V_{IL}$				0.3 $V_{DDx}$	
Logic High Output Voltages	$V_{OH}$	$V_{DDx} - 0.1$	$V_{DDx}$		V	$I_{Ox} = -20\ \mu\text{A}$ , $V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.5$	$V_{DDx} - 0.2$		V	$I_{Ox} = -3.2\ \text{mA}$ , $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	$V_{OL}$	0.0		0.1	V	$I_{Ox} = 20\ \mu\text{A}$ , $V_{Ix} = V_{IxL}$
		0.2		0.4	V	$I_{Ox} = 3.2\ \text{mA}$ , $V_{Ix} = V_{IxL}$
Input Current per Channel	$I_i$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DD1(Q)}$		0.4	0.8	mA	
Quiescent Output Supply Current	$I_{DD0(Q)}$		0.5	0.8	mA	
Dynamic Input Supply Current	$I_{DD1(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DD0(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity <sup>1</sup>	$ CM $	25	35		kV/ $\mu\text{s}$	$V_{Ix} = V_{DDx}$ , $V_{CM} = 1000\text{ V}$ , transient magnitude = 800 V
Refresh Rate	$f_r$		1.1		Mbps	

<sup>1</sup>  $|CM|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

**ELECTRICAL CHARACTERISTICS—5 V, 125°C OPERATION**

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 5\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

**Table 13.**

Parameter	Symbol	WA Grade			WB Grade, T Grade			WC Grade			Unit	Test Conditions/ Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{PLH}$	20		50	20		50	20		50	ns	50% input to 50% output
Pulse Width Distortion	PWD			5			3			3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			6			5			5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	$t_{PSK}$			20			18			18	ns	Between any two units
Channel Matching												
Codirectional	$t_{PSKCD}$			5			3			3	ns	
Opposing Directional	$t_{PSKOD}$			20			18			18	ns	
Output Rise/Fall Time	$t_r/t_f$		2.5			2.5			2.5		ns	10% to 90%

**Table 14.**

Parameter	Symbol	1 Mbps—WA Grade, WB Grade, WC Grade, T Grade			10 Mbps—WB Grade, WC Grade			10 Mbps—T Grade			25 Mbps—WC Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT														
ADuM3210	$I_{DD1}$	1.3	1.7		3.5	4.8		3.5	4.8		7.6	9.9		mA
	$I_{DD2}$	1.0	1.6		2.0	2.8		2.0	2.8		3.8	5.1		mA
ADuM3211	$I_{DD1}$	1.1	1.5		3.0	4.0		3.0	4.0		6.4	8.7		mA
	$I_{DD2}$	1.3	1.8		3.1	4.1		3.1	4.1		6.1	8.0		mA

**Table 15. For All Models**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	$V_{IH}$	$0.7 V_{DDx}$			V	
Logic Low Input Threshold	$V_{IL}$				V	
Logic High Output Voltages	$V_{OH}$	$V_{DDx} - 0.1$	5.0		V	$I_{Ox} = -20\ \mu\text{A}, V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.5$	4.8		V	$I_{Ox} = -3.2\ \text{mA}, V_{Ix} = V_{IxH}$
Logic Low Output Voltages	$V_{OL}$	0.0			V	$I_{Ox} = 20\ \mu\text{A}, V_{Ix} = V_{IxL}$
		0.2			V	$I_{Ox} = 3.2\ \text{mA}, V_{Ix} = V_{IxL}$
Input Current per Channel	$I_i$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$	0.4			mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$	0.4			mA	
Dynamic Input Supply Current	$I_{DDI(D)}$	0.19			mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$	0.05			mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity <sup>1</sup>	$ CM $	25	35		kV/ $\mu\text{s}$	$V_{Ix} = V_{DDx}, V_{CM} = 1000\text{ V}$ , transient magnitude = 800 V
Refresh Rate	$f_r$	1.2			Mbps	

<sup>1</sup>  $|CM|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.



**ELECTRICAL CHARACTERISTICS—3.3 V, 125°C OPERATION**

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 3.3\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

Table 16.

Parameter	Symbol	WA Grade			WB Grade, T Grade			WC Grade			Unit	Test Conditions/ Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{PLH}$	20		60	20		60	20		60	ns	50% input to 50% output
Pulse Width Distortion	PWD			6			4			4	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			6			5			5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	$t_{PSK}$			29			22			22	ns	Between any two units
Channel Matching												
Codirectional	$t_{PSKCD}$			5			3			3	ns	
Opposing Directional	$t_{PSKOD}$			29			20			20	ns	
Output Rise/Fall Time	$t_r/t_f$		3.0			3.0			3.0		ns	10% to 90%

Table 17.

Parameter	Symbol	1 Mbps—WA Grade, WB Grade, WC Grade, T Grade			10 Mbps—WB Grade, WC Grade			10 Mbps—T Grade			25 Mbps—WC Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT														
ADuM3210	$I_{DD1}$	0.8	1.3		2.1	3.2		2.1	3.2		4.6	6.1		mA
	$I_{DD2}$	0.7	1.0		1.3	1.9		1.3	1.9		2.4	3.4		mA
ADuM3211	$I_{DD1}$	0.7	1.3		1.8	2.6		1.8	2.6		3.8	5.4		mA
	$I_{DD2}$	0.8	1.6		1.9	2.5		1.9	2.5		3.7	5.0		mA

Table 18. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	$V_{IH}$	$0.7 V_{DDx}$			V	
Logic Low Input Threshold	$V_{IL}$				$0.3 V_{DDx}$	
Logic High Output Voltages	$V_{OH}$	$V_{DDx} - 0.1$	3.0		V	$I_{Ox} = -20\ \mu\text{A}, V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.5$	2.8		V	
Logic Low Output Voltages	$V_{OL}$	0.0		0.1	V	$I_{Ox} = 20\ \mu\text{A}, V_{Ix} = V_{IxL}$
		0.2		0.4	V	
Input Current per Channel	$I_i$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity <sup>1</sup>	$ CM $	25	35		kV/ $\mu\text{s}$	$V_{Ix} = V_{DDx}, V_{CM} = 1000\text{ V}$ , transient magnitude = 800 V
Refresh Rate	$f_r$		1.1		Mbps	

<sup>1</sup>  $|CM|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

**ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V, 125°C OPERATION**

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

**Table 19.**

Parameter	Symbol	WA Grade			WB Grade, T Grade			WC Grade			Unit	Test Conditions/ Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{PLH}$	15		55	15		55	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD			5			3			3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			6			5			5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	$t_{PSK}$			29			22			22	ns	Between any two units
Channel Matching												
Codirectional	$t_{PSKCD}$			5			3			3	ns	
Opposing Directional	$t_{PSKOD}$			29			20			20	ns	
Output Rise/Fall Time	$t_r/t_f$		3.0			3.0			3.0		ns	10% to 90%

**Table 20.**

Parameter	Symbol	1 Mbps—WA Grade, WB Grade, WC Grade, T Grade			10 Mbps—WB Grade, WC Grade			10 Mbps—T Grade			25 Mbps—WC Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT														
ADuM3210	$I_{DD1}$	1.3	1.7		3.5	4.8		3.5	4.8		7.6	9.9		mA
	$I_{DD2}$	0.7	1.0		1.3	1.9		1.3	1.9		2.4	3.4		mA
ADuM3211	$I_{DD1}$	1.1	1.5		2.9	4.0		2.9	4.0		6.4	8.7		mA
	$I_{DD2}$	0.8	1.6		1.9	2.5		1.9	2.5		3.7	5.0		mA

**Table 21. For All Models**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments	
DC SPECIFICATIONS							
Logic High Input Threshold	$V_{IH}$	$0.7 V_{DDx}$			V		
Logic Low Input Threshold	$V_{IL}$				$0.3 V_{DDx}$		
Logic High Output Voltages	$V_{OH}$	$V_{DDx} - 0.1$	$V_{DDx}$		V	$I_{Ox} = -20\ \mu\text{A}$ , $V_{Ix} = V_{IxH}$	
		$V_{DDx} - 0.5$	$V_{DDx} - 0.2$		V	$I_{Ox} = -3.2\ \text{mA}$ , $V_{Ix} = V_{IxH}$	
Logic Low Output Voltages	$V_{OL}$	0.0			0.1	V	$I_{Ox} = 20\ \mu\text{A}$ , $V_{Ix} = V_{IxL}$
		0.2			0.4	V	$I_{Ox} = 3.2\ \text{mA}$ , $V_{Ix} = V_{IxL}$
Input Current per Channel	$I_i$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$	
Supply Current per Channel							
Quiescent Input Supply Current	$I_{DD1(Q)}$	0.4			0.8	mA	
Quiescent Output Supply Current	$I_{DD0(Q)}$	0.3			0.5	mA	
Dynamic Input Supply Current	$I_{DD1(D)}$	0.19				mA/Mbps	
Dynamic Output Supply Current	$I_{DD0(D)}$	0.03				mA/Mbps	
AC SPECIFICATIONS							
Common-Mode Transient Immunity <sup>1</sup>	$ CM $	25	35		kV/ $\mu\text{s}$	$V_{Ix} = V_{DDx}$ , $V_{CM} = 1000\text{ V}$ , transient magnitude = 800 V	
Refresh Rate	$f_r$	1.2			Mbps		

<sup>1</sup>  $|CM|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

**ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V, 125°C OPERATION**

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 3.3\text{ V}$ ,  $V_{DD2} = 5.0\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

Table 22.

Parameter	Symbol	WA Grade			WB Grade, T Grade			WC Grade			Unit	Test Conditions/ Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{PLH}$	15		55	15		55	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD			6			4			4	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			6			5			5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	$t_{PSK}$			29			22			22	ns	Between any two units
Channel Matching												
Codirectional	$t_{PSKCD}$			15			3			3	ns	
Opposing Directional	$t_{PSKOD}$			29			20			20	ns	
Output Rise/Fall Time	$t_r/t_f$		2.5			2.5			2.5		ns	10% to 90%

Table 23.

Parameter	Symbol	1 Mbps—WA Grade, WB Grade, WC Grade, T Grade			10 Mbps—WB Grade, WC Grade			10 Mbps—T Grade			25 Mbps—WC Grade		Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	
SUPPLY CURRENT													
ADuM3210	$I_{DD1}$	0.8	1.3		2.1	3.2		2.1	3.2		4.6	6.1	mA
	$I_{DD2}$	1.0	1.6		2.0	2.8		2.0	2.8		3.7	5.1	mA
ADuM3211	$I_{DD1}$	0.7	1.3		1.8	2.6		1.8	2.6		3.8	5.4	mA
	$I_{DD2}$	1.3	1.8		3.1	4.1		3.1	4.1		6.1	8.0	mA

Table 24. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	$V_{IH}$	$0.7 V_{DDx}$			V	
Logic Low Input Threshold	$V_{IL}$				$0.3 V_{DDx}$	
Logic High Output Voltages	$V_{OH}$	$V_{DDx} - 0.1$	$V_{DDx}$		V	$I_{Ox} = -20\text{ }\mu\text{A}$ , $V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.5$	$V_{DDx} - 0.2$		V	$I_{Ox} = -3.2\text{ mA}$ , $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	$V_{OL}$	0.0		0.1	V	$I_{Ox} = 20\text{ }\mu\text{A}$ , $V_{Ix} = V_{IxL}$
		0.2		0.4	V	$I_{Ox} = 3.2\text{ mA}$ , $V_{Ix} = V_{IxL}$
Input Current per Channel	$I_i$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$	0.4		0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$	0.5		0.8	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$	0.10			mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$	0.05			mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity <sup>1</sup>	$ CM $	25	35		kV/ $\mu\text{s}$	$V_{Ix} = V_{DDx}$ , $V_{CM} = 1000\text{ V}$ , transient magnitude = 800 V
Refresh Rate	$f_r$		1.1		Mbps	

<sup>1</sup>  $|CM|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{DD}$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## PACKAGE CHARACTERISTICS

Table 25.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output) <sup>1</sup>	R <sub>I-O</sub>		10 <sup>12</sup>		Ω	
Capacitance (Input-to-Output) <sup>1</sup>	C <sub>I-O</sub>		1.0		pF	f = 1 MHz
Input Capacitance	C <sub>I</sub>		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ <sub>JCI</sub>		46		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	θ <sub>JCO</sub>		41		°C/W	

<sup>1</sup> The device is considered a 2-terminal device; Pin 1 through Pin 4 are shorted together, and Pin 5 through Pin 8 are shorted together.

## REGULATORY INFORMATION

The ADuM3210/ADuM3211 are approved by the organizations listed in Table 26.

Table 26.

UL	CSA	CQC	VDE
Recognized under UL 1577 component recognition program <sup>1</sup> Single/basic 2500 V rms isolation voltage	Approved under CSA Component Acceptance Notice #5A  Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage  Functional insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage	Approved under CQC11-471543-2012  Basic insulation per GB4943.1-2011 400 V rms (588 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 meters	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 <sup>2</sup>  Reinforced insulation, 560 V peak
File E214100	File 205078	File CQC14001114896	File 2471900-4880-0001

<sup>1</sup> In accordance with UL 1577, each ADuM3210/ADuM3211 is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 sec (current leakage detection limit = 5 μA).

<sup>2</sup> In accordance with DIN V VDE V 0884-10 (VDE V 0884-10):2006-12, each ADuM3210/ADuM3211 is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (\*) marking branded on the component designates DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval.

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 27.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Clearance in the Plane of the PCB	CL <sub>PCB</sub>	4.5	mm min	Measured from input terminals to output terminals, shortest line of sight distance through air in the plane of the PCB
Minimum External Air Gap (Clearance)	L(I01)	4.0	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.0	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Distance (Internal Clearance)		0.017 min	mm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303, Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

**INSULATION CHARACTERISTICS (DIN V VDE V 0884-10 (VDE V 0884-10):2006-12)**

These isolators are suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (\*) marking branded on the component designates DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval for a 560 V peak working voltage.

**Table 28.**

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms			I to IV I to III I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		$V_{IORM}$	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$ , 100% production test, $t_m = 1$ sec, partial discharge < 5 pC	$V_{PR}$	1050	V peak
Input-to-Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.6 = V_{PR}$ , $t_m = 60$ sec, partial discharge < 5 pC	$V_{PR}$	896	V peak
After Input and/or Safety Tests Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$ , $t_m = 60$ sec, partial discharge < 5 pC	$V_{PR}$	672	V peak
Highest Allowable Overvoltage	Transient overvoltage, $t_{TR} = 10$ sec	$V_{TR}$	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		$T_S$	150	°C
Side 1 Current		$I_{S1}$	160	mA
Side 2 Current		$I_{S2}$	170	mA
Insulation Resistance at $T_S$	$V_{IO} = 500$ V	$R_S$	>10 <sup>9</sup>	Ω

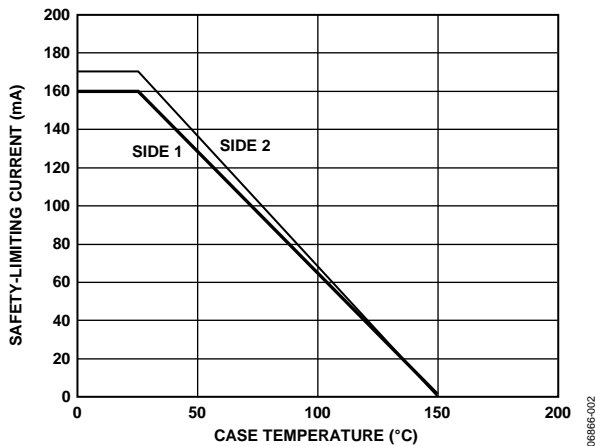


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature per DIN V VDE V 0884-10

**RECOMMENDED OPERATING CONDITIONS**

**Table 29.**

Parameter	Symbol	Rating
Operating Temperature	$T_A$	-40°C to +105°C
ADuM3210A/ADuM3211A		-40°C to +105°C
ADuM3210B/ADuM3211B		-40°C to +105°C
ADuM3210T/ADuM3211T		-40°C to +125°C
ADuM3210WA/ADuM3211WA		-40°C to +125°C
ADuM3210WB/ADuM3211WB		-40°C to +125°C
ADuM3210WC/ADuM3211WC		-40°C to +125°C
Supply Voltages <sup>1</sup>	$V_{DD1}, V_{DD2}$	3 V to 5.5 V
Maximum Input Signal Rise and Fall Times		1 ms

<sup>1</sup> All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information about immunity to external magnetic fields.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 30.

Parameter	Rating
Storage Temperature ( $T_{ST}$ )	$-55^\circ\text{C}$ to $+150^\circ\text{C}$
Ambient Operating Temperature ( $T_A$ )	$-40^\circ\text{C}$ to $+125^\circ\text{C}$
Supply Voltages ( $V_{DD1}$ , $V_{DD2}$ ) <sup>1</sup>	$-0.5\text{ V}$ to $+7.0\text{ V}$
Input Voltage ( $V_{IA}$ , $V_{IB}$ ) <sup>1,2</sup>	$-0.5\text{ V}$ to $V_{DD1} + 0.5\text{ V}$
Output Voltage ( $V_{OA}$ , $V_{OB}$ ) <sup>1,2</sup>	$-0.5\text{ V}$ to $V_{DDO} + 0.5\text{ V}$
Average Output Current per Pin ( $I_o$ ) <sup>3</sup>	$-22\text{ mA}$ to $+22\text{ mA}$
Common-Mode Transients ( $CM_H$ , $CM_L$ ) <sup>4</sup>	$-100\text{ kV}/\mu\text{s}$ to $+100\text{ kV}/\mu\text{s}$

<sup>1</sup> Each voltage is relative to its respective ground.

<sup>2</sup>  $V_{DD1}$  and  $V_{DDO}$  refer to the supply voltages on the input and output sides of a given channel, respectively.

<sup>3</sup> See Figure 3 for maximum allowable current values for various temperatures.

<sup>4</sup> Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 31. Maximum Continuous Working Voltage<sup>1</sup>

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDEV 0884-10
DC Voltage			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDEV 0884-10

<sup>1</sup> Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

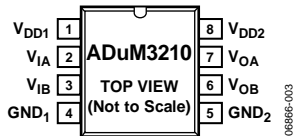


Figure 4. ADuM3210 Pin Configuration

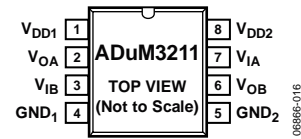


Figure 5. ADuM3211 Pin Configuration

Table 32. ADuM3210 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V.
2	V <sub>IA</sub>	Logic Input A.
3	V <sub>IB</sub>	Logic Input B.
4	GND <sub>1</sub>	Ground 1. Ground reference for Isolator Side 1.
5	GND <sub>2</sub>	Ground 2. Ground reference for Isolator Side 2.
6	V <sub>OB</sub>	Logic Output B.
7	V <sub>OA</sub>	Logic Output A.
8	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V.

Table 33. ADuM3211 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V.
2	V <sub>OA</sub>	Logic Output A.
3	V <sub>IB</sub>	Logic Input B.
4	GND <sub>1</sub>	Ground 1. Ground reference for Isolator Side 1.
5	GND <sub>2</sub>	Ground 2. Ground reference for Isolator Side 2.
6	V <sub>OB</sub>	Logic Output B.
7	V <sub>IA</sub>	Logic Input A.
8	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V.

## TRUTH TABLES

Table 34. ADuM3210 Truth Table (Positive Logic)

V <sub>IA</sub> Input <sup>1</sup>	V <sub>IB</sub> Input <sup>1</sup>	V <sub>DD1</sub> State	V <sub>DD2</sub> State	V <sub>OA</sub> Output <sup>1</sup>	V <sub>OB</sub> Output <sup>1</sup>	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	L	L	Outputs return to the input state within 1 μs of V <sub>DD1</sub> power restoration
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 μs of V <sub>DD0</sub> power restoration

<sup>1</sup> H is logic high, L is logic low, and X is don't care.

Table 35. ADuM3211 Truth Table (Positive Logic)

V <sub>IA</sub> Input <sup>1</sup>	V <sub>IB</sub> Input <sup>1</sup>	V <sub>DD1</sub> State	V <sub>DD2</sub> State	V <sub>OA</sub> Output <sup>1</sup>	V <sub>OB</sub> Output <sup>1</sup>	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	Indeterminate	L	Outputs return to the input state within 1 μs of V <sub>DD1</sub> power restoration
X	X	Powered	Unpowered	L	Indeterminate	Outputs return to the input state within 1 μs of V <sub>DD0</sub> power restoration

<sup>1</sup> H is logic high, L is logic low, and X is don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

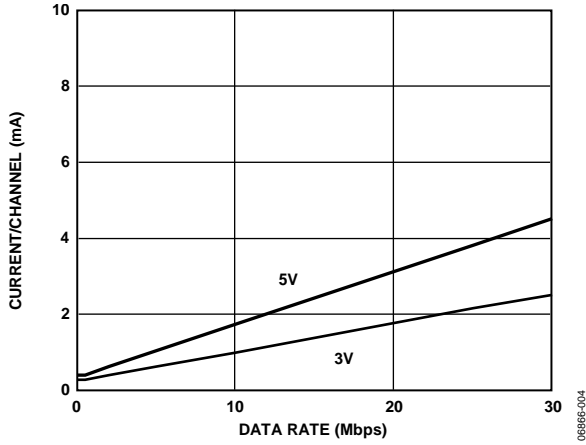


Figure 6. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3.3 V Operation

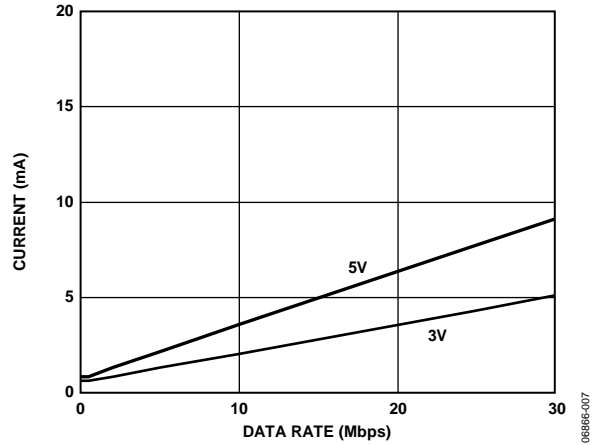


Figure 9. ADuM3210 Typical  $I_{DD1}$  Supply Current vs. Data Rate for 5 V and 3.3 V Operation

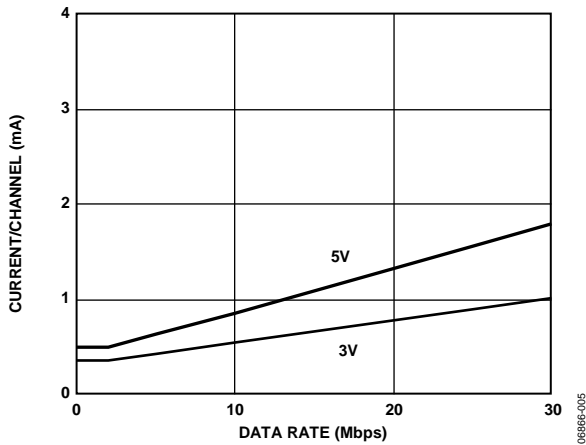


Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3.3 V Operation (No Output Load)

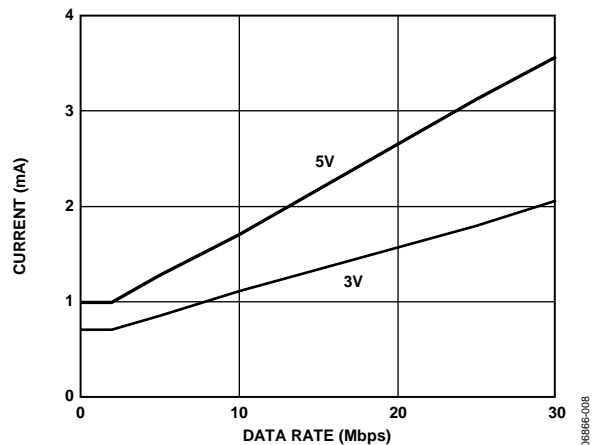


Figure 10. ADuM3210 Typical  $I_{DD2}$  Supply Current vs. Data Rate for 5 V and 3.3 V Operation

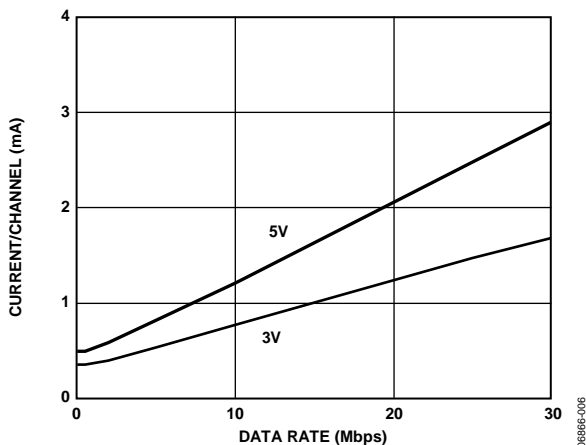


Figure 8. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3.3 V Operation (15 pF Output Load)

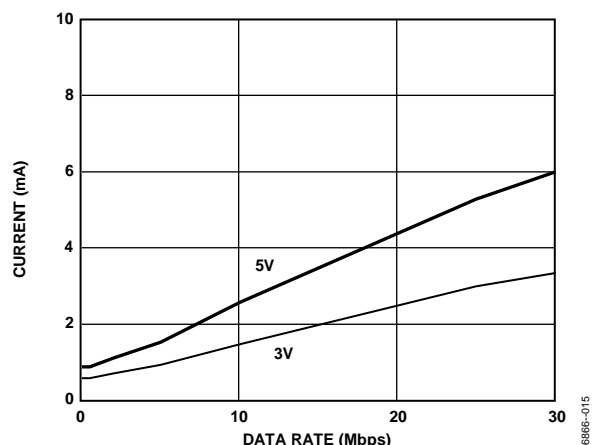


Figure 11. ADuM3211 Typical  $I_{DD1}$  or  $I_{DD2}$  Supply Current vs. Data Rate for 5 V and 3.3 V Operation



## APPLICATIONS INFORMATION

### PC BOARD LAYOUT

The ADuM3210/ADuM3211 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins. The capacitor value should be between 0.01 μF and 0.1 μF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 2 mm.

See the AN-1109 Application Note for board layout guidelines.

### SYSTEM-LEVEL ESD CONSIDERATIONS AND ENHANCEMENTS

System-level ESD reliability (for example, per IEC 61000-4-x) is highly dependent on system design, which varies widely by application. The ADuM3210/ADuM3211 incorporate many enhancements to make ESD reliability less dependent on system design. The enhancements include

- ESD protection cells are added to all input/output interfaces.
- Key metal trace resistances are reduced using wider geometry and paralleling of lines with vias.
- The SCR effect inherent in CMOS devices is minimized by use of a guarding and isolation technique between the PMOS and NMOS devices.
- Areas of high electric field concentration are eliminated using 45° corners on metal traces.
- Supply pin overvoltage is prevented with larger ESD clamps between each supply pin and its respective ground.

Although the ADuM3210/ADuM3211 improve system-level ESD reliability, they are no substitute for a robust system-level design. For detailed recommendations on board layout and system-level design, see the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products*.

### PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output.

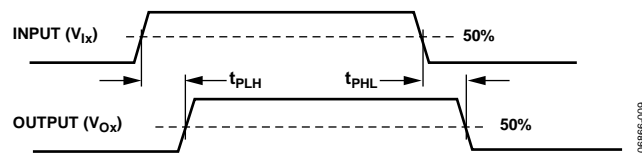


Figure 12. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM3210/ADuM3211 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM3210/ADuM3211 components operating under the same conditions.

### DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 2 μs, a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5 μs, the input side is assumed to be unpowered or nonfunctional, and the isolator output is forced to a default state by the watchdog timer circuit (see Table 34 and Table 35).

The ADuM3210/ADuM3211 are immune to external magnetic fields. The limitation on the magnetic field immunity of the ADuM3210/ADuM3211 is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM3210/ADuM3211 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at approximately 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2; n = 1, 2, \dots, N$$

where:

$\beta$  is the magnetic flux density (gauss).

$r_n$  is the radius of the  $n^{\text{th}}$  turn in the receiving coil (cm).

$N$  is the total number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM3210/ADuM3211 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 13.

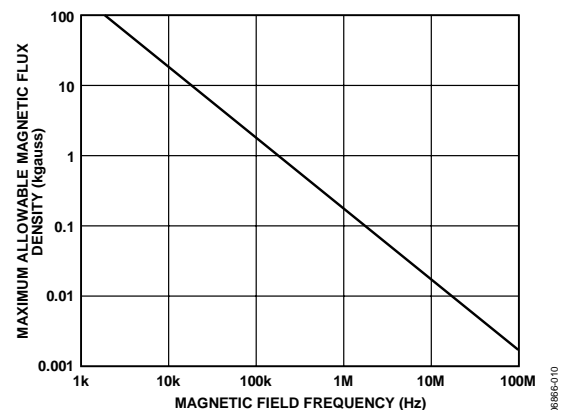


Figure 13. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. The voltage is approximately 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V, which is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM3210/ADuM3211 transformers. Figure 14 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 14, the ADuM3210/ADuM3211 are immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example, a 0.5 kA current placed 5 mm away from the ADuM3210/ADuM3211 is required to affect the operation of the component.

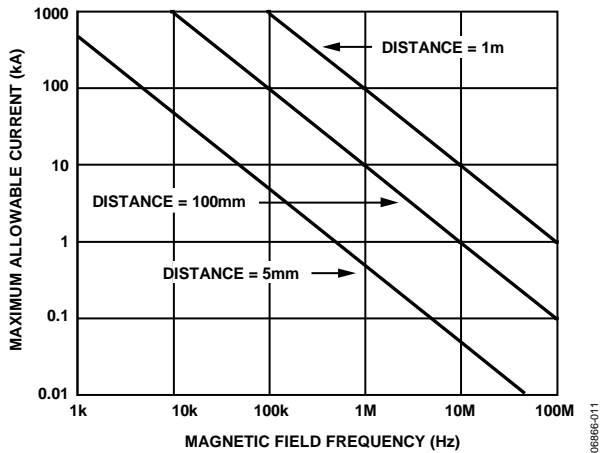


Figure 14. Maximum Allowable Current for Various Current-to-ADuM3210/ADuM3211 Spacings

Note that at combinations of strong magnetic fields and high frequency, any loops formed by the printed circuit board (PCB) traces can induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

**POWER CONSUMPTION**

The supply current at a given channel of the ADuM3210/ADuM3211 isolator is a function of the supply voltage, channel data rate, and channel output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \quad f > 0.5f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \quad f > 0.5f_r$$

where:

$I_{DDI(D)}$ ,  $I_{DDO(D)}$  are the input and output dynamic supply currents per channel (mA/Mbps).

$I_{DDI(Q)}$ ,  $I_{DDO(Q)}$  are the specified input and output quiescent supply currents (mA).

$C_L$  is the output load capacitance (pF).

$V_{DDO}$  is the output supply voltage (V).

$f$  is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

$f_r$  is the input stage refresh rate (Mbps).

To calculate the total  $I_{DD1}$  and  $I_{DD2}$  supply current, the supply currents for each input and output channel corresponding to  $I_{DD1}$  and  $I_{DD2}$  are calculated and totaled.

Figure 6 provides the input supply currents per channel as a function of data rate. Figure 7 and Figure 8 provide the output supply currents per channel as a function of data rate for an unloaded output condition and for a 15 pF output condition, respectively. Figure 9 through Figure 11 provide total  $I_{DD1}$  and  $I_{DD2}$  supply current as a function of data rate for the ADuM3210 and ADuM3211 channel configurations.

## INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the [ADuM3210/ADuM3211](#).

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 31 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the [ADuM3210/ADuM3211](#) depends on the voltage waveform type imposed across the isolation barrier. The iCoupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 15, Figure 16, and Figure 17 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the bipolar ac condition determines the maximum working voltage recommended by Analog Devices.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 31 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage cases.

Any cross-insulation voltage waveform that does not conform to Figure 16 or Figure 17 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 31.

Note that the voltage presented in Figure 16 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

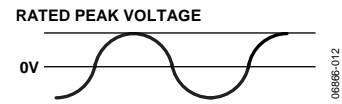


Figure 15. Bipolar AC Waveform

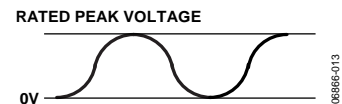


Figure 16. Unipolar AC Waveform

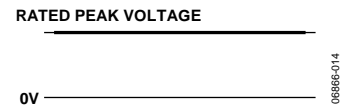
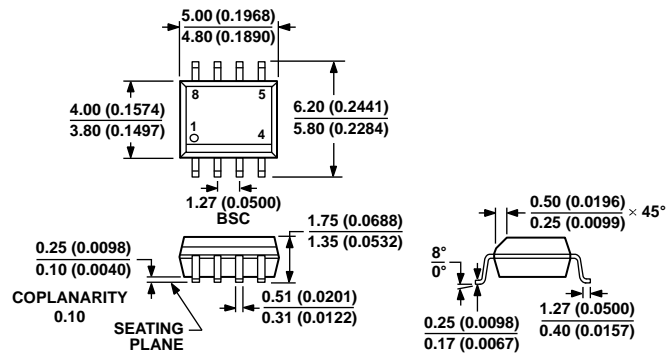


Figure 17. DC Waveform

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 18. 8-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-8)

Dimensions shown in millimeters and (inches)

012407-A