Data Sheet

ADuM340E/ADuM341E/ADuM342E

5.7 kV rms Quad Digital Isolators

FEATURES

- High common-mode transient immunity: 180 kV/µs typical
- High robustness to radiated and conducted noise
- Low propagation delay
  - 6.2 ns typical (10 ns maximum) for 5 V operation
- Low dynamic power consumption, <1.65 mA/ch at 1 Mbps
- 2.25 V to 5.5 V level translation
- 150 Mbps maximum guaranteed data rate for 5 V operation
- High temperature operation: 125°C
- Safety and regulatory approvals
  - UL recognition: 5700 V rms for 1 minute per UL 1577
  - VDE certificate of conformity (pending)
    - DIN V VDE V 0884-11 (VDE V 0884-11):2017-01
    - V_{IORM} = 1173 V peak
    - 10,000 V peak reinforced surge isolation voltage
  - CSA certification per IEC 62368-1 and IEC 61010-1 (pending)
  - TÜV Süd certification per EN 62368-1 (pending)
  - CQC certification per GB4943.1-2022 (pending)
- ±8 kV IEC 61000-4-2 ESD protection across isolation barrier
- ±5 kV HBM ESD protection on input/output pins
- Fail-safe high (E1) or low (E0) options
- 16-lead, RoHS compliant, SOIC package
- Backward compatibility with
  - ADuM1400/ADuM1401/ADuM1402
  - ADuM2400/ADuM2401/ADuM2402
  - ADuM140E/ADuM141E/ADuM142E
  - ADuM240E/ADuM241E/ADuM242E
- AEC-Q100 qualified for automotive applications

APPLICATIONS

- Serial peripheral interface (SPI) data converter isolation
- RS-485 and controller area network with flexible data rate (CAN FD) industrial field bus isolation
- PWM controller signal isolation
- General-purpose multichannel isolation

GENERAL DESCRIPTION

The ADuM340E/ADuM341E/ADuM342E[1] are quad-channel digital isolators based on Analog Devices, Inc., *i*Coupler® technology. Combining high speed, complementary metal-oxide semiconductor (CMOS) and back-to-back monolithic air core transformer technology, these isolation components provide outstanding performance characteristics and meet CISPR 32/EN 55032 Class B limits at 5 Mbps. The maximum propagation delay is 10 ns with a pulse width distortion of less than 3 ns at 5 V operation. Channel matching is tight at 3.0 ns maximum.

The ADuM340E/ADuM341E/ADuM342E data channels are independent and are available in a variety of configurations with a withstand voltage rating of 5.7 kV rms (see Figure 26). The devices operate with the supply voltage on either side ranging from 2.25 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier.

Two different fail-safe options are available, by which the outputs transition to a predetermined state when the input power supply is not applied.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

Rev. 0

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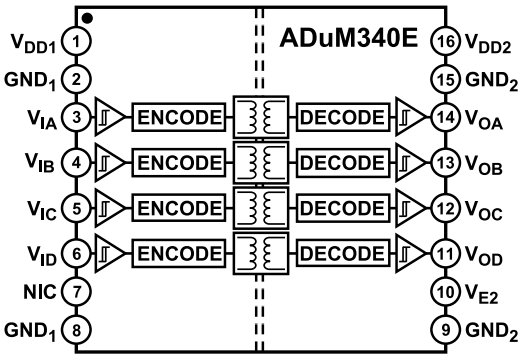
REVISION HISTORY

1/2023—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAMS



NOTES
1. NIC = NO INTERNAL CONNECTION. LEAVE THIS PIN FLOATING.

Figure 1. ADuM340E Functional Block Diagram

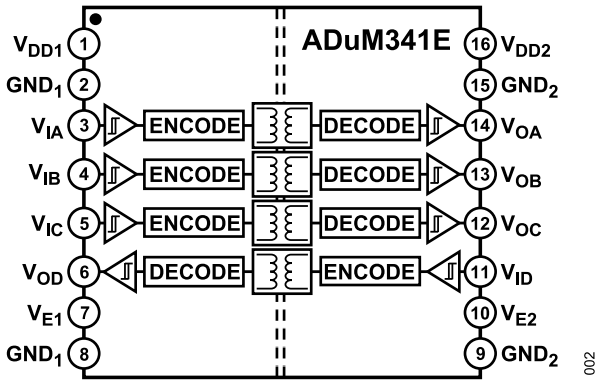


Figure 2. ADuM341E Functional Block Diagram

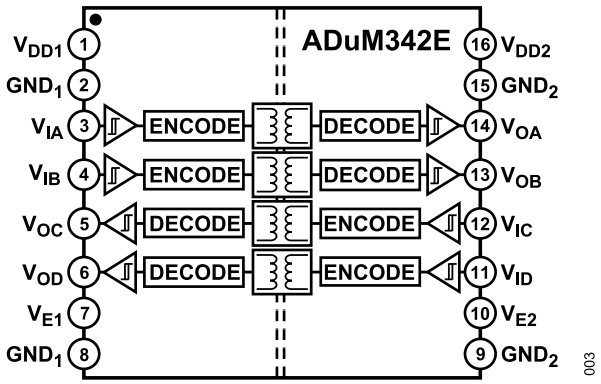


Figure 3. ADuM342E Functional Block Diagram

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty-cycle signals.

Table 1. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within pulse width distortion (PWD) limit
Data Rate		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	3.5	6.2	10	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.3	3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			6.1	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.3	3.0	ns	
Opposing Direction	t_{PSKOD}		0.3	3.0	ns	
Jitter[1]						See the Jitter Measurement section
Random Jitter, RMS (1σ)[2]	$t_{JIT(RJ)}$		7.19		ps	1 MHz clock input, all channels switching
Deterministic Jitter, Peak-to-Peak[3, 4]	$t_{JIT(DJ)}$		223		ps	100 Mbps, 2^{15} − 1 PRBS input
Total Jitter, Peak-to-Peak, at Bit Error Rate (BER) 1 × 10^{-12}	$t_{JIT(TJ)}$					100 Mbps, 2^{15} − 1 PRBS input[5]
Without Crosstalk			292		ps	Single channel switching
With Crosstalk			559		ps	All channels switching
Output Enabled to High-Z	t_{PHZ}, t_{PLZ}	3	5.5	12	ns	Output high/low to high impedance
Output High-Z to Enabled	t_{PZH}, t_{PZL}	3	5.5	12	ns	Output high impedance to high/low
DC SPECIFICATIONS						
Input Threshold Voltage						V_{Ix}, V_{Ex}
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Input Hysteresis	V_{HYS}		0.85		V	V_{IH} − V_{IL}
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[6] = −20 μA, V_{Ix} = V_{IxH}[7]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[6] = −4 mA, V_{Ix} = V_{IxH}[7]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[6] = 20 μA, V_{Ix} = V_{IxL}[8]
			0.2	0.4	V	I_{Ox}[6] = 4 mA, V_{Ix} = V_{IxL}[8]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}, 0 V ≤ V_{Ex} ≤ V_{DDx}
V_{E1}, V_{E2} Enable Input Pull-Up Current	I_{PU}	−10	−6		μA	V_{Ex} = 0 V
Tristate Output Current per Channel	I_{OZ}	−10	+0.01	+10	μA	0 V ≤ V_{Ox} ≤ V_{DDx}, V_{Ex} ≤ V_{IL}
Quiescent Supply Current						
ADuM340E						
	$I_{DD1 (Q)}$		0.61	0.85	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD2 (Q)}$		1.5	2.3	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD1 (Q)}$		7.6	11.2	mA	V_I[9] = 1 (E0), 0 (E1)[10]
	$I_{DD2 (Q)}$		3.3	5.1	mA	V_I[9] = 1 (E0), 0 (E1)[10]
ADuM341E						
	$I_{DD1 (Q)}$		0.8	1.3	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD2 (Q)}$		1.3	1.9	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD1 (Q)}$		6.3	9.2	mA	V_I[9] = 1 (E0), 0 (E1)[10]
	$I_{DD2 (Q)}$		4.2	6	mA	V_I[9] = 1 (E0), 0 (E1)[10]

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM342E						
	$I_{DD1 (Q)}$		1.0	1.7	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD2 (Q)}$		1.0	1.7	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD1 (Q)}$		5.2	8.0	mA	V_I[9] = 1 (E0), 0 (E1)[10]
	$I_{DD2 (Q)}$		5.3	7.8	mA	V_I[9] = 1 (E0), 0 (E1)[10]
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.005		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.015		mA/Mbps	Inputs switching, 50% duty cycle, C_L = 0 nF
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{UVLO+}		2.0	2.2	V	Rising supply voltage enable threshold
Negative V_{DDx} Threshold	V_{UVLO-}	1.7	1.8		V	Falling supply voltage lockout threshold
V_{DDx} Hysteresis	V_{UVLO_HYS}		0.2		V	UVLO hysteresis
UVLO Release Time[11]	t_{UVLO}			60	µs	UVLO release delay after V_{UVLO+} threshold
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[11, 12]	$\|CM_H\|$	100	180		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V
	$\|CM_L\|$	100	180		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V

1 Jitter parameters are guaranteed by design and characterization. Values do not include stimulus jitter.

2 This specification is measured over a population of ~100,000 edges.

3 Peak-to-peak jitter specifications include jitter due to PWD.

4 This specification is measured over a population of ~300,000 edges.

5 Using the following formula: $t_{JIT(TJ)} = 14 \times t_{JIT(RJ)} + t_{JIT(DJ)}$.

6 I_{Ox} is the Channel x output current, where x = A, B, C, or D.

7 V_{IxH} is the input side logic high.

8 V_{IxL} is the input side logic low.

9 V_I is the voltage input.

10 E0 refers to the ADuM340E0/ADuM341E0/ADuM342E0 models, and E1 refers to the ADuM340E1/ADuM341E1/ADuM342E1 models. See the Ordering Guide section.

11 Guaranteed by design and not subject to production test.

12 $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 2. Total Supply Current vs. Data Throughput

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
ADuM340E						
1 Mbps						
Supply Current Side 1	I_{DD1}		4.2	6.1	mA	
Supply Current Side 2	I_{DD2}		2.5	3.6	mA	C_L = 0 nF
25 Mbps						
Supply Current Side 1	I_{DD1}		4.6	6.4	mA	
Supply Current Side 2	I_{DD2}		3.9	5.3	mA	C_L = 0 nF
100 Mbps						
Supply Current Side 1	I_{DD1}		6.3	8.7	mA	
Supply Current Side 2	I_{DD2}		8.5	10.9	mA	C_L = 0 nF
ADuM341E						
1 Mbps						
Supply Current Side 1	I_{DD1}		3.6	5.3	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		2.8	4.1	mA	C_L = 0 nF

SPECIFICATIONS

Table 2. Total Supply Current vs. Data Throughput (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
25 Mbps						
Supply Current Side 1	I_{DD1}		4.4	6.0	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		4.0	5.6	mA	C_L = 0 nF
100 Mbps						
Supply Current Side 1	I_{DD1}		6.7	9.2	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		7.9	10.5	mA	C_L = 0 nF
ADuM342E						
1 Mbps						
Supply Current Side 1	I_{DD1}		3.1	4.9	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		3.2	4.8	mA	C_L = 0 nF
25 Mbps						
Supply Current Side 1	I_{DD1}		4.1	6.1	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		4.2	5.9	mA	C_L = 0 nF
100 Mbps						
Supply Current Side 1	I_{DD1}		7.3	10.0	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		7.3	10.0	mA	C_L = 0 nF

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty-cycle signals.

Table 3. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	3.6	6.6	10	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.5	3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.5	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.5	3.0	ns	
Opposing Direction	t_{PSKOD}		0.5	3.0	ns	
Jitter[1]						See the Jitter Measurement section
Random Jitter, RMS (1σ)[2]	$t_{JIT(RJ)}$		7.1		ps	1 MHz clock input
Deterministic Jitter, Peak-to-Peak[3, 4]	$t_{JIT(DJ)}$		243		ps	100 Mbps, 2^{15} − 1 PRBS input
Total Jitter, Peak-to-Peak, at Bit Error Rate (BER) 1 × 10^{-12}	$t_{JIT(TJ)}$					100 Mbps, 2^{15} − 1 PRBS input[5]
Without Crosstalk			318		ps	Single channel switching
With Crosstalk			444		ps	All channels switching
Output Enabled to High-Z	t_{PHZ}, t_{PLZ}	3	5	12	ns	Output high/low to high Impedance
Output High-Z to Enabled	t_{PZH}, t_{PZL}	3	5	12	ns	Output high impedance to high/low
DC SPECIFICATIONS						
Input Threshold Voltage						V_{Ix}, V_{Ex}
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Input Hysteresis	V_{HYS}		0.7		V	V_{IH} − V_{IL}
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[6] = −20 μA, V_{Ix} = V_{IxH}[7]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[6] = −2 mA, V_{Ix} = V_{IxH}[7]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[6] = 20 μA, V_{Ix} = V_{IxL}[8]
			0.2	0.4	V	I_{Ox}[6]= 2 mA, V_{Ix} = V_{IxL}[8]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}, 0 V ≤ V_{Ex} ≤ V_{DDx}
V_{E2} Enable Input Pull-Up Current	I_{PU}	−10	−4		μA	V_{E2} = 0 V
Tristate Output Current per Channel	I_{OZ}	−10	+0.01	+10	μA	0 V ≤ V_{Ox} ≤ V_{DDx}, V_{Ex} ≤ V_{IL}
Quiescent Supply Current						
ADuM340E						
	$I_{DD1 (Q)}$		0.6	0.82	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD2 (Q)}$		1.4	2.2	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD1 (Q)}$		7.5	11.0	mA	V_I[9] = 1 (E0), 0 (E1)[10]
	$I_{DD2 (Q)}$		3.2	5.0	mA	V_I[9] = 1 (E0), 0 (E1)[10]
ADuM341E						
	$I_{DD1 (Q)}$		0.8	1.3	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD2 (Q)}$		1.2	1.8	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD1 (Q)}$		6.6	8.8	mA	V_I[9] = 1 (E0), 0 (E1)[10]
	$I_{DD2 (Q)}$		4.1	5.9	mA	V_I[9] = 1 (E0), 0 (E1)[10]

SPECIFICATIONS

Table 3. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM342E						
	$I_{DD1 (Q)}$		0.9	1.6	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD2 (Q)}$		1.0	1.6	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD1 (Q)}$		5.1	7.6	mA	V_I[9] = 1 (E0), 0 (E1)[10]
	$I_{DD2 (Q)}$		5.2	7.6	mA	V_I[9] = 1 (E0), 0 (E1)[10]
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.004		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.009		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{UVLO+}		2.0	2.2	V	Rising supply voltage enable threshold
Negative V_{DDx} Threshold	V_{UVLO-}	1.7	1.8		V	Falling supply voltage lockout threshold
V_{DDx} Hysteresis	V_{UVLO_HYS}		0.2		V	UVLO hysteresis
UVLO Release Time[11]	t_{UVLO}			60	µs	UVLO release delay after V_{UVLO+} threshold
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[11, 12]	$\|CM_H\|$	100	180		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	100	180		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] Jitter parameters are guaranteed by design and characterization. Values do not include stimulus jitter.

[2] This specification is measured over a population of ~100,000 edges.

[3] Peak-to-peak jitter specifications include jitter due to PWD.

[4] This specification is measured over a population of ~300,000 edges.

[5] Using the following formula: $t_{JIT(TJ)} = 14 \times t_{JIT(RJ)} + t_{JIT(DJ)}$.

[6] I_{Ox} is the Channel x output current, where x = A, B, C, or D.

[7] V_{IxH} is the input side logic high.

[8] V_{IxL} is the input side logic low.

[9] V_I is the voltage input.

[10] E0 refers to ADuM340E0/ADuM341E0/ADuM342E0 models, and E1 refers to ADuM340E1/ADuM341E1/ADuM342E1 models. See the Ordering Guide section.

[11] Guaranteed by design and not subject to production test.

[12] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 4. Total Supply Current vs. Data Throughput

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
ADuM340E						
1 Mbps						
Supply Current Side 1	I_{DD1}		4.1	6.0	mA	
Supply Current Side 2	I_{DD2}		2.4	3.5	mA	C_L = 0 nF
25 Mbps						
Supply Current Side 1	I_{DD1}		4.5	6.2	mA	
Supply Current Side 2	I_{DD2}		3.4	4.6	mA	C_L = 0 nF
100 Mbps						
Supply Current Side 1	I_{DD1}		5.8	7.5	mA	
Supply Current Side 2	I_{DD2}		6.3	8.8	mA	C_L = 0 nF
ADuM341E						
1 Mbps						

SPECIFICATIONS

Table 4. Total Supply Current vs. Data Throughput (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply Current Side 1	I_{DD1}		3.7	4.9	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		2.7	3.9	mA	C_L = 0 nF
25 Mbps						
Supply Current Side 1	I_{DD1}		4.3	5.4	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		3.5	4.9	mA	C_L = 0 nF
100 Mbps						
Supply Current Side 1	I_{DD1}		6.2	7.5	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		6.1	8.4	mA	C_L = 0 nF
ADuM342E						
1 Mbps						
Supply Current Side 1	I_{DD1}		3.1	4.7	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		3.2	4.7	mA	C_L = 0 nF
25 Mbps						
Supply Current Side 1	I_{DD1}		3.7	5.4	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		3.8	5.4	mA	C_L = 0 nF
100 Mbps						
Supply Current Side 1	I_{DD1}		6.0	8.5	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		5.9	8.1	mA	C_L = 0 nF

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 2.5 V. Minimum/maximum specifications apply over the entire recommended operation range: 2.25 V ≤ V_{DD1} ≤ 2.75 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty-cycle signals.

Table 5. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	10			ns	Within PWD limit
Data Rate		100			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	4.1	7.2	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.3	4.5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			6.8	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.4	5.0	ns	
Opposing Direction	t_{PSKOD}		0.4	5.0	ns	
Jitter[1]						See the Jitter Measurement section
Random Jitter, RMS (1σ)[2]	$t_{JIT(RJ)}$		8.58		ps	1 MHz clock input
Deterministic Jitter, Peak to Peak[3, 4]	$t_{JIT(DJ)}$		222		ps	100 Mbps, 2^{15} − 1 PRBS
Total Jitter, Peak to Peak, at Bit Error Rate (BER) 1 × 10^{-12}	$t_{JIT(TJ)}$					100 Mbps, 2^{15} − 1 PRBS[5]
Without Crosstalk			295		ps	Single channel switching
With Crosstalk			450		ps	All channels switching
Output Enabled to High-Z	t_{PHZ}, t_{PLZ}		6	20	ns	Output high/low to high impedance
Output High-Z to Enabled	t_{PZH}, t_{PZL}		6	20	ns	Output high impedance to high/low
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Input Hysteresis	V_{HYS}		0.65		V	$V_{IH} - V_{IL}$
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[6] = −20 μA, V_{Ix} = V_{IxH}[7]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[6] = −2 mA, V_{Ix} = V_{IxH}[7]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[6] = 20 μA, V_{Ix} = V_{IxL}[8]
			0.2	0.4	V	I_{Ox}[6] = 2 mA, V_{Ix} = V_{IxL}[8]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
V_{E2} Enable Input Pull-Up Current	I_{PU}	−10	−3		μA	V_{E2} = 0 V
Tristate Output Current per Channel	I_{OZ}	−10	+0.01	+10	μA	0 V ≤ V_{Ox} ≤ V_{DDx}, V_{Ex} ≤ V_{IL}
Quiescent Supply Current						
ADuM340E						
	$I_{DD1 (Q)}$		0.6	0.82	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD2 (Q)}$		1.4	2.2	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD1 (Q)}$		7.6	10.4	mA	V_I[9] = 1 (E0), 0 (E1)[10]
	$I_{DD2 (Q)}$		3.2	4.8	mA	V_I[9] = 1 (E0), 0 (E1)[10]
ADuM341E						
	$I_{DD1 (Q)}$		0.8	1.3	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD2 (Q)}$		1.2	2.0	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD1 (Q)}$		6.6	8.9	mA	V_I[9] = 1 (E0), 0 (E1)[10]
	$I_{DD2 (Q)}$		4.1	5.9	mA	V_I[9] = 1 (E0), 0 (E1)[10]

SPECIFICATIONS

Table 5. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM342E						
	$I_{DD1 (Q)}$		1.0	1.6	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD2 (Q)}$		1.0	1.6	mA	V_I[9] = 0 (E0), 1 (E1)[10]
	$I_{DD1 (Q)}$		5.1	8.1	mA	V_I[9] = 1 (E0), 0 (E1)[10]
	$I_{DD2 (Q)}$		5.2	7.6	mA	V_I[9] = 1 (E0), 0 (E1)[10]
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.004		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.008		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout						
Positive V_{DDx} Threshold	V_{UVLO+}		2.0	2.2	V	Rising supply voltage enable threshold
Negative V_{DDx} Threshold	V_{UVLO-}	1.7	1.8		V	Falling supply voltage lockout threshold
V_{DDx} Hysteresis	V_{UVLO_HYS}		0.2		V	UVLO hysteresis
UVLO Release Time[11]	t_{UVLO}			60	µs	UVLO release delay after V_{UVLO+} threshold
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[11, 12]	$\|CM_H\|$	100	180		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	100	180		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] Jitter parameters are guaranteed by design and characterization. Values do not include stimulus jitter.

[2] This specification is measured over a population of ~100,000 edges.

[3] Peak-to-peak jitter specifications include jitter due to PWD.

[4] This specification is measured over a population of ~300,000 edges.

[5] Using the following formula: $t_{JIT(TJ)} = 14 \times t_{JIT(RJ)} + t_{JIT(DJ)}$.

[6] I_{Ox} is the Channel x output current, where x = A, B, C, or D.

[7] V_{IxH} is the input side logic high.

[8] V_{IxL} is the input side logic low.

[9] V_I is the voltage input.

[10] E0 refers to ADuM340E0/ADuM341E0/ADuM342E0 models, and E1 refers to ADuM340E1/ADuM341E1/ADuM342E1 models. See the Ordering Guide section.

[11] Guaranteed by design and not subject to production test.

[12] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 6. Total Supply Current vs. Data Throughput

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
ADuM340E						
1 Mbps						
Supply Current Side 1	I_{DD1}		4.0	5.9	mA	
Supply Current Side 2	I_{DD2}		2.4	3.5	mA	C_L = 0 nF
25 Mbps						
Supply Current Side 1	I_{DD1}		4.5	6.1	mA	
Supply Current Side 2	I_{DD2}		3.1	4.3	mA	C_L = 0 nF
100 Mbps						
Supply Current Side 1	I_{DD1}		5.6	7.3	mA	
Supply Current Side 2	I_{DD2}		5.4	7.4	mA	C_L = 0 nF
ADuM341E						
1 Mbps						

SPECIFICATIONS

Table 6. Total Supply Current vs. Data Throughput (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply Current Side 1	I_{DD1}		3.7	4.9	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		2.7	3.9	mA	C_L = 0 nF
25 Mbps						
Supply Current Side 1	I_{DD1}		4.2	5.6	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		3.3	4.9	mA	C_L = 0 nF
100 Mbps						
Supply Current Side 1	I_{DD1}		5.8	7.6	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		5.4	8.4	mA	C_L = 0 nF
ADuM342E						
1 Mbps						
Supply Current Side 1	I_{DD1}		3.1	4.7	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		3.2	4.7	mA	C_L = 0 nF
25 Mbps						
Supply Current Side 1	I_{DD1}		3.6	5.3	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		3.7	5.3	mA	C_L = 0 nF
100 Mbps						
Supply Current Side 1	I_{DD1}		5.4	7.5	mA	C_L = 0 nF
Supply Current Side 2	I_{DD2}		5.5	7.5	mA	C_L = 0 nF

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 7. RW-16 Wide-Body [SOIC_W] Package

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5700	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	7.8	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	7.8	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.1	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Distance through insulation	DTI	34	µm	Minimum internal clearance
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	Tested in accordance to IEC 60112
Material Group		I		Material Group per IEC 60664-1

PACKAGE CHARACTERISTICS

Table 8. RW-16 Wide-Body [SOIC_W] Package

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Insulation Resistance[1]	R_{I-O}		10^{13}		Ω	Input to output voltage (V_{I-O}) = 500 V DC
Insulation Capacitance[1]	C_{I-O}		0.85		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		65		°C/W	Simulated per JEDEC JESD-51

[1] The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

[2] Input capacitance is from any input data pin to the respective ground.

SPECIFICATIONS

REGULATORY INFORMATION

See Table 13 for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels. Certifications available at Safety and Regulatory Certification for Digital Isolation.

Table 9. RW-16 Wide-Body [SOIC_W] Package

Regulatory Agency	Standard Certification/Approval	File
UL	Recognized under 1577 component recognition program	E214100 Volume 1, Section 21
	Single protection, 5700 V rms[1] isolation voltage	
VDE (Pending)	Certified according to DIN V VDE V 0884-11 (VDE V 0884-11):2017-01	Pending
	Reinforced insulation, V_{IORM} = 1173 V peak[2], V_{IOSM} = 10,000 V peak	
CSA[3] (Pending)	Approved under CSA component acceptance	Pending
	CSA 62368-1-19, EN 62368-1:2020, and IEC 62368-1:2018 third edition:	
	Basic insulation at 780 V rms	
	Reinforced insulation at 390 V rms	
	IEC 60601-1 Edition 3.1, CSA 60601-1:14:	
	Basic insulation (1 means of patient protection (1 MOPP)), 490 V rms	
	CSA 61010-1-12 and IEC 61010-1 third edition:	
	Basic insulation at 300 V rms mains	
	Reinforced insulation at 600 V rms mains	
TÜV Süd (Pending)	Certified as component level device	Pending
	EN 62368-1: 2020+A11:2020	
CQC (Pending)	Certified by CQC11-471543-2012, GB4943.1-2022	Pending
	Basic insulation at 760 V rms (1075 V peak)	
	Reinforced insulation at 380 V rms (537 V peak), tropical climate, altitude ≤5000 meters	

[1] In accordance with UL 1577, each product is proof tested by applying an insulation test voltage ≥6840 V rms for 1 sec.

[2] In accordance with DIN V VDE V 0884-11, each product is proof tested by applying an insulation test voltage ≥ 2199 V peak for 1 sec (partial discharge detection limit = 5 pC).

[3] Working voltages are quoted for Pollution Degree 2, Material Group III.

DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS (PENDING)

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The asterisk (*) marking on packages denotes DIN V VDE V 0884-11 approval (pending).

Table 10. DIN V VDE V 0884-11 (VDE V 0884-11) Insulation Characteristics (Pending)

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to III	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	1173	V peak
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{pd\ (m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	2199	V peak
Input to Output Test Voltage, Method A		$V_{pd\ (m)}$		
After Environmental Tests Subgroup 1	V_{IORM} × 1.5 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		1759	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		1407	V peak
Highest Allowable Overvoltage		V_{IOTM}	8000	V peak

SPECIFICATIONS

Table 10. DIN V VDE V 0884-11 (VDE V 0884-11) Insulation Characteristics (Pending) (Continued)

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Surge Isolation Voltage Reinforced	V_{PEAK} = 16 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	10000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	1.92	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

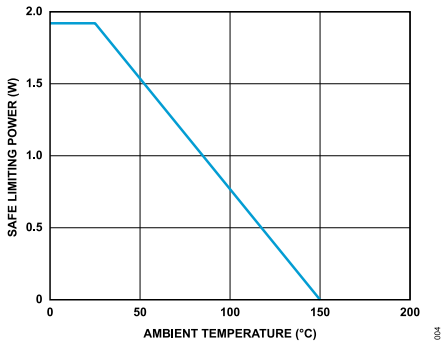


Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-11

RECOMMENDED OPERATING CONDITIONS

Table 11. Recommended Operating Conditions

Parameter	Symbol	Rating
Operating Temperature	T_A	−40°C to +125°C
Supply Voltages		
V_{DD1}		2.25 V to 5.5 V
V_{DD2}		2.25 V to 5.5 V
Input Signal Rise and Fall Times		1.0 ms

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 12. Absolute Maximum Ratings

Parameter	Rating
Supply Voltages	
V_{DD1} to GND_1	−0.5 V to +7.0 V
V_{DD2} to GND_2	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{E1}, V_{E2})[1]	−0.5 V to V_{DDI} + 0.5 V
Output Voltages (V_{OA}, V_{OB}, V_{OC}, V_{OD})[2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	
Side 1 Output Current (I_{O1})	−10 mA to +10 mA
Side 2 Output Current (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[4]	−300 kV/µs to +300 kV/µs
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C
Moisture Sensitivity Level	MSL3

[1] V_{DDI} is the input side supply voltage.

[2] V_{DDO} is the output side supply voltage.

[3] See Figure 4 for the maximum rated current values for various ambient temperatures.

[4] Refers to the common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latchup or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 13. Maximum Continuous Working Voltage, RW-16 Wide-Body [SOIC_W] Package

Parameter	Rating[1]	Constraint
AC Voltage		
Bipolar Waveform		
Basic Insulation	1000 V rms	Basic insulation rating per IEC60747-17. Accumulative failure rate over lifetime (FROL) ≤ 1000 ppm at 20 years.
Reinforced Insulation	779 V rms	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment.
DC Voltage		
Basic Insulation	1414 V DC	Basic insulation rating per IEC60747-17. Accumulative failure rate over lifetime (FROL) ≤ 1000 ppm at 20 years.
Reinforced Insulation	779 V DC	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment.

[1] Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier in a Pollution Degree 2 environment. See the Insulation Lifetime section for more details.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2.

ESD Ratings for ADuM340E/ADuM341E/ADuM342E

Table 14. ADuM340E/ADuM341E/ADuM342E, 16-Lead SOIC_W

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±5000	3A
CDM[1]	±1250	C3
IEC[2]	±8000	Level 4

[1] With respect to local V_{DDx} and GND_x pins.

[2] Across the isolation barrier between GND_1 and GND_2.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

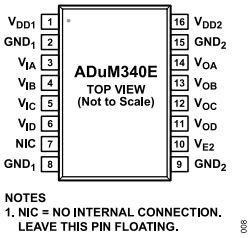


Figure 5. ADuM340E Pin Configuration

Table 15. ADuM340E Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1. This pin requires a 0.1 µF bypass capacitor.
2, 8	GND_1	Ground Reference for Isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{ID}	Logic Input D.
7	NIC	No Internal Connection. Leave this pin floating.
9, 15	GND_2	Ground Reference for Isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. When V_{E2} is high or disconnected, the V_{OA}, V_{OB}, V_{OC}, and V_{OD} outputs are enabled. When V_{E2} is low, the V_{OA}, V_{OB}, V_{OC}, and V_{OD} outputs are disabled to the high-Z state.
11	V_{OD}	Logic Output D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2. This pin requires a 0.1 µF bypass capacitor.

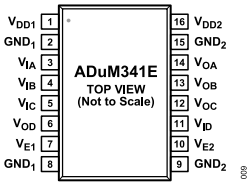


Figure 6. ADuM341E Pin Configuration

Table 16. ADuM341E Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1. This pin requires a 0.1 µF bypass capacitor.
2, 8	GND_1	Ground Reference for Isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{OD}	Logic Output D.
7	V_{E1}	Output Enable 1. Active high logic input. When V_{E1} is high or disconnected, the V_{OD} output is enabled. When V_{E1} is low, the V_{OD} output is disabled to the high-Z state.
9, 15	GND_2	Ground Reference for Isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. When V_{E2} is high or disconnected, the V_{OA}, V_{OB}, and V_{OC} outputs are enabled. When V_{E2} is low, the V_{OA}, V_{OB}, and V_{OC} outputs are disabled to the high-Z state.
11	V_{ID}	Logic Input D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 16. ADuM341E Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
16	V_{DD2}	Supply Voltage for Isolator Side 2. This pin requires a 0.1 µF bypass capacitor.

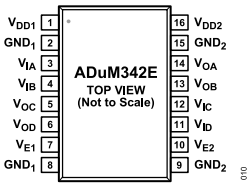


Figure 7. ADuM342E Pin Configuration

Table 17. ADuM342E Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1. This pin requires a 0.1 µF bypass capacitor.
2, 8	GND_1	Ground Reference for Isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{OC}	Logic Output C.
6	V_{OD}	Logic Output D.
7	V_{E1}	Output Enable 1. Active high logic input. When V_{E1} is high or disconnected, the V_{OD} output is enabled. When V_{E1} is low, the V_{OD} output is disabled to the high-Z state.
9, 15	GND_2	Ground Reference for Isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. When V_{E2} is high or disconnected, the V_{OA}, V_{OB}, and V_{OC} outputs are enabled. When V_{E2} is low, the V_{OA}, V_{OB}, and V_{OC} outputs are disabled to the high-Z state.
11	V_{ID}	Logic Input D.
12	V_{IC}	Logic Input C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2. This pin requires a 0.1 µF bypass capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

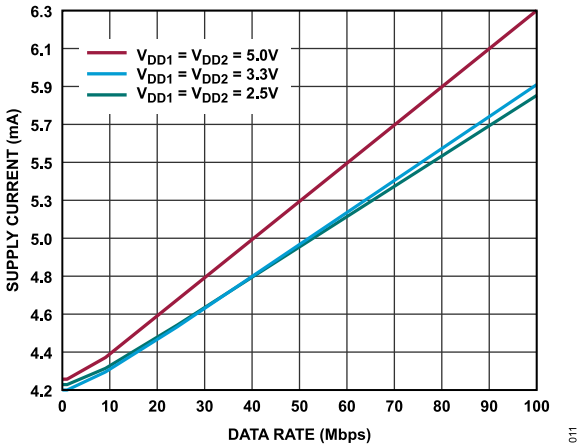


Figure 8. ADuM340E I_{DD1} Supply Current vs. Data Rate at Various Voltages

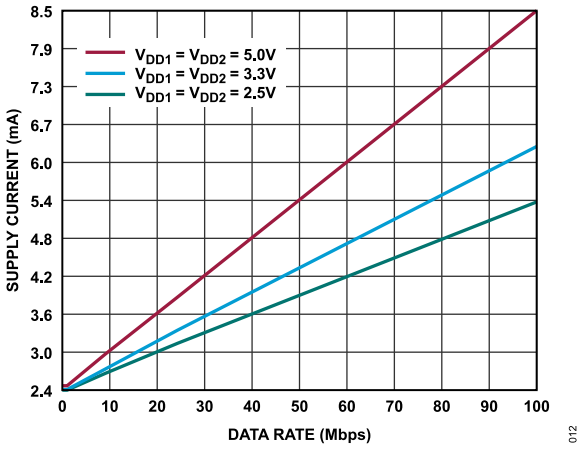


Figure 9. ADuM340E I_{DD2} Supply Current vs. Data Rate at Various Voltages

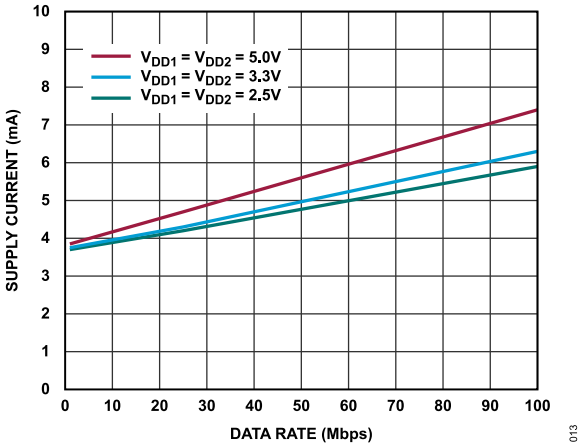


Figure 10. ADuM341E I_{DD1} Supply Current vs. Data Rate at Various Voltages

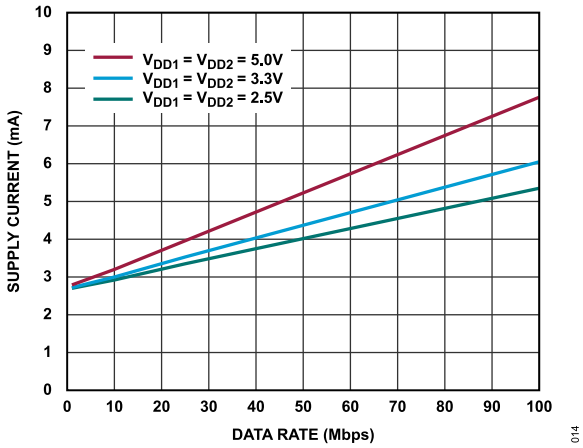


Figure 11. ADuM341E I_{DD2} Supply Current vs. Data Rate at Various Voltages

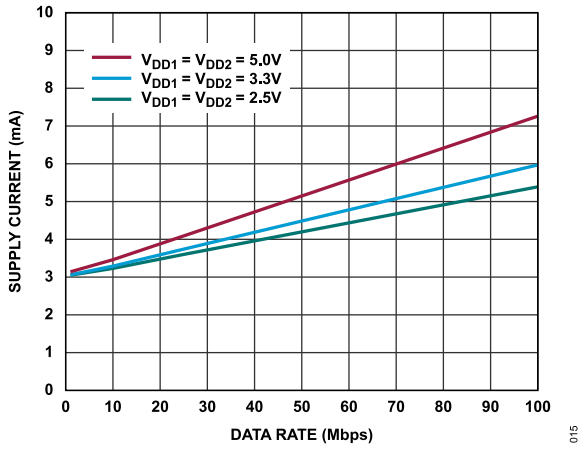


Figure 12. ADuM342E I_{DD1} Supply Current vs. Data Rate at Various Voltages

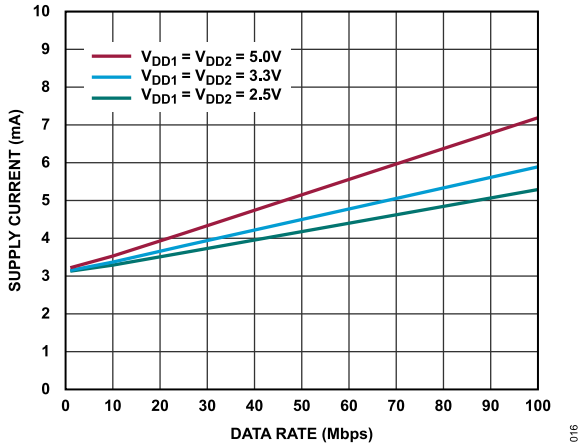


Figure 13. ADuM342E I_{DD2} Supply Current vs. Data Rate at Various Voltages

TYPICAL PERFORMANCE CHARACTERISTICS

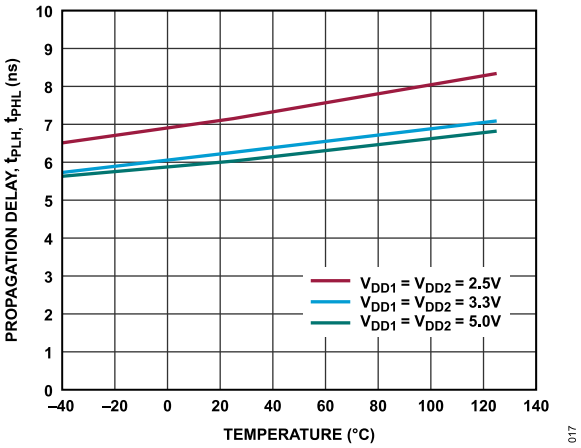


Figure 14. Propagation Delay, t_{PLH}, t_{PHL} vs. Temperature at Various Voltages

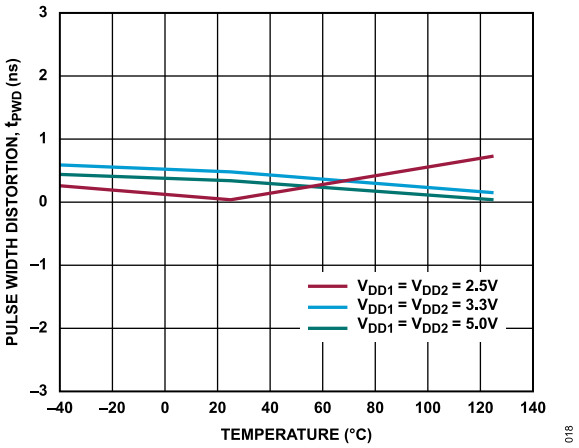


Figure 15. Pulse Width Distortion, t_{PWD} vs. Temperature at Various Voltages

THEORY OF OPERATION

The ADuM340E/ADuM341E/ADuM342E use a high frequency carrier to transmit data across the isolation barrier via *i*Coupler chip scale transformer coils separated by layers of polyimide isolation. Using an on/off keying (OOK) technique and the differential architecture shown in Figure 16 and Figure 17, the ADuM340E/ADuM341E/ADuM342E have very low propagation delay and high speed.

There is no interdependency between the V_{DD1} and V_{DD2} supplies. They can simultaneously operate at any voltage within their specified operating ranges and can sequence in any order. This feature enables the isolator to perform voltage translation of 2.5 V, 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient (CMTI) immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques.

Figure 16 illustrates the waveforms for models of the ADuM340E/ADuM341E/ADuM342E that have the condition of the fail-safe output state equal to low, where the carrier waveform is off when the input state is low. If the input side is off or not operating, the low fail-safe output state (ADuM340E0/ ADuM341E0/ ADuM342E0) sets the output to low. For the ADuM340E/ADuM341E/ADuM342E that have a high fail-safe output state, Figure 17 illustrates the conditions where the carrier waveform is off when the input state is high. When the input side is off or not operating, the high fail-safe output state (ADuM340E1/ ADuM341E1/ ADuM342E1) sets the output to high. See Figure 26 for the model numbers that have the fail-safe output state of low or the fail-safe output state of high.

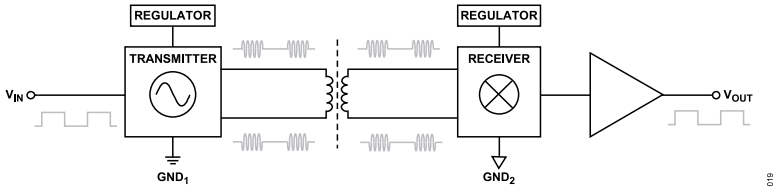


Figure 16. Operational Block Diagram of a Single Channel with a Low Fail-Safe Output State

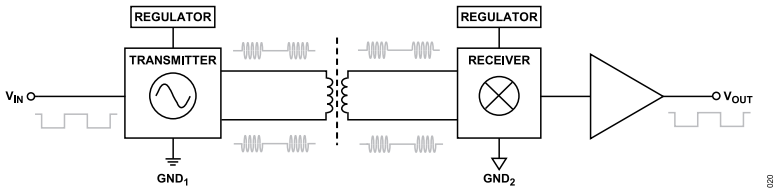


Figure 17. Operational Block Diagram of a Single Channel with a High Fail-Safe Output State

THEORY OF OPERATION

TRUTH TABLE

Table 18. ADuM340E/ADuM341E/ADuM342E Truth Table (Positive Logic)

V_{Ix} Input[1, 2]	V_{Ex} Input[1, 2]	V_{DDI} State[2]	V_{DDO} State[2]	Default Low (E0), V_{Ox} Output[1, 2, 3]	Default High (E1), V_{Ox} Output[1, 2, 3]	Test Conditions/ Comments
L	H or NC	Powered	Powered	L	L	Normal operation
H	H or NC	Powered	Powered	H	H	Normal operation
X	L	Powered	Powered	Z	Z	Outputs disabled
L	H or NC	Undervoltage	Powered	L	H	Fail-safe output
X[4]	L[4]	Undervoltage	Powered	Z	Z	Outputs disabled
X[4]	X[4]	Powered	Undervoltage	Indeterminate	Indeterminate	

1 L means low, H means high, X means don't care, NC means not connected, and Z means high impedance within one diode drop of GND_x.

2 V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D). V_{Ex} refers to the output enable signal on the same side as the V_{Ox} outputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.

3 E0 refers to ADuM340E0/ADuM341E0/ADuM342E0 models, and E1 refers to ADuM340E1/ADuM341E1/ADuM342E1 models. See the Ordering Guide section.

4 Input pins (V_{Ix}, V_{Ex}) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

I/O Schematics

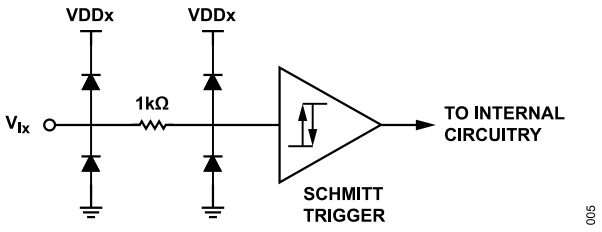


Figure 18. V_{IA}, V_{IB}, V_{IC}, V_{ID} Input Schematics

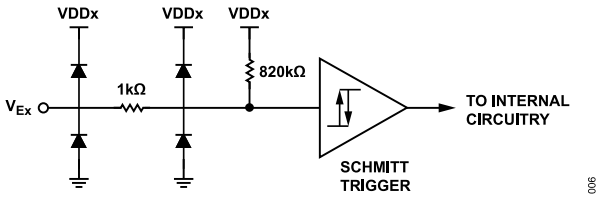


Figure 19. V_{E1}, V_{E2} Input Schematics

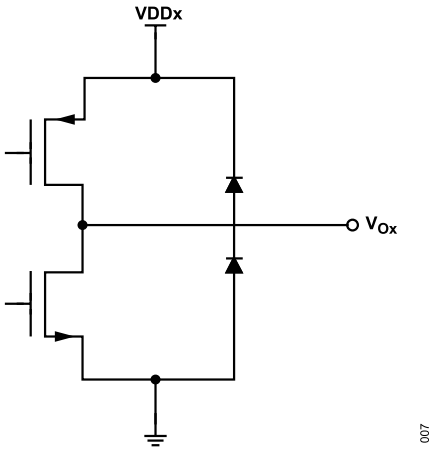


Figure 20. V_{OA}, V_{OB}, V_{OC}, V_{OD} Output Schematics

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM340E/ADuM341E/ADuM342E digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 21). Bypass capacitors are to be connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. The required bypass capacitor value is between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm. Low ESR capacitors are important for direct power injection (DPI) and CMTI performance. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 must also be considered, unless the ground pair on each package side is connected close to the package.

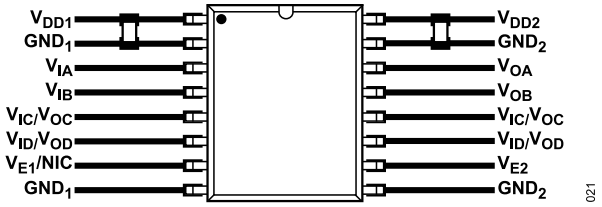


Figure 21. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this design can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage (see Table 12).

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time required for a logic signal to propagate through a component. The propagation delay to a Logic 0 output may differ from the propagation delay to a Logic 1 output.

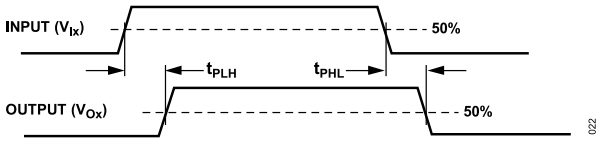


Figure 22. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel matching is the maximum amount the propagation delay differs between channels within a single ADuM340E/ADuM341E/ADuM342E component.

Propagation delay skew is the maximum amount the propagation delay differs between multiple ADuM340E/ADuM341E/ADuM342E components operating under the same conditions.

JITTER MEASUREMENT

Figure 23 shows the resulting eye diagram for the ADuM341E. The measurement was taken using a Keysight 81160A pulse pattern generator at 100 Mbps with a pseudorandom bit sequence (PRBS15) input. Jitter was measured using the Tektronix 6 Series B mixed-signal oscilloscope, with a TAP1500 probe and using the Tektronix jitter and analysis software. The 10% to 90% rise and fall times of the input signal from the generator approximately equals 1.2 ns. The result shows a typical output eye diagram measured on the ADuM341E. Figure 23 shows random and deterministic jitter characteristics for a PRBS input.

Total Jitter is evaluated at a BER of 1×10^{-12} and calculated for a PRBS input with and without the effects of crosstalk. The total jitter measurement without crosstalk consists of examining one channels input, while the adjacent channels inputs are grounded. The jitter measurement with crosstalk consists of all channels switching simultaneously at the same rate.

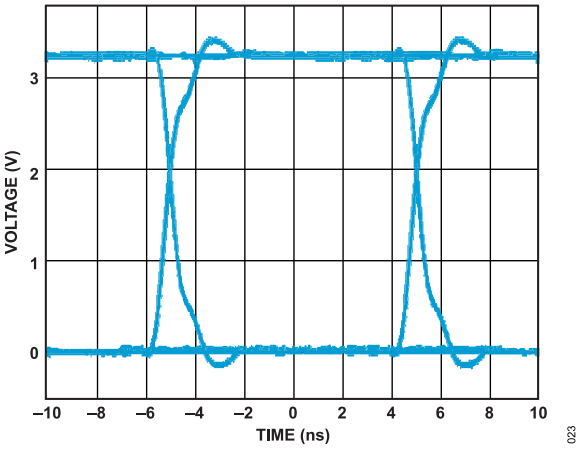


Figure 23. ADuM341E Output Channel Eye Diagram (V_{DD1} = V_{DD2} = 3.3 V, 100 Mbps, T_A = 25°C, C_L = 15 pF, PRBS15 Input

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking, and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

APPLICATIONS INFORMATION

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total RMS voltage across the isolation, pollution degree, and material group. The material group and creepage for the ADuM340E/ADuM341E/ADuM342E isolators are presented in Table 7.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling have shown that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as DC stress, which causes very little wear out because there is no displacement current, and an AC component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz AC and DC across the barrier as shown in Equation 1. Because only the AC portion of the stress causes wear out, the equation can be rearranged to solve for the AC RMS voltage, as is shown in Equation 2. For insulation wear out with the polyimide materials used in these products, the AC RMS voltage determines the product lifetime.

$$V_{RMS} = \sqrt{{V_{AC\ RMS}}^2 + {V_{DC}}^2} \quad (1)$$

or

$$V_{AC\ RMS} = \sqrt{{V_{RMS}}^2 - {V_{DC}}^2} \quad (2)$$

where:
V_{RMS} is the total RMS working voltage.
$V_{AC\ RMS}$ is the time varying portion of the working voltage.
V_{DC} is the DC offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power-conversion applications. Assume that the line voltage on one side of the isolation is 240 V AC rms and a 400 V DC bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance, and lifetime of a device, see Figure 24 and the following equations.

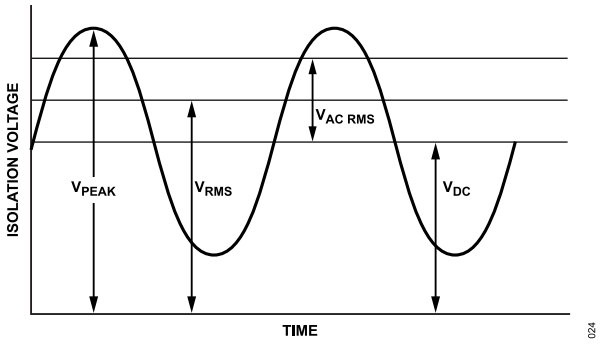


Figure 24. Critical Voltage Example

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{{V_{AC\ RMS}}^2 + {V_{DC}}^2}$$
$$V_{RMS} = \sqrt{240^2 + 400^2} \quad (3)$$
$$V_{RMS} = 466 \quad \text{V}$$

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the AC RMS voltage, use Equation 2.

$$V_{AC\ RMS} = \sqrt{{V_{RMS}}^2 - {V_{DC}}^2}$$
$$V_{AC\ RMS} = \sqrt{466^2 - 400^2} \quad (4)$$
$$V_{AC\ RMS} = 240 \quad \text{V rms}$$

In this case, the AC RMS voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage in Table 13 for the expected lifetime, less than a 60 Hz sine wave, and it is well within the limit for a 50-year service life.

Note that the DC working voltage limit in Table 13 is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

OUTLINE DIMENSIONS

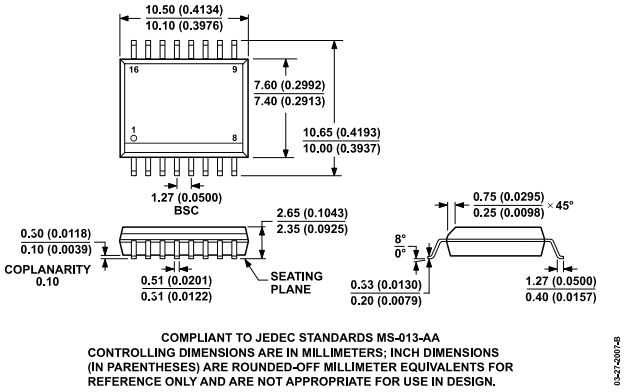


Figure 25. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

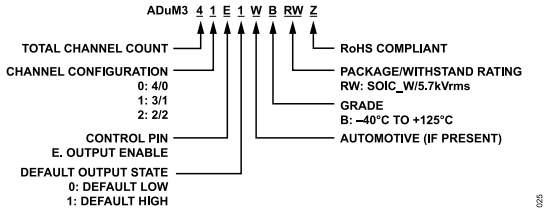


Figure 26. Product Selector Guide

Updated: January 12, 2023

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADUM340E0BRWZ	-40°C to +125°C	16-Lead SOIC Wide		RW-16
ADUM340E0BRWZ-RL	-40°C to +125°C	16-Lead SOIC Wide	Reel, 1000	RW-16
ADUM340E0WBRWZ	-40°C to +125°C	16-Lead SOIC Wide		RW-16
ADUM340E0WBRWZ-RL	-40°C to +125°C	16-Lead SOIC Wide	Reel, 1000	RW-16
ADUM340E1BRWZ	-40°C to +125°C	16-Lead SOIC Wide		RW-16
ADUM340E1BRWZ-RL	-40°C to +125°C	16-Lead SOIC Wide	Reel, 1000	RW-16
ADUM340E1WBRWZ	-40°C to +125°C	16-Lead SOIC Wide		RW-16
ADUM340E1WBRWZ-RL	-40°C to +125°C	16-Lead SOIC Wide	Reel, 1000	RW-16
ADUM341E0BRWZ	-40°C to +125°C	16-Lead SOIC Wide		RW-16
ADUM341E0BRWZ-RL	-40°C to +125°C	16-Lead SOIC Wide	Reel, 1000	RW-16
ADUM341E0WBRWZ	-40°C to +125°C	16-Lead SOIC Wide		RW-16
ADUM341E0WBRWZ-RL	-40°C to +125°C	16-Lead SOIC Wide	Reel, 1000	RW-16
ADUM341E1BRWZ	-40°C to +125°C	16-Lead SOIC Wide		RW-16
ADUM341E1BRWZ-RL	-40°C to +125°C	16-Lead SOIC Wide	Reel, 1000	RW-16
ADUM342E0BRWZ	-40°C to +125°C	16-Lead SOIC Wide		RW-16
ADUM342E0BRWZ-RL	-40°C to +125°C	16-Lead SOIC Wide	Reel, 1000	RW-16
ADUM342E0WBRWZ	-40°C to +125°C	16-Lead SOIC Wide		RW-16
ADUM342E0WBRWZ-RL	-40°C to +125°C	16-Lead SOIC Wide	Reel, 1000	RW-16
ADUM342E1BRWZ	-40°C to +125°C	16-Lead SOIC Wide		RW-16
ADUM342E1BRWZ-RL	-40°C to +125°C	16-Lead SOIC Wide	Reel, 1000	RW-16
ADUM342E1WBRWZ	-40°C to +125°C	16-Lead SOIC Wide		RW-16