Small, 3.75 kV RMS Quad Digital Isolators

Data Sheet

ADuM3480/ADuM3481/ADuM3482

FEATURES

- Up to 25 Mbps data rate (NRZ)
- Low propagation delay: 25 ns typical
- Low dynamic power consumption
- 1.8 V to 5 V level translation
- High temperature operation: 125°C
- High common-mode transient immunity: >25 kV/µs
- Output default select
- 20-lead, RoHS-compliant, SSOP package
- Safety and regulatory approvals:
  - UL recognition: 3750 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A
  - VDE certificate of conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 560 V peak

APPLICATIONS

- General-purpose multichannel isolation
- SPI interface/data converter isolation
- Industrial field bus isolation

GENERAL DESCRIPTION

The ADuM3480/ADuM3481/ADuM3482[1] are quad-channel digital isolators based on the Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices and other integrated couplers. With typical propagation delay reduced to 25 ns, pulse width distortion is also halved.

The four channels of the ADuM3480/ADuM3481/ADuM3482 are available in a variety of channel configurations with two data rate grades up to 25 Mbps (see the Ordering Guide section). All models use separate core and I/O power supplies. The core operates between 3.0 V and 5.5 V, whereas the I/O supply can range from 1.8 V to 5.5 V. If I/O operation is required within the range of the core supply, the two supplies can be tied together to allow single-supply operation. When the I/O must interface with logic levels that are different from the core supply voltage, the I/O supply operates independently of the core supply over its wider range. The minimum I/O supply voltage is 1.8 V, which allows compatibility with low voltage logic. Both core and I/O supplies are required for proper operation.

FUNCTIONAL BLOCK DIAGRAMS

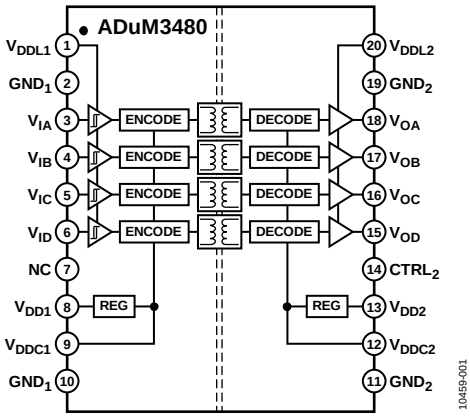

Figure 1. ADuM3480

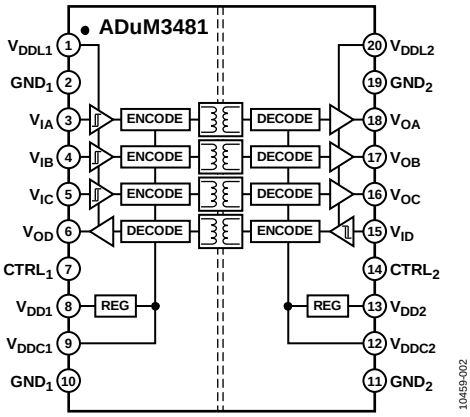

Figure 2. ADuM3481

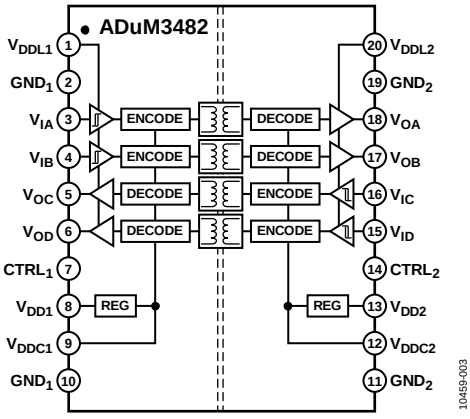

Figure 3. ADuM3482

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

Rev. A
Document Feedback

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Changes to Ordering Guide ... 20

7/12—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DDL1} = V_{DD1} = V_{DDL2} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DDL1}, V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DDL2}, V_{DD2} ≤ 5.5 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF, and CMOS signal levels, unless otherwise noted.

Table 1.

		A Grade			B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS									
Pulse Width	PW	1000			40			ns	Within PWD limit
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		65	90		25	33	ns	50% input to 50% output
Pulse Width Distortion	PWD			6			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			7			3		ps/°C	
Propagation Delay Skew	t_{PSK}			50			17	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			19			5	ns	
Opposing Direction	t_{PSKOD}			25			7	ns	
Jitter			2			2		ns	

Table 2.

		1 Mbps—A, B Grades			25 Mbps—B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT									
ADuM3480	I_{DD1}		2.0	2.9		8.6	12	mA	
	I_{DDL1}		0.11	0.4		0.2	0.6	mA	
	I_{DD2}		5.1	6.9		6.0	7.5	mA	
	I_{DDL2}		0.2	0.7		2.1	4.8	mA	C_L = 0 pF
ADuM3481	I_{DD1}		2.8	3.0		7.9	10	mA	
	I_{DDL1}		0.14	0.5		0.7	1.4	mA	C_L = 0 pF
	I_{DD2}		4.3	5.7		6.7	7.8	mA	
	I_{DDL2}		0.18	0.6		1.6	3.2	mA	C_L = 0 pF
ADuM3482	I_{DD1}		3.5	4.1		7.3	8.8	mA	
	I_{DDL1}		0.16	0.5		1.2	2.4	mA	C_L = 0 pF
	I_{DD2}		3.5	4.7		7.3	8.8	mA	
	I_{DDL2}		0.16	0.65		1.2	2.4	mA	C_L = 0 pF

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Voltage Threshold						
Logic High	V_{IH}	0.7 V_{DDLx}			V	
Logic Low	V_{IL}			0.3 V_{DDLx}	V	
Output Voltages						
Logic High	V_{OH}	V_{DDLx} − 0.1	5.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDLx} − 0.4	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDLx}, 0 V ≤ V_{CTRLx} ≤ V_{DDLx}
Supply Current per Channel						
Quiescent Supply Current						
Regulator Input Side	$I_{DDI (Q)}$		0.50	0.60	mA	
I/O Input	$I_{DDIL (Q)}$		0.027	0.05	mA	
Regulator Output Side	$I_{DDO (Q)}$		1.26	1.7	mA	
I/O Output	$I_{DDOL (Q)}$		0.031	0.10	mA	
Dynamic Supply Current						
Regulator Input Side	$I_{DDI (D)}$		0.070		mA/Mbps	
I/O Input	$I_{DDIL (D)}$		0.90		µA/Mbps	
Regulator Output Side	$I_{DDO (D)}$		0.010		mA/Mbps	
I/O Output	$I_{DDOL (D)}$		0.020		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDLx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Period	t_r		1.66		µs	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{OL} < 0.8 × V_{DDLx} or V_{OH} > 0.7 × V_{DDIx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DDL1} = V_{DD1} = V_{DDL2} = V_{DD2} = 3.0 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DDL1},V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DDL2}, V_{DD2} ≤ 3.6 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 4.

		A Grade			B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS									
Pulse Width	PW	1000			40			ns	Within PWD limit
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		71	99		28	38	ns	50% input to 50% output
Pulse Width Distortion	PWD		2	12		3	5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			7			3		ps/°C	
Propagation Delay Skew	t_{PSK}			58			20	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			20			6	ns	
Opposing Direction	t_{PSKOD}			26			9	ns	
Jitter			4			3		ns	

Table 5.

		1 Mbps—A, B Grades			25 Mbps—B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT									
ADuM3480	I_{DD1}		1.4	2.9		8.1	11	mA	
	I_{DDL1}		0.08	0.4		0.13	0.5	mA	
	I_{DD2}		4.9	6.7		5.8	7.2	mA	
	I_{DDL2}		0.14	0.40		1.4	2.5	mA	C_L = 0 pF
ADuM3481	I_{DD1}		2.3	3.0		7.5	9.8	mA	
	I_{DDL1}		0.09	0.4		0.46	1.4	mA	C_L = 0 pF
	I_{DD2}		4.0	5.7		6.4	7.5	mA	
	I_{DDL2}		0.12	0.5		1.1	2.7	mA	C_L = 0 pF
ADuM3482	I_{DD1}		3.2	4.2		7.0	8.8	mA	
	I_{DDL1}		0.11	0.5		0.78	1.7	mA	C_L = 0 pF
	I_{DD2}		3.2	4.2		7.0	8.8	mA	
	I_{DDL2}		0.11	0. 5		0.78	1.7	mA	C_L = 0 pF

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Voltage Threshold						
Logic High	V_{IH}	0.7 V_{DDLx}			V	
Logic Low	V_{IL}			0.3 V_{DDLx}	V	
Output Voltages						
Logic High	V_{OH}	V_{DDLx} − 0.1	3.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDLx} − 0.4	2.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDLx}, 0 V ≤ V_{CTRLx} ≤ V_{DDLx}
Supply Current per Channel						
Quiescent Supply Current						
Regulator Input Side	$I_{DDI (Q)}$		0.36	0.5	mA	
I/O Input	$I_{DDIL (Q)}$		0.019	0.050	mA	
Regulator Output Side	$I_{DDO (Q)}$		1.21	1.7	mA	
I/O Output	$I_{DDOL (Q)}$		0.021	0.050	mA	
Dynamic Supply Current						
Regulator Input Side	$I_{DDI (D)}$		0.070		mA/Mbps	
I/O Input	$I_{DDIL (D)}$		0.53		µA/Mbps	
Regulator Output Side	$I_{DDO (D)}$		0.010		mA/Mbps	
I/O Output	$I_{DDOL (D)}$		0.013		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		3		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDLx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Period	t_r		1.66		µs	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{OL} < 0.8 × V_{DDLx} or V_{OH} > 0.7 × V_{DDIx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—1.8 V OPERATION

All typical specifications are at T_A = 25°C, V_{DDL1} = 1.8 V, V_{DD1} = 3.0 V, V_{DDL2} = 1.8 V, V_{DD2} = 3.0 V. Minimum/maximum specifications apply over the entire recommended operation range: V_{DDL1} = 1.8 V, 3.0 V ≤ V_{DD1} ≤ 3.6 V, V_{DDL2} = 1.8 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V,−40°C ≤ T_A ≤ +125°C; unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 7.

		A Grade			B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS									
Pulse Width	PW	1000			40			ns	Within PWD limit
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		86	145		43	85	ns	50% input to 50% output
Pulse Width Distortion	PWD		6	32		6	30	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			7			3		ps/°C	
Propagation Delay Skew	t_{PSK}			93			60	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			40			34	ns	
Opposing Direction	t_{PSKOD}			55			37	ns	
Jitter			4			3		ns	

Table 8.

		1 Mbps—A, B Grades			25 Mbps—B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT									
ADuM3480	I_{DD1}		1.4	1.9		8.1	11	mA	
	I_{DDL1}		0.04	0.3		0.07	0.4	mA	
	I_{DD2}		4.7	6.5		5.7	7.3	mA	
	I_{DDL2}		0.08	0.5		0.82	1.5	mA	C_L = 0 pF
ADuM3481	I_{DD1}		2.3	2.8		7.5	10	mA	
	I_{DDL1}		0.05	0.35		0.25	0.7	mA	C_L = 0 pF
	I_{DD2}		3.9	5.7		6.3	8.0	mA	
	I_{DDL2}		0.07	0.4		0.63	1.3	mA	C_L = 0 pF
ADuM3482	I_{DD1}		3.1	3.8		6.9	8.7	mA	
	I_{DDL1}		0.06	0.4		0.44	1.1	mA	C_L = 0 pF
	I_{DD2}		3.1	4.5		6.9	8.8	mA	
	I_{DDL2}		0.06	0.40		0.44	1.1	mA	C_L = 0 pF

Table 9.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Voltage Threshold						
Logic High	V_{IH}	0.7 V_{DDLx}			V	
Logic Low	V_{IL}			0.3 V_{DDLx}	V	
Output Voltages						
Logic High	V_{OH}	V_{DDLx} − 0.1	1.8		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDLx} − 0.4	1.6		V	I_{Ox} = −2 mA, V_{Ix} = V_{IxH}
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDLx}, 0 V ≤ V_{CTRLx} ≤ V_{DDLx}
Supply Current per Channel						
Quiescent Supply Current						
Regulator Input Side	$I_{DDI (Q)}$		0.39	0.45	mA	
I/O Input	$I_{DDIL (Q)}$		0.010	0.025	mA	
Regulator Output Side	$I_{DDO (Q)}$		1.17	1.5	mA	
I/O Output	$I_{DDOL (Q)}$		0.012	0.038	mA	
Dynamic Supply Current						
Regulator Input Side	$I_{DDI (D)}$		0.071		mA/Mbps	
I/O Input	$I_{DDIL (D)}$		0.25		μA/Mbps	
Regulator Output Side	$I_{DDO (D)}$		0.010		mA/Mbps	
I/O Output	$I_{DDOL (D)}$		0.0077		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		3		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDLx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Period	t_r		1.66		μs	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{OL} < 0.8 × V_{DDLx} or V_{OH} > 0.7 × V_{DDIx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 10.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Case Thermal Resistance	θ_{JC}		50.5		°C/W	Thermocouple located at center of package underside, test conducted on 4-layer board with thin traces

[1] The device is considered a 2-terminal device: Pin 1 to Pin 10 are shorted together; Pin 11 to Pin 20 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM3480/ADuM3481/ADuM3482 are approved by the organizations listed in Table 11. See Table 16 and the Insulation Lifetime section for the recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

REGULATORY APPROVALS

Table 11.

UL	CSA	VDE
Recognized under the UL 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single protection, 3750 V rms isolation voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM3480/ADuM3481/ADuM3482 is proof tested by applying an insulation test voltage of ≥4500 V rms for 1 second (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10, each of the ADuM348x is proof tested by applying an insulation test voltage of ≥1050 V peak for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 12.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3750	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	>5.1	mm	Measured from input terminals to output terminals, shortest distance through air, in the plane of the PCB
Minimum External Tracking (Creepage)	L(I02)	>5.1	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on packages denotes DIN V VDE V 0884-10 approval.

Table 13.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V_{PEAK}
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m =$ 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1050	V_{PEAK}
Input-to-Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	840	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	672	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	4000	V_{PEAK}
Withstand Isolation Voltage	1 minute withstand rating	V_{ISO}	3750	V_{RMS}
Surge Isolation Voltage	V_{PEAK} = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Case Temperature		T_S	150	°C
Total Power Dissipation		I_{S1}	2.47	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

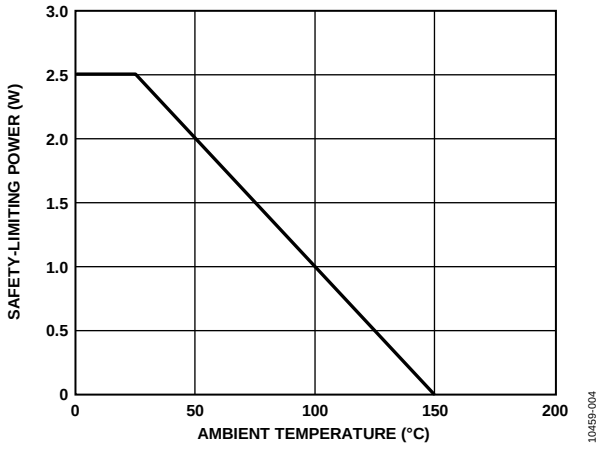


Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 14.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+125	°C
Supply Voltages[1]	V_{DDL1}, V_{DDL2}	1.8	5.5	V
	V_{DD1}, V_{DD2}	3.0	5.5	V
Input Signal Rise and Fall Times			1.0	ms

[1] See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 15.

Parameter	Rating
Supply Voltages (V_{DD1}, V_{DD2}, V_{DDL1}, V_{DDL2}, V_{DDC1}, V_{DDC2})	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{CTRL1}, V_{CTRL2})	−0.5 V to V_{DDI} + 0.5 V
Output Voltages (V_{OA}, V_{OB}, V_{OC}, V_{OD})	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[1]	−10 mA to +10 mA
Common-Mode Transients[2]	−100 kV/µs to +100 kV/µs
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C

[1] See Figure 4 for maximum rated current values for various temperatures.
[2] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 16. Maximum Continuous Working Voltage Supporting 50-Year Minimum Lifetime[1]

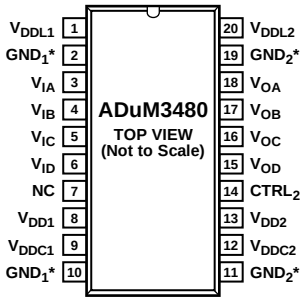
Parameter	Max	Unit	Applicable Certification
AC Voltage, Bipolar Waveform	565	V peak	All certifications
AC Voltage, Unipolar Waveform	848	V peak	
DC Voltage	848	V peak	

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECTION. THIS PIN IS NOT CONNECTED INTERNALLY AND CAN BE LEFT FLOATING OR CONNECTED TO V_{DD1} OR GND_1.

*PIN 2 AND PIN 10 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO PCB SIDE 1 GROUND IS RECOMMENDED. PIN 11 AND PIN 19 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO PCB SIDE 2 GROUND IS RECOMMENDED.

10459-005

Figure 5. ADuM3480 Pin Configuration

Table 17. ADuM3480 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DDL1}	1.8 V to 5.5 V Supply Voltage for Isolator Side 1 Input/Output Circuits. Bypass V_{DDL1} to GND_1 with a 0.01 µF to 0.1 µF ceramic capacitor. For 3.0 V to 5.5 V input/output operation, V_{DDL1} can be connected directly to V_{DD1}.
2	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both to the PCB ground plane as close to the part as possible is recommended.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{ID}	Logic Input D.
7	NC	No Connection. This pin is not connected internally and can be left floating or connected to V_{DD1} or GND_1.
8	V_{DD1}	3.0 V to 5.5 V Supply Voltage for Isolator Side 1.
9	V_{DDC1}	Output Pin of an Internal Regulator for Side 1. Bypass V_{DDC1} to GND_1 with a 0.01 µF to 0.1 µF ceramic capacitor. Do not use this pin to power external circuits.
10	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both to the PCB ground plane as close to the part as possible is recommended.
11	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both to the PCB ground plane as close to the part as possible is recommended.
12	V_{DDC2}	Output Pin of an Internal Regulator for Side 2. Bypass V_{DDC2} to GND_2 with a 0.01 µF to 0.1 µF ceramic capacitor. Do not use this pin to power external circuits.
13	V_{DD2}	3.0 V to 5.5 V Supply Voltage for Isolator Side 2.
14	$CTRL_2$	Select Side 2 Output Default Level. Low = default output low. High = default output high.
15	V_{OD}	Logic Output D.
16	V_{OC}	Logic Output C.
17	V_{OB}	Logic Output B.
18	V_{OA}	Logic Output A.
19	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both to the PCB ground plane as close to the part as possible is recommended.
20	V_{DDL2}	1.8 V to 5.5 V Supply Voltage for Isolator Side 2 Input/Output Circuits. Bypass V_{DDL2} to GND_2 with a 0.01 µF to 0.1 µF ceramic capacitor. For 3.0 V to 5.5 V input/output operation, V_{DDL2} can be connected directly to V_{DD2}.

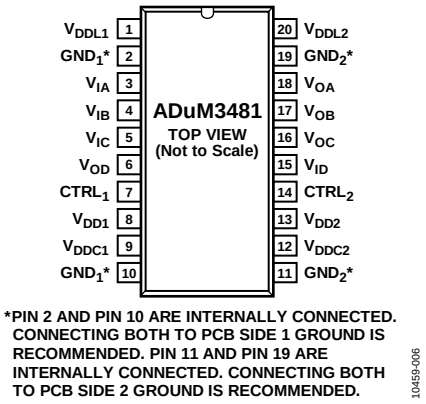


Figure 6. ADuM3481 Pin Configuration

Table 18. ADuM3481 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DDL1}	1.8 V to 5.5 V Supply Voltage for Isolator Side 1 Input/Output Circuits. Bypass V_{DDL1} to GND_1 with a 0.01 µF to 0.1 µF ceramic capacitor. For 3.0 V to 5.5 V input/output operation, V_{DDL1} can be connected directly to V_{DD1}.
2	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both to the PCB ground plane as close to the part as possible is recommended.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{OD}	Logic Output D.
7	$CTRL_1$	Select Side 1 Output Default Level. Low = default output low. High = default output high.
8	V_{DD1}	3.0 V to 5.5 V Supply Voltage for Isolator Side 1.
9	V_{DDC1}	Output Pin of an Internal Regulator for Side 1. Bypass V_{DDC1} to GND_1 with a 0.01 µF to 0.1 µF ceramic capacitor. Do not use this pin to power external circuits.
10	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both to the PCB ground plane as close to the part as possible is recommended.
11	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both to the PCB ground plane as close to the part as possible is recommended.
12	V_{DDC2}	Output Pin of an Internal Regulator for Side 2. Bypass V_{DDC2} to GND_2 with a 0.01 µF to 0.1 µF ceramic capacitor. Do not use this pin to power external circuits.
13	V_{DD2}	3.0 V to 5.5 V Supply Voltage for Isolator Side 2.
14	$CTRL_2$	Select Side 2 Output Default Level. Low = default output low. High = default output high.
15	V_{ID}	Logic Input D.
16	V_{OC}	Logic Output C.
17	V_{OB}	Logic Output B.
18	V_{OA}	Logic Output A.
19	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both to the PCB ground plane as close to the part as possible is recommended.
20	V_{DDL2}	1.8 V to 5.5 V Supply Voltage for Isolator Side 2 Input/Output Circuits. Bypass V_{DDL2} to GND_2 with a 0.01 µF to 0.1 µF ceramic capacitor. For 3.0 V to 5.5 V input/output operation, V_{DDL2} can be connected directly to V_{DD2}.

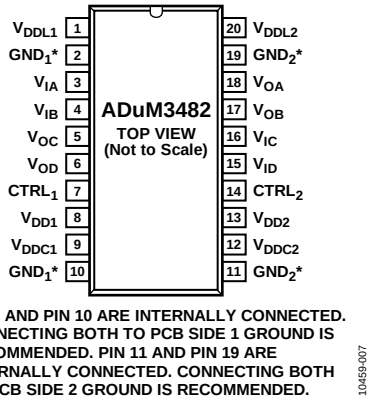


Figure 7. ADuM3482 Pin Configuration

Table 19. ADuM3482 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DDL1}	1.8 V to 5.5 V Supply Voltage for Isolator Side 1 Input/Output Circuits. Bypass V_{DDL1} to GND_1 with a 0.01 µF to 0.1 µF ceramic capacitor. For 3.0 V to 5.5 V input/output operation, V_{DDL1} can be connected directly to V_{DD1}.
2	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both to the PCB ground plane as close to the part as possible is recommended.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{OC}	Logic Output C.
6	V_{OD}	Logic Output D.
7	$CTRL_1$	Select Side 1 Output Default Level. Low = default output low. High = default output high.
8	V_{DD1}	3.0 V to 5.5 V Supply Voltage for Isolator Side 1.
9	V_{DDC1}	Output Pin of Internal Regulator for Side 1. Bypass V_{DDC1} to GND_1 with a 0.01 µF to 0.1 µF ceramic capacitor. Do not use this pin to power external circuits.
10	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both to the PCB ground plane as close to the part as possible is recommended.
11	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both to the PCB ground plane as close to the part as possible is recommended.
12	V_{DDC2}	Output Pin of Internal Regulator for Side 2. Bypass V_{DDC2} to GND_2 with a 0.01 µF to 0.1 µF ceramic capacitor. Do not use this pin to power external circuits.
13	V_{DD2}	3.0 V to 5.5 V Supply Voltage for Isolator Side 2.
14	$CTRL_2$	Select Side 2 Output Default Level. Low = default output low. High = default output high.
15	V_{ID}	Logic Input D.
16	V_{IC}	Logic Input C.
17	V_{OB}	Logic Output B.
18	V_{OA}	Logic Output A.
19	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both to the PCB ground plane as close to the part as possible is recommended.
20	V_{DDL2}	1.8 V to 5.5 V Supply Voltage for Isolator Side 2 Input/Output Circuits. Bypass V_{DDL2} to GND_2 with a 0.01 µF to 0.1 µF ceramic capacitor. For 3.0 V to 5.5 V input/output operation, V_{DDL2} can be connected directly to V_{DD2}.

TYPICAL PERFORMANCE CHARACTERISTICS

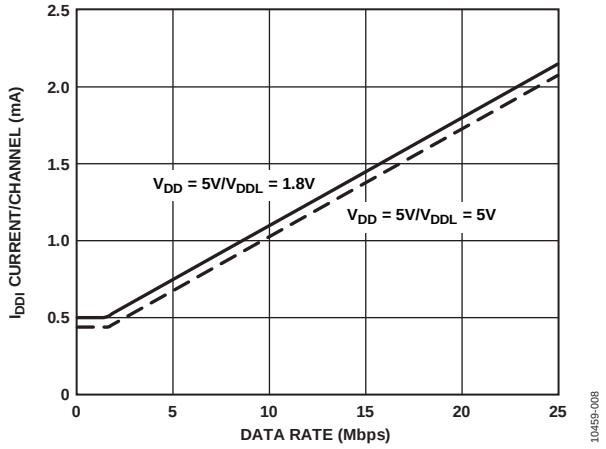


Figure 8. Typical V_{DDI} = 5 V Supply Current per Input Channel vs. Data Rate for 5 V and 1.8 V I/O Operation

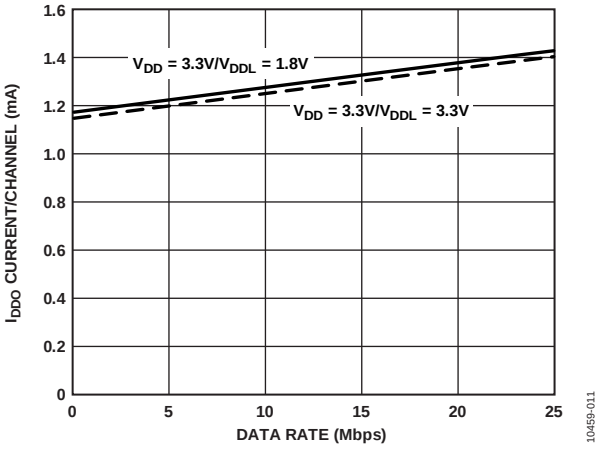


Figure 11. Typical V_{DDO} = 3.3 V Supply Current per Output Channel vs. Data Rate for 3.3 V and 1.8 V I/O Operation

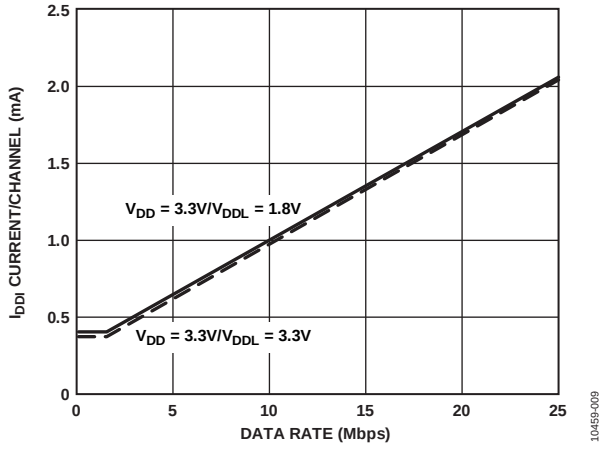


Figure 9. Typical V_{DDI} = 3.3 V Supply Current per Input Channel vs. Data Rate for 3.3 V, and 1.8 V I/O Operation

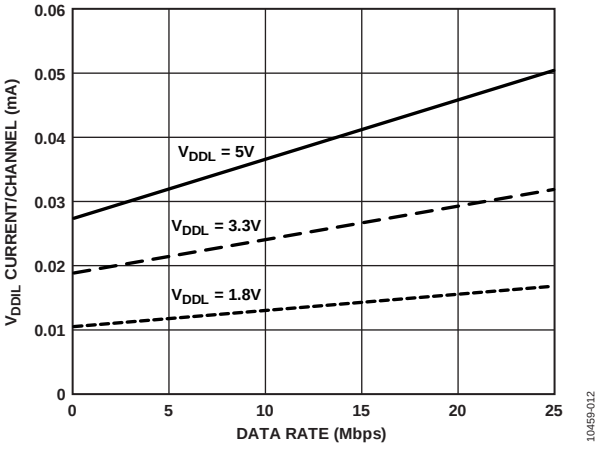


Figure 12. Typical V_{DDIL} Input Supply Current vs. Data Rate for 5 V, 3.3 V, and 1.8 V Operation

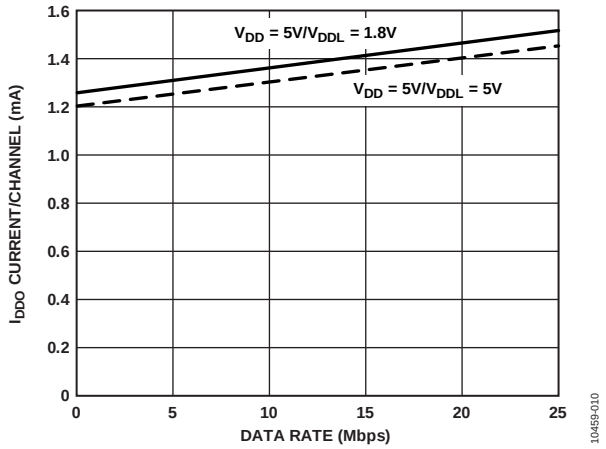


Figure 10. Typical V_{DDO} = 5 V Supply Current per Output Channel vs. Data Rate for 5 V and 1.8 V I/O Operation

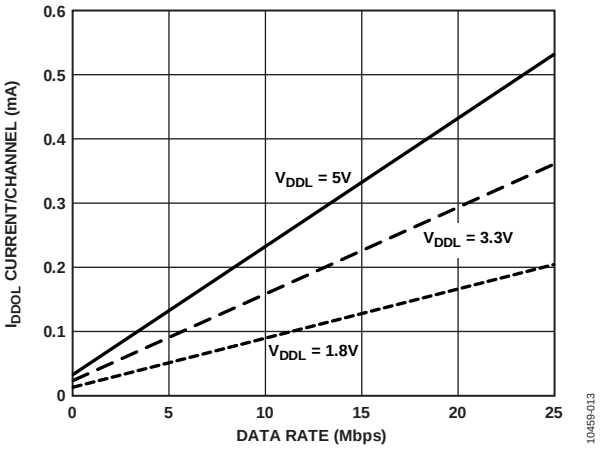


Figure 13. Typical V_{DDOL} Output Supply Current vs. Data Rate for 5 V, 3.3 V, and 1.8 V, C_L = 0 pF Operation

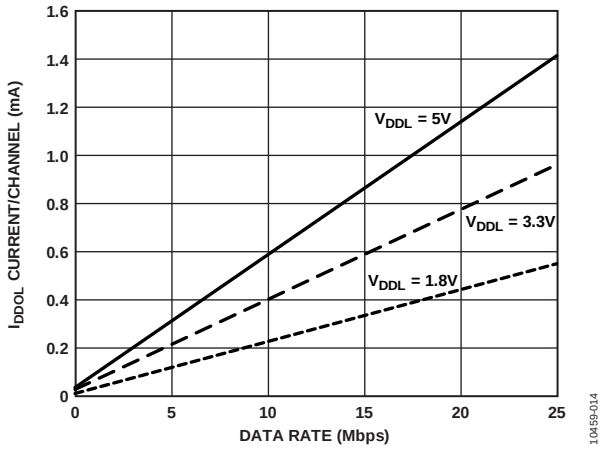


Figure 14. Typical V_{DDOL} Output Supply Current vs. Data Rate for 5 V, 3.3 V, and 1.8 V, C_L = 15 pF Operation

APPLICATIONS INFORMATION

SUPPLY VOLTAGES

The ADuM3480/ADuM3481/ADuM3482 devices are built around a fixed voltage internal data transfer core. The core voltage is 2.7 V, which is generated by regulating the V_{DD1} and V_{DD2} voltages with an internal LDO. To ensure proper headroom for the LDO, the V_{DD1} and V_{DD2} inputs must be in the 3.0 V to 5.5 V range. Additional pins, V_{DDC1} and V_{DDC2}, are provided for direct bypass of the LDO output, ensuring clean stable core operation. Bypass capacitors to ground of between 0.01 µF and 0.1 µF are required for each of these supply or dedicated bypass pins.

The ADuM3480/ADuM3481/ADuM3482 provide independent supplies for the I/O buffers, V_{DDL1} and V_{DDL2}, which have wider operating ranges than that required for the core. This allows the I/O supply voltage to range between 1.8 V and 5.5 V. The V_{DDLx} supplies must also be bypassed with between 0.01 µF and 0.1 µF capacitors.

Having independent power supplies for the I/O and core allows several power configurations depending on the I/O voltage required and the available power supply rails. If one power supply is available, the V_{DDx} and V_{DDLx} pins can be connected together and operate between 3.0 V and 5.5 V. If lower I/O supply voltage is required, to interface with low voltage logic, two supply rails are required. For example, if the I/O is 1.8 V logic, the V_{DDLx} pin can be connected to a 1.8 V supply rail. The core supply voltage for V_{DDx} requires an input of between 3.0 V and 5.5 V, so an available 3.3 V or 5 V supply rail can be used. The I/O and core supply voltage on each side are independent and different configurations can be used on each side of the device.

PRINTED CIRCUIT BOARD LAYOUT

The ADuM3480/ADuM3481/ADuM3482 digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing to the local ground is required at all four power supply pins, V_{DD1}, V_{DDL1}, V_{DD2}, and V_{DDL2}, as well as at the two internal regulator bypass pins: V_{DDC1} and V_{DDC2} (see Figure 15). Placement of the recommended bypass capacitors is shown in Figure 15. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

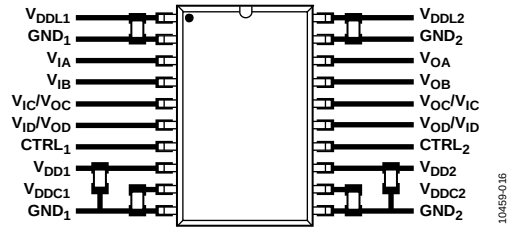


Figure 15. Recommended Printed Circuit Board (PCB) Layout

In applications involving high common-mode transients, it is important to minimize board coupling across the isolation barrier. Furthermore, design the board layout so that any coupling that does occur equally affects all pins on a given component side. Failure to follow this design guideline can allow voltage differentials between pins that exceed the absolute maximum ratings of the device during high voltage transients, which can lead to latch-up or permanent damage.

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The input-to-output propagation delay time for a high to low transition may differ from the propagation delay time of a low to high transition.

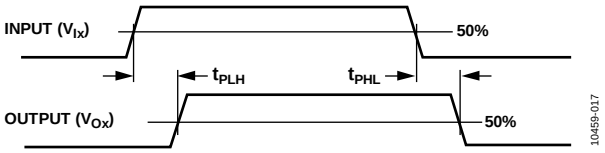


Figure 16. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and an indication of how accurately the timing of the input signal is preserved.

Channel to channel matching refers to the maximum amount of time that the propagation delay differs between channels within a single ADuM3480/ADuM3481/ADuM3482 component.

Propagation delay skew refers to the maximum amount of time that the propagation delay differs between multiple ADuM3480/ADuM3481/ADuM3482 components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and is, therefore, either set or reset by the pulses indicating input logic transitions. In the absence of logic transitions at the input for more than ~1.7 µs, the current dc state is sent to the output to ensure dc correctness at the output.

If the decoder receives no pulses for more than about 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 17, Table 18, or Table 19) by the watchdog timer circuit.

The limitation on the magnetic field immunity of the device is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to either falsely set or reset the decoder. The following analysis defines such conditions. The ADuM3480/ADuM3481/ADuM3482 are examined in a 3 V operating condition because it represents the most susceptible mode of operation of these products.

The pulses at the transformer output have an amplitude of greater than 1.5 V. The decoder has a sensing threshold of approximately = 1.0 V, thereby establishing a 0.5 V margin within which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta / dt)\Sigma\pi r_n^2; n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density.
r_n is the radius of the nth turn in the receiving coil.
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM3480/ADuM3481/ADuM3482 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 17.

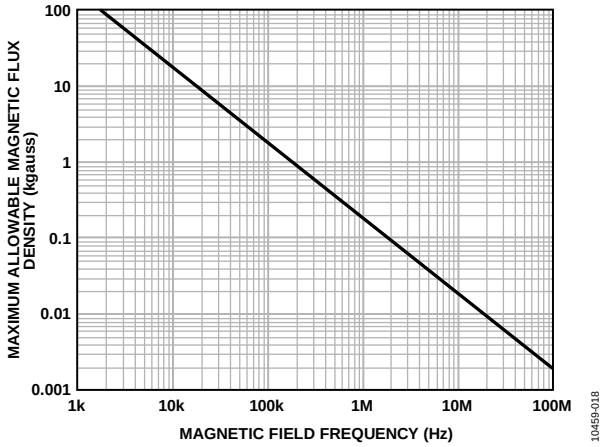


Figure 17. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.5 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. If such an event occurs, with the worst-case polarity, during a transmitted pulse, it reduces the received pulse from >1.0 V to 0.75 V. This is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM3480/ADuM3481/ADuM3482 transformers. Figure 18 expresses these allowable current magnitudes as a function of frequency for selected distances. The ADuM3480/ADuM3481/ADuM3482 are very insensitive to external fields. Only extremely large, high frequency currents that are very close to the component are a concern. For the 1 MHz example noted, a 1.2 kA current would need to be placed 5 mm away from the ADuM3480/ADuM3481/ADuM3482 to affect component operation.

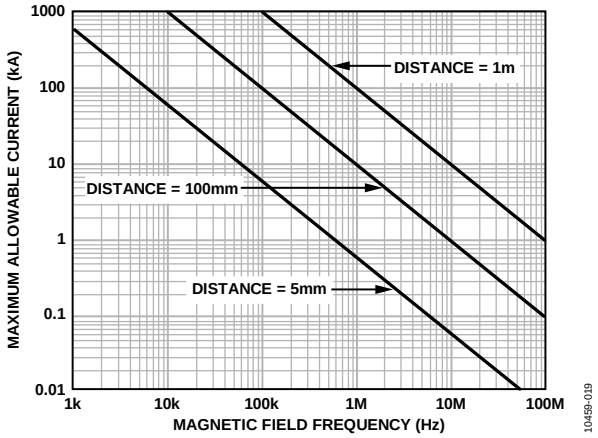


Figure 18. Maximum Allowable Current for Various Current to ADuM3480 Spacings

Note that at combinations of strong magnetic field and high frequency, or any loops formed by PCB traces, can induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Take care to avoid PCB structures that form loops.

POWER CONSUMPTION

The supply current at a given channel of the ADuM3480/ADuM3481/ADuM3482 isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

Calculating I_{DD1} or I_{DD2}

For each input channel, assuming worst case I/O voltage, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad R_D \leq 2.5 \times R_R$$

$$I_{DDI} = I_{DDI\,(D)} \times (R_D - R_R) + I_{DDI\,(Q)} \qquad R_D > 2.5 \times R_R$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(D)} \times R_D + I_{DDO\,(Q)}$$

Calculating I_{DDL1} or I_{DDL2}

For each input channel, the supply current is given by

$$I_{DDIL} = I_{DDIL(D)} \times R_D + I_{DDIL(Q)}$$

For each output channel, the supply current is given by

$$I_{DDOL} = \left(I_{DDOL(D)} + \frac{C_L \times V_{DDOL} \times 10^{-3}}{2} \right) R_D + I_{DDOL(Q)}$$

where:
C_L is the output load capacitance (pF).
V_{DDOL} is the output supply voltage (V).
R_D is the input logic signal data rate (Mbps); it is twice the input frequency, expressed in units of MHz.
R_R is the input stage refresh rate (Mbps) = 1/t_r (μs)
$I_{DDI(Q)}$, $I_{DDIL(Q)}$, $I_{DDO(Q)}$, $I_{DDOL(Q)}$ are the specified input and output quiescent supply currents (mA).
$I_{DDI(D)}$, $I_{DDIL(D)}$, $I_{DDO(D)}$, and $I_{DDOL(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

As inputs and outputs can be present on each side of the device, the calculations refer to the current drawn from the local supply. For example, if an output is on Side 2 of a part, the I_{DDOL} current is drawn from the V_{DDL2} pin of the part. The I_{DDL1} and I_{DDL2} currents are dependent on V_{DDL1} and V_{DDL2}, the data rate, and the capacitive load. It is nearly independent of the value of the core supplies.

To calculate the total I_{DD1}, I_{DDL1}, I_{DD2}, and I_{DDL2} supply current, the supply currents for each input and output channel corresponding to V_{DD1}, V_{DDL1}, V_{DD2}, and V_{DDL2} are calculated and totaled, or read from Figure 8 through Figure 14.

The input current for the regulated core power supplies is nearly independent of the I/O voltage, and scales with data rate. The I_{DDI} current is not linear down to dc, but goes to a minimum value between about 2.5 × R_R and dc. This is due to the refresh circuit establishing a minimum data rate; the values in Figure 8 and Figure 9 and the quiescent currents in Table 3, Table 6, and Table 9 approximate the current in this region. V_{DDI}, V_{DDO}, V_{DDIL}, and V_{DDOL} represent the voltages on the core and I/O power supply pins for the input and output of a given channel. I represents an input, O is an output, and L denotes an I/O supply.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation depends on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM3480/ADuM3481/ADuM3482.

Analog Devices performs accelerated life testing using voltage levels that are higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 16 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM3480/ADuM3481/ADuM3482 depends on the voltage waveform type imposed across the isolation barrier. The iCoupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 19, Figure 20,and Figure 21 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the maximum working voltage recommended by Analog Devices.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 16 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage case. Treat any cross-insulation voltage waveform that does not conform to Figure 19, Figure 20, or Figure 21 as a bipolar ac waveform, and limit its peak voltage to the 50-year lifetime voltage value listed in Table 16.

Note that the voltage presented in Figure 20 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

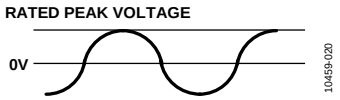


Figure 19. Bipolar AC Waveform

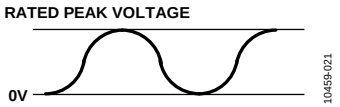


Figure 20. Unipolar AC Waveform

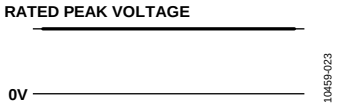


Figure 21. DC Waveform