Data Sheet

ADuM4195-1

Isolated Amplifier with Fixed Gain and Single-Ended Output

FEATURES

- Wide input/output range 0.25 V to 4.3 V (typ)
- High-impedance input for isolated voltage measurement
- Fixed gain = 1
- Low offset error and drift: ±5 mV (max) at 25°C and −22 µV/°C (typ)
- Low gain error and drift: ±0.5% (max) and ±42 ppm/°C (max)
- Voltage-supply range
  - V_{DD1}: 4.5 V to 5.5 V
  - V_{DD2}: 4.5 V to 5.5 V
- Bandwidth: 210 kHz
- Isolation voltage: 5000 V rms
- Safety and regulatory approvals (pending)
  - UL recognition: 5000 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A
  - VDE certificate of conformity
  - DIN V VDE V 0884-11 (VDE V 0884-11)
  - V_{IORM} = 1401 V peak
- Wide temperature range
  - −40°C to +125°C ambient operation
  - 150°C maximum junction temperature
- AEC-Q100 qualified for automotive applications

APPLICATIONS

- Inverters
- DC-DC converter
- On-board chargers

GENERAL DESCRIPTION

The ADuM4195-1[1] is an isolation amplifier based on Analog Devices, Inc., *i*Coupler® technology. The ADuM4195-1 has very low offset and gain error, making it ideal for many isolated voltage sensing applications.

Unlike optocoupler-based solutions, which have an uncertain current transfer ratio over a lifetime and is unstable at high temperatures, the ADuM4195-1 transfer function does not change over its lifetime, and is stable over a wide temperature range of −40°C to +125°C.

The ADuM4195-1 has been certified to provide galvanic isolation up to 5 kV rms according to UL1577.

The ADuM4195-1 is packaged in a small 8-lead wide body SOIC package with increased creepage.

FUNCTIONAL BLOCK DIAGRAM

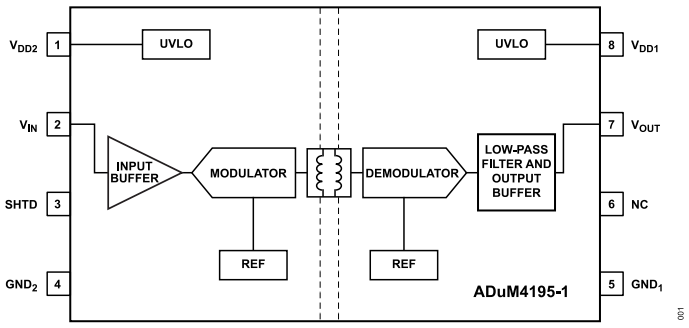

Figure 1.

[1] Protected by U.S. Patents 5,952,849, 6,873,065, and 7,075,329. Other patents are pending.

TABLE OF CONTENTS

REVISION HISTORY

5/2023—Rev. 0 to Rev. A

Changed V RMS to V rms (Throughout) ... 1
Changes to Features Section ... 1
Changes to Input-Bias Current Parameter and Note 1 to Note 4, Table 1 ... 3
Changes to Table 10 ... 8

1/2023—Revision 0: Initial Version

SPECIFICATIONS

V_{DD1} = V_{DD2} = 4.5 V to 5.5 V for T_A = T_{MIN} to T_{MAX}. All typical specifications are at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V, unless otherwise noted.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Voltage Range	V_{IN} < V_{DD2}	0.0		V_{DD2}	V
Input Resistance			1		GΩ
Input Capacitance			5		pF
Input-Bias Current[1]	V_{IN} = 2.5 V, T_A = 25°C	−0.2		+0.2	nA
Input-Bias Current Drift[1]		15		25	pA/°C
OUTPUT CHARACTERISTICS					
Linear Output Voltage Range[2]		0.25		V_{DD2} − 0.7	V
Output Offset Voltage	V_{OUT} − V_{IN}, T_A = 25°C, V_{IN} = 2.5 V	−5.0		+5.0	mV
Output Offset Drift	V_{IN} = 2.5 V, T_A = −40°C to +125°C		−22		µV/°C
Output Gain[3]			1		
Output Gain Error		−0.5		+0.5	%
Output Gain Drift		−42		+42	ppm/°C
Output −3 dB Bandwidth			210		kHz
Output Delay	50% input to 50% output within V_{IN} = 1 V to 4 V		3		µs
Output Rise and Fall Time	10% to 90% within V_{IN} = 1 V to 4 V		2		µs
Output Noise	Over 100 kHz		540		µV rms
	Over 200 kHz		1		mV rms
Signal-to-Noise Ratio (SNR)	f_{IN} = 1 kHz, bandwidth = 100 kHz		69		dB
	f_{IN} = 1 kHz, bandwidth = 200 kHz		64		dB
Signal-to-Noise and Distortion (SINAD) Ratio	f_{IN} = 1 kHz, bandwidth = 100 kHz		57		dB
	f_{IN} = 1 kHz, bandwidth = 200 kHz		56		dB
Total Harmonic Distortion Plus Noise (THD + N) Ratio	f_{IN} = 1 kHz, bandwidth = 100 kHz		−54		dB
	f_{IN} = 1 kHz, bandwidth = 200 kHz		−56		dB
Power-Supply Rejection Ratio (PSRR)	DC, V_{DD1} = V_{DD2} = 4.5 V to 5.5 V		−60		dB
Output Resistive Load		10			kΩ
Output Capacitive-Load				100	pF
Common-Mode Transient Immunity (CMTI)[1, 4]	CMTI, |GND_1 – GND_2| = 1.5 kV	100	150		kV/µs
POWER SUPPLY					
Side 1 Operating Range	V_{DD1}	4.5	5.0	5.5	V
Undervoltage Lockout (UVLO) Positive Going Threshold			4.2		V
UVLO Negative Going Threshold			4.0		V
Side 2 Operating Range	V_{DD2}	4.5	5.0	5.5	V
UVLO Positive Going Threshold			4.2		V
UVLO Negative Going Threshold			4.0		V
V_{OUT} Impedance	V_{DD1} = 5 V, V_{DD2} < UVLO threshold		35		Ω
	V_{DD1} < UVLO threshold		3.7		kΩ
Supply Current					
I_{DD1}			4.1	4.9	mA
I_{DD2}			5.9	7.3	mA
SHUTDOWN INPUT					
Operating Range		0.0		V_{DD2}	V
V_{SHTD} High		3.0			V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
V_{SHTD} Low				2.2	V

1 Guaranteed by design and characterization. Not production tested.

2 For a maximum deviation of ±1.25% from the best-fit line over the specified input range of 1 V to 3.5 V.

3 Output gain is defined as the slope of the best-fit line over the specified input range, with the offset error adjusted out.

4 CMTI error is an output disturbance greater than 100 mV lasting more than 2 µs.

PACKAGE CHARACTERISTICS

Table 2. Package Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RESISTANCE						
Input-to-Output[1]	R_{I-O}		10^{13}		Ω	
CAPACITANCE						
Input-to-Output[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	

1 The device is considered a 2-terminal device; Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

2 Input capacitance is from any input pin to ground.

REGULATORY INFORMATION (PENDING)

Table 3. Regulatory Information (Pending)

UL	CSA[1]	VDE[2]
Recognized Under 1577 Component Recognition Program[3]	Approved under CSA Component Acceptance Notice #5A Basic insulation per CSA 62638-1-03 and IEC 62638-1, 600 V rms (849 V_{PEAK}) maximum working voltage	Certified according to DIN V VDE V 0884-11
Single Protection, 5000 V rms Isolation Voltage, 8-Lead SOIC_IC	Reinforced insulation per CSA 62638-1-03 and IEC 62638-1, 900 V rms (1273 V_{PEAK}) maximum working voltage	Reinforced insulation, 1401 V_{PEAK}, V_{IOTM} = 7000 V_{PEAK}, V_{IOSM} = 8000 V_{PEAK}
File E214400	File 205078	

1 Working voltages are quoted for Pollution Degree 2, Material Group III.

2 In accordance with DIN V VDE V 0884-11, each ADuM4195-1 is proof tested by applying an insulation test voltage ≥ 2627 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-11 approval.

3 In accordance with UL 1577, each ADuM4195-1 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec (current leakage detection limit = 5 µA).

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 4. Insulation and Safety Related Specifications

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L (I01)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	8.3	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		0.041	mm min	Insulation distance through insulation

SPECIFICATIONS

Table 4. Insulation and Safety Related Specifications (Continued)

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303, Part 1
Isolation Group		I		Material Group DIN VDE 0110, 1/89, Table 1

RECOMMENDED OPERATING CONDITIONS

Table 5. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
OPERATING TEMPERATURE	T_A	−40	+125	°C
SUPPLY VOLTAGES[1]	V_{DD1}, V_{DD2}	4.5	5.5	V

[1] All voltages are relative to their respective grounds.

DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS (PENDING)

These isolators are suitable for reinforced isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The asterisk (*) marking branded on the package denotes DIN V VDE V 0884-11 approval for a 1273 V_{PEAK} working voltage.

Table 6. DIN V VDE V 0884-11 (VDE V 0884-11) Insulation Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	1401	V_{PEAK}
Input-to-Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{PD\ (M)}$, 100% production test, t_{INI} = t_M = 1 sec, partial discharge < 5 pC	$V_{PD\ (M)}$	2627	V_{PEAK}
Input-to-Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	V_{IORM} × 1.5 = $V_{PD\ (M)}$, t_{INI} = 60 sec, t_M = 10 sec, partial discharge < 5 pC	$V_{PD\ (M)}$	2102	V_{PEAK}
After Input or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{PD\ (M)}$, t_{INI} = 60 sec, t_M = 10 sec, partial discharge < 5 pC	$V_{PD\ (M)}$	1681	V_{PEAK}
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{IOTM}	7000	V_{PEAK}
Withstand Isolation Voltage	1 minute withstand rating	V_{ISO}	5000	V rms
Surge Isolation Voltage	V_{PEAK} = 12.8 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	8000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	1.5	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

SPECIFICATIONS

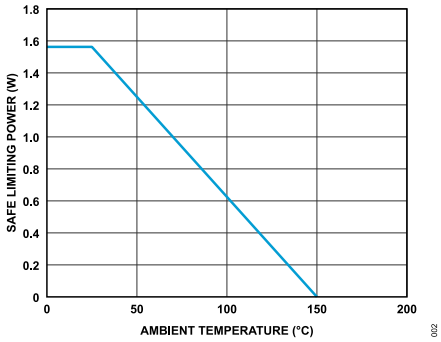

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, Per DIN V VDE V 0884-11

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
Supply Voltages	
V_{DD1}, V_{DD2}[1]	−0.5 V to +7.0 V
Input Voltages	
V_{IN}, SHTD[1]	−0.5 V to V_{DD2} + 0.5 V
Output Voltage	
V_{OUT}[1]	−0.5 V to V_{DD1} + 0.5 V
Output Current per Output Pin	−11 mA to +11 mA
Temperature	
Storage Temperature (T_{ST}) Range	−65°C to +150°C
T_A Operating Range	−40°C to +125°C
T_J Range	−40°C to +150°C
Common-Mode Transients[2]	−200 kV/µs to +200 kV/µs

1 All voltages are relative to their respective grounds.

2 Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latchup or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operation environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 8. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
RI-8-1	83	34	°C/W

1 Thermocouple is located at the center of the package underside.

The maximum continuous working voltage refers to continuous voltage magnitude imposed across the isolation barrier in Pollution Degree 2 environments.

Table 9. Maximum Continuous Working Voltage

Parameter	Rating	Constraint
AC Voltage Bipolar Waveform		
Basic Insulation	991 V rms	Basic insulation rating per IEC 60747-17. Accumulative failure rate over lifetime (FROL) ≤ 1000 ppm at 20 years.
Reinforced Insulation	830 V rms	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment.
DC Voltage Bipolar Waveform		
Basic Insulation	1401 V DC	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment.
Reinforced Insulation	830 V DC	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

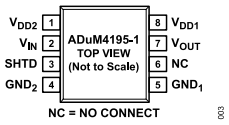

Figure 3. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD2}	Supply Voltage for Side 2 (4.5 V to 5.5 V). Connect a 0.1 µF capacitor and a 1 µF capacitor between V_{DD2} and GND_2.
2	V_{IN}	Operational Amplifier (Op Amp) Buffer Input.
3	SHTD	Shutdown Input, Active-High, with Internal Pull-Down Resistor (Typical Value: 100 kΩ). SHTD must be actively driven or shorted to GND_2. Do not leave SHTD floating.
4	GND_2	Ground Reference for Side 2.
5	GND_1	Ground Reference for Side 1.
6	NC	No Connect. Connect Pin 6 to GND_1 or V_{DD1}. Do not leave Pin 6 floating.
7	V_{OUT}	Analog Output Voltage.
8	V_{DD1}	Supply Voltage for Side 1 (4.5 V to 5.5 V). Connect a 0.1 µF capacitor and a 1 µF capacitor between V_{DD1} and GND_1.

TYPICAL PERFORMANCE CHARACTERISTICS

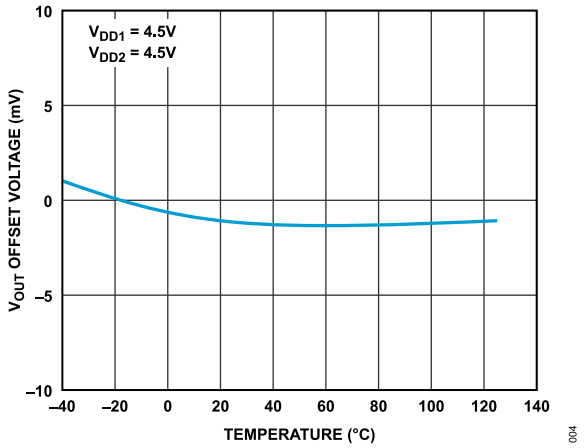

Figure 4. V_{OUT} Offset Voltage vs. Temperature

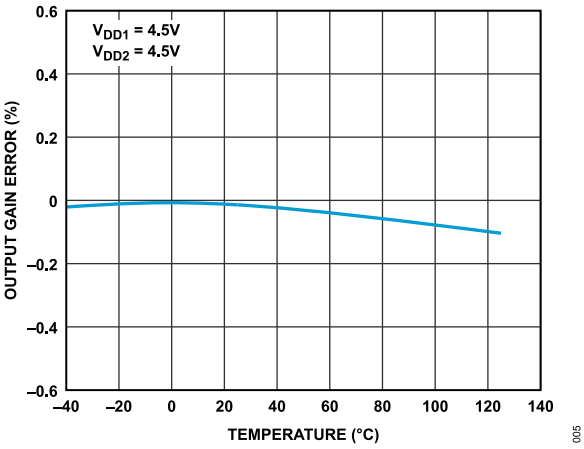

Figure 5. Output Gain Error vs. Temperature

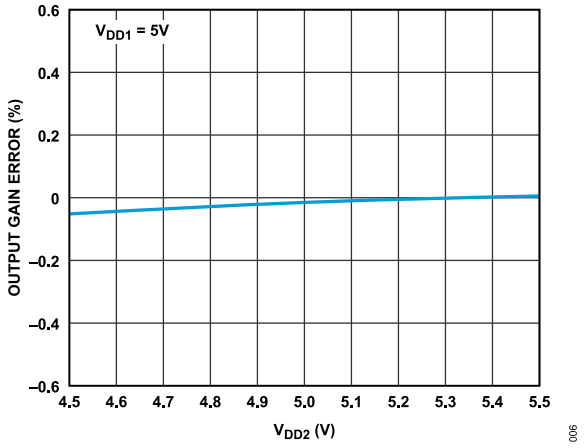

Figure 6. Output Gain Error vs. V_{DD2}

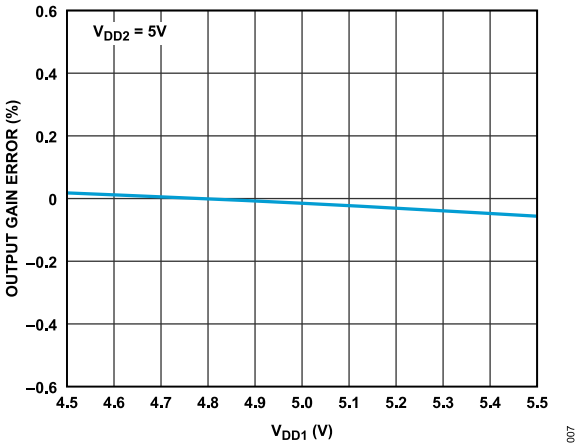

Figure 7. Output Gain Error vs. V_{DD1}

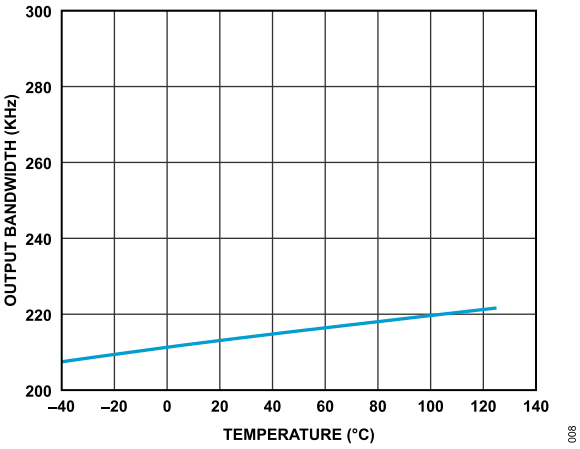

Figure 8. Output Bandwidth vs. Temperature

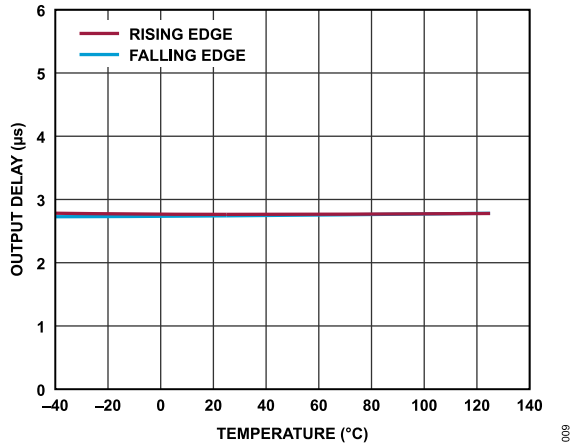

Figure 9. Output Delay vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

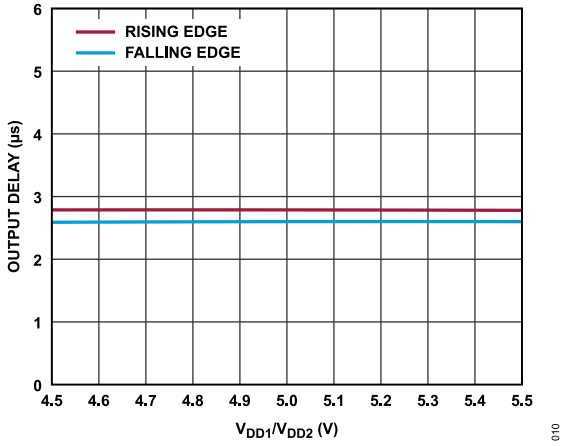

Figure 10. Output Delay vs. Supply Voltage

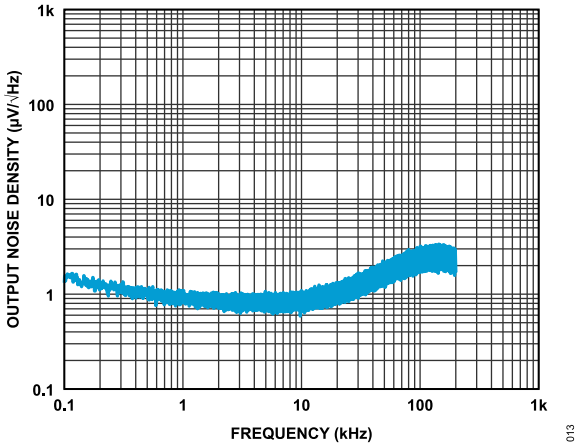

Figure 13. Output Noise Density vs. Frequency

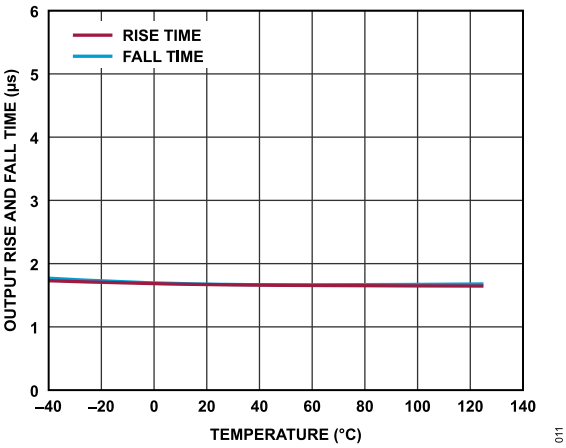

Figure 11. Output Rise and Fall Time vs. Temperature

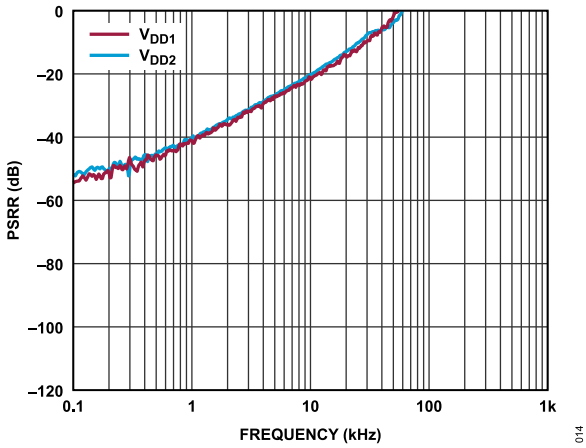

Figure 14. PSRR vs. Frequency

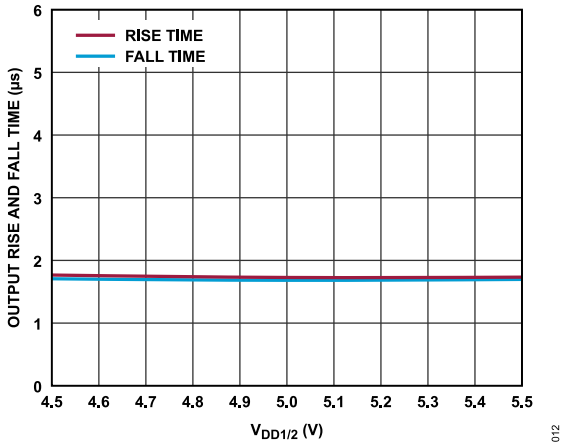

Figure 12. Output Rise and Fall Time vs. Supply Voltage

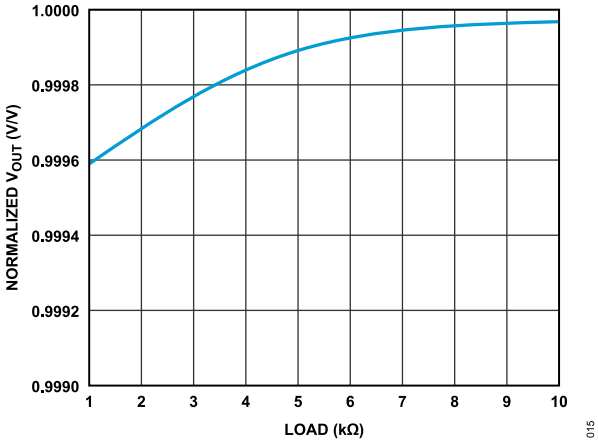

Figure 15. Normalized V_{OUT} vs. Load

TYPICAL PERFORMANCE CHARACTERISTICS

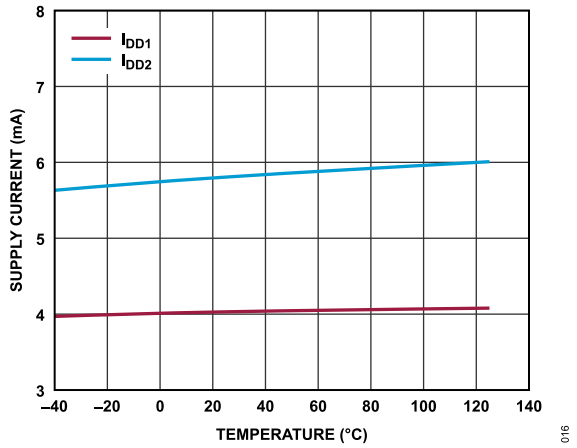

Figure 16. Typical Supply Currents vs. Temperature for V_{DD1} = V_{DD2} = 5.5 V

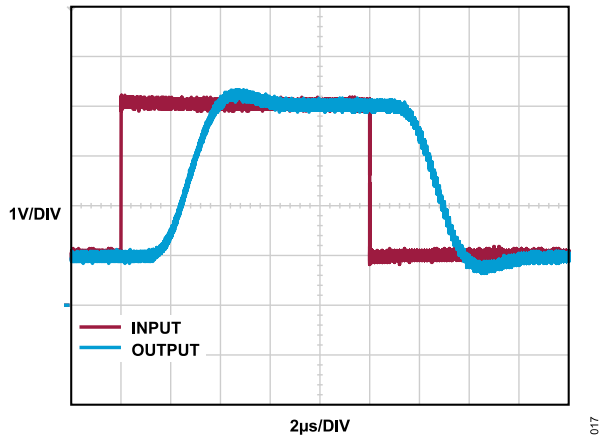

Figure 17. Output Square-Wave Response

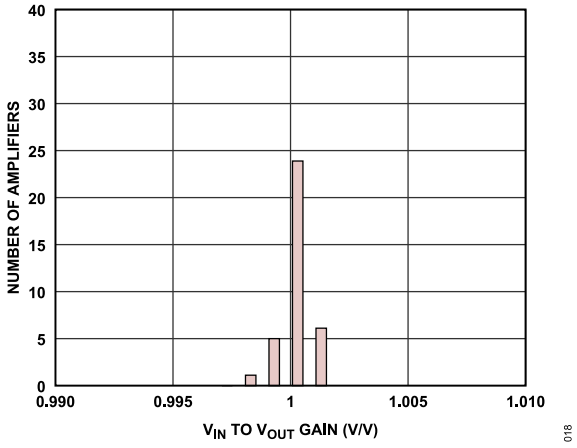

Figure 18. V_{IN} to V_{OUT} Gain Distribution at 25°C

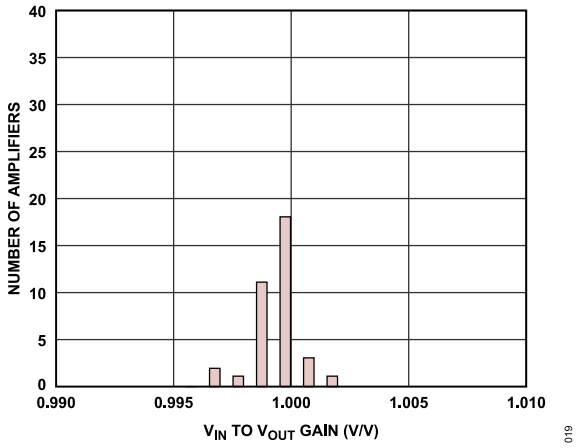

Figure 19. V_{IN} to V_{OUT} Gain Distribution at 125°C

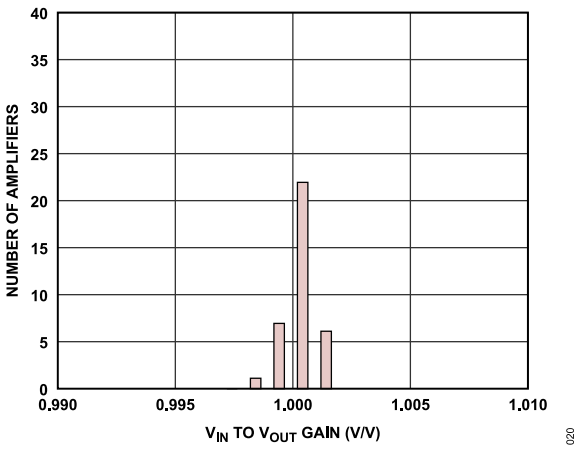

Figure 20. V_{IN} to V_{OUT} Gain Distribution at −40°C

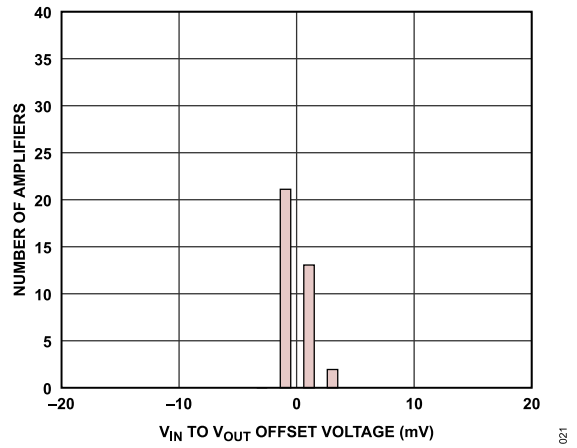

Figure 21. V_{IN} to V_{OUT} Offset-Voltage Distribution at 25°C, Output Offset-Voltage for V_{IN} = 2.5 V

TYPICAL PERFORMANCE CHARACTERISTICS

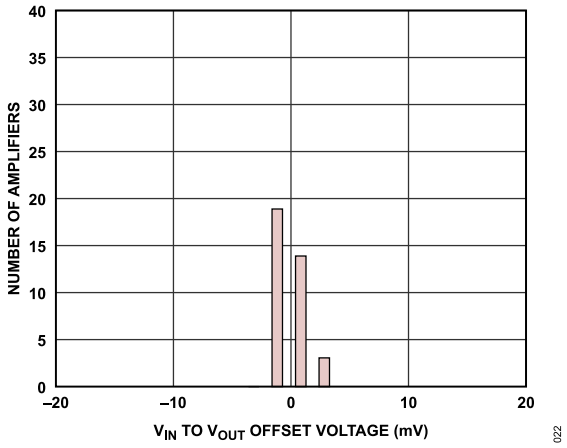

Figure 22. V_{IN} to V_{OUT} Offset-Voltage Distribution at 125°C, Output Offset-Voltage for V_{IN} = 2.5 V

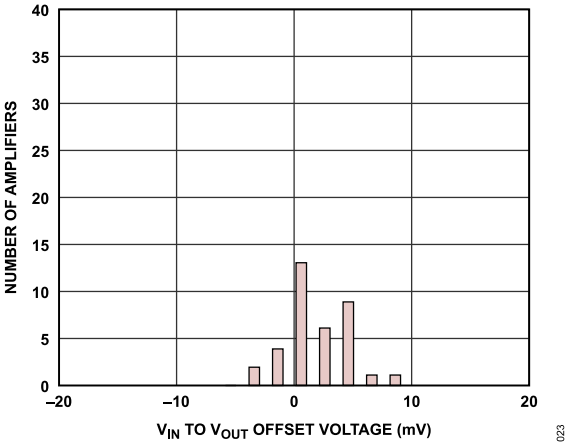

Figure 23. V_{IN} to V_{OUT} Offset-Voltage Distribution at −40°C, Output Offset-Voltage for V_{IN} = 2.5 V

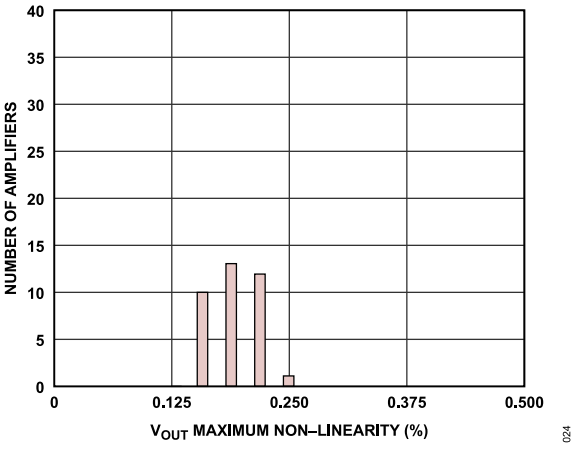

Figure 24. V_{OUT} Maximum Non-Linearity Distribution at 25°C, Maximum Non-Linearity Defined Within V_{IN} Input Range: 1 V to 3.5 V, as an Absolute Value

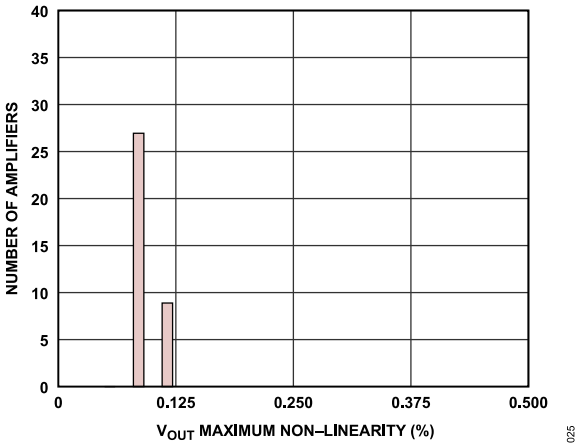

Figure 25. V_{OUT} Maximum Non-Linearity Distribution at 125°C (Maximum Non-Linearity Defined Within V_{IN} Input Range: 1 V to 3.5 V, as an Absolute Value

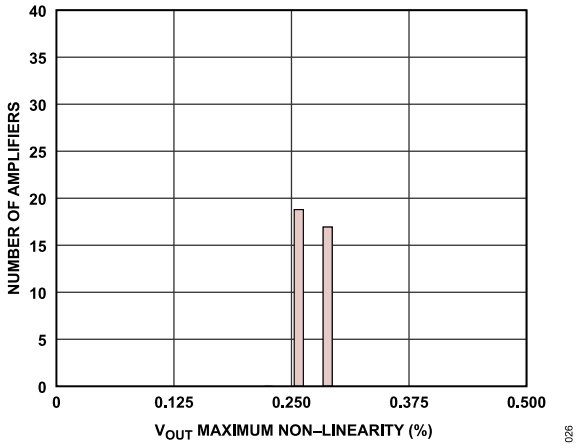

Figure 26. V_{OUT} Maximum Non-Linearity Distribution at −40°C, Maximum Non-Linearity Defined Within V_{IN} Input Range: 1 V to 3.5 V, as an Absolute Value

THEORY OF OPERATION

The ADuM4195-1 is an isolated amplifier (IA) based on Analog Devices, Inc., *i*Coupler® technology. The input side of the IA consists of an operational amplifier with input V_{IN} and an active-high SHTD pin. A highly linear pulse-width modulation (PWM) compares the output of the operational amplifier to an internal voltage reference and transmits the duty-cycle (ratio) information to the demodulator through a coreless transformer. On the output side of the IA, the demodulator uses the ratio information and an internal reference voltage to reconstruct the output voltage, which is then low-pass filtered, buffered, and presented at output pin as V_{OUT}, which follows V_{IN} with a fixed gain of 1.

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APPLICATION BLOCK DIAGRAM

Figure 27 shows a typical application for the ADuM4195-1 as an isolated voltage monitor. It offers unique linearity, high common-mode noise immunity, low gain errors, and temperature drift. These features make it a robust and high performance isolated amplifier for industrial applications with high-voltage sensing required.

The high-voltage bus is sensed through voltage-divider R1 and voltage-divider R2. As the IA acts as a unity-gain amplifier, the voltage at V_{OUT} is equal to the sensed bus voltage multiplied by the voltage-divider ratio. Due to the very high input impedance of the V_{IN} pin, the current through the resistive divider can be kept low without sacrificing accuracy, therefore allowing for low-power dissipation on the resistors. For very high voltages on the bus voltage however, possible pollution on the PCB must also be taken into consideration when planning to design for low input currents. Also, protective elements (such as diodes or Zener-diodes) in parallel with the voltage-divider R2 can negatively affect the accuracy of the voltage divider and must be selected for the lowest reverse leakage currents over the desired temperature range. In such a case, a capacitive protection method as shown in Figure 27 may be a more viable approach.

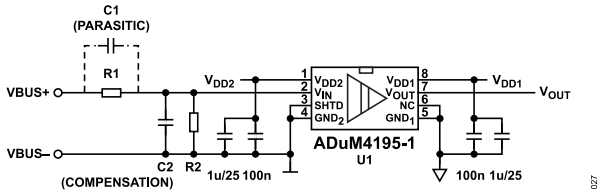

Figure 27. DC Bus Voltage Monitoring Using ADuM4195-1

DESIGN EXAMPLE

For a typical DC bus voltage monitoring application as shown in Figure 27, the following design procedure can be used:

Table 11. Example Design Parameters

Parameter	Value	Comment
V_{DD2} (min)	5.0 VDC	Lowest V_{DD2} supply
VBUS (max)	1000 VDC	Highest expected bus voltage
I_{DIV}	500 µA	Limit power loss in divider to 0.5 W

Determine the V_{DD2} (min) in your system. This in turn determines the maximum V_{IN} (max) that can be linearly transmitted across the isolation barrier.

$$V_{IN}\text{ (max)} = V_{DD2}\text{ (min)} - 0.7\text{ V} = 5.0\text{ V} - 0.7\text{ V} = 4.3\text{ V} \quad (1)$$

Determine the ratio 1/K of the voltage divider R1 and the voltage divider R2 for a given maximum of the VBUS (max), so that 1/K is about 0 to 10% larger than the VBUS (max)/V_{IN} (max).

$$1/K = (R1 + R2)/R2 = \text{VBUS (max)}/V_{IN}\text{ (max)} \quad (2)$$

$$1/K = 1 \ldots 1.1 \times (1000\text{ V}/4.3\text{ V}) = 232.558 \ldots 255.814 \quad (3)$$

For the given I_{DIV}, the minimum divider input resistance R_{IN} must meet as

$$R_{IN} = (R1 + R2) > \text{VBUS (max)}/I_{DIV} = 1\text{ kVDC}/500\text{ µA} = 2\text{ MΩ} \quad (4)$$

Also, the ratio of R1 and R2 can be expressed as

$$R1/R2 = (1/K) - 1 = 231.558 \ldots 254.814 \quad (5)$$

Thus, when selecting R1 as two 1 MΩ high-voltage resistors in a series, R2 can be calculated as

$$R2 = 2\text{ MΩ} \times K = 8.6\text{ kΩ} \ldots 7.82\text{ kΩ} \quad (6)$$

The divider's output resistance (R_{OUT}) with the input-bias current (I_{BIAS}) defines the amount of bias error, which adds to the total error of the system. Avoid bias error by selecting R1 and R2 so that

$$R_{OUT} = R1||R2 < 100\text{ kΩ} \quad (7)$$

With the previous calculated resistors R1 and R2,

$$R_{OUT} = 2\text{ MΩ}||7.82\text{ kΩ} = 7.8\text{ kΩ}, \quad (8)$$

which is well below the limit for R_{OUT}.

DEALING WITH PARASITIC CAPACITANCES

When monitoring very high bus voltages, the parasitic capacitances of R1 can impose a risk of overvoltage spikes on the V_{IN} during switching events on the VBUS. Therefore, it is recommended to connect the compensation capacitor C2 in parallel to R2. The proper compensation for the flat frequency response of the voltage divider is achieved by selecting C2 such that

$$C2 = R1 \times C1/R2 \quad (9)$$

The value of C2 is not critical but must be selected slightly higher than the calculated value to suppress any overshoot on the V_{IN} during switching events on the VBUS. For the previous design example, with R1 = 2 MΩ and R2 = 8.6 kΩ, and an estimated parasitic capacitance C1 of approximately 10 pF, the compensation capacitance necessary for C2 becomes

$$C2 \geq 2\text{ MΩ} \times 10\text{ pF}/8.6\text{ kΩ} = 2.3\text{ nF} \quad (10)$$

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder through the transformer. The decoder is bistable and is either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than 1 µs at the input, a periodic set of refresh pulses indicative of the correct input state are sent to ensure DC correctness at the output. If the decoder receives no internal pulses for more than approximately 3 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default high-impedance state by the watchdog timer circuit. In addition, the outputs are in a default high-impedance state while the power is increasing before the UVLO threshold is

APPLICATIONS INFORMATION

crossed. The ADuM4195-1 is immune to external magnetic fields. The limitation on the ADuM4195-1 magnetic field immunity is set by the condition whereby induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 4.5 V operating condition of the ADuM4195-1 is examined because it represents the most susceptible mode of operation. The decoder can tolerate up to 1.6 V noise induced by an external magnetic field. Assuming that there is 50% margin, the decoder can safely operate with up to 0.8 V induced noise. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \Sigma\pi r_n^2, n = 1, 2, \ldots, N \quad (11)$$

where:
β is the magnetic field strength (Gs).
r_n is the radius of the nth turn in the receiving coil (cm).
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM4195-1 and an imposed requirement that the induced voltage be, at most, 50% of the 1.6 V threshold at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 28.

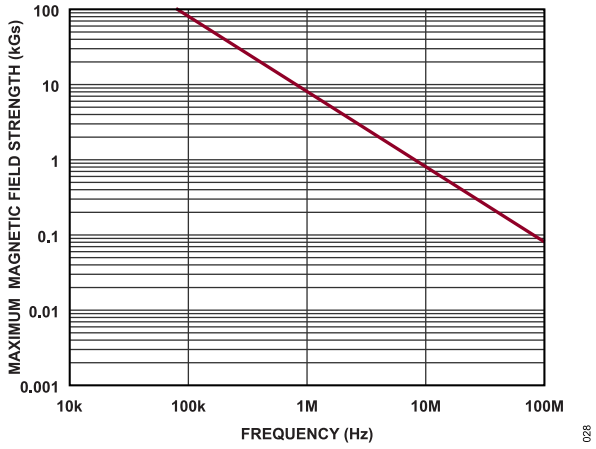

Figure 28. Maximum Allowable External Magnetic Field Strength

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 8 kGs induces a voltage of 0.8 V at the receiving coil. This is approximately 50% of the decoder threshold and does not cause a faulty output transition. The preceding magnetic field strength values correspond to specific current magnitudes at given distances away from the ADuM4195-1 transformers. Figure 29 shows these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 29, the ADuM4195-1 is immune and can be affected only by extremely large currents operating at a high frequency very close to the component. For the 1 MHz example, a 20 kA current must be placed 5 mm away from the ADuM4195-1 to affect the operation of the device.

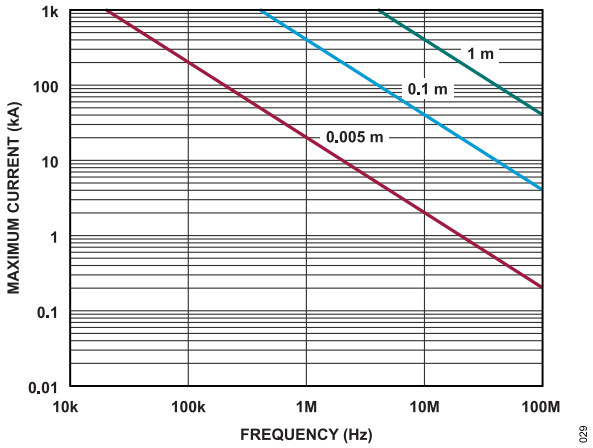

Figure 29. Maximum Allowable Current for Various Current-to-ADuM4195-1 Spacings

LAYOUT CONSIDERATIONS

V_{DD1} and V_{DD2} must be decoupled to their respective GND_1 and GND_2 with capacitors of at least 1 µF in parallel with 100 nF. In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. To fully use the specified isolation properties of the ADuM4195-1, the top and bottom copper layers of the PCB must not reach underneath the package but instead must only reach as far as the solder-pad area. Place any decoupling used as close to the supply pins as possible. See Figure 30 for component placement suggestion.

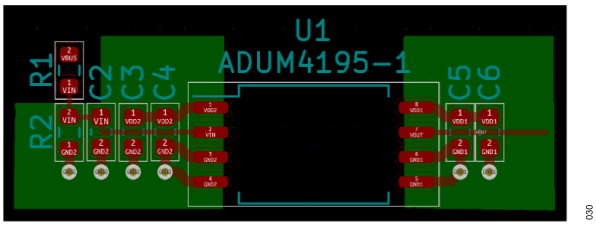

Figure 30. Placement of Decoupling Capacitors, Ground Plane GND_1, and Ground Plane GND_2