Isolated Precision Half-Bridge Driver, 4 A Output

Data Sheet

ADuM3224/ADuM4224

FEATURES

- 4 A peak output current
- Working voltage
  - High-side or low-side relative to input: 537 V peak
- High frequency operation: 1 MHz maximum
- 3.3 V to 5 V CMOS input logic
- 4.5 V to 18 V output drive
- Secondary UVLO
  - ADuM3224A/ADuM4224A UVLO at 4.1 V V_{DDA}/V_{DDB}
  - ADuM3224B/ADuM4224B UVLO at 6.9 V V_{DDA}/V_{DDB}
  - ADuM3224C/ADuM4224C UVLO at 10.5 V V_{DDA}/V_{DDB}
- Precise timing characteristics
  - 59 ns maximum isolator and driver propagation delay
  - 5 ns maximum channel-to-channel matching
- CMOS input logic levels
- High common-mode transient immunity: >25 kV/µs
- Enhanced system-level ESD performance per IEC 61000-4-x
- High junction temperature operation: 125°C
- Default low output
- Safety and regulatory approvals
  - ADuM3224 narrow-body, 16-lead SOIC
    - UL recognition per UL 1577
      - 3000 V rms for 1 minute SOIC long package
    - CSA Component Acceptance Notice 5A
    - VDE certificate of conformity (pending)
      - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
      - V_{IORM} = 560 V peak
  - ADuM4224 wide-body, 16-lead SOIC
    - UL recognition per UL 1577
      - 5000 V rms for 1 minute SOIC long package
    - CSA Component Acceptance Notice 5A
    - VDE certificate of conformity (pending)
      - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
      - V_{IORM} = 849 V peak
- Qualified for automotive applications

APPLICATIONS

- Switching power supplies
- Isolated IGBT/MOSFET gate drives
- Industrial inverters

FUNCTIONAL BLOCK DIAGRAM

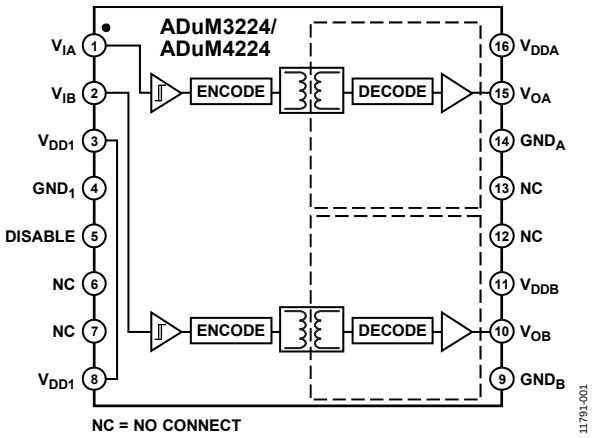

Figure 1.

GENERAL DESCRIPTION

The ADuM3224/ADuM4224[1] are 4 A isolated, half-bridge gate drivers that employ the Analog Devices, Inc., *i*Coupler® technology to provide independent and isolated high-side and low-side outputs. The ADuM3224 provides 3000 V rms isolation in the narrow-body, 16-lead SOIC package, and the ADuM4224 provides 5000 V rms isolation in the wide-body, 16-lead SOIC package. Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics superior to the alternatives, such as the combination of pulse transformers and gate drivers.

The ADuM3224/ADuM4224 isolators each provide two independent isolated channels. They operate with an input supply ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems. In comparison to gate drivers employing high voltage level translation methodologies, the ADuM3224/ADuM4224 offer the benefit of true, galvanic isolation between the input and each output. Each output can be continuously operated up to 537 V peak relative to the input, thereby supporting low-side switching to negative voltages. The differential voltage between the high-side and low-side can be as high as 800 V peak.

As a result, the ADuM3224/ADuM4224 provide reliable control over the switching characteristics of IGBT/MOSFET configurations over a wide range of positive or negative switching voltages.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,239. Other patents pending.

Rev. B
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12/13—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground. 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DDA} ≤ 18 V, 4.5 V ≤ V_{DDB} ≤ 18 V, unless stated otherwise. All minimum/maximum specifications apply over T_J = −40°C to +125°C. All typical specifications are at T_J = 25°C, V_{DD1} = 5 V, V_{DDA} = V_{DDB} = 12 V. Switching specifications are tested with CMOS signal levels.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DDI(Q)}$		1.4	2.4	mA	
Output Supply Current, Per Channel, Quiescent	$I_{DDO(Q)}$		2.3	3.2	mA	
Supply Current at 1 MHz						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.6	2.5	mA	Up to 1 MHz, no load
V_{DDA}/V_{DDB} Supply Current	$I_{DDA(Q)}$/$I_{DDB(Q)}$		5.6	8.0	mA	Up to 1 MHz, no load
Input Currents	I_{IA}, I_{IB}	−1	+0.01	+1	µA	0 V ≤ V_{IA}, V_{IB} ≤ V_{DD1}
Logic High Input Threshold	V_{IH}	0.7 × V_{DD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 × V_{DD1}	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	V_{DDA}/ V_{DDB} − 0.1	V_{DDA}/ V_{DDB}		V	I_{Ox} = −20 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.15	V	I_{Ox} = +20 mA, V_{Ix} = V_{IxL}
Undervoltage Lockout, V_{DDA}/V_{DDB} Supply						
A Grade						
Positive Going Threshold	V_{DDAUV+}, V_{DDBUV+}		4.1	4.4	V	
Negative Going Threshold	V_{DDAUV-}, V_{DDBUV-}	3.2	3.6		V	
Hysteresis	V_{DDAUVH}, V_{DDBUVH}		0.5		V	
B Grade						
Positive Going Threshold	V_{DDAUV+}, V_{DDBUV+}		6.9	7.4	V	
Negative Going Threshold	V_{DDAUV-}, V_{DDBUV-}	5.7	6.2		V	
Hysteresis	V_{DDAUVH}, V_{DDBUVH}		0.7		V	
C Grade						
Positive Going Threshold	V_{DDAUV+}, V_{DDBUV+}		10.5	11.1	V	
Negative Going Threshold	V_{DDAUV-}, V_{DDBUV-}	8.9	9.6		V	
Hysteresis	V_{DDAUVH}, V_{DDBUVH}		0.9		V	
Output Short-Circuit Pulsed Current[1]	$I_{OA(SC)}$, $I_{OB(SC)}$	2.0	4.0		A	V_{DDA}/V_{DDB} = 12 V
Output Pulsed Source Resistance	R_{OA}, R_{OB}	0.3	1.1	3.0	Ω	V_{DDA}/V_{DDB} = 12 V
Output Pulsed Sink Resistance	R_{OA}, R_{OB}	0.3	0.6	3.0	Ω	V_{DDA}/V_{DDB} = 12 V
SWITCHING SPECIFICATIONS						
Pulse Width[2]	PW	50			ns	C_L = 2 nF, V_{DDA}/V_{DDB} = 12 V
Maximum Data Rate[3]		1			MHz	C_L = 2 nF, V_{DDA}/V_{DDB} = 12 V
Propagation Delay[4]	t_{DHL}, t_{DLH}	31	43	54	ns	C_L = 2 nF, V_{DDA}/V_{DDB} = 12 V; see Figure 20
ADuM3224A/ADuM4224A	t_{DHL}, t_{DLH}	35	47	59	ns	C_L = 2 nF, V_{DDA}/V_{DDB} = 4.5 V; see Figure 20
Propagation Delay Skew[5]	t_{PSK}			12	ns	C_L = 2 nF, V_{DDA}/V_{DDB} = 12 V; see Figure 20
Channel-to-Channel Matching[6]	t_{PSKCD}		1	5	ns	C_L = 2 nF, V_{DDA}/V_{DDB} = 12 V; see Figure 20
	t_{PSKCD}		1	7	ns	C_L = 2 nF, V_{DDA}/V_{DDB} = 4.5 V; see Figure 20
Output Rise/Fall Time (10% to 90%)	t_R/t_F	6	12	18	ns	C_L = 2 nF, V_{DDA}/V_{DDB} = 12 V; see Figure 20
Dynamic Input Supply Current Per Channel	$I_{DDI(D)}$		0.05		mA/Mbps	V_{DDA}/V_{DDB} = 12 V
Dynamic Output Supply Current Per Channel	$I_{DDO(D)}$		1.65		mA/Mbps	V_{DDA}/V_{DDB} = 12 V
Refresh Rate	f_r		1.2		Mbps	

[1] Short-circuit duration less than 1 µs. Average power must conform to the limit shown in the Absolute Maximum Ratings section.
[2] The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified timing parameter is guaranteed.
[4] The t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% level of the V_{Ox} signal. The t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_{Ox} signal. See Figure 20 for waveforms of propagation delay parameters.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 20 for waveforms of propagation delay parameters.
[6] Channel-to-channel matching is the absolute value of the difference in propagation delays between the two channels.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All voltages are relative to their respective ground. 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DDA} ≤ 18 V, 4.5 V ≤ V_{DDB} ≤ 18 V, unless stated otherwise. All minimum/maximum specifications apply over T_J = −40°C to +125°C. All typical specifications are at T_J = 25°C, V_{DD1} = 3.3 V, V_{DDA} = V_{DDB} = 12 V. Switching specifications are tested with CMOS signal levels.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DDI(Q)}$		0.87	1.4	mA	
Output Supply Current, Per Channel, Quiescent	$I_{DDO(Q)}$		2.3	3.2	mA	
Supply Current at 1 MHz						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.1	1.5	mA	Up to 1 MHz, no load
V_{DDA}/V_{DDB} Supply Current	$I_{DDA(Q)}$/$I_{DDB(Q)}$		5.6	8.0	mA	Up to 1 MHz, no load
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	0 V ≤ V_{IA}, V_{IB} ≤ V_{DD1}
Logic High Input Threshold	V_{IH}	0.7 × V_{DD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 × V_{DD1}	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	V_{DDA}/V_{DDB} − 0.1	V_{DDA}/V_{DDB}		V	I_{Ox} = −20 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.15	V	I_{Ox} = +20 mA, V_{Ix} = V_{IxL}
Undervoltage Lockout, V_{DDA}/V_{DDB} Supply						
A Grade						
Positive Going Threshold	V_{DDAUV+}, V_{DDBUV+}		4.1	4.4	V	
Negative Going Threshold	V_{DDAUV-}, V_{DDBUV-}	3.2	3.6		V	
Hysteresis	V_{DDAUVH}, V_{DDBUVH}		0.5		V	
B Grade						
Positive Going Threshold	V_{DDAUV+}, V_{DDBUV+}		6.9	7.4	V	
Negative Going Threshold	V_{DDAUV-}, V_{DDBUV-}	5.7	6.2		V	
Hysteresis	V_{DDAUVH}, V_{DDBUVH}		0.7		V	
C Grade						
Positive Going Threshold	V_{DDAUV+}, V_{DDBUV+}		10.5	11.1	V	
Negative Going Threshold	V_{DDAUV-}, V_{DDBUV-}	8.9	9.6		V	
Hysteresis	V_{DDAUVH}, V_{DDBUVH}		0.9		V	
Output Short-Circuit Pulsed Current[1]	$I_{OA(SC)}$, $I_{OB(SC)}$	2.0	4.0		A	V_{DDA}/V_{DDB} = 12 V
Output Pulsed Source Resistance	R_{OA}, R_{OB}	0.3	1.1	3.0	Ω	V_{DDA}/V_{DDB} = 12 V
Output Pulsed Sink Resistance	R_{OA}, R_{OB}	0.3	0.6	3.0	Ω	V_{DDA}/V_{DDB} = 12 V
SWITCHING SPECIFICATIONS						
Pulse Width[2]	PW	50			ns	C_L = 2 nF, V_{DDA}/V_{DDB} = 12 V
Maximum Data Rate[3]		1			MHz	C_L = 2 nF, V_{DDA}/V_{DDB} = 12 V
Propagation Delay[4]	t_{DHL}, t_{DLH}	35	47	59	ns	C_L = 2 nF, V_{DDA}/V_{DDB} = 12 V, see Figure 20
ADuM3224A/ADuM4224A	t_{DHL}, t_{DLH}	37	51	65	ns	C_L = 2 nF, V_{DDA}/V_{DDB} = 4.5 V, see Figure 20
Propagation Delay Skew[5]	t_{PSK}			12	ns	C_L = 2 nF, V_{DDA}/V_{DDB} = 12 V, see Figure 20
Channel-to-Channel Matching[6]	t_{PSKCD}		1	5	ns	C_L = 2 nF, V_{DDA}/V_{DDB} = 12 V, see Figure 20
	t_{PSKCD}		1	7	ns	C_L = 2 nF, V_{DDA}/V_{DDB} = 4.5 V, see Figure 20
Output Rise/Fall Time (10% to 90%)	t_R/t_F	6	12	22	ns	C_L = 2 nF, V_{DDA}/V_{DDB} = 12 V, see Figure 20
Dynamic Input Supply Current Per Channel	$I_{DDI(D)}$		0.05		mA/Mbps	V_{DDA}/V_{DDB} = 12 V
Dynamic Output Supply Current Per Channel	$I_{DDO(D)}$		1.65		mA/Mbps	V_{DDA}/V_{DDB} = 12 V
Refresh Rate	f_r		1.1		Mbps	

[1] Short-circuit duration less than 1 µs. Average power must conform to the limit shown in the Absolute Maximum Ratings section.
[2] The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified timing parameter is guaranteed.
[4] The t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% level of the V_{Ox} signal. The t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_{Ox} signal. See Figure 20 for waveforms of propagation delay parameters.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 20 for waveforms of propagation delay parameters.
[6] Channel-to-channel matching is the absolute value of the difference in propagation delays between the two channels.

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output)	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)	C_{I-O}		2.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance						
ADuM3224	θ_{JA}		76		°C/W	
ADuM4224	θ_{JA}		45		°C/W	
IC Junction-to-Case Thermal Resistance						
ADuM3224	θ_{JC}		42		°C/W	
ADuM4224	θ_{JC}		29		°C/W	

INSULATION AND SAFETY RELATED SPECIFICATIONS

ADuM3224 Specifications

Table 4.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	4.0 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.0 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

ADuM4224 Specifications

Table 5.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.6 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.6 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

REGULATORY INFORMATION

The ADuM3224 is approved or pending approval by the organizations listed in Table 6.

Table 6.

UL	CSA	VDE (Pending)
Recognized under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2]
Single/Protection 3000 V rms Isolation Voltage	Basic insulation per CSA 60950-1-07 and IEC 60950-1, 380 V rms (537 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM3224 is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 second (current leakage detection limit = 6 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM3224 is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC). An asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

The ADuM4224 is approved or pending approval by the organizations listed in Table 7.

Table 7.

UL	CSA	VDE (Pending)
Recognized under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2]
Single/Protection 5000 V rms Isolation Voltage	Reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 380 V rms (537 V peak) maximum working voltage Basic insulation per CSA 60950-1-07 and IEC 60950-1, 760 V rms (1074 V peak) maximum working voltage	Reinforced insulation, 849 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM4224 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM4224 is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 second (partial discharge detection limit = 5 pC). An asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on the package denotes DIN V VDE V 0884-10 approval for a 560 V peak working voltage.

Table 8. ADuM3224 VDE Characteristics (Pending)

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1050	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	672	V peak
Highest Allowable Overvoltage		V_{IOTM}	4242	V peak
Surge Isolation Voltage	$V_{PEAK} = 10$ kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Maximum Junction Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	1.64	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

Table 9. ADuM4224 VDE Characteristics (Pending)

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$		
After Environmental Tests Subgroup 1			1273	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1018	V peak
Highest Allowable Overvoltage		V_{IOTM}	7071	V peak
Surge Isolation Voltage	$V_{PEAK} = 10$ kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Maximum Junction Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	2.77	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

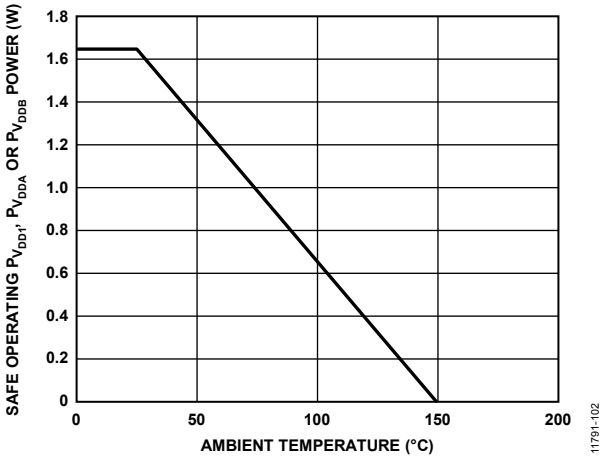


Figure 2. ADuM3224 Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN V VDE V 0884-10

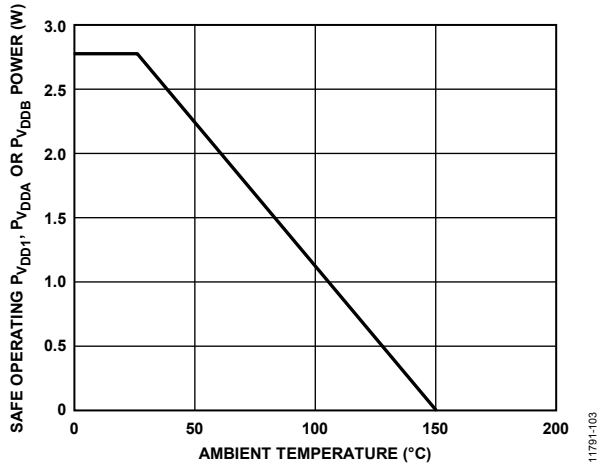


Figure 3. ADuM4224 Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 10.

Parameter	Symbol	Rating
Operating Junction Temperature	T_J	−40°C to +125°C
Supply Voltages[1]		
	V_{DD1}	3.0 V to 5.5 V
	V_{DDA}, V_{DDB}	4.5 V to 18 V
V_{DD1} Rise Time	t_{VDD1}	1 V/µs
V_{DDA}, V_{DDB} Rise Time	t_{VDDA}, t_{VDDB}	10 V/µs
Maximum Input Signal Rise and Fall Times	t_{VIA}, t_{VIB}	1 ms
Common-Mode Transient, Static[2]		−50 kV/µs to +50 kV/µs
Common-Mode Transient Immunity, Dynamic[3]		−25 kV/µs to +25 kV/µs

[1] All voltages are relative to their respective ground. See the Applications Information section for information on immunity to external magnetic fields.
[2] Static common-mode transient immunity is defined as the largest dv/dt between GND_1 and GND_A/GND_B with inputs held either high or low such that the output voltage remains either above $0.8 \times V_{DDA}/V_{DDB}$ for V_{IA}/V_{IB} = high, or 0.8 V for V_{IA}/V_{IB} = low. Operation with transients above the recommended levels can cause momentary data upsets.
[3] Dynamic common-mode transient immunity is defined as the largest dv/dt between GND_1 and GND_A/GND_B with the switching edge coincident with the transient test pulse. Operation with transients above the recommended levels can cause momentary data upsets.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 11.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Operating Junction Temperature (T_J)	−40°C to +150°C
Supply Voltages[1]	
V_{DD1}	−0.5 V to +7.0 V
V_{DDA}, V_{DDB}	−0.5 V to +20 V
Input Voltage (V_{IA}, V_{IB}, DISABLE)[1]	−0.5 V to V_{DD1} + 0.5 V
Output Voltage[1]	
V_{OA}	−0.5 V to V_{DDA} + 0.5 V
V_{OB}	−0.5 V to V_{DDB} + 0.5 V
Average Output Current, per Pin (I_O)[2]	−35 mA to +35 mA
Common-Mode Transients (CM_H, CM_L)[3]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] See Figure 2 and Figure 3 for information on maximum allowable current for various temperatures.
[3] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 12. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform	1131	V peak	50-year minimum lifetime
DC Voltage	1131	V peak	50-year minimum lifetime

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

Table 13. ADuM3224/ADuM4224 (Positive Logic) Truth Table[1]

DISABLE	V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DDA}/V_{DDB} State	V_{OA} Output	V_{OB} Output	Notes
L	L	L	Powered	Powered	L	L	Outputs return to the input state within 1 µs of DISABLE = L assertion.
L	L	H	Powered	Powered	L	H	Outputs return to the input state within 1 µs of DISABLE = L assertion.
L	H	L	Powered	Powered	H	L	Outputs return to the input state within 1 µs of DISABLE = L assertion.
L	H	H	Powered	Powered	H	H	Outputs return to the input state within 1 µs of DISABLE = L assertion.
H	X	X	Powered	Powered	L	L	Outputs take on default low state within 3 µs of DISABLE = H assertion.
L	L	L	Unpowered	Powered	L	L	Outputs return to the input state within 1 µs of V_{DD1} power restoration.
X	X	X	Powered	Unpowered	L	L	Outputs return to the input state within 50 µs of V_{DDA}/V_{DDB} power restoration.

[1] X = don't care, L = low, and H = high.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

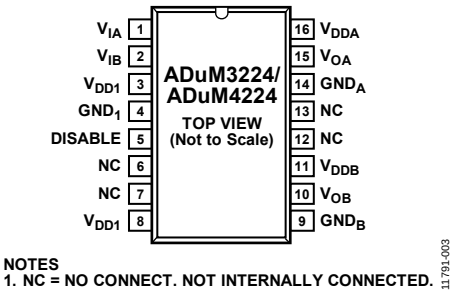


Figure 4. Pin Configuration

Table 14. ADuM3224/ADuM4224 Pin Function Descriptions

Pin No.[1]	Mnemonic	Description
1	V_{IA}	Logic Input A.
2	V_{IB}	Logic Input B.
3, 8	V_{DD1}	Input Supply Voltage.
4	GND_1	Ground Reference for Input Logic Signals.
5	DISABLE	Input Disable. Disables the isolator inputs and refresh circuits. Outputs take on the default low state within 3 µs of a DISABLE = high assertion. Outputs return to the input state within 1 µs of a DISABLE = low assertion.
6, 7, 12, 13	NC	No Connect. These pins are not internally connected.
9	GND_B	Ground Reference for Output B.
10	V_{OB}	Output B.
11	V_{DDB}	Output B Supply Voltage.
14	GND_A	Ground Reference for Output A.
15	V_{OA}	Output A.
16	V_{DDA}	Output A Supply Voltage.

[1] Pin 3 and Pin 8 are internally connected; connecting both pins to the V_{DD1} supply is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

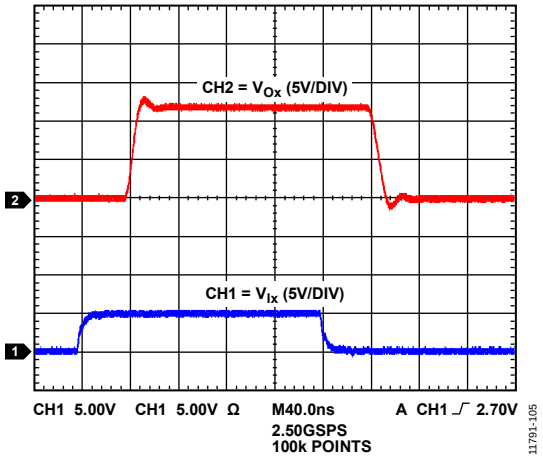


Figure 5. Output Waveform for 2 nF Load with 12 V Output Supply

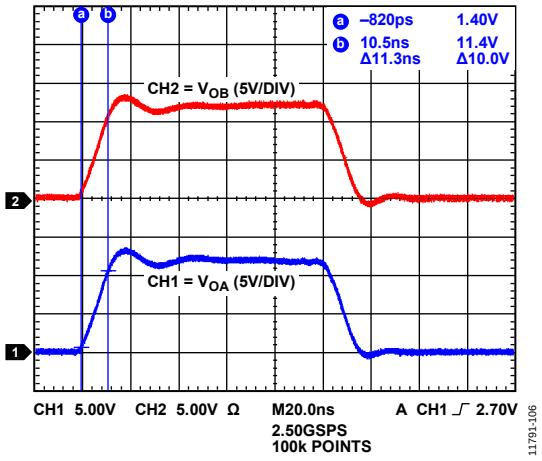


Figure 6. Output Matching and Rise Time Waveforms for 2 nF Load with 12 V Output Supply

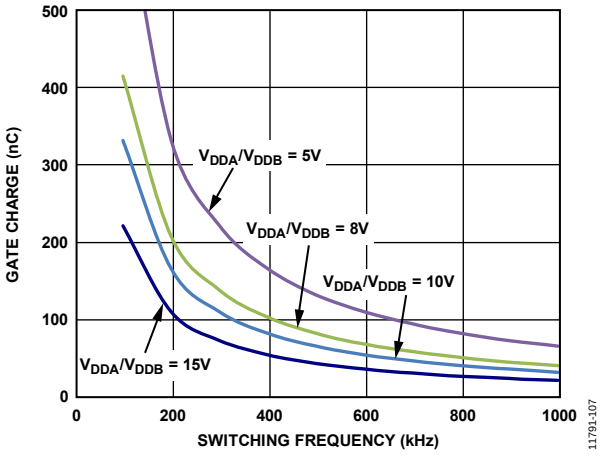


Figure 7. Typical ADuM3224 Maximum Load vs. Switching Frequency (R_G = 1 Ω)

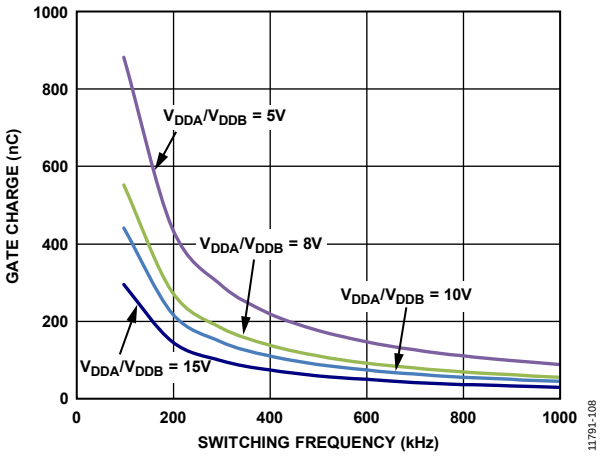


Figure 8. Typical ADuM4224 Maximum Load vs. Switching Frequency (R_G = 1 Ω)

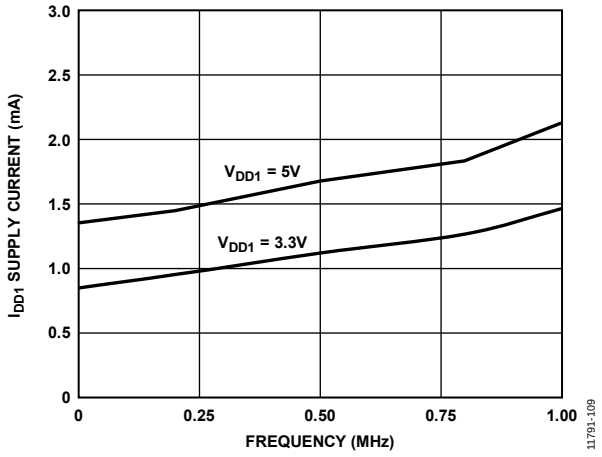


Figure 9. Typical I_{DD1} Supply Current vs. Frequency

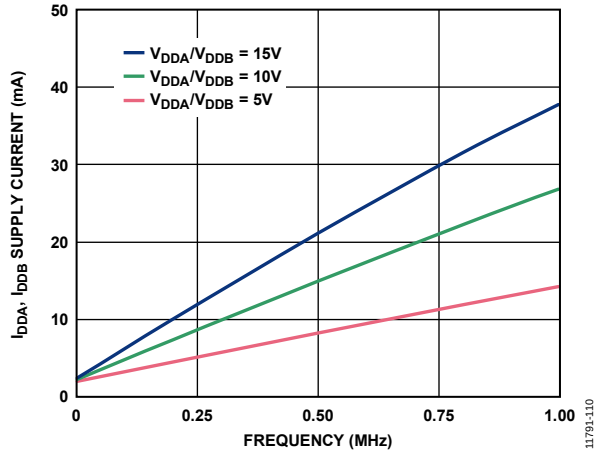


Figure 10. Typical I_{DDA}, I_{DDB} Supply Current vs. Frequency with 2 nF Load

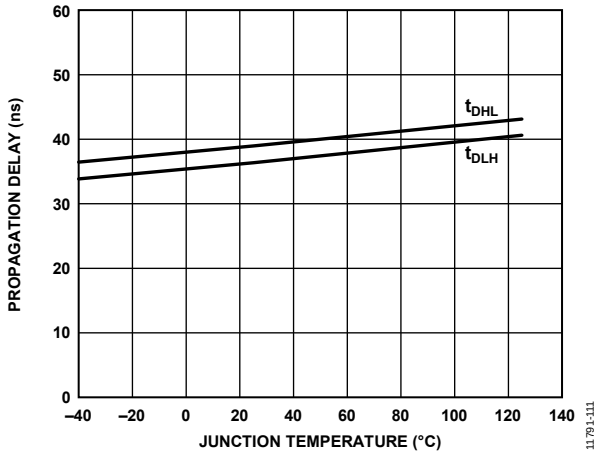


Figure 11. Typical Propagation Delay vs. Junction Temperature

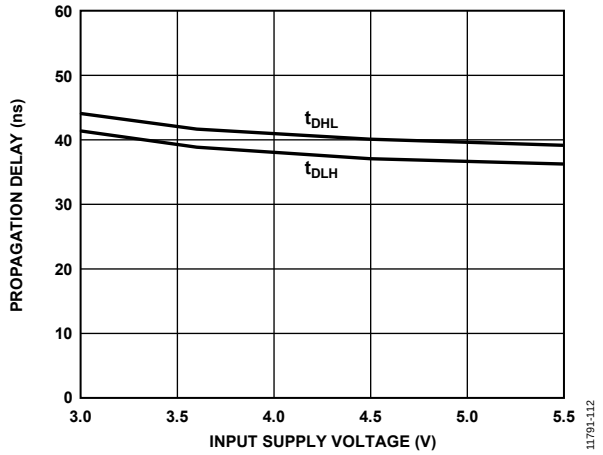


Figure 12. Typical Propagation Delay vs. Input Supply Voltage; V_{DDA}, V_{DDB} = 12 V

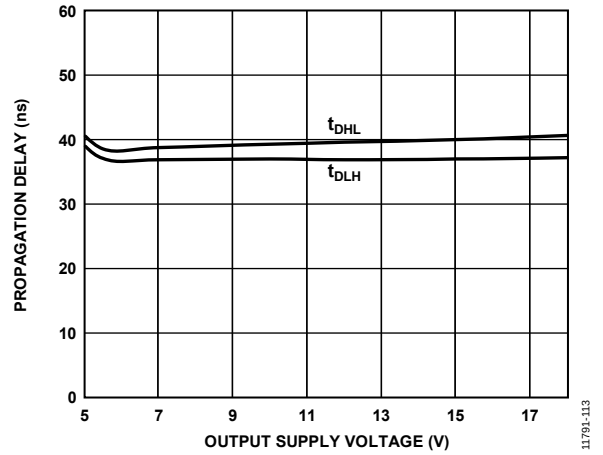


Figure 13. Typical Propagation Delay vs. Output Supply Voltage, V_{DD1} = 5 V

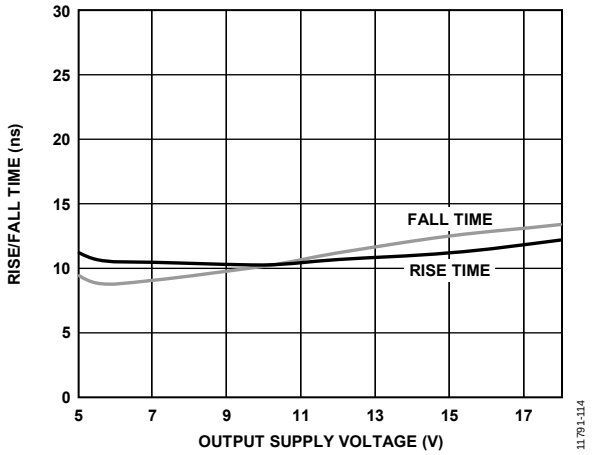


Figure 14. Typical Rise/Fall Time Variation vs. Output Supply Voltage

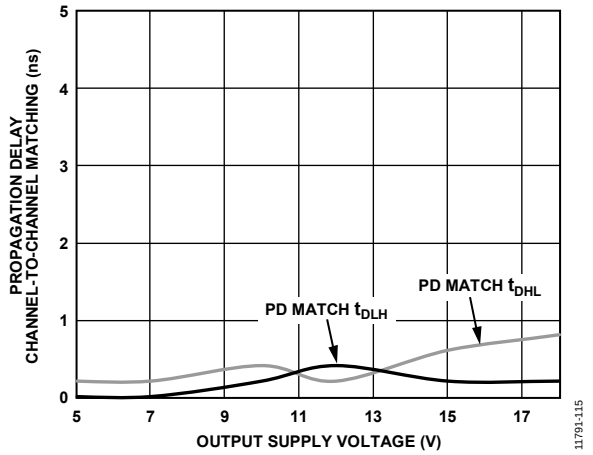


Figure 15. Typical Propagation Delay (PD) Channel-to-Channel Matching vs. Output Supply Voltage

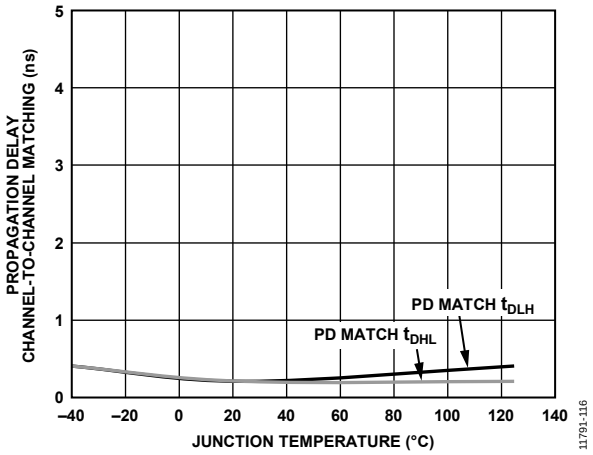


Figure 16. Typical Propagation Delay (PD) Channel-to-Channel Matching vs. Temperature; V_{DDA}, V_{DDB} = 12 V

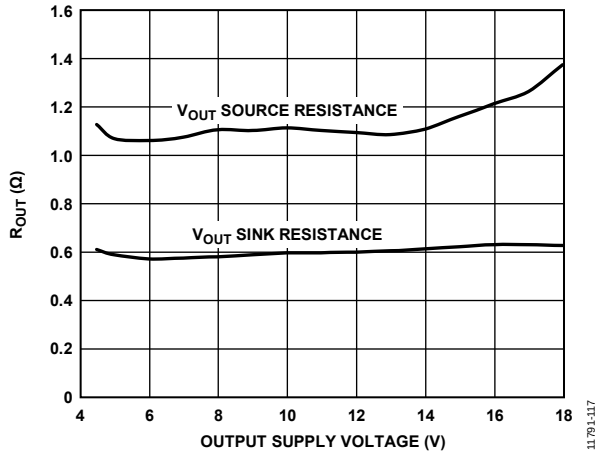


Figure 17. Typical Output Resistance (R_{OUT}) vs. Output Supply Voltage

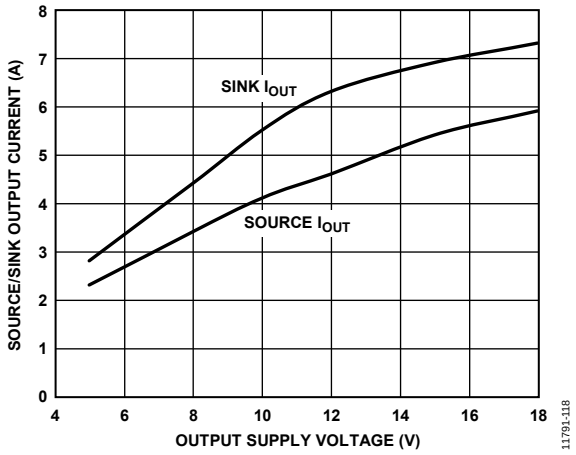


Figure 18. Typical Source/Sink Output Current vs. Output Supply Voltage

APPLICATIONS INFORMATION

PRINTED CIRCUIT BOARD LAYOUT

The ADuM3224/ADuM4224 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins, as shown in Figure 19. Use a small ceramic capacitor with a value between 0.01 µF and 0.1 µF to provide a good high frequency bypass. On the output power supply pin, V_{DDA} or V_{DDB}, it is recommended to also add a 10 µF capacitor to provide the charge required to drive the gate capacitance at the ADuM3224/ADuM4224 outputs. On the output supply pin, avoid the use of vias on the bypass capacitor, or use multiple vias to reduce the inductance in the bypassing. The total lead length between both ends of the smaller capacitor and the input or output power supply pin must not exceed 5 mm. For specific layout guidelines, refer to the AN-1109 Application Note, *Recommendations for Control of Radiated Emissions with iCoupler Devices*.

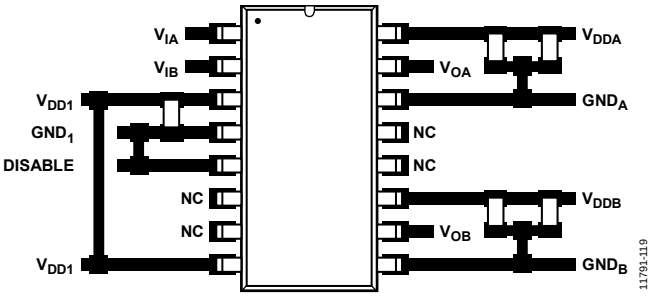


Figure 19. Recommended PCB Layout

UNDERVOLTAGE LOCKOUT

For the output of a channel of the ADuM3224/ADuM4224 to be valid, both the V_{DD1} and the V_{DDA} or V_{DDB} power supplies must be above the positive going undervoltage lockout (UVLO) threshold. If, during operation, the supply voltage drops below the negative going UVLO threshold, the output is brought low to protect the switch from being underdriven. The V_{DD1} threshold is typically around 2.5 V. There are three options for the secondary supply thresholds, which can be selected by the different grades (see the Ordering Guide). The UVLO of each output channel acts independently of the other, but in the case of a V_{DD1} UVLO, both channels are brought low.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output. The ADuM3224/ADuM4224 specify t_{DLH} (see Figure 20) as the time between the rising input high logic threshold, V_{IH}, to the output rising 10% threshold. Likewise, the falling propagation delay, t_{DHL}, is defined as the time between the input falling logic low threshold, V_{IL}, and the output falling 90% threshold. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, which is the industry standard for gate drivers.

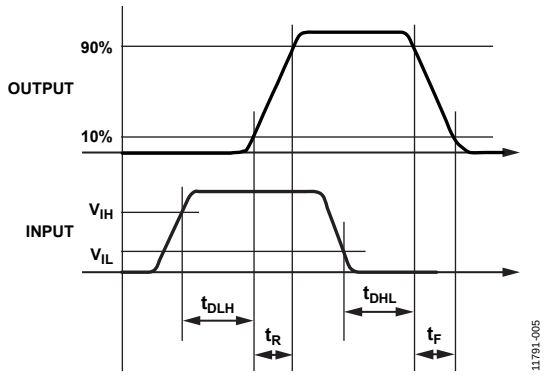


Figure 20. Propagation Delay Parameters

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM3224/ADuM4224 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM3224/ADuM4224 components operating under the same conditions.

THERMAL LIMITATIONS AND SWITCH LOAD CHARACTERISTICS

For isolated gate drivers, the necessary separation between the input and output circuits prevents the use of a single thermal pad beneath the device, and heat is, therefore, dissipated mainly through the package pins.

Package thermal dissipation limits the performance of output load vs. switching frequency, as illustrated in Figure 7 and Figure 8 for the maximum load capacitance that can be driven with a 1 Ω series gate resistance for different values of output voltage. For example, Figure 7 shows that a typical ADuM3224 can drive a large MOSFET with 140 nC gate charge at 8 V output (which is equivalent to a 17 nF load) up to a frequency of about 300 kHz.

Do not allow the internal junction temperature of the ADuM3224/ADuM4224 to exceed the maximum junction temperature of 150°C. Operation above this value causes damage to the device. There is no internal thermal shutdown to protect the ADuM3224/ADuM4224. If a thermal shutdown is desired, see the ADuM3223/ADuM4223 data sheet.

OUTPUT LOAD CHARACTERISTICS

The ADuM3224/ADuM4224 output signals depend on the characteristics of the output load, which is typically an N-channel MOSFET. The driver output response to an N-channel MOSFET load can be modeled with a switch output resistance (R_{SW}), an inductance due to the printed circuit board trace (L_{TRACE}), a series gate resistor (R_{GATE}), and a gate-to-source capacitance (C_{GS}), as shown in Figure 21.

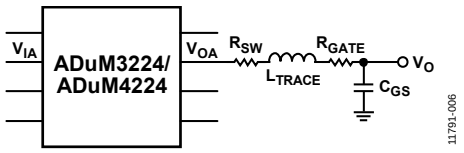


Figure 21. RLC Model of the Gate of an N-Channel MOSFET

R_{SW} is the switch resistance of the internal ADuM3224/ADuM4224 driver output, which is about 1.1 Ω. R_{GATE} is the intrinsic gate resistance of the MOSFET and any external series resistance. A MOSFET that requires a 4 A gate driver has a typical intrinsic gate resistance of about 1 Ω and a gate-to-source capacitance, C_{GS}, of between 2 nF and 10 nF. L_{TRACE} is the inductance of the printed circuit board trace, typically a value of 5 nH or less for a well designed layout with a very short and wide connection from the ADuM3224/ADuM4224 output to the gate of the MOSFET.

The following equation defines the Q factor of the resistor/inductor/capacitor (RLC) circuit, which indicates how the ADuM3224/ADuM4224 output responds to a step change. For a well damped output, Q is less than 1. Adding a series gate resistance dampens the output response.

$$Q = \frac{1}{(R_{SW} + R_{GATE})} \times \sqrt{\frac{L_{TRACE}}{C_{GS}}}$$

In Figure 5, the ADuM3224/ADuM4224 output waveforms for a 12 V output are shown for a C_{GS} of 2 nF. Note the small amount of ringing of the output in Figure 5 with a C_{GS} of 2 nF, R_{SW} of 1.1 Ω, R_{GATE} of 0 Ω, and a calculated Q factor of 0.75, where less than 1 is desired for good damping.

Output ringing can be reduced by adding a series gate resistance to dampen the response. For applications of less than 1 nF load, it is recommended to add a series gate resistor of about 2 Ω to 5 Ω.

BOOTSTRAPPED HALF-BRIDGE OPERATION

The ADuM3224/ADuM4224 are well suited to the operation of two output gate signals that are referenced to separate grounds, as in the case of a half-bridge configuration. Because isolated auxiliary supplies are often expensive, it is beneficial to reduce the amount of supplies. One method to perform this is to use a bootstrap configuration for the high-side supply of the ADuM3224/ADuM4224. In this topology, the decoupling capacitor, C_A, acts as the energy storage for the high-side supply, and is filled whenever the low-side switch is closed, bringing GND_A to GND_B. During the charging time of C_A, the dv/dt of the V_{DDA} voltage must be controlled to reduce the possibility of glitches on the output. Keeping the dv/dt below 10 V/µs is recommended for the ADuM3224/ADuM4224. This can be controlled by introducing a series resistance, R_{BOOT}, into the charging path of C_A. As an example, if V_{AUX} is 12 V, C_A has a total capacitance of 10 µF, and the forward voltage drop of the bootstrap diode is 1 V.

$$V_{BOOT} = \frac{V_{AUX} - V_{D_{BOOT}}}{C_A \times dv/dt_{MAX}} = \frac{12\,\text{V} - 1\,\text{V}}{10\,\mu\text{F} \times 10\,\text{V}/\mu\text{s}} 0.11\Omega$$

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than 1 µs at the input, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output.

If the decoder receives no internal pulses for more than about 3 µs, the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default low state by the watchdog timer circuit. In addition, the outputs are in a low default state while the power is coming up before the UVLO threshold is crossed.

The ADuM3224/ADuM4224 are immune to external magnetic fields. The limitation on the ADuM3224/ADuM4224 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM3224/ADuM4224 is examined because it represents the most susceptible mode of operation. The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\ \Sigma\pi\ r_n^2,\ n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
r_n is the radius of the nth turn in the receiving coil (cm).
N is the number of turns in the receiving coil.

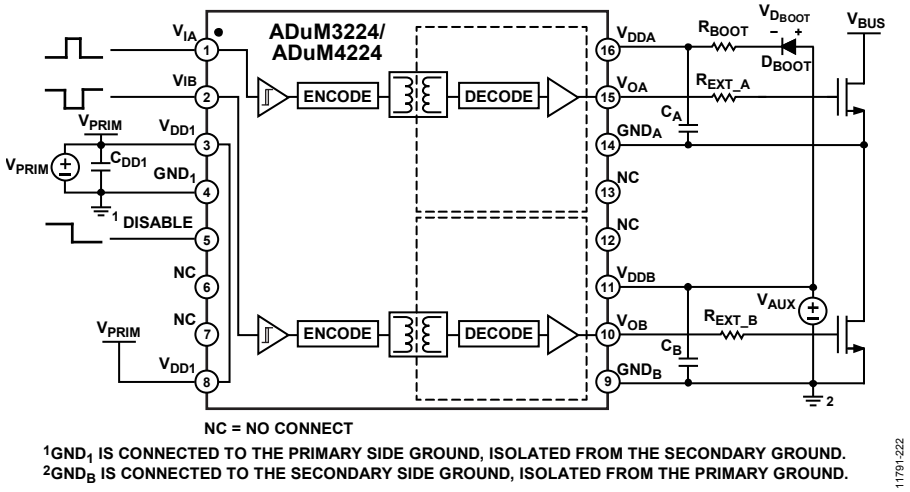


Figure 22. Circuit of Bootstrapped Half-Bridge Operation

Given the geometry of the receiving coil in the ADuM3224/ADuM4224 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 23.

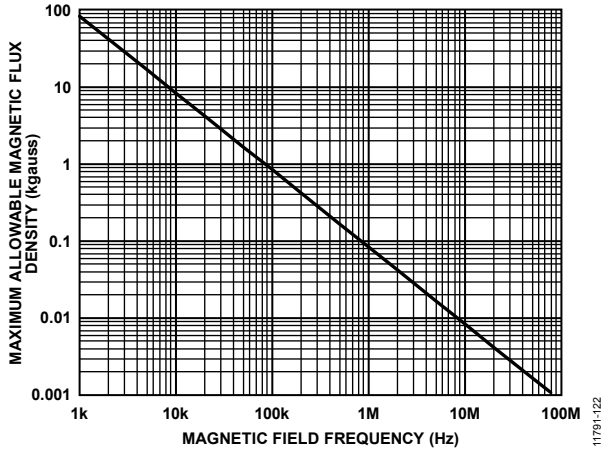


Figure 23. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.08 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and had the worst-case polarity), the received pulse is reduced from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM3224/ADuM4224 transformers. Figure 24 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 24, the ADuM3224/ADuM4224 are immune and only can be affected by extremely large currents operated at a high frequency and very close to the component. For the 1 MHz example, a 0.2 kA current must be placed 5 mm from the ADuM3224/ADuM4224 to affect the operation of the component.

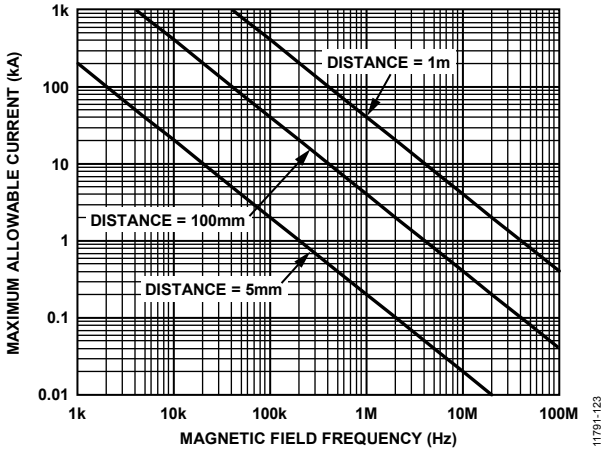


Figure 24. Maximum Allowable Current for Various Current-to-ADuM3224/ADuM4224 Spacings

POWER CONSUMPTION

The supply current at a given channel of the ADuM3224/ADuM4224 isolator is a function of the supply voltage, channel data rate, and channel output load.

During the driving of a MOSFET gate, the driver must dissipate power. This power is not insignificant and can lead to thermal shutdown (TSD) if considerations are not made. The gate of a MOSFET can be simulated approximately as a capacitive load. Due to Miller capacitance and other nonlinearities, it is common practice to take the stated input capacitance, C_{ISS}, of a given MOSFET and multiply it by a factor of 5 to arrive at a conservative estimate to approximate the load being driven. With this value, the estimated total power dissipation per channel due to switching action is given by

$$P_{DISS} = C_{EST} \times (V_{DDx})^2 \times f_S$$

where:
$C_{EST} = C_{ISS} \times 5$.
f_S is the switching frequency.

Alternately, use the gate charge to obtain a more precise value for P_{DISS}.

$$P_{DISS} = Q_{GATE} \times V_{DDx} \times f_S$$

where:
Q_{GATE} is the gate charge for the MOSFET.
f_S is the switching frequency.

This power dissipation is shared between the internal on resistances of the internal gate driver switches and the external gate resistances, R_{GON} and R_{GOFF}. The ratio of the internal gate resistances to the total series resistance allows the calculation of losses seen within the ADuM3224/ADuM4224 chips per channel.

$$P_{DISS\_IC} = P_{DISS} \times ½ \times (R_{DSON\_P}/(R_{EXT\_X} + R_{DSON\_P}) + R_{DSON\_N}/(R_{EXT\_X} + R_{DSON\_N}))$$

Taking the power dissipation found inside the chip and multiplying it by θ_{JA} gives the rise above ambient temperature that the ADuM3224/ADuM4224 experiences, multiplied by two to reflect that there are two channels.

$$T_J = \theta_{JA} \times 2 \times P_{DISS\_IC} + T_{AMB}$$

For the device to remain within specification, T_J must not exceed 125°C. If T_J exceeds 150°C (typical), the device enters TSD.

Quiescent power dissipation may also be added to give a more accurate number for temperature rise, but the switching power losses are often the largest source of power dissipation, and quiescent losses can often be ignored. To calculate the total supply current, the quiescent supply currents for each input and output channel corresponding to $I_{DD1(Q)}$, $I_{DDA(Q)}$, and $I_{DDB(Q)}$ are added. The full equation for the T_J becomes

$$T_J = \theta_{JA} \times (2 \times P_{DISS\_IC} + V_{DD1} \times I_{DD1(Q)} + V_{DDA} \times I_{DDA(Q)} + V_{DDB} \times I_{DDB(Q)}) + T_{AMB}$$

Figure 9 provides total input I_{DD1} supply current as a function of data rate for both input channels. Figure 10 provides total I_{DDA} or I_{DDB} supply current as a function of data rate for both outputs loaded with 2 nF capacitance.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM3224/ADuM4224.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 12 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM3224/ADuM4224 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 25, Figure 26, and Figure 27 illustrate these different isolation voltage waveforms.

A bipolar ac voltage environment is the worst case for the *i*Coupler products and is the 50-year operating lifetime that Analog Devices recommends for maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. Treat any cross insulation voltage waveform that does not conform to Figure 26 or Figure 27 as a bipolar ac waveform, and limit its peak voltage to the 50-year lifetime voltage value listed in Table 12.

Note that the voltage presented in Figure 26 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

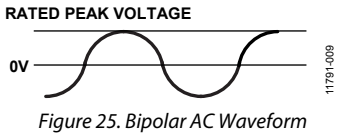


Figure 25. Bipolar AC Waveform

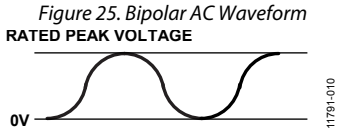


Figure 26. Unipolar AC Waveform

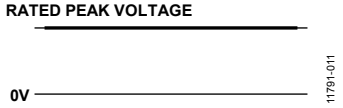
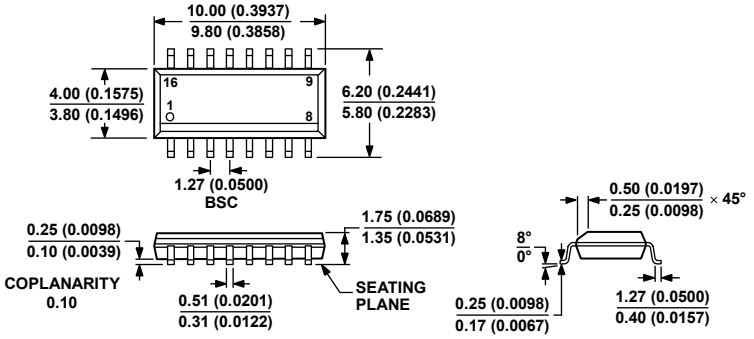


Figure 27. DC Waveform

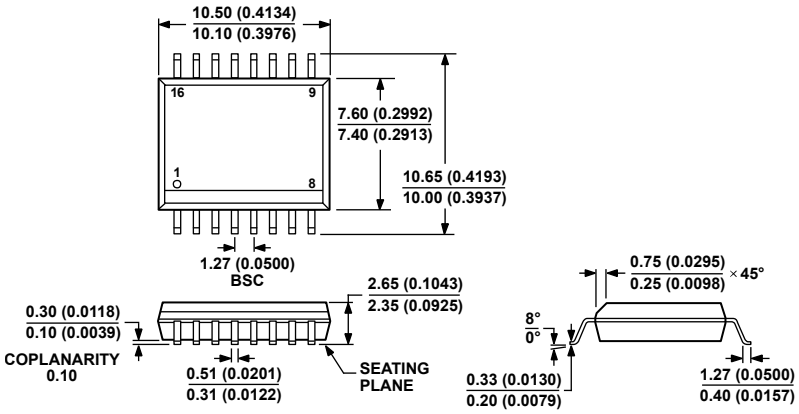
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 28. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

03-27-2007-B

Figure 29. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)