Isolated Half-Bridge Gate Driver with Integrated Isolated High-Side Supply

Data Sheet

ADuM6132

FEATURES

- ***iso*Power integrated isolated high-side supply**
- **275 mW isolated dc-to-dc converter**
- **200 mA output sink current, 200 mA output source current**
- **High common-mode transient immunity: >50 kV/µs**
- **Wide-body 16-lead SOIC package**
- **Safety and regulatory approvals**
  - **UL recognition**
    - **3750 V rms for 1 minute per UL 1577**
  - **CSA Component Acceptance Notice #5A**
    - **CSA/IEC 60950-1, 400 V rms**
  - **VDE certificate of conformity (pending)**
    - **DIN V VDE V 0884-10 (VDE V 0884-10):2006-12**
    - **V_{IORM} = 560 V peak**

APPLICATIONS

- **MOSFET/IGBT gate drivers**
- **Motor drives**
- **Solar panel inverters**
- **Power supplies**

GENERAL DESCRIPTION

The ADuM6132[1] is an isolated half-bridge gate driver that employs the Analog Devices, Inc., *i*Coupler® technology to provide an isolated high-side driver with an integrated 275 mW high-side supply. This supply, provided by an internal isolated dc-to-dc converter, powers not only the ADuM6132 high-side output but also any external buffer circuitry that is commonly used with the ADuM6132. This functionality eliminates the cost, space, and performance issues associated with external supply configurations such as a bootstrap circuit.

The architecture of the ADuM6132 isolates the high-side channel and the high-side power from the control and low-side interface circuitry. Care has been taken to ensure close matching between the high-side and low-side driver timing characteristics to reduce the need for a dead time margin.

In comparison to gate drivers that employ high voltage level translation methodologies, the ADuM6132 offers the benefit of true, galvanic isolation. The differential voltage between high-side and low-side channels can be as high as 800 V with good insulation lifetime (see Table 12).

*iso*Power® uses high frequency switching elements to transfer power through its transformer. Special care must be taken during printed circuit board (PCB) layout to meet emissions standards. Refer to the AN-0971 Application Note for information about board layout considerations.

FUNCTIONAL BLOCK DIAGRAM

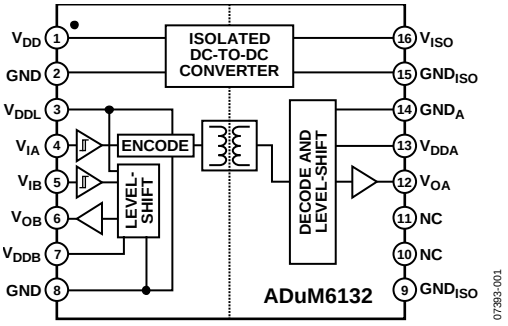

Figure 1.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; 7,075,329; and other pending patents.

Rev. B **Document Feedback**

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REVISION HISTORY

4/14—Rev. A to Rev. B

Change to Table 3 ... 4

6/12—Rev. 0 to Rev. A

Created Hyperlink for Safety and Regulatory Approvals Entry in Features Section ... 1
Changes to Regulatory Information Section and Table 3 ... 4
Change to PCB Layout Section ... 12
Updated Outline Dimensions ... 15

7/08—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

All voltages are relative to their respective ground; 4.5 V ≤ V_{DD} = V_{DDL} ≤ 5.5 V; 12.5 V ≤ V_{DDB} ≤ 17.0 V; V_{DDA} = V_{ISO}. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD} = V_{DDL} = 5.0 V, V_{DDB} = 15 V, V_{DDA} = V_{ISO}.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Isolated Power Supply						
Input Current, Quiescent	$I_{DD(Q)}$			280	mA	I_{ISO} = 0 mA, dc signal inputs
Input Current, Loaded	I_{DD}			350	mA	I_{ISO} = $I_{ISO(MAX)}$
Maximum Output Current[1]	$I_{ISO(MAX)}$	22			mA	12.5 V ≤ V_{ISO} ≤ 17.0 V
Output Voltage	V_{ISO}	12.5	15	17	V	0 mA ≤ I_{ISO} ≤ 22 mA
Logic Supply						
Input Current	I_{DDL}		1.8	3.0	mA	
Output Supplies, Channel A or Channel B[2]						
Supply Current, Quiescent	$I_{DDA(Q)}$, $I_{DDB(Q)}$		1.0	2.0	mA	
Supply Current, f_{IN} = 20 kHz	$I_{DDA(20)}$, $I_{DDB(20)}$		1.1	2.1	mA	C_L = 200 pF
Supply Current, f_{IN} = 100 kHz	$I_{DDA(100)}$, $I_{DDB(100)}$		1.3	2.3	mA	C_L = 200 pF
Supply Current, f_{IN} = 1000 kHz	$I_{DDA(1000)}$, $I_{DDB(1000)}$		4.5	5.5	mA	C_L = 200 pF
Logic Inputs, Channel A or Channel B						
Input Current	I_{IA}, I_{IB}	−10	+0.01	+10	μA	0 V ≤ V_{IA}, V_{IB} ≤ 5.5 V
Logic High Input Voltage	V_{IAH}, V_{IBH}	0.7 × V_{DDL}			V	
Logic Low Input Voltage	V_{IAL}, V_{IBL}			0.3 × V_{DDL}	V	
Outputs, Channel A or Channel B						
Channel A High Level Output Voltage	V_{OAH}	V_{DDA} − 0.1			V	I_{OAH} = −1 mA
Channel B High Level Output Voltage	V_{OBH}	V_{DDB} − 0.1			V	I_{OBH} = −1 mA
Low Level Output Voltages	V_{OAL},V_{OBL}			0.1	V	I_{OAL}, I_{OBL} = 1 mA
High Level Output Current, Peak[3]	I_{OAH}, I_{OBH}	200			mA	
Low Level Output Current, Peak[3]	I_{OAL}, I_{OBL}	200			mA	
Undervoltage Lockout, V_{DDA} or V_{DDB} Supply[4]						
Positive Going Threshold	V_{DDAUV+}, V_{DDBUV+}	11.0	11.7	12.3	V	
Negative Going Threshold	V_{DDAUV-}, V_{DDBUV-}	10.0	10.7	11.2	V	
Hysteresis	V_{DDAUVH}, V_{DDBUVH}		1.0		V	
Undervoltage Lockout, V_{DDL} Supply[4]						
Positive Going Threshold	V_{DDLUV+}	3.5		4.2	V	
Negative Going Threshold	V_{DDLUV-}	3.1		3.8	V	
Hysteresis	V_{DDLUVH}		0.5		V	
SWITCHING SPECIFICATIONS						
Minimum Pulse Width[1]	PW			50	ns	C_L = 200 pF
Maximum Switching Frequency[1]	f_{IN}	1000			kHz	C_L = 200 pF
Propagation Delay[1]	t_{PHL}, t_{PLH}	40	60	100	ns	C_L = 200 pF
Change vs. Temperature			100		ps/°C	
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$	PWD			10	ns	C_L = 200 pF
Channel-to-Channel Matching, Rising or Falling Matching Edge Polarity[1]	t_{M2}			20	ns	C_L = 200 pF
Channel-to-Channel Matching, Rising vs. Falling Opposite Edge Polarity[1]	t_{M1}			20	ns	C_L = 200 pF

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Part-to-Part Matching[1]				60	ns	C_L = 200 pF
Output Rise Time (10% to 90%)	t_R			15	ns	C_L = 200 pF
Output Fall Time (10% to 90%)	t_F			15	ns	C_L = 200 pF

[1] See the Terminology section.
[2] I_{DDA} is supplied by the output of the integrated isolated dc-to-dc power supply. I_{DDB} is supplied by an external power connection to the V_{DDB} pin. See Figure 16.
[3] Duration less than 1 second. Average output current must conform to the limit shown in the Absolute Maximum Ratings section.
[4] Undervoltage lockout (UVLO) holds the outputs in a low state if the corresponding input or output power supply is below the referenced threshold. Hysteresis is built into the detection threshold to prevent oscillations and noise sensitivity.

PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input Side to High-Side Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input Side to High-Side Output)[1]	C_{I-O}		2.0		pF	
Input Capacitance	C_I		4.0		pF	
Junction-to-Ambient Thermal Resistance	θ_{JA}		45		°C/W	4-layer PCB

[1] The device is considered a two-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

REGULATORY INFORMATION

Table 3.

UL	CSA	VDE (Pending)
Recognized under UL 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single protection, 3750 V rms isolation voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 250 V rms (354 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM6132 is proof-tested by applying an insulation test voltage ≥ 4500 V rms for 1 second (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM6132 is proof-tested by applying an insulation test voltage ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3750	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	>8.0	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	>8.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

The ADuM6132 is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on the package denotes DIN V VDE V 0884-10 approval.

Table 5.

Parameter	Test Conditions/Comments	Symbol	Value	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge <5 pC	V_{PR}	1050	V peak
Input-to-Output Test Voltage, Method A		V_{PR}		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge <5 pC		896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge <5 pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{TR}	6000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	555	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	>109	Ω

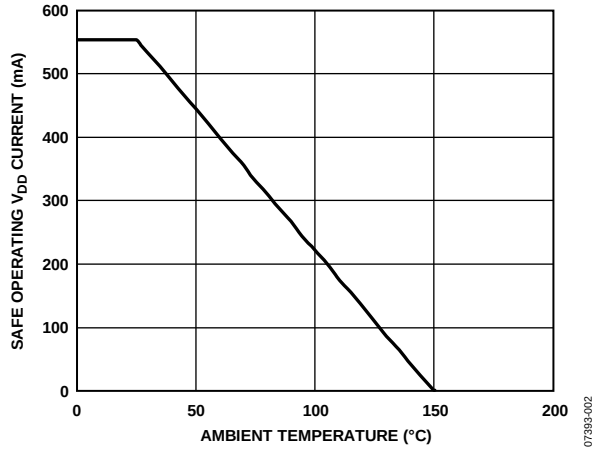

Figure 2. Thermal Derating Curve, Dependence of Safety-Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 6.

Parameter	Rating
Operating Temperature Range, T_A	−40°C to +85°C
Input Supply Voltage, V_{DD} and V_{DDL}[1]	4.5 V to 5.5 V
Channel A, Channel B Supply Voltage, V_{DDA} and V_{DDB}[1]	12.5 V to 17 V
Input Signal Rise and Fall Times	1 ms
Common-Mode Transient Immunity, Input to Output	−50 kV/µs to +50 kV/µs
Minimum Power-On Slew Rate (P_{SLEW}), V_{DD} and V_{DDL}[2]	1 V/ms

[1] All voltages are relative to their respective ground.
[2] The ADuM6132 power supply may fail to properly initialize if V_{DD} and V_{DDL} are applied too slowly. The power supply slew rate must be faster than specified over the entire turn-on ramp. Power-on should start from a completely discharged state.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
Storage Temperature Range, T_{ST}	−55°C to +150°C
Ambient Operating Temperature Range, T_A	−40°C to +85°C
Input Supply Voltage, V_{DDL}, V_{DD}[1]	−0.5 V to +7.0 V
Channel A, Channel B Supply Voltage, V_{DDA}, V_{DDB}[1]	−0.5 V to +27 V
Input Voltage, V_{IA}, V_{IB}[1]	−0.5 V to V_{DDL} + 0.5 V
Output Voltage, V_{OA}[1]	−0.5 V to V_{ISO} + 0.5 V
Output Voltage, V_{OB}[1]	−0.5 V to V_{DDB} + 0.5 V
Average DC Output Current, I_{OA}, I_{OB}	−10 mA to +10 mA
Peak Output Current, I_{OA}, I_{OB}	−200 mA to +200 mA
Common-Mode Transients[2]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] Refers to common-mode transients across any insulation barrier. Common-mode transients exceeding the absolute maximum ratings can cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

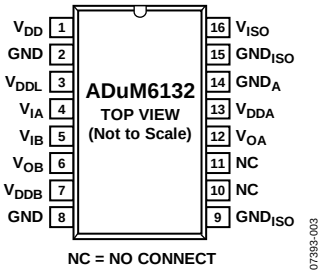

Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Input Supply Voltage for Isolated Power Supply, 4.5 V to 5.5 V.
2, 8	GND	Ground Reference for Isolated Power Supply Input and Logic Inputs.
3	V_{DDL}	Input Supply Voltage for Logic, 4.5 V to 5.5 V.
4	V_{IA}	Logic Input A.
5	V_{IB}	Logic Input B.
6	V_{OB}	Output B (Nonisolated).
7	V_{DDB}	Output B Supply Voltage Input (Nonisolated), 12.5 V to 17 V.
9, 15	GND_{ISO}	Ground Reference for Isolated Power Supply Output.
10, 11	NC	No Connect.
12	V_{OA}	Output A (Isolated).
13	V_{DDA}	Output A Supply Voltage Input. Must be connected externally to V_{ISO} (Pin 16).
14	GND_A	Output A Ground Reference. Must be connected externally to GND_{ISO} (Pin 15).
16	V_{ISO}	Isolated Power Supply Voltage Output.

Table 9. Truth Table (Positive Logic)[1]

V_{IA} Input	V_{IB} Input	V_{DDL} State	V_{DDB} State	V_{OA} Output	V_{OB} Output	Notes
L	L	Powered	Powered	L	L	
L	H	Powered	Powered	L	H	
H	L	Powered	Powered	H	L	
H	H	Powered	Powered	H	H	
X	X	Unpowered	Powered	L	L	V_{OA} returns to input state within 1 µs of V_{DDL} power restoration
X	X	Powered	Unpowered	L	L	

[1] L = low; H = high; X = high or low.

TYPICAL PERFORMANCE CHARACTERISTICS

All typical performance curves are based on operation at T_A = 25°C, unless otherwise noted.

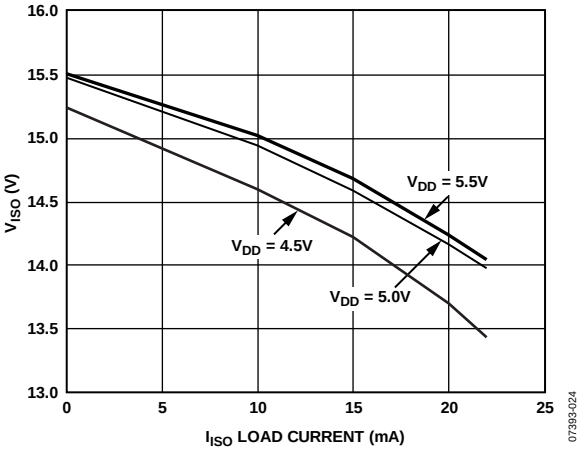

Figure 4. Typical V_{ISO} Supply Voltage vs. I_{ISO} External Load

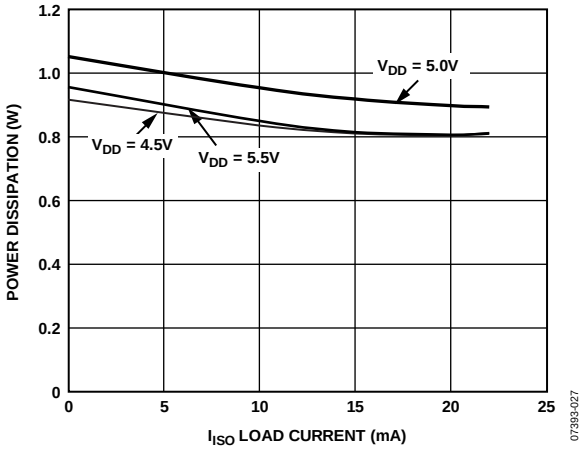

Figure 7. Typical Total Power Dissipation vs. I_{ISO} External Load

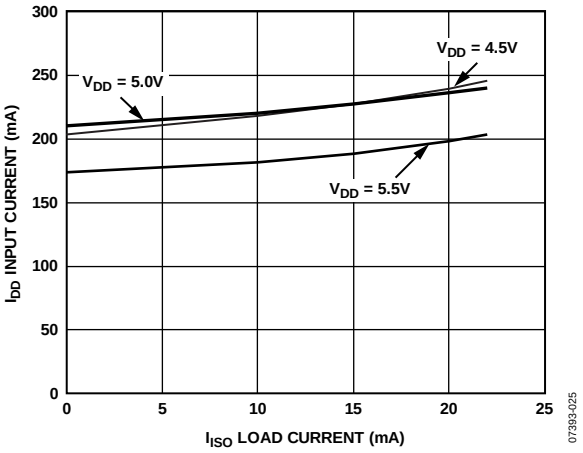

Figure 5. Typical I_{DD} Supply Current vs. I_{ISO} External Load

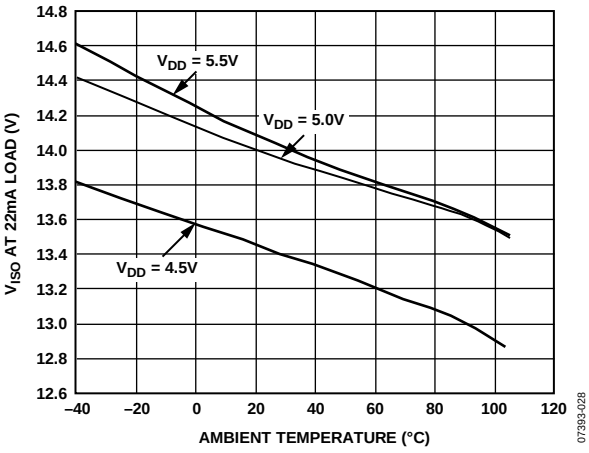

Figure 8. Typical V_{ISO} Output Voltage at Maximum Combined Load over Temperature

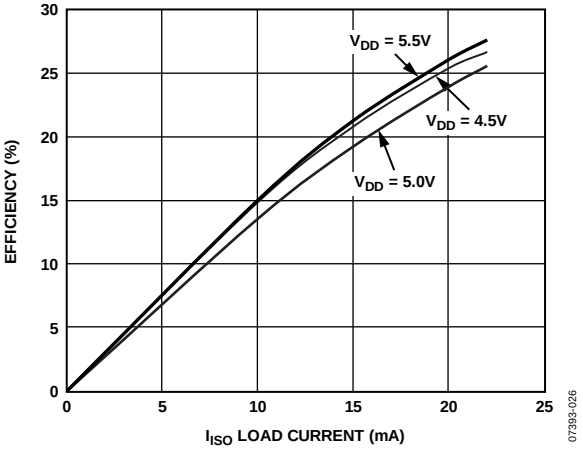

Figure 6. Typical V_{ISO} Supply Efficiency vs. I_{ISO} External Load

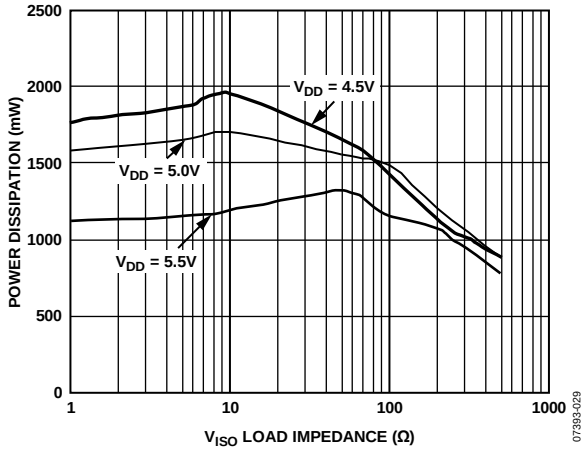

Figure 9. Power Dissipation vs. Load Impedance for Fault Conditions

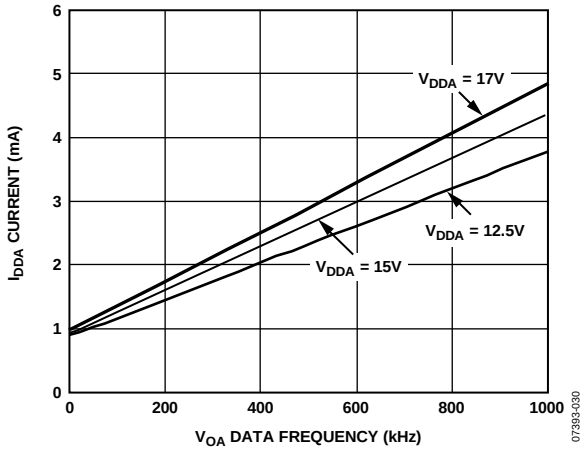

Figure 10. Typical I_{DDA} Supply Current, C_L = 200 pF

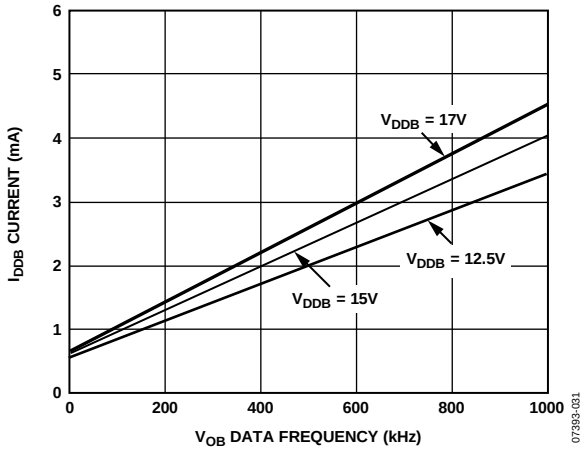

Figure 11. Typical I_{DDB} Supply Current, C_L = 200 pF

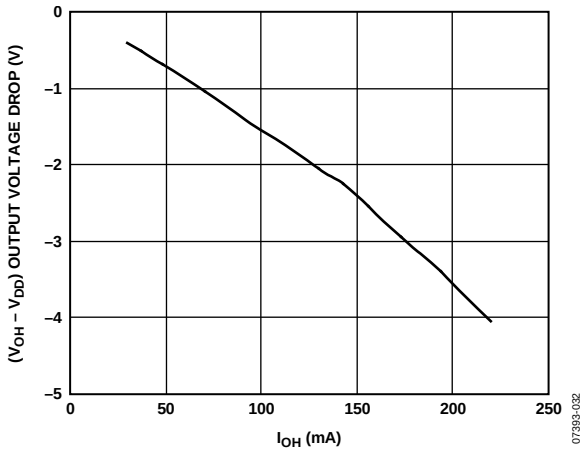

Figure 12. Typical V_{OH} Voltage Drop vs. I_{OH} (V_{DD} = V_{DDL} = 5 V, V_{DDA} = V_{DDB} = 12 V to 17 V)

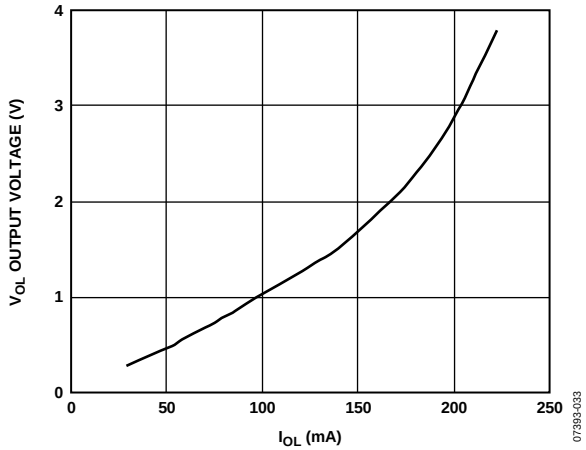

Figure 13. Typical V_{OL} vs. I_{OL} (V_{DD} = V_{DDL} = 5 V, V_{DDA} = V_{DDB} = 12 V to 17 V)

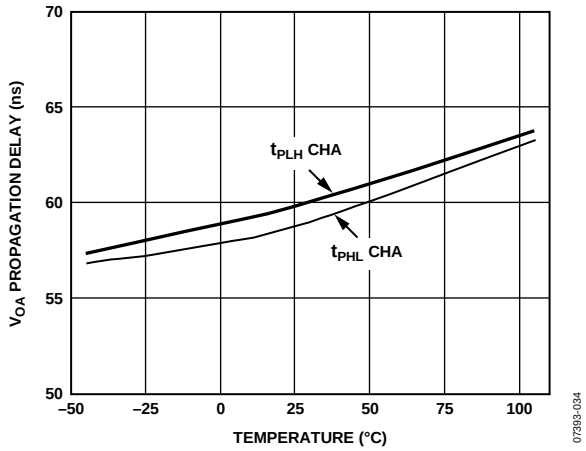

Figure 14. Typical Channel A Propagation Delay vs. Temperature

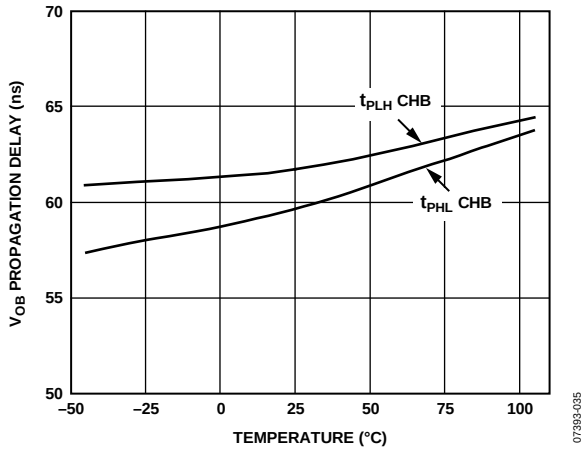

Figure 15. Typical Channel B Propagation Delay vs. Temperature

TERMINOLOGY

Channel-to-Channel Matching
Channel-to-channel matching with rising or falling matching edge polarity is the magnitude of the propagation delay difference between two channels of the same part when the inputs are both rising edges or both falling edges. The loads on each channel are equal.

Channel-to-channel matching with rising vs. falling opposite edge polarity is the magnitude of the propagation delay difference between two channels of the same part when one input is a rising edge and one input is a falling edge. The loads on each channel are equal.

Maximum Output Current
The maximum output current is the maximum isolated supply current that the ADuM6132 can provide. This current supports external loads as well as the needs of the ADuM6132 Channel A output circuitry. This is achieved via external connection of the V_{ISO} pin to the V_{DDA} pin and of the GND_{ISO} pin to the GND_A pin (see Figure 16). The net current available to power external loads is the ADuM6132 output current, I_{ISO}, minus the Channel A supply current, I_{DDA}.

Maximum Switching Frequency
The maximum switching frequency is the maximum signal frequency at which the specified timing parameters are guaranteed. Operation beyond the maximum switching frequency is not recommended, because high switching rates can cause droop in the output supply voltage.

Minimum Pulse Width
The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed. Operation below the minimum pulse width is not recommended.

Part-to-Part Matching
Part-to-part matching is the magnitude of the propagation delay difference between the same channels of two different parts. This includes rising vs. rising edges, falling vs. falling edges, or rising vs. falling edges. The supply voltages, temperatures, and loads of each part are equal.

Propagation Delay
The propagation delay is the time that it takes a logic signal to propagate through a component. The propagation delay to a logic low output may differ from the propagation delay to a logic high output.

The t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{IA} or V_{IB} signal to the 50% level of the falling edge of the V_{OA} or V_{OB} signal. The t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{IA} or V_{IB} signal to the 50% level of the rising edge of the V_{OA} or V_{OB} signal.

Capacitive Load (C_L)
The output capacitive load simulates a typical FET, IGBT, or buffer for timing or current measurements. This load includes all discrete and parasitic capacitive loads on the output.

APPLICATIONS INFORMATION

TYPICAL APPLICATION USAGE

The architecture of the ADuM6132 is ideal for motor drive and inverter applications where the low-side channels are common to the controller. This arrangement requires only two isolation regions in a package. All the isolated signals and the isolated power are grouped on one side of the package to maintain full package creepage and clearance. The low-side driver, as well as the control signals, share a common reference and are also grouped.

To maximize the effectiveness of external bypass capacitors, the *iso*Power dc-to-dc converter is not internally tied to the data channels, and should be treated as a completely independent subsystem, except for a UVLO function (see the Undervoltage Lockout section). This means that power must be applied to V_{DD} to operate the dc-to-dc converter. Power must also be applied to V_{DDL} and V_{DDB} to operate the data input and the Channel B driver output. On the secondary side, the power generated at the V_{ISO} pin must be applied as an input power supply to the V_{DDA} pin. GND_{ISO} and GND_A must also be connected.

The ADuM6132 is intended for use in driving low gate capacitance transistors (200 pF typically). Most high voltage applications involve larger transistors than this. To accommodate these applications, users can implement a buffer configuration with the ADuM6132, as shown in Figure 16. In many cases, this buffer configuration is the least expensive option to drive high capacitance devices and provides the greatest amount of design flexibility. The precise buffer/high voltage transistor combination can be selected to suit the requirements of the application.

PCB LAYOUT

The ADuM6132 digital isolator with integrated 275 mW *iso*Power dc-to-dc converter requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 17). The power supply section of the ADuM6132 uses a very high oscillator frequency to efficiently pass power through its chip scale transformers. In addition, the normal operation of the data section of the *i*Coupler introduces switching transients on the power supply pins. Bypass capacitors are required for several operating frequencies. Noise suppression requires a low ESR, high frequency capacitor; ripple suppression and proper regulation require a large value capacitor in parallel (see Table 10). The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

Table 10. Recommended Bypass Capacitors

Supply	Pins	Bypass Capacitors
V_{DD}	1, 2	0.1 µF, 10 µF
V_{DDB}	7, 8	0.1 µF
V_{DDL}	2, 3	0.1 µF
V_{DDA}	13, 14	0.1 µF
V_{ISO}	15, 16	0.1 µF, 10 µF

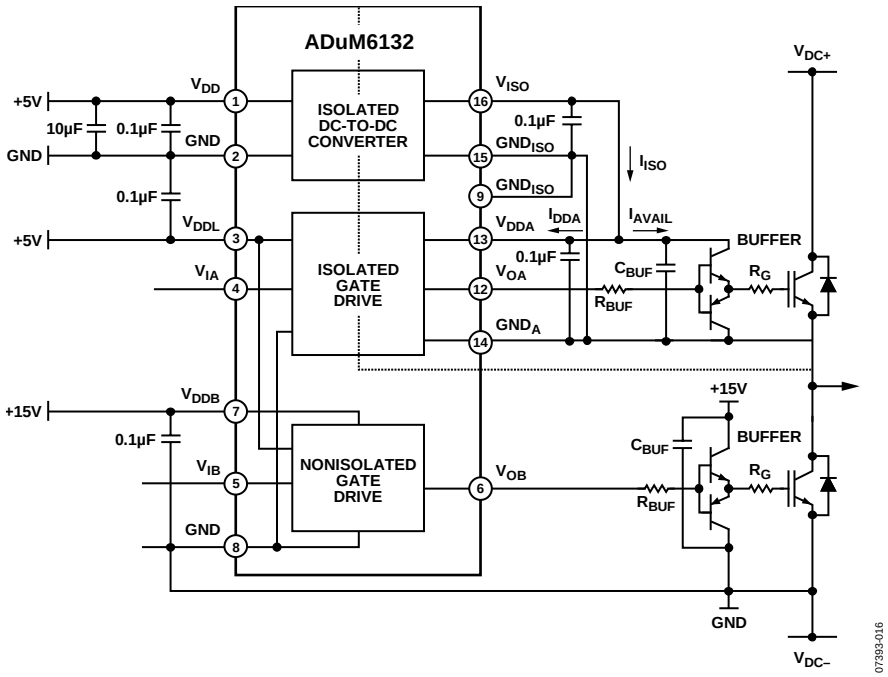

Figure 16. Typical Application Circuit

In applications involving high common-mode transients, care should be taken to ensure that board capacitive coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed so that any coupling that does occur affects all pins on a given component side equally. Failure to ensure this may cause voltage differentials between pins that exceed the absolute maximum ratings of the device (see Table 7), leading to latch-up or permanent damage.

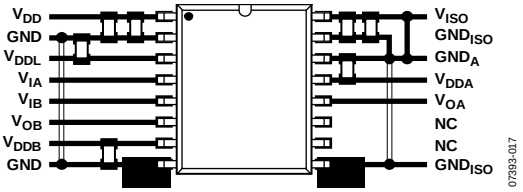

Figure 17. Recommended PCB Layout

The ADuM6132 is a power device that dissipates approximately 1 W of power when fully loaded and running at maximum speed. Because it is not possible to apply a heat sink to an isolation device, the device depends primarily on heat dissipation into the PCB through the GND pins. If the device will be used at high ambient temperatures, provide a thermal path from the GND pins to the PCB ground plane.

The board layout in Figure 17 shows enlarged pads for Pin 8 (GND) and Pin 9 (GND_{ISO}). Multiple vias should be implemented from the pad to the ground plane. This layout significantly reduces the temperatures inside the chip. The dimensions of the expanded pads are left to the discretion of the designer and the available board space. See the AN-0971 Application Note for board layout recommendations.

THERMAL ANALYSIS

The ADuM6132 consists of several internal die attached to two lead frame paddles. For the purposes of thermal analysis, the part is treated as a thermal unit with the highest junction temperature determining θ_{JA}, as shown in Table 2. The value of θ_{JA} is based on measurements taken with the part mounted on a JEDEC standard 4-layer board with fine width traces and still air. Under normal operating conditions, the ADuM6132 operates at full load across the full temperature range without derating the output current. However, following the recommendations in the PCB Layout section decreases the thermal resistance to the PCB, allowing increased thermal margin at high ambient temperatures.

Under V_{ISO} output short-circuit conditions, as shown in Figure 9, the package power dissipation quickly exceeds the safe operating limit of 1.44 W for ambient temperatures up to 85°C. At low input voltage, the power dissipation can approach 2 W. Because internal compensation of the PWM makes low V_{DD} a worst-case condition, input voltage limiting is not an effective strategy for protecting the ADuM6132 from output load fault conditions. Therefore, the preferred protection methods, where required, are either limiting ambient temperature to 60°C or the use of a fuse.

UNDERVOLTAGE LOCKOUT

The ADuM6132 has undervoltage lockout (UVLO) circuits on the V_{DDL}, V_{DDA}, and V_{DDB} supplies. For each supply, the respective UVLO circuit monitors the supply voltage and takes a predetermined action based on whether the supply voltage is above or below a given threshold. These thresholds are specified in Table 1.

In the recommended configuration shown in Figure 16, only two independent supplies are controlled by the user: V_{DDB} and V_{DDL}/V_{DD} ($V_{DDL} = V_{DD}$ in Figure 16). V_{DDA} is supplied by the internal dc-to-dc converter via the $V_{ISO} = V_{DDA}$ external connection. Nevertheless, the V_{DDA} UVLO functionality is included in Table 11 to show how the V_{OA} output behaves when the internal dc-to-dc converter powers on and off.

Table 11. Undervoltage Lockout Functionality[1]

User-Provided Supplies		V_{ISO} Powered Supply	
V_{DDL}	V_{DDB}	V_{DDA}	Effect
H	H	H	Normal operation. Internal dc-to-dc converter is active. V_{OA}/V_{OB} output logic states match V_{IA}/V_{IB} input logic states.
H	H	L	Internal dc-to-dc converter is active but V_{ISO} is below UVLO threshold. V_{OA} output is driven low. V_{OB} output operates normally.
X	L	X	Internal dc-to-dc converter is turned off (V_{ISO} = 0 V). V_{OA} output is driven low. V_{OB} output is driven low.
L	X	X	Internal dc-to-dc converter is turned off (V_{ISO} = 0 V). V_{OA} output is driven low. V_{OB} output is driven low.

[1] H: supply voltage > UVLO threshold; L: supply voltage < UVLO threshold; X: supply voltage level is irrelevant.

When all three supplies are above their respective UVLO thresholds, the ADuM6132 operates normally. The internal dc-to-dc converter is active, and both outputs operate as determined by their respective input logic signals. If either of the user-provided supplies is below its UVLO threshold, the ADuM6132 is put into a disabled mode. In this mode, the internal dc-to-dc converter is turned off and both outputs are driven low.

The V_{OB} output is driven low by either the V_{DDL} or V_{DDB} UVLO circuit (whichever is below its threshold). The V_{OA} output is driven low when the internal dc-to-dc converter is turned off. The V_{ISO} supply voltage drops to 0 V, causing V_{DDA} to drop also because V_{ISO} and V_{DDA} are externally connected. When V_{DDA} is below its UVLO threshold, the V_{DDA} UVLO circuit drives V_{OA} low.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output may differ from the propagation delay to a logic high output.

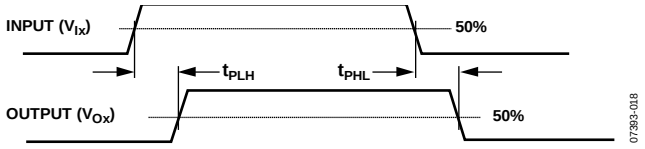

Figure 18. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM6132 component.

MAGNETIC FIELD IMMUNITY

The ADuM6132 is extremely immune to external magnetic fields. The limitation on the ADuM6132 magnetic field immunity is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to falsely set or reset the decoder. The following analysis defines the conditions under which this may occur.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at approximately 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\ \Sigma\pi r_n^2\ ;\ n = 1, 2, \ldots N$$

where:

β is the magnetic flux density (gauss).
r_n is the radius of the nth turn in the receiving coil (cm).
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM6132 and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic flux density is calculated, as shown in Figure 19.

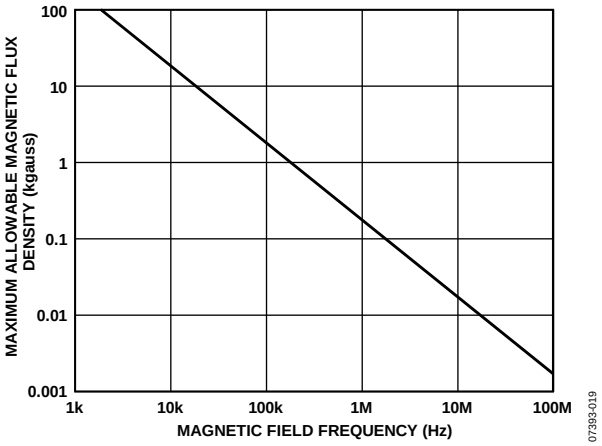

Figure 19. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic flux density of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This voltage is approximately 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (with the worst-case polarity), the received pulse is reduced from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM6132 transformers. Figure 20 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 20, the ADuM6132 is extremely immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For example, at a magnetic field frequency of 1 MHz, a 0.5 kA current would need to be placed 5 mm away from the ADuM6132 to affect the operation of the component.

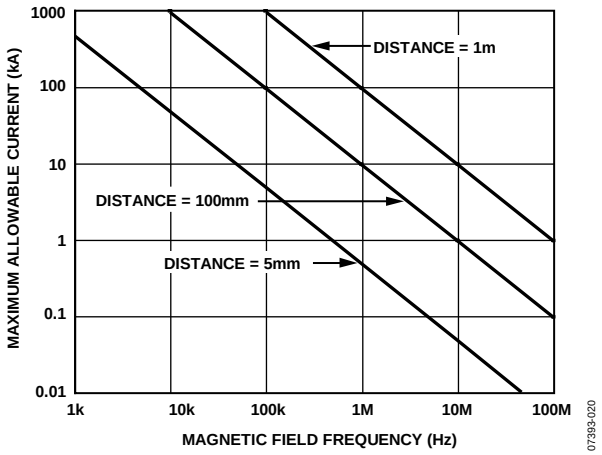

Figure 20. Maximum Allowable Current for Various Current-to-ADuM6132 Spacings

Note that in the presence of strong magnetic fields and high frequencies, any loops formed by PCB traces may induce sufficiently large error voltages to trigger the threshold of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation depends on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM6132.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. Table 12 summarizes the recommended peak working voltages for 50 years and 15 years of service life for various operating conditions evaluated by Analog Devices. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM6132 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 21, Figure 22, and Figure 23 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the bipolar ac condition determines the maximum working voltage recommended by Analog Devices.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower, which allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 12 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage cases.

Any cross-insulation voltage waveform that does not conform to Figure 22 or Figure 23 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 12. Note that the voltage shown in Figure 22 is sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

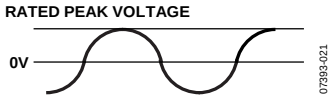

Figure 21. Bipolar AC Waveform

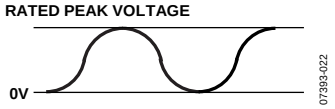

Figure 22. Unipolar AC Waveform

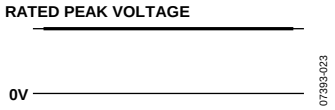

Figure 23. DC Waveform

Table 12. Maximum Continuous Working Voltage[1]

Parameter	Peak Voltage	Lifetime
AC Voltage, Bipolar Waveform	424 V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform		
Basic Insulation	800 V peak	15-year minimum lifetime
Basic Insulation	660 V peak	50-year minimum lifetime
DC Voltage Waveform		
Basic Insulation	800 V peak	15-year minimum lifetime
Basic Insulation	660 V peak	50-year minimum lifetime

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

OUTLINE DIMENSIONS

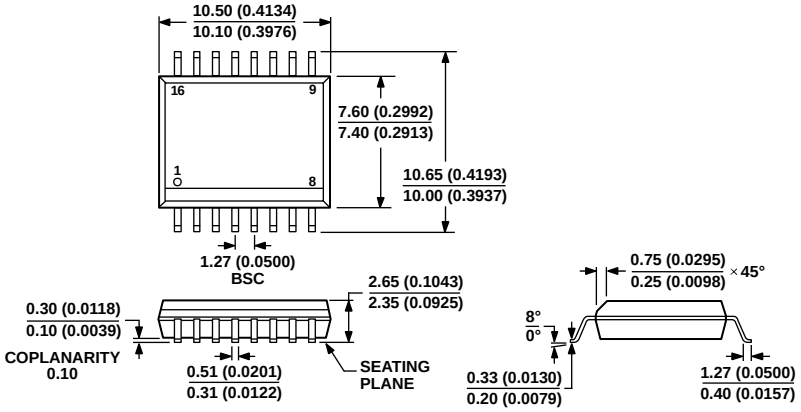

Figure 24. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	No. of Channels	Output Peak Current (A)	Output Voltage (V)	Temperature Range	Package Description	Package Option
ADuM6132ARWZ	2	0.2	15	−40°C to +85°C	16-Lead SOIC_W	RW-16
ADuM6132ARWZ-RL	2	0.2	15	−40°C to +85°C	16-Lead SOIC_W, 13-inch Tape and Reel Option (1,000 Units)	RW-16

[1] Z = RoHS Compliant Part.