Quad-Channel Isolators with Integrated DC-to-DC Converter

Data Sheet **ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A**

FEATURES

- *iso*Power integrated, isolated dc-to-dc converter
- 100 mA output supply
- AEC-Q100 qualified for automotive applications
  - ADuM6421AW (ADuM6423AW pending)
- Meets CISPR 32/EN55032 Class B emission limits up to
  - 5 Mbps at a full load on a 2-layer PCB
- Quad dc to 100 Mbps signal isolation channels
- 28-lead, fine pitch, SOIC with 8.3 mm minimum creepage
- High temperature operation: 125°C maximum
- High common-mode transient immunity: 100 kV/µs
- Safety and regulatory approvals (pending)
  - UL recognition (pending)
    - 5000 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A (pending)
  - VDE V 0884-11 certificate of conformity (pending)
    - V_{IORM} = 566 V peak
  - CQC certification per GB4943.1-2011 (pending)

APPLICATIONS

- RS-232 transceivers
- Power supply start-up bias and gate drives
- Isolated sensor interfaces
- Automotive on-board charger (OBC) and dc to dc
- Industrial programmable logic controllers (PLCs)

FUNCTIONAL BLOCK DIAGRAM

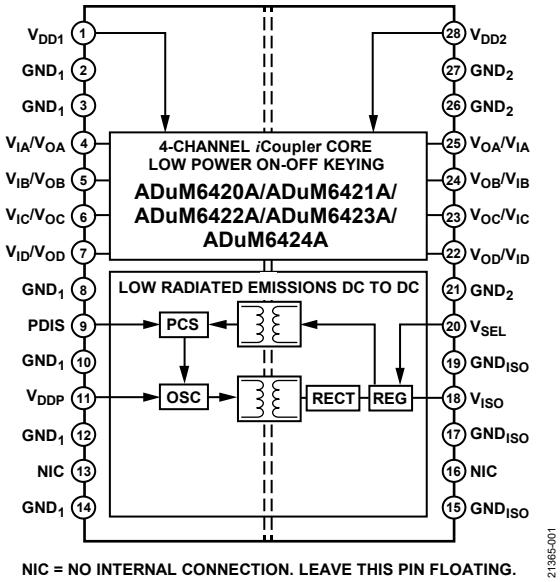

Figure 1.

GENERAL DESCRIPTION

The ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A[1] are quad-channel digital isolators with an *iso*Power®, integrated, isolated dc-to-dc converter. Based on the Analog Devices, Inc., *i*Coupler® technology, the dc-to-dc converter provides regulated, isolated power that meets CISPR 32/EN 55032 Class B limits at a full load on a 2-layer printed circuit board (PCB) with ferrites. Popular voltage combinations and the associated output current levels are listed in Table 1.

The ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A eliminate the need for a separate, isolated dc-to-dc converter in 500 mW, isolated designs. The *i*Coupler chip scale transformer technology is used for isolated logic signals and for the magnetic components of the dc-to-dc converter. The result is a small form factor, total isolation solution.

The ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A isolators provide four independent isolation channels (see the Pin Configurations and Function Descriptions for additional information).

Table 1. ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A Output Current Levels

		ISO Current, I_{ISO} (mA)		
V_{DDP} (V)	V_{ISO} (V)	85°C	105°C	125°C
5	5	100	65	30
5	3.3	100	65	30
3.3	3.3	60	60	20

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/5 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DDP} = V_{ISO} = 5 V. Minimum and maximum specifications apply over the entire recommended operation range, which is 4.5 V ≤ (V_{DDP}, V_{ISO}) ≤ 5.5 V and −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 2. DC-to-DC Converters Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTERS SUPPLY						
Setpoint	V_{ISO}	4.75	5.0	5.25	V	ISO current (I_{ISO}) = 10 mA
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 50 mA, V_{DDP} = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1	5	%	I_{ISO} = 10 mA to 90 mA
Output Ripple	$V_{ISO (RIP)}$		75		mV p-p	20 MHz bandwidth, bulk output capacitance (C_{BO}) = 0.1 µF||10 µF, I_{ISO} = 90 mA
Output Noise	$V_{ISO (NOISE)}$		200		mV p-p	C_{BO} = 0.1 µF||10 µF, I_{ISO} = 90 mA
Switching Frequency	f_{OSC}		180		MHz	
Pulse-Width Modulation (PWM) Frequency	f_{PWM}		625		kHz	
Output Supply[1]	$I_{ISO (MAX)}$	100			mA	4.5 V < V_{ISO} < 5.25 V
		50			mA	4.75 V < V_{ISO} < 5.25 V
Efficiency at $I_{ISO (MAX)}$[1]			34		%	I_{ISO} = 100 mA
V_{DD1} Supply Current						
No V_{ISO} Load	$I_{DDP (Q)}$		14	25	mA	
Full V_{ISO} Load	$I_{DDP (MAX)}$		310		mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

[1] Maximum V_{ISO} output current is derated by 1.75 mA/°C for T_A > 85°C.

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DDP} = 5.0 V, V_{ISO} = 3.3 V. Minimum and maximum specifications apply over the entire recommended operation range, which is 4.5 V ≤ V_{DDP} ≤ 5.5 V, 3.0 V ≤ V_{ISO} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 3. DC-to-DC Converters Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTERS SUPPLY						
Setpoint	V_{ISO}	3.135	3.3	3.465	V	I_{ISO} = 10 mA
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 50 mA, V_{DDP} = 3.0 V to 3.6 V
Load Regulation	$V_{ISO (LOAD)}$		1	5	%	I_{ISO} = 10 mA to 90 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF||10 µF, I_{ISO} = 90 mA
Output Noise	$V_{ISO (NOISE)}$		130		mV p-p	C_{BO} = 0.1 µF||10 µF, I_{ISO} = 90 mA
Switching Frequency	f_{OSC}		180		MHz	
Pulse-Width Modulation Frequency	f_{PWM}		625		kHz	
Output Supply[1]	$I_{ISO (MAX)}$	100			mA	3.0 V < V_{ISO} < 3.4 V
		50			mA	3.135 V < V_{ISO} < 3.465 V
Efficiency at $I_{ISO (MAX)}$[1]			34		%	I_{ISO} = 100 mA
V_{DDP} Supply Current						
No V_{ISO} Load	$I_{DDP (Q)}$		14	20	mA	
Full V_{ISO} Load	$I_{DDP (MAX)}$		250		mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

[1] Maximum V_{ISO} output current is derated by 1.75 mA/°C for T_A > 85°C.

ELECTRICAL CHARACTERISTICS—3.3 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DDP} = V_{ISO} = 3.3 V. Minimum and maximum specifications apply over the entire recommended operation range, which is 3.0 V ≤ V_{DDP}, V_{ISO} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 4. DC-to-DC Converters Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTERS SUPPLY						
Setpoint	V_{ISO}	3.135	3.3	3.465	V	I_{ISO} = 10 mA
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 30 mA, V_{DDP} = 3.0 V to 3.6 V
Load Regulation	$V_{ISO (LOAD)}$		1	5	%	I_{ISO} = 6 mA to54 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF||10 µF, I_{ISO} = 60 mA
Output Noise	$V_{ISO (NOISE)}$		130		mV p-p	C_{BO} = 0.1 µF||10 µF, I_{ISO} = 60 mA
Switching Frequency	f_{OSC}		180		MHz	
Pulse-Width Modulation Frequency	f_{PWM}		625		kHz	
Output Supply[1]	$I_{ISO (MAX)}$	60			mA	3.0 V < V_{ISO} < 3.465 V
		30			mA	3.135 V < V_{ISO} < 3.465 V
Efficiency at $I_{ISO (MAX)}$[1]			34		%	I_{ISO} = 60 mA
V_{DDP} Supply Current						
No V_{ISO} Load	$I_{DDP (Q)}$		14	20	mA	
Full V_{ISO} Load	$I_{DDP (MAX)}$		190		mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

[1] Maximum V_{ISO} output current is derated by 2.0 mA/°C for T_A > 105°C.

ELECTRICAL CHARACTERISTICS—5.0 V OPERATION DIGITAL ISOLATOR CHANNELS ONLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5.0 V. Minimum and maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} , V_{DD2} ≤ 5.5 V and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 5. Data Channel Supply Current Specifications

		1 Mbps			10 Mbps			100 Mbps				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT												C_L = 0 pF
ADuM6420ABRNZ5												
	I_{DD1}		4.9	8.7		5.5	9.5		8.0	12.2	mA	
	I_{DD2}		1.5	2.5		2.3	3.6		8.0	11.0	mA	
ADuM6420ABRNZ3												
	I_{DD1}		4.9	8.7		5.5	9.5		8.0	12.2	mA	
	I_{DD2}		1.5	2.5		2.3	3.6		9.3	15.0	mA	
ADuM6421ABRNZ5												
	I_{DD1}		4.2	8.4		4.5	8.5		8.0	12.0	mA	
	I_{DD2}		2.3	4.5		2.8	5.7		8.8	12.0	mA	
ADuM6421ABRNZ3 and ADuM6421AWBRNZ5												
	I_{DD1}		4.2	8.4		4.5	8.5		8.0	12.0	mA	
	I_{DD2}		2.3	4.5		2.8	5.7		9.4	15.0	mA	
ADuM6422ABRNZ5												
	I_{DD1}		3.3	6.0		3.9	6.2		8.3	12.0	mA	
	I_{DD2}		3.0	6.0		4.0	6.5		9.5	13.5	mA	
ADuM6422ABRNZ3												
	I_{DD1}		3.3	6.0		3.9	6.2		8.3	12.0	mA	
	I_{DD2}		3.0	6.0		4.0	6.5		9.5	14.0	mA	

Parameter	Symbol	1 Mbps Min	1 Mbps Typ	1 Mbps Max	10 Mbps Min	10 Mbps Typ	10 Mbps Max	100 Mbps Min	100 Mbps Typ	100 Mbps Max	Unit	Test Conditions/Comments
ADuM6423ABRNZ5 and ADuM6423ABRNZ3												
	I_{DD1}		2.3	4.5		3.1	5.7		9.0	15.0	mA	
	I_{DD2}		4.2	8.4		4.5	8.5		8.2	12.0	mA	
ADuM6424ABRNZ5 and ADuM6424ABRNZ3												
	I_{DD1}		1.5	2.5		2.5	3.6		9.6	15.0	mA	
	I_{DD2}		4.8	8.7		5.0	9.5		8.1	12.2	mA	

Table 6. Switching Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	10			ns	Within pulse width distortion (PWD) limit
Data Rate				100	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	7.0	10	15	ns	50% input to 50% output
Pulse Width Distortion	PWD		1	5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			8.0	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		1	5.0	ns	
Opposing Direction	t_{PSKOD}		1	5.0	ns	
Jitter			816		ps p-p	

Table 7. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	$0.7 \times V_{DDx}$			V	
Logic Low	V_{IL}			$0.3 \times V_{DDx}$	V	
Output Voltage						
Logic High	V_{OH}	$V_{DDx} - 0.2$	V_{DDx}		V	I_{Ox}[1] = −20 μA, $V_{Ix} = V_{IxH}$[2]
		$V_{DDx} - 0.5$	$V_{DDx} - 0.2$		V	I_{Ox}[1] = −3.2 mA, $V_{Ix} = V_{IxH}$[2]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[1] = 20 μA, $V_{Ix} = V_{IxL}$[3]
			0.0	0.4	V	I_{Ox}[1] = 3.2 mA, $V_{Ix} = V_{IxL}$[3]
Undervoltage Lockout	UVLO					V_{DD1}, V_{DD2}, and V_{DDP} supply
Positive Going Threshold	V_{UV+}		1.6		V	
Negative Going Threshold	V_{UV-}		1.5		V	
Hysteresis	V_{UVH}		0.1		V	
Input Currents per Channel	I_I	−10	+0.01	+10	μA	$0 \text{ V} \le V_{Ix} \le V_{DDx}$
Quiescent Supply Current						
ADuM6420A						
	$I_{DD1 (Q)}$		0.37	1.2	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		1.2	1.9	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		9.5	16	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		1.5	2.5	mA	V_{Ix} = Logic 1
ADuM6421A						
	$I_{DD1 (Q)}$		0.5	1.4	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.9	1.5	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		7.5	14	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		3.3	6.2	mA	V_{Ix} = Logic 1

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM6422A						
	$I_{DD1 (Q)}$		0.7	1.2	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.72	1.3	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		5.4	9.5	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		5.3	9.7	mA	V_{Ix} = Logic 1
ADuM6423A						
	$I_{DD1 (Q)}$		0.96	1.5	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.5	1.4	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		3.5	6.2	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		7.5	14	mA	V_{Ix} = Logic 1
ADuM6424A						
	$I_{DD1 (Q)}$		1.2	1.9	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.4	1.2	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		1.7	2.5	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		9.5	16	mA	V_{Ix} = Logic 1
Dynamic Supply Current						
Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Output	$I_{DDO (D)}$		0.02		mA/Mbps	Inputs switching, 50% duty cycle
AC SPECIFICATIONS						
Output Rise Time/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	$\|CM_H\|$	75	100		kV/µs	$V_{Ix} = V_{DD1}$ or V_{ISO}, common-mode voltage (V_{CM}) = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] I_{Ox} is the Channel x output current, where x is A, B, C, or D.
[2] V_{IXH} is the input side logic high.
[3] V_{IXL} is the input side logic low.
[4] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both the rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION DIGITAL ISOLATOR CHANNELS ONLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum and maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 8. Data Channel Supply Current Specifications

		1 Mbps			10 Mbps			100 Mbps				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT												C_L = 0 pF
ADuM6420ABRNZ5												
	I_{DD1}		4.8	8.5		4.9	9.0		7.0	11.0	mA	
	I_{DD2}		1.4	2.5		2.1	3.4		7.5	11.0	mA	
ADuM6420ABRNZ3												
	I_{DD1}		4.8	8.5		4.9	9.0		7.0	11.0	mA	
	I_{DD2}		1.4	2.5		2.1	3.4		7.5	12.0	mA	
ADuM6421ABRNZ5												
	I_{DD1}		4.0	8.3		4.3	8.4		7.1	11.6	mA	
	I_{DD2}		2.1	4.4		2.7	5.6		8.0	11.6	mA	
ADuM6421ABRNZ3 and ADuM6421AWBRNZ5												
	I_{DD1}		4.0	8.3		4.3	8.4		7.1	11.6	mA	
	I_{DD2}		2.1	4.4		2.7	5.6		8.0	12.0	mA	

Parameter	Symbol	1 Mbps Min	1 Mbps Typ	1 Mbps Max	10 Mbps Min	10 Mbps Typ	10 Mbps Max	100 Mbps Min	100 Mbps Typ	100 Mbps Max	Unit	Test Conditions/Comments
ADuM6422ABRNZ5												
	I_{DD1}		3.1	6.0		3.6	6.2		7.4	11.0	mA	
	I_{DD2}		3.0	6.0		3.7	6.2		8.5	12.0	mA	
ADuM6422ABRNZ3												
	I_{DD1}		3.1	6.0		3.6	6.0		7.4	11.0	mA	
	I_{DD2}		3.0	6.0		3.7	6.2		8.5	13.0	mA	
ADuM6423ABRNZ5 and ADuM6423ABRNZ3												
	I_{DD1}		2.3	4.4		2.9	5.6		8.0	12.0	mA	
	I_{DD2}		4.2	8.3		4.3	8.4		7.1	11.6	mA	
ADuM6424ABRNZ5 and ADuM6424ABRNZ3												
	I_{DD1}		1.5	2.5		2.3	3.4		8.0	12.0	mA	
	I_{DD2}		4.8	8.5		4.8	9.0		7.0	11.0	mA	

Table 9. Switching Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	10			ns	Within PWD limit
Data Rate				100	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	7.0	10	16	ns	50% input to 50% output
Pulse Width Distortion	PWD		1.0	5.0	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			8.0	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		1.0	5.0	ns	
Opposing Direction	t_{PSKOD}		1.0	5.0	ns	
Jitter			816		ps p-p	

Table 10. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.2	V_{DDx}		V	I_{Ox}[1] = −20 μA, V_{Ix} = V_{IxH}[2]
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox}[1] = −3.2 mA, V_{Ix} = V_{IxH}[2]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[1] = 20 μA, V_{Ix} = V_{IxL}[3]
			0.0	0.4	V	I_{Ox}[1] = 3.2 mA, V_{Ix} = V_{IxL}[3]
Undervoltage Lockout	UVLO					V_{DD1}, V_{DD2}, and V_{DDP} supply
Positive Going Threshold	V_{UV+}		1.6		V	
Negative Going Threshold	V_{UV-}		1.5		V	
Hysteresis	V_{UVH}		0.1		V	
Input Currents per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Quiescent Supply Current						
ADuM6420A						
	$I_{DD1 (Q)}$		0.34	1.2	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		1.1	1.8	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		9.5	16	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		1.5	2.4	mA	V_{Ix} = Logic 1
ADuM6421A						
	$I_{DD1 (Q)}$		0.48	1.1	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.8	1.5	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		7.4	13.5	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		3.2	6.2	mA	V_{Ix} = Logic 1
ADuM6422A						
	$I_{DD1 (Q)}$		0.65	1.2	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.7	1.2	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		5.3	9.5	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		5.4	9.6	mA	V_{Ix} = Logic 1
ADuM6423A						
	$I_{DD1 (Q)}$		0.94	1.5	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.5	1.1	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		3.5	6.2	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		7.4	13.5	mA	V_{Ix} = Logic 1
ADuM6424A						
	$I_{DD1 (Q)}$		1.2	1.8	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.35	1.2	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		1.7	2.4	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		9.4	16	mA	V_{Ix} = Logic 1
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	$\|CM_H\|$	75	100		kV/µs	$V_{Ix} = V_{DD1}$ or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] I_{Ox} is the Channel x output current, where x is A, B, C, or D.
[2] V_{IxH} is the input side logic high.
[3] V_{IxL} is the input side logic low.
[4] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both the rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION DIGITAL ISOLATOR CHANNELS ONLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 2.5 V. Minimum and maximum specifications apply over the entire recommended operation range: 2.25 V ≤ V_{DD1} ≤ 2.75 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 11. Data Channel Supply Current Specifications

		1 Mbps			10 Mbps			100 Mbps				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT												C_L = 0 pF
ADuM6420ABRNZ5 and ADuM6420ABRNZ3												
	I_{DD1}		4.8	8.5		4.8	9.0		6.4	11.0	mA	
	I_{DD2}		1.4	2.3		2.0	3.3		6.5	9.5	mA	
ADuM6421ABRNZ5, ADuM6421ABRNZ3, and ADuM6421AWBRNZ5												
	I_{DD1}		4.2	8.0		4.4	8.2		6.7	11.5	mA	
	I_{DD2}		2.3	4.4		2.4	5.4		6.5	10.0	mA	
ADuM6422ABRNZ5 and ADuM6422ABRNZ3												
	I_{DD1}		3.0	6.0		3.4	6.1		6.4	9.5	mA	
	I_{DD2}		3.0	6.0		3.4	6.1		6.4	9.5	mA	
ADuM6423ABRNZ5 and ADuM6423ABRNZ3												
	I_{DD1}		2.3	4.4		2.8	5.4		6.5	10.0	mA	
	I_{DD2}		4.2	8.0		4.4	8.2		6.7	11.5	mA	
ADuM6424ABRNZ5 and ADuM6424ABRNZ3												
	I_{DD1}		1.5	2.3		2.0	3.3		6.5	9.5	mA	
	I_{DD2}		4.8	8.5		4.8	9.0		6.5	11.0	mA	

Table 12. Switching Specifications

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS						
Pulse Width	PW	10			ns	Within PWD limit
Data Rate				100	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	8.0	11	16	ns	50% input to 50% output
Pulse Width Distortion	PWD		1.0	5.0	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			8.0	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		1.0	5.0	ns	
Opposing Direction	t_{PSKOD}		1.0	5.0	ns	
Jitter			816		ps p-p	

Table 13. Input and Output Characteristics

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.2	V_{DDx}		V	I_{Ox}[1] = −20 μA, V_{Ix} = V_{IxH}[2]
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox}[1] = −3.2 mA, V_{Ix} = V_{IxH}[2]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[1] = 20 μA, V_{Ix} = V_{IxL}[3]
			0.0	0.4	V	I_{Ox}[1] = 3.2 mA, V_{Ix} = V_{IxL}[3]
Undervoltage Lockout	UVLO					V_{DD1}, V_{DD2}, and V_{DDP} supply
Positive Going Threshold	V_{UV+}		1.6		V	
Negative Going Threshold	V_{UV-}		1.5		V	
Hysteresis	V_{UVH}		0.1		V	
Input Currents per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
ADuM6420A						
	$I_{DD1 (Q)}$		0.33	1.0	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		1.1	1.7	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		1.5	16	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		9.5	2.2	mA	V_{Ix} = Logic 1
ADuM6421A						
	$I_{DD1 (Q)}$		0.5	1.0	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.9	1.5	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		7.4	13.5	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		3.2	6.2	mA	V_{Ix} = Logic 1
ADuM6422A						
	$I_{DD1 (Q)}$		0.55	1.2	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.55	1.2	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		5.3	9.5	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		5.3	9.5	mA	V_{Ix} = Logic 1
ADuM6423A						
	$I_{DD1 (Q)}$		0.94	1.5	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.5	1	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		3.5	6.2	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		7.3	13.5	mA	V_{Ix} = Logic 1
ADuM6424A						
	$I_{DD1 (Q)}$		1.2	1.7	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.35	1	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		1.7	2.2	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		9.3	16	mA	V_{Ix} = Logic 1
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	$\|CM_H\|$	75	100		kV/μs	V_{Ix} = V_{DD1} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/μs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] I_{Ox} is the Channel x output current, where x means A, B, C, or D.
[2] V_{IxH} is the input side logic high.
[3] V_{IxL} is the input side logic low.
[4] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both the rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—1.8 V OPERATION DIGITAL ISOLATOR CHANNELS ONLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 1.8 V. Minimum and maximum specifications apply over the entire recommended operation range: 1.7 V ≤ V_{DD1} ≤ 1.9 V, 1.7 V ≤ V_{DD2} ≤ 1.9 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 14. Data Channel Supply Current Specifications

		1 Mbps			10 Mbps			100 Mbps				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT												C_L = 0 pF
ADuM6420ABRNZ5 and ADuM6420ABRNZ3												
	I_{DD1}		4.3	8.5		4.9	8.5		6.4	10.6	mA	
	I_{DD2}		1.3	2.3		1.4	2.5		6.4	9.0	mA	
ADuM6421ABRNZ5, ADuM6421ABRNZ3, and ADuM6421AWBRNZ5												
	I_{DD1}		4.1	8.0		4.4	8.0		6.7	11.5	mA	
	I_{DD2}		2.3	4.4		2.6	5.3		6.5	9.5	mA	
ADuM6422ABRNZ5 and ADuM6422ABRNZ3												
	I_{DD1}		3.0	6.0		3.4	6.2		6.2	9.0	mA	
	I_{DD2}		3.0	6.0		3.4	6.2		6.0	9.0	mA	
ADuM6423ABRNZ5 and ADuM6423ABRNZ3												
	I_{DD1}		2.3	4.4		2.8	5.3		6.5	9.5	mA	
	I_{DD2}		4.2	8.0		4.4	8.0		6.5	11.5	mA	
ADuM6424ABRNZ5 and ADuM6424ABRNZ3												
	I_{DD1}		1.5	2.3		2.0	2.5		6.3	9.0	mA	
	I_{DD2}		4.7	8.5		4.7	8.5		6.2	10.6	mA	

Table 15. Switching Specifications

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS						
Pulse Width	PW	10			ns	Within PWD limit
Data Rate				100	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	8.0	12	17	ns	50% input to 50% output
Pulse Width Distortion	PWD		1.0	5.0	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			8.0	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		1.0	5.0	ns	
Opposing Direction	t_{PSKOD}		1.0	5.0	ns	
Jitter			816		ps p-p	

Table 16. Input and Output Characteristics

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Output Voltages						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[1] = −20 μA, V_{Ix} = V_{IxH}[2]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[1] = −3.2 mA, V_{Ix} = V_{IxH}[2]

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[1] = 20 µA, $V_{Ix} = V_{IxL}$[3]
			0.2	0.4	V	I_{Ox}[1] = 3.2 mA, $V_{Ix} = V_{IxL}$[3]
Undervoltage Lockout	UVLO					V_{DD1}, V_{DD2}, and V_{DDP} supply
Positive Going Threshold	V_{UV+}		1.6		V	
Negative Going Threshold	V_{UV-}		1.5		V	
Hysteresis	V_{UVH}		0.1		V	
Input Currents per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
ADuM6420A						
	$I_{DD1 (Q)}$		0.35	1.0	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q}$		1.0	1.7	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		9.4	16	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		1.4	2.2	mA	V_{Ix} = Logic 1
ADuM6421A						
	$I_{DD1 (Q)}$		0.5	1.0	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.9	1.4	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		7.5	13.5	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		3.2	6.2	mA	V_{Ix} = Logic 1
ADuM6422A						
	$I_{DD1 (Q)}$		0.6	1.2	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.65	1.2	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		5.3	9.5	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		5.3	9.5	mA	V_{Ix} = Logic 1
ADuM6423A						
	$I_{DD1 (Q)}$		0.91	1.4	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.45	1	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		3.5	6.2	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		7.2	13.5	mA	V_{Ix} = Logic 1
ADuM6424A						
	$I_{DD1 (Q)}$		1.2	1.7	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.35	1	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		1.6	2.2	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		9.3	16	mA	V_{Ix} = Logic 1
Dynamic Supply Current						
Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	$\|CM_H\|$	75	100		kV/µs	$V_{Ix} = V_{DD1}$ or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] I_{Ox} is the Channel x output current, where x means A, B, C, or D.
[2] V_{IxH} is the input side logic high.
[3] V_{IxL} is the input side logic low.
[4] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both the rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 17. Thermal and Isolation Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	Frequency = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		45		°C/W	Thermocouple located at center of package underside, test conducted on 4-layer board with thin traces[3]

[1] The device is considered a 2-terminal device: Pin 1 to Pin 14 are shorted together, and Pin 15 to Pin 28 are shorted together.
[2] Input capacitance is from any input data pin to ground.
[3] See the Thermal Analysis section for thermal model definitions.

REGULATORY APPROVALS

Table 18.

UL (Pending)[1]	CSA (Pending)	VDE (Pending)[2]	CQC (Pending)
Recognized Under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN V VDE V 0884-11 (VDE V 0884-11):2017-1	Certified under CQC11-471543-2012
Single Protection, 5000 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2:	Reinforced insulation 566 V peak, V_{IOSM} = 6000 V peak	GB4943.1-2011: Basic insulation at 815 V rms (1173 V peak)
	Basic insulation at 830 V rms (1173 V peak)	Transient voltage, V_{IOTM} = 8000 V peak	Reinforced insulation at 415 V rms (586 V peak)
	Reinforced insulation at 415 V rms (586 V peak)		
	IEC 60601-1 Edition 3.1:		
	Basic insulation (1 means of patient protection (1 MOPP)), 250 V rms		
	CSA 61010-1-12 and IEC 61010-1 third edition:		
	Basic insulation at 300 V rms mains, 815 V rms (1173 V peak) secondary		
	Reinforced insulation at 300 V rms mains, 415 V rms (586 V peak)		
File E214100	File 205078	File (pending)	File (pending)

[1] In accordance with UL 1577, each ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-11, each ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A is proof tested by applying an insulation test voltage ≥1059 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-11 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 19. Critical Safety Related Dimensions and Material Properties

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.3	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the PCB	L (PCB)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5	µm min	Minimum distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303, Part 1
Isolation Group		I		Material group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-11 INSULATION CHARACTERISTICS

The ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by the protective circuits. The asterisk (*) marking on packages denotes DIN V VDE V 0884-11 approval.

Table 20. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to IV	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	566	V peak
Input to Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	1059	V peak
Input to Output Test Voltage, Method a		V_{PR}		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	849	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	679	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{IOTM}	8000	V peak
Withstand Isolation Voltage	1-minute withstand rating	V_{ISO}	5000	V rms
Surge Isolation Voltage Reinforced	$V_{IOSM(TEST)}$ = 12.8 kV; 1.2 µs rise time; 50 µs, 50% fall time	V_{IOSM}	8000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Total Power Dissipation at 25°C		I_{S1}	2.78	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	>10^9	Ω

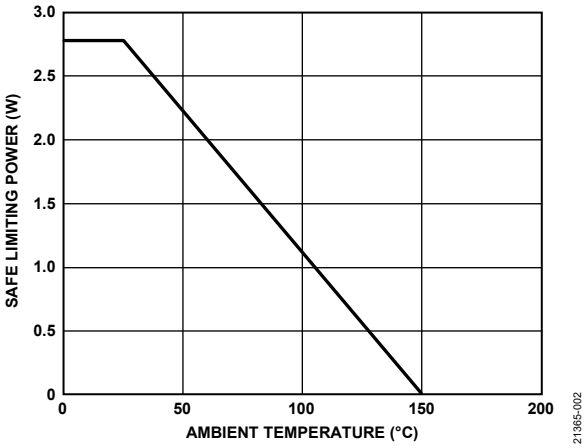


Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN 60747-5-2

RECOMMENDED OPERATING CONDITIONS

Table 21.

Parameter	Min	Max	Unit
Operating Temperature (T_A)[1]	−40	+125	°C
Supply Voltages[2]			
V_{DDP} at V_{SEL} = GND_{ISO}	3.0	5.5	V
V_{DDP} at V_{SEL} = V_{ISO}	4.5	5.5	V
V_{DD1}, V_{DD2}	1.7	5.5	V

[1] Operation at >85°C requires reduction of the maximum load current.
[2] Each voltage is relative to its respective ground.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 22.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature	−40°C to +125°C
Supply Voltages (V_{DD1}, V_{DDP}, V_{DD2}, V_{ISO})[1]	−0.5 V to +7.0 V
V_{ISO} Supply Current[2]	100 mA
Input Voltage (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{SEL}, PDIS)[1, 3]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB}, V_{OC}, V_{OD})[1, 3]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current Per Data Output Pin[4]	−10 mA to +10 mA
Common-Mode Transients[5]	−200 kV/µs to +200 kV/µs

[1] All voltages are relative to their respective ground.
[2] The V_{ISO} pin provides current for dc and dynamic loads on the V_{ISO} input and output channels. This current must be included when determining the total V_{ISO} supply current. For ambient temperatures between 85°C and 125°C, the maximum allowed current is reduced.
[3] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PCB Layout section.
[4] See Figure 2 for the maximum rated current values for various temperatures.
[5] Common-mode transients refer to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

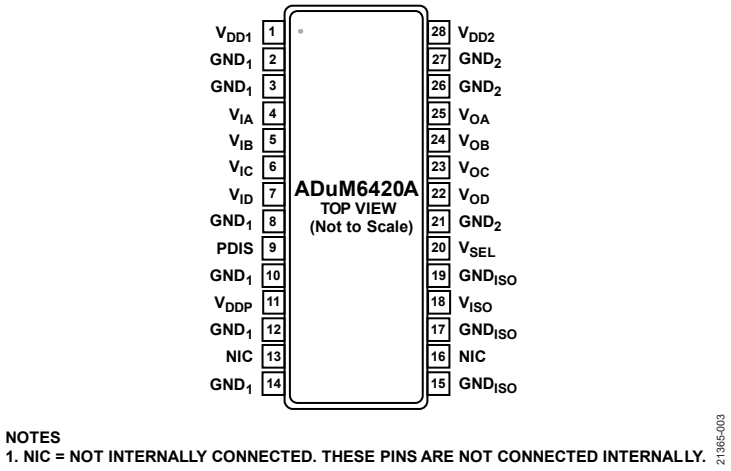
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 23. Maximum Continuous Working Voltage[1]

Parameter	Rating	Constraint
AC Voltage		
Bipolar Waveform		
Basic Insulation	636 V peak	
Reinforced Insulation	566 V peak	
Unipolar Waveform		
Basic Insulation	1130 V peak	
Reinforced Insulation	932 V peak	
DC Voltage		
Basic Insulation	1158 V peak	Limited by package creepage per IEC 60664-1, Pollution Degree 2, Material Group II
Reinforced Insulation	579 V peak	Limited by package creepage per IEC 60664-1, Pollution Degree 2, Material Group II

[1] Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED. THESE PINS ARE NOT CONNECTED INTERNALLY.

Figure 3. ADuM6420A Pin Configuration

Table 24. ADuM6420A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply for the Side 1 Logic Circuits of the Device. V_{DD1} requires a 100 nF bypass capacitor. V_{DD1} is independent of V_{DDP} and can operate with power supply voltages between 1.7 V and 5.5 V.
2, 3, 8, 10, 12, 14	GND_1	Ground 1. Ground references for the primary isolator. Pin 2, Pin 3, Pin 8, Pin 10, Pin 12, and Pin 14 are internally connected, and it is recommended to connect the GND_1 pins to a common ground.
4	V_{IA}	Logic Input A.
5	V_{IB}	Logic Input B.
6	V_{IC}	Logic Input C.
7	V_{ID}	Logic Input D.
9	PDIS	Power Disable. When PDIS is tied to GND_1, the power converter is active. When a logic high voltage is applied to PDIS, the power supply enters low power standby mode.
11	V_{DDP}	Primary Supply Voltage, 3.0 V to 5.5 V. V_{DDP} requires 100 nF and 10 µF bypass capacitors to GND_1.
13, 16	NIC	Not Internally Connected. These pins are not connected internally.
15, 17, 19	GND_{ISO}	Ground References for V_{ISO} on Side 2. It is recommended to connect the GND_{ISO} pins together. The GND_{ISO} pins are internally isolated from GND_2.
18	V_{ISO}	Secondary Supply Voltage Output for External Loads. Connect to V_{DD2} to power the isolator channels.
20	V_{SEL}	Output Voltage Select Input. Connect V_{SEL} to V_{ISO} for a 5 V output or to GND_{ISO} for a 3.3 V output.
21, 26, 27	GND_2	Ground References for V_{DD2} on Side 2. It is recommended that the GND_2 pins be connected together. The GND_2 pins are internally isolated from GND_{ISO}.
22	V_{OD}	Logic Output D.
23	V_{OC}	Logic Output C.
24	V_{OB}	Logic Output B.
25	V_{OA}	Logic Output A.
28	V_{DD2}	Power Supply for the Side 2 Logic Circuits of the Device. V_{DD2} requires a 100 nF bypass capacitor. V_{DD2} is independent of V_{ISO} and can operate with power supply voltages between 1.7 V and 5.5 V.

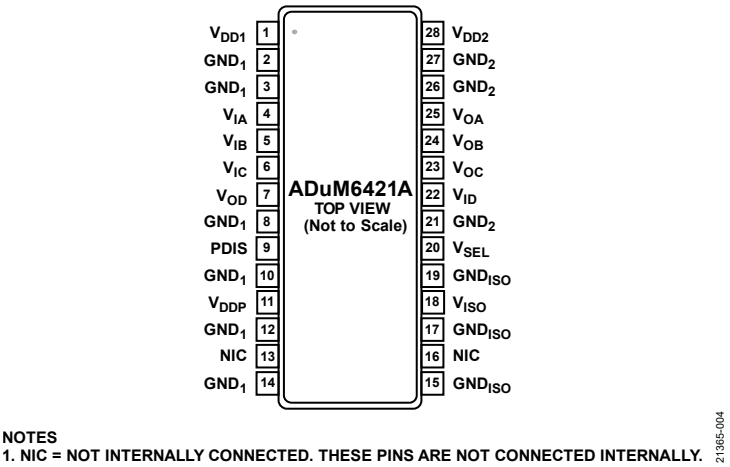


Figure 4. ADuM6421A Pin Configuration

Table 25. ADuM6421A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply for the Side 1 Logic Circuits of the Device. V_{DD1} requires a 0.10 µF bypass capacitor to GND_1. V_{DD1} is independent of V_{DDP} and can operate with power supply voltages between 1.7 V and 5.5 V.
2, 3, 8, 10, 12, 14	GND_1	Ground 1. Ground references for the primary isolator. Pin 2, Pin 3, Pin 8, Pin 10, Pin 12, and Pin14 are internally connected, and it is recommended to connect the GND_1 pins to a common ground.
4	V_{IA}	Logic Input A.
5	V_{IB}	Logic Input B.
6	V_{IC}	Logic Input C.
7	V_{OD}	Logic Output D.
9	PDIS	Power Disable. When PDIS is tied to GND_1, the power converter is active. When a logic high voltage is applied to PDIS, the power supply enters low power standby mode.
11	V_{DDP}	DC-to-DC Converter Supply Voltage, 3.0 V to 5.5 V. V_{DDP} requires 0.10 µF and 10 µF bypass capacitors to GND_1.
13, 16	NIC	Not Internally Connected. These pins are not connected internally.
15, 17, 19	GND_{ISO}	Grounds for the Isolated DC-to-DC Converter. Connect the GND_{ISO} pins together through one ferrite bead to PCB ground. The GND_{ISO} pins are internally isolated from GND_2.
18	V_{ISO}	Secondary Supply Voltage Output for External Loads. V_{ISO} requires 0.10 µF and 10 µF capacitors to GND_{ISO}. Connect V_{ISO} through a ferrite bead to external loads.
20	V_{SEL}	Output Voltage Select Input. Connect V_{SEL} to V_{ISO} for a 5 V output or to GND_{ISO} for a 3.3 V output.
21, 26, 27	GND_2	Ground References for V_{DD2} on Side 2. It is recommended that the GND_2 pins be connected together. The GND_2 pins are internally isolated from GND_{ISO}.
22	V_{ID}	Logic Input D.
23	V_{OC}	Logic Output C.
24	V_{OB}	Logic Output B.
25	V_{OA}	Logic Output A.
28	V_{DD2}	Power Supply for the Side 2 Logic Circuits of the Device. V_{DD2} requires a 100 nF bypass capacitor. V_{DD2} is independent of V_{ISO} and can operate with power supply voltages between 1.7 V and 5.5 V.

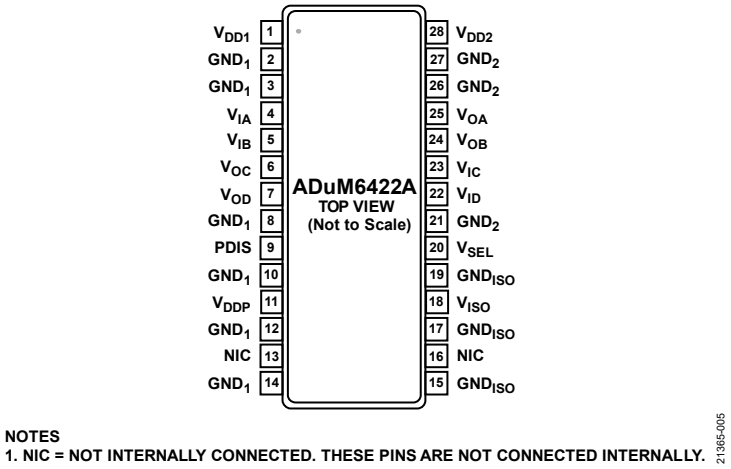


Figure 5. ADuM6422A Pin Configuration

Table 26. ADuM6422A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply for the Side 1 Logic Circuits of the Device. V_{DD1} requires a 0.10 µF bypass capacitor to GND_1. V_{DD1} is independent of V_{DDP} and can operate with power supply voltages between 1.7 V and 5.5 V.
2, 3, 8, 10, 12, 14	GND_1	Ground 1. Ground references for the primary isolator. Pin 2, Pin 3, Pin 8, Pin 10, Pin 12, and Pin 14 are internally connected, and it is recommended to connect the GND_1 pins to a common ground.
4	V_{IA}	Logic Input A.
5	V_{IB}	Logic Input B.
6	V_{OC}	Logic Output C.
7	V_{OD}	Logic Output D.
9	PDIS	Power Disable. When PDIS is tied to GND_1, the power converter is active. When a logic high voltage is applied to PDIS, the power supply enters a low power standby mode.
11	V_{DDP}	DC-to-DC Converter Supply Voltage, 3.0 V to 5.5 V. V_{DDP} requires 0.10 µF and 10 µF bypass capacitors to GND_1.
13, 16	NIC	Not Internally Connected. These pins are not connected internally.
15, 17, 19	GND_{ISO}	Grounds for the Isolated DC-to-DC Converter. Connect the GND_{ISO} pins together through one ferrite bead to PCB ground. The GND_{ISO} pins are internally isolated from GND_2.
18	V_{ISO}	Secondary Supply Voltage Output for External Loads. V_{ISO} requires 0.10 µF and 10 µF capacitors to GND_{ISO}. Connect V_{ISO} through a ferrite bead to external loads.
20	V_{SEL}	Output Voltage Select Input. Connect V_{SEL} to V_{ISO} for a 5 V output or to GND_{ISO} for a 3.3 V output.
21, 26, 27	GND_2	Ground Reference for V_{DD2} on Side 2. It is recommended that the GND_2 pins be connected together. The GND_2 pins are internally isolated from GND_{ISO}.
22	V_{ID}	Logic Input D.
23	V_{IC}	Logic Input C.
24	V_{OB}	Logic Output B.
25	V_{OA}	Logic Output A.
28	V_{DD2}	Power Supply for the Side 2 Logic Circuits of the Device. V_{DD2} requires a 100 nF bypass capacitor. V_{DD2} is independent of V_{ISO} and can operate with power supply voltages between 1.7 V and 5.5 V.

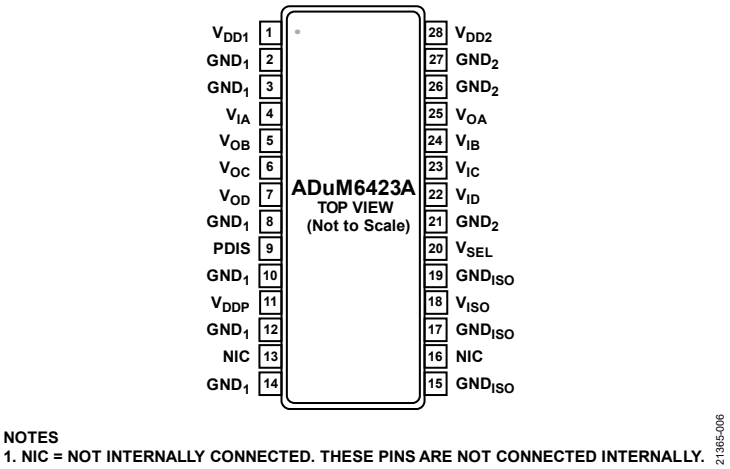
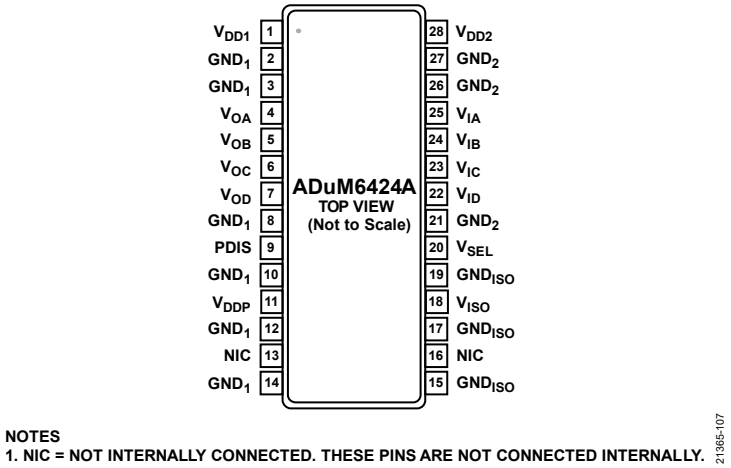


Figure 6. ADuM6423A Pin Configuration

Table 27. ADuM6423A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply for the Side 1 Logic Circuits of the Device. V_{DD1} requires a 0.10 µF bypass capacitor to GND_1. V_{DD1} is independent of V_{DDP} and can operate with power supply voltages between 1.7 V and 5.5 V.
2, 3, 8, 10, 12, 14	GND_1	Ground 1. Ground references for the primary isolator. Pin 2, Pin 3, Pin 8, Pin 10, Pin 12, and Pin 14 are internally connected, and it is recommended to connect the GND_1 pins to a common ground.
4	V_{IA}	Logic Input A.
5	V_{OB}	Logic Output B.
6	V_{OC}	Logic Output C.
7	V_{OD}	Logic Output D.
9	PDIS	Power Disable. When PDIS is tied to GND_1, the power converter is active. When a logic high voltage is applied to PDIS, the power supply enters a low power standby mode.
11	V_{DDP}	DC-to-DC Converter Supply Voltage, 3.0 V to 5.5 V. V_{DDP} requires 0.10 µF and 10 µF bypass capacitors to GND_1.
13, 16	NIC	Not Internally Connected. These pins are not connected internally.
15, 17, 19	GND_{ISO}	Grounds for the Isolated DC-to-DC Converter. Connect the GND_{ISO} pins together through one ferrite bead to PCB ground. The GND_{ISO} pins are internally isolated from GND_2.
18	V_{ISO}	Secondary Supply Voltage Output for External Loads. V_{ISO} requires 0.10 µF and 10 µF capacitors to GND_{ISO}. Connect V_{ISO} through a ferrite bead to external loads.
20	V_{SEL}	Output Voltage Select Input. Connect V_{SEL} to V_{ISO} for a 5 V output or to GND_{ISO} for a 3.3 V output.
21, 26, 27	GND_2	Ground Reference for V_{DD2} on Side 2. It is recommended that the GND_2 pins be connected together. The GND_2 pins are internally isolated from GND_{ISO}.
22	V_{ID}	Logic Input D.
23	V_{IC}	Logic Input C.
24	V_{IB}	Logic Input B.
25	V_{OA}	Logic Output A.
28	V_{DD2}	Power Supply for the Side 2 Logic Circuits of the Device. V_{DD2} requires a 100 nF bypass capacitor. V_{DD2} is independent of V_{ISO} and can operate with power supply voltages between 1.7 V and 5.5 V.



NOTES
1. NIC = NOT INTERNALLY CONNECTED. THESE PINS ARE NOT CONNECTED INTERNALLY.

Figure 7. ADuM6424A Pin Configuration

Table 28. ADuM6424A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply for the Side 1 Logic Circuits of the Device. V_{DD1} requires a 0.10 µF bypass capacitor to GND_1. V_{DD1} is independent of V_{DDP} and can operate with power supply voltages between 1.7 V and 5.5 V.
2, 3, 8, 10, 12, 14	GND_1	Ground 1. Ground references for the primary isolator. Pin 2, Pin 3, Pin 8, Pin 10, Pin 12, and Pin 14 are internally connected, and it is recommended to connect the GND_1 pins to a common ground.
4	V_{OA}	Logic Output A.
5	V_{OB}	Logic Output B.
6	V_{OC}	Logic Output C.
7	V_{OD}	Logic Output D.
9	PDIS	Power Disable. When PDIS is tied to GND_1, the power converter is active. When a logic high voltage is applied to PDIS, the power supply enters a low power standby mode.
11	V_{DDP}	DC-to-DC Converter Supply Voltage, 3.0 V to 5.5 V. V_{DDP} requires 0.10 µF and 10 µF bypass capacitors to GND_1.
13, 16	NIC	Not Internally Connected. These pins are not connected internally.
15, 17, 19	GND_{ISO}	Grounds for the Isolated DC-to-DC Converter. Connect the GND_{ISO} pins together through one ferrite bead to PCB ground. The GND_{ISO} pins are internally isolated from GND_2.
18	V_{ISO}	Secondary Supply Voltage Output for External Loads. V_{ISO} requires 0.10 µF and 10 µF capacitors to GND_{ISO}. Connect V_{ISO} through a ferrite bead to external loads.
20	V_{SEL}	Output Voltage Select Input. Connect V_{SEL} to V_{ISO} for a 5 V output or to GND_{ISO} for a 3.3 V output.
21, 26, 27	GND_2	Ground Reference for V_{DD2} on Side 2. It is recommended that the GND_2 pins be connected together. The GND_2 pins are internally isolated from GND_{ISO}.
22	V_{ID}	Logic Input D.
23	V_{IC}	Logic Input C.
24	V_{IB}	Logic Input B.
25	V_{IA}	Logic Input A.
28	V_{DD2}	Power Supply for the Side 2 Logic Circuits of the Device. V_{DD2} requires a 100 nF bypass capacitor. V_{DD2} is independent of V_{ISO} and can operate with power supply voltages between 1.7 V and 5.5 V.

TRUTH TABLE

Table 29. Data Section Truth Table (Positive Logic)

V_{DDI} State[1]	V_{Ix} Input[1]	V_{DDO} State[1]	V_{Ox} Output[1]	Notes
Powered	High	Powered	High	Normal operation, data is high.
Powered	Low	Powered	Low	Normal operation, data is low.
Don't care	Don't care	Unpowered	High-Z	Output is off.
Unpowered	Low	Powered	Low	Output default low.
Unpowered	High	Powered	Indeterminate	If a high level is applied to an input when no supply is present, the input can parasitically power the input side, causing unpredictable operation.

[1] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively. V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (Channel A, Channel B, Channel C, or Channel D).

Table 30. Power Section Truth Table (Positive Logic)

V_{DDP} (V)	V_{SEL} Input	PDIS Input	V_{ISO} (V)
5	High	Low	5
5	Don't care	High	0
5	Low	Low	3.3
3.3	Low	Low	3.3
3.3	High	Low	Condition not supported
3.3	Don't care	High	0

TYPICAL PERFORMANCE CHARACTERISTICS

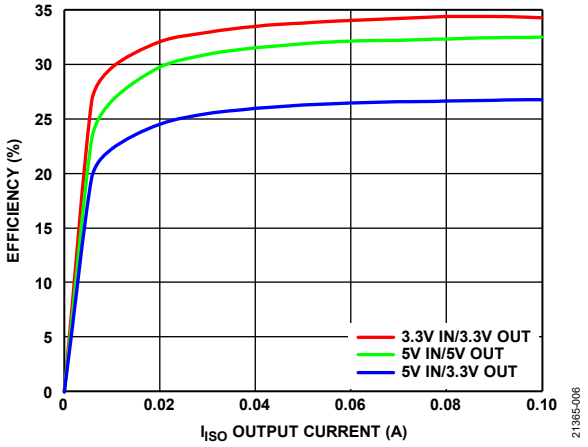


Figure 8. Power Supply Efficiency in Supported Power Configurations

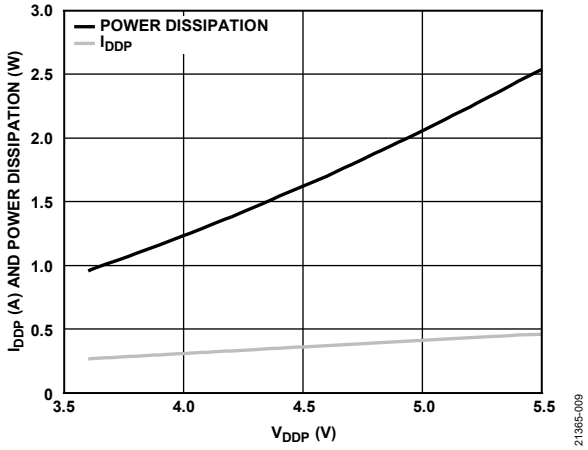


Figure 11. Short-Circuit Input Current (I_{DDP}) and Power Dissipation vs. V_{DDP}

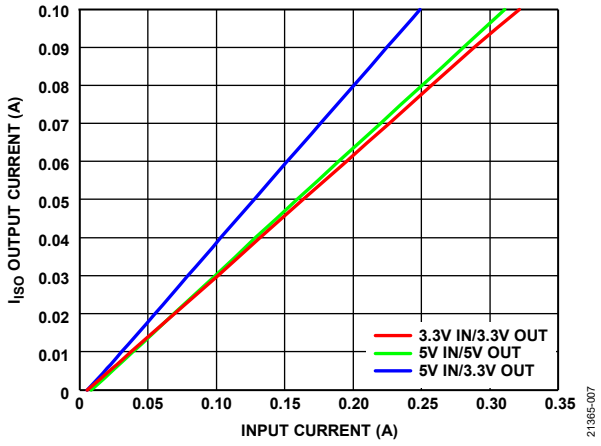


Figure 9. I_{ISO} Output Current vs. Input Current in Supported Power Configurations

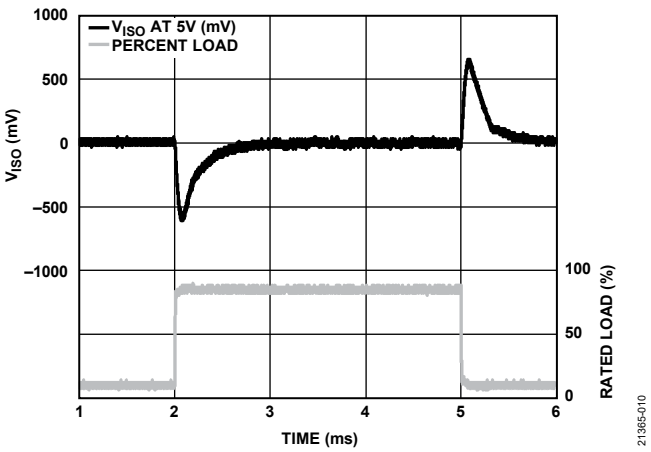


Figure 12. V_{ISO} Transient Load Response, 5 V Output, 10% to 90% Load Step

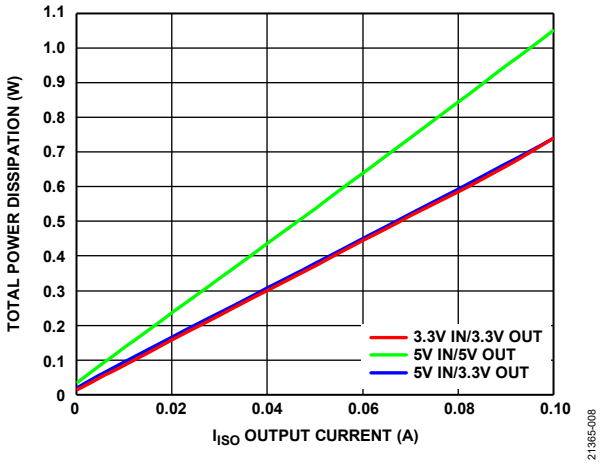


Figure 10. Total Power Dissipation vs. I_{ISO} Output Current in Supported Power Configurations

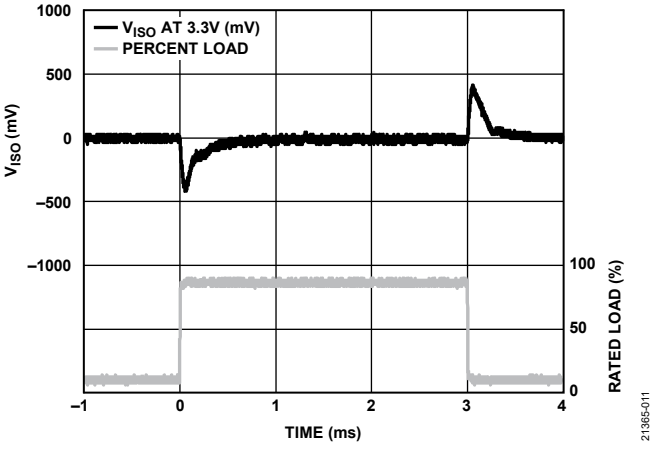


Figure 13. V_{ISO} Transient Load Response, 5 V Input, 3.3 V Output, 10% to 90% Load Step

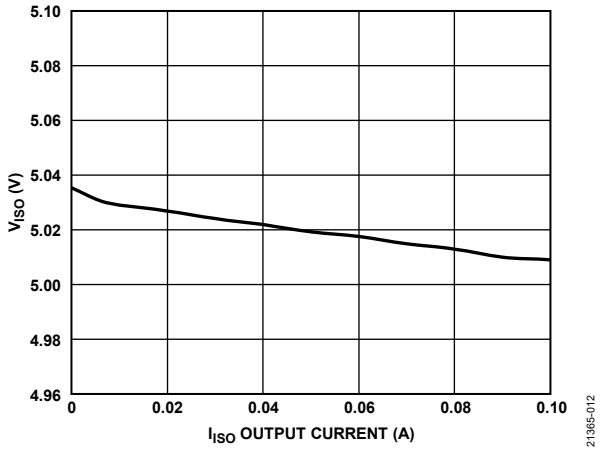


Figure 14. V_{ISO} vs. I_{ISO} Output Current, Input = 5 V, V_{ISO} = 5 V

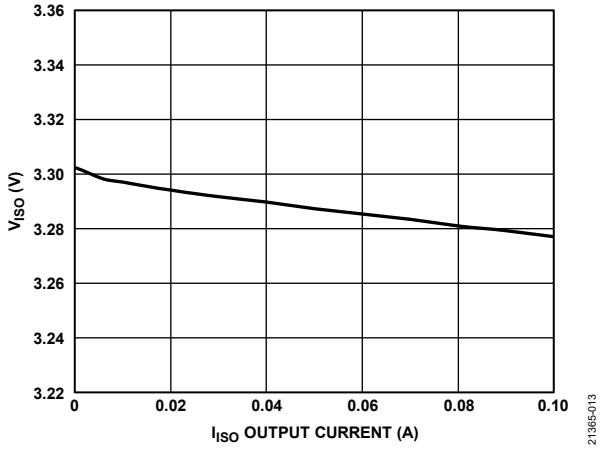


Figure 15. V_{ISO} vs. I_{ISO} Output Current, Input = 5 V, V_{ISO} = 3.3 V

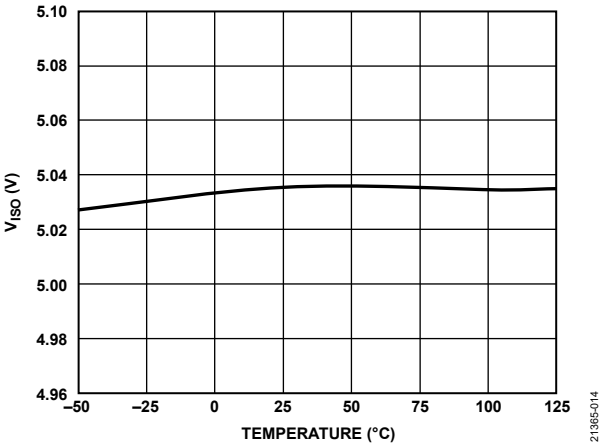


Figure 16. V_{ISO} vs. Temperature, Input = 5 V, V_{ISO} = 5 V

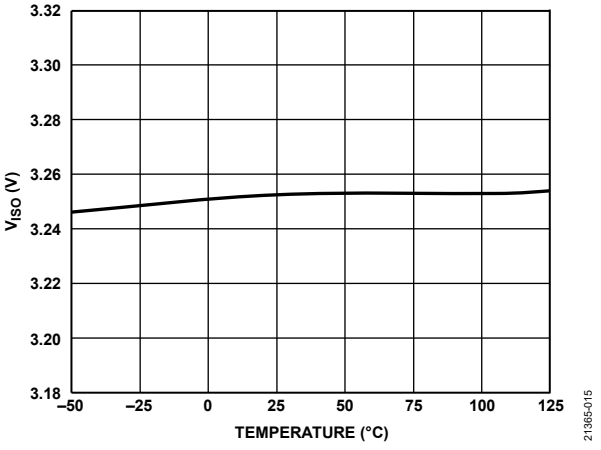


Figure 17. V_{ISO} vs. Temperature, Input = 3.3 V, V_{ISO} = 3.3 V

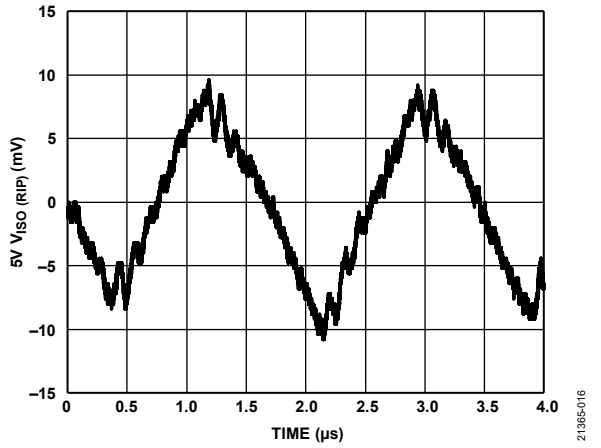


Figure 18. Output Voltage Ripple at 90% Load, V_{ISO} = 5 V

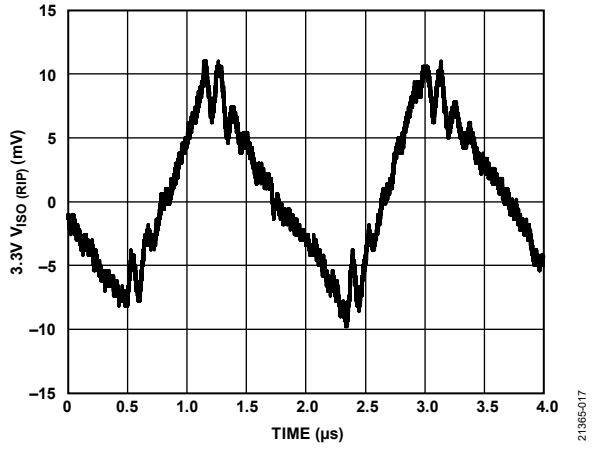


Figure 19. Output Voltage Ripple at 90% Load, V_{ISO} = 3.3 V

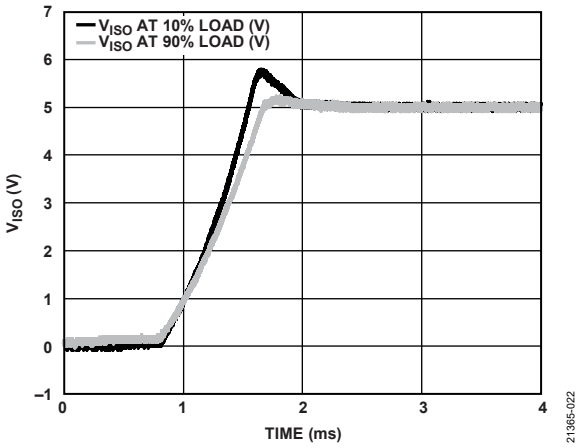


Figure 20. 5 V Input to 5 V Output V_{ISO} Start-Up Transient at 10% and 90% Load

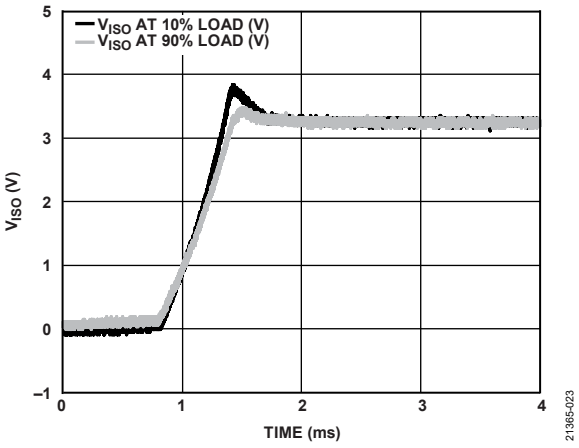


Figure 21. 5 V Input to 3.3 V Output V_{ISO} Start-Up Transient at 10% and 90% Load

TERMINOLOGY

I_{DD1}
I_{DD1} is the supply current required for the primary side of the digital isolator.

I_{DD2}
I_{DD2} is the supply current required for the secondary side of the digital isolator.

I_{DDP}
I_{DDP} is the supply current required for the primary side of the isolated dc-to-dc converter.

I_{ISO}
I_{ISO} is the available isolated current supply available to an external load.

Propagation Delay, t_{PHL}
t_{PHL} is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal.

Propagation Delay, t_{PLH}
t_{PLH} is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

Propagation Delay Skew, t_{PSK}
t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Channel to Channel Matching, t_{PSKCD}/t_{PSKOD}
t_{PSKCD} is the absolute value of the difference in propagation delays between two codirectional channels when operated with identical loads. t_{PSKOD} is the absolute value of the difference in propagation delays between two channels transmitting in opposing directions.

Minimum Pulse Width
The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

Maximum Data Rate
The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

THEORY OF OPERATION

The dc-to-dc converter section of the ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A works on principles that are common to most modern power supplies. The ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A have a split controller architecture with isolated PWM feedback. V_{DDP} power is supplied to an oscillating circuit that switches current into a chip scale, air core transformer. Power transferred to the secondary side is rectified and regulated to a value of 3.3 V or 5 V, depending on the setting of the V_{SEL} pin. The secondary (V_{ISO}) side controller regulates the output by creating a PWM control signal that is sent to the primary (V_{DDP}) side by a dedicated *i*Coupler data channel. The PWM modulates the oscillator circuit to control the power being sent to the secondary side. Feedback allows for significantly higher power and efficiency.

The ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A implement undervoltage lockout (UVLO) with hysteresis on the primary and the secondary side input and output pins as well as the V_{DDP} power input. This feature ensures that the converter does not enter oscillation due to noisy input power or slow power-on ramp rates.

The digital isolator channels use a high frequency carrier to transmit data across the isolation barrier using *i*Coupler chip scale transformer coils separated by layers of polyimide isolation. Using an on/off keying technique and the differential architecture shown in Figure 22, the digital isolator channels have low propagation delay and high speed. Internal regulators and input and output design techniques allow logic and supply voltages over a wide range from 1.7 V to 5.5 V, offering voltage translation of 1.8 V, 2.5 V, 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum on/off keying carrier and other techniques.

Figure 22 shows the waveforms of the digital isolator channels that have the condition of the fail-safe output state equal to low, where the carrier waveform is off when the input state is low. If the input side is off or not operating, the low fail-safe output state sets the output to low.

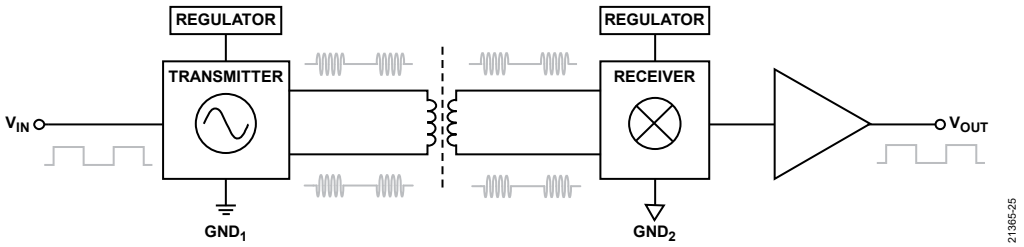


Figure 22. Operational Block Diagram of a Single Channel with a Low Fail-Safe Output State, V_{IN} Is the Input Voltage and V_{OUT} Is the Output Voltage

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A digital isolators with an *iso*Power integrated dc-to-dc converter require no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 23, Figure 24, and Figure 25). For proper data channel operation, low equivalent series resistance (ESR) bypass capacitors of 0.01 µF to 0.1 µF are required between the V_{DD1} pin and GND_1 pin as close to the chip pads as possible. Low ESR bypass capacitors of 0.1 µF or 0.22 µF are required between the V_{ISO} pin and GND_{ISO} pin as close to the chip pads as possible (see the C_{ISO} notes in Figure 24 and Figure 25). Installing the bypass capacitor with traces more than 2 mm in length may result in data corruption. The *iso*Power inputs require several passive components to bypass the power effectively, as well as set the output voltage.

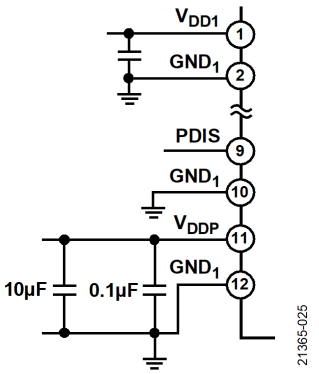


Figure 23. V_{DD1} and V_{DDP} Bias and Bypass Components

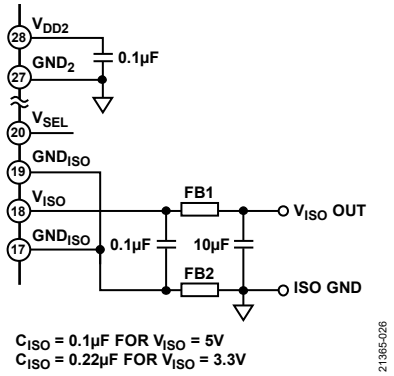


Figure 24. V_{DD2} and V_{ISO} Bias and Bypass Components

The power supply section of the ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A use a 180 MHz oscillator frequency to efficiently pass power through the chip scale transformers. Bypass capacitors are required for several operating frequencies. Noise suppression requires a low inductance, high frequency capacitor. Ripple suppression and proper regulation require a large value capacitor. These capacitors are connected between the V_{DDP} pin and GND_1 pin and between the V_{ISO} pin and GND_{ISO} pin. To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The required capacitor values are 0.1 µF and 10 µF for V_{DD1}. The smaller capacitor must have a low ESR. For example, use of a ceramic capacitor is advised. The total lead length between the ends of the low ESR capacitor and the input power supply pin must not exceed 2 mm.

To reduce the level of electromagnetic radiation, the impedance to high frequency currents between the V_{ISO} and the GND_{ISO} pins and the PCB trace connections can be increased. Using this method of electromagnetic interference (EMI) suppression controls the radiating signal at the signal source by placing surface-mount ferrite beads in series with the V_{ISO} and GND_{ISO} pins, as seen in Figure 25. Note that if ferrite beads are used, all guaranteed electrical specifications may not be met due to the additional series resistance (DCR). The impedance of the ferrite beads must be approximately 1.8 kΩ between the 100 MHz and 1 GHz frequency range to reduce the emissions at the 180 MHz primary switching frequency and the 360 MHz secondary side, rectifying frequency and harmonics. See Table 31 for examples of appropriate surface-mount ferrite beads.

Table 31. Surface-Mount Ferrite Bead Examples

Manufacturer	Part No.	Size	DCR (Ω)
Taiyo Yuden	BKH1005LM182-T	0402	2.0
Murata Electronics	BLM15HD182SN1	0402	2.2
Murata Electronics	BLM18HE152SN1	0603	0.5

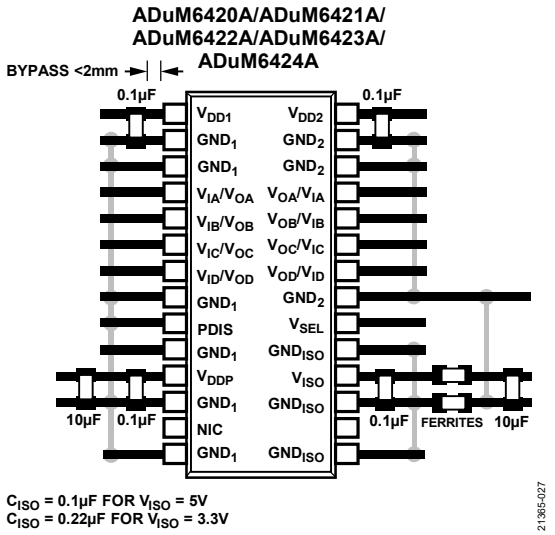


Figure 25. Recommended PCB Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure these steps can cause voltage differentials between pins, exceeding the absolute maximum ratings specified in Table 22, thereby leading to latch-up and/or permanent damage.

THERMAL ANALYSIS

The ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A consist of five internal die attached to a split lead frame with two die attach pads. For the purposes of thermal analysis, the die is treated as a thermal unit, with the highest junction temperature reflected in the θ_{JA} value from Table 17. The value of θ_{JA} is based on measurements taken with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A can operate at full load. However, at temperatures above 85°C, derating the output current may be needed, as shown in Figure 2.

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component (see Figure 26). The propagation delay to a logic low output may differ from the propagation delay to a logic high.

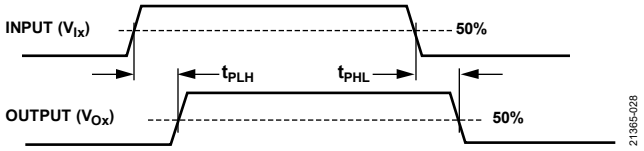


Figure 26. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal timing is preserved.

Channel to channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A components operating under the same conditions.

EMI CONSIDERATIONS

The dc-to-dc converter section of the ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A components must, of necessity, operate at a high frequency to allow efficient power transfer through the small transformers, which creates high frequency currents that can propagate in circuit board ground and power planes, requiring proper power supply bypassing at the input and output supply pins (see Figure 25). Using proper layout and bypassing techniques, the dc-to-dc converter is designed to provide regulated, isolated power that is below CISPR 32/EN 55032 Class B limits up to 5 Mbps at full load on a 2-layer PCB with ferrites.

POWER CONSUMPTION

The V_{DDP} power supply input only provides power to the converter. Power for the data channels is provided through V_{DD1} and V_{DD2}. These power supplies can be connected to V_{DDP} and V_{ISO} if desired, or the supplies can receive power from an independent source. Treat the converter as a standalone supply to be utilized at the discretion of the designer.

The V_{DD1} or V_{DD2} supply current at a given channel of the ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A isolators is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

The V_{DD1} and V_{DD2} supply current and the total supply currents as a function of data rate for each model of the ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A for an unloaded output condition are shown under typical supply and room temperature conditions in the figures in the Typical Performance Characteristics section. The total I_{ISO} output current as a function of input current for the ADuM6420A/ADuM6421A/ADuM6422A/ADuM6423A/ADuM6424A is shown in Figure 9. In addition, the total power dissipation as a function of output current is shown in Figure 10.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the digital isolator channels are presented in Table 19.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling show that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as dc stress, which causes little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as shown in Equation 2. For insulation wear out with the polyimide materials used in these products, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\,RMS}{}^2 + V_{DC}{}^2} \quad (1)$$

or

$$V_{AC\,RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2} \quad (2)$$

where:
V_{RMS} is the total rms working voltage.
$V_{AC\,RMS}$ is the time varying portion of the working voltage.
V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V ac rms and a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance and lifetime of a device, see Figure 27 and the following equations.

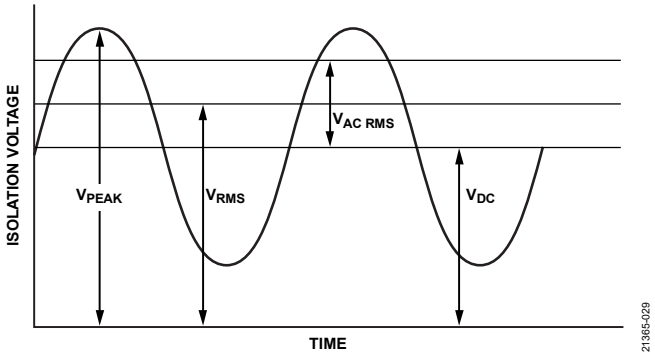


Figure 27. Critical Voltage Example

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\,RMS}{}^2 + V_{DC}{}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

V_{RMS} = 466 V

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 2.

$$V_{AC\,RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2}$$

$$V_{AC\,RMS} = \sqrt{466^2 - 400^2}$$

$V_{AC\,RMS}$ = 240 V rms

In this case, the ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage in Table 23 for the expected lifetime, which is less than a 60 Hz sine wave, and it is well within the limit for a 50-year service life.

Note that the dc working voltage limit is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

OUTLINE DIMENSIONS

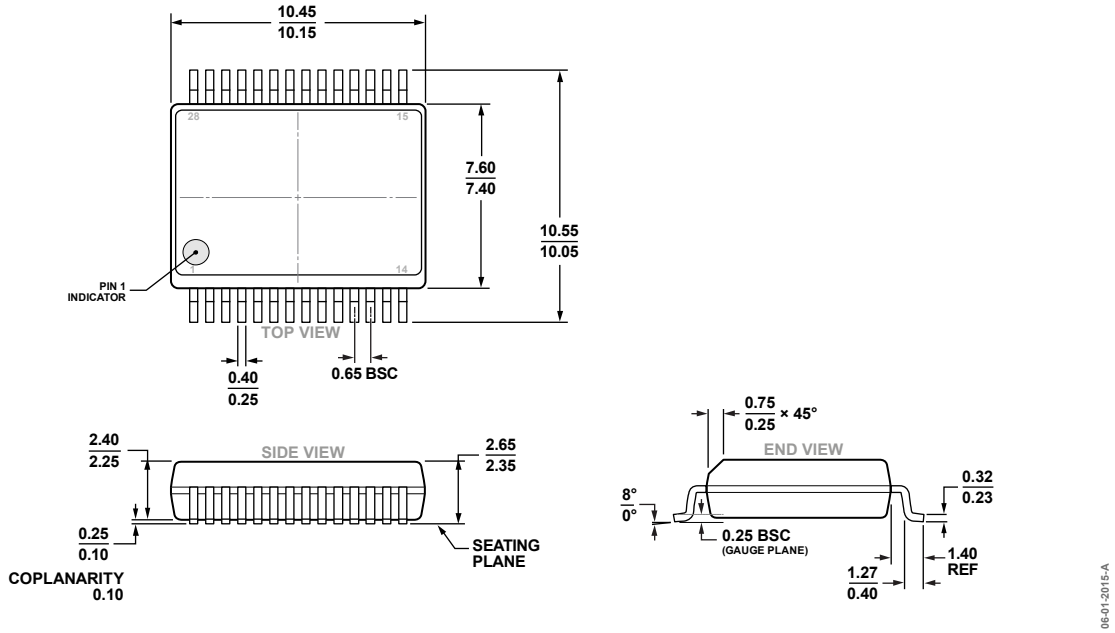


Figure 28. 28-Lead Standard Small Outline, Wide Body, with Finer Pitch [SOIC_W_FP]
(RN-28-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3, 4]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{ISO} Side	Automotive Qualified	V_{DDP} Voltage Range (V)	Temperature Range (°C)	Package Description	Package Option
ADuM6420ABRNZ5	4	0	No	4.5 to 5.5	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6420ABRNZ5-RL	4	0	No	4.5 to 5.5	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6421ABRNZ5	3	1	No	4.5 to 5.5	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6421ABRNZ5-RL	3	1	No	4.5 to 5.5	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6421AWBRNZ5	3	1	Yes	4.5 to 5.5	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6421AWBRNZ5-RL	3	1	Yes	4.5 to 5.5	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6422ABRNZ5	2	2	No	4.5 to 5.5	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6422ABRNZ5-RL	2	2	No	4.5 to 5.5	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6423ABRNZ5	1	3	No	4.5 to 5.5	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6423ABRNZ5-RL	1	3	No	4.5 to 5.5	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6424ABRNZ5	0	4	No	4.5 to 5.5	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6424ABRNZ5-RL	0	4	No	4.5 to 5.5	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6420ABRNZ3	4	0	No	3.0 to 3.6	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6420ABRNZ3-RL	4	0	No	3.0 to 3.6	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6421ABRNZ3	3	1	No	3.0 to 3.6	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6421ABRNZ3-RL	3	1	No	3.0 to 3.6	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6422ABRNZ3	2	2	No	3.0 to 3.6	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6422ABRNZ3-RL	2	2	No	3.0 to 3.6	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6423ABRNZ3	1	3	No	3.0 to 3.6	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6423ABRNZ3-RL	1	3	No	3.0 to 3.6	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6424ABRNZ3	0	4	No	3.0 to 3.6	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1
ADuM6424ABRNZ3-RL	0	4	No	3.0 to 3.6	−40°C to +125°C	28-Lead SOIC_W_FP	RN-28-1