800 MHz, 2:1 Analog Multiplexers

Data Sheet

ADV3219/ADV3220

FEATURES

- Excellent ac performance
  - −3 dB bandwidth
    - 800 MHz (200 mV p-p)
    - 730 MHz (2 V p-p)
  - Slew rate: 2800 V/µs
- Low power: 75 mW, V_S = ±5 V
- Excellent video performance
  - >100 MHz, 0.1 dB gain flatness
  - 0.02% differential gain/0.02° differential phase error (R_L = 150 Ω)
- Gain = +1 (ADV3219) or gain = +2 (ADV3220)
- Low crosstalk of −82 dB at 5 MHz and −60 dB at 100 MHz
- High impedance output disable allows connection of multiple devices without loading the output bus
- 8-lead LFCSP

APPLICATIONS

- Routing of high speed signals including
  - Video (NTSC, PAL, S, SECAM, YUV, and RGB)
  - Compressed video (MPEG, wavelet)
  - 3-level digital video (HDB3)
- Data communications
- Telecommunications

FUNCTIONAL BLOCK DIAGRAM

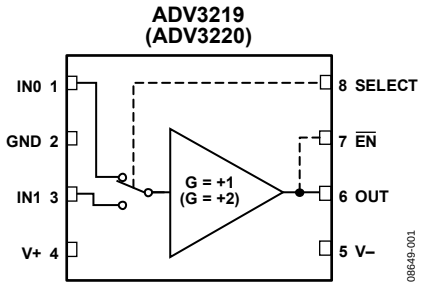

Figure 1.

GENERAL DESCRIPTION

The ADV3219 and ADV3220 are high speed, high slew rate, buffered, 2:1 analog multiplexers. They offer a −3 dB signal bandwidth greater than 800 MHz and channel switch times of less than 20 ns with 1% settling. With −82 dB of crosstalk and −88 dB isolation (at 5 MHz), the ADV3219 and ADV3220 are useful in many high speed applications. The differential gain of less than 0.02% and the differential phase of less than 0.02°, together with 0.1 dB flatness beyond 100 MHz while driving a 75 Ω back terminated load, make the ADV3219 and ADV3220 ideal for all types of signal switching.

The ADV3219/ADV3220 include an output buffer that can be placed into a high impedance state to allow multiple outputs to be connected together for cascading stages without the off channels loading the output bus. The ADV3219 has a gain of +1, and the ADV3220 has a gain of +2; they both operate on ±5 V supplies while consuming less than 7.5 mA of idle current.

The ADV3219/ADV3220 are available in the 8-lead LFCSP package over the extended industrial temperature range of −40°C to +85°C.

Rev. A

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REVISION HISTORY

5/2016—Rev. 0 to Rev. A

Changes to General Description Section 1
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Updated Outline Dimensions 18

4/2010—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5 V, T_A = 25°C, R_L = 150 Ω, C_L = 4 pF, ADV3219 at G = +1, ADV3220 at G = +2, unless otherwise noted.

Table 1.

		ADV3219			ADV3220			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE								
−3 dB Bandwidth	200 mV p-p		840			800		MHz
	2 V p-p		600			730		MHz
Gain Flatness	0.1 dB, 200 mV p-p		100			100		MHz
	0.1 dB, 2 V p-p		100			100		MHz
Propagation Delay	2 V p-p		700			650		ps
Settling Time	1%, 2 V step		5			5		ns
Slew Rate	2 V step, peak		2200			2800		V/µs
NOISE/DISTORTION PERFORMANCE								
Differential Gain Error	NTSC or PAL		0.02			0.02		%
Differential Phase Error	NTSC or PAL		0.02			0.02		Degrees
Crosstalk	f = 5 MHz		−90			−82		dB
	f = 100 MHz		−70			−60		dB
Off Isolation, Input to Output	f = 5 MHz, one channel		−92			−88		dB
Input Second-Order Intercept	f = 70 MHz, ADV3220, R_L = 100 Ω					47		dBm
Input Third-Order Intercept	f = 70 MHz, ADV3220, R_L = 100 Ω					34		dBm
Output 1 dB Compression Point	f = 70 MHz, ADV3220, R_L = 100 Ω					20		dBm
Input Voltage Noise	10 MHz to 100 MHz		16			17		nV/√Hz
DC PERFORMANCE								
Gain Error	No load			1			1	%
	R_L = 150 Ω		0.75	1.1		0.75	1.1	%
Gain Matching	Channel-to-channel, no load		1			1		%
OUTPUT CHARACTERISTICS								
Output Impedance	DC, enabled		0.02			0.04		Ω
	Disabled	1			1			MΩ
Output Disable Capacitance	Disabled		1.0			1.2		pF
Output Leakage Current	Disabled		2			2		µA
Output Voltage Range	No load	2.9	±3		2.9	±3		V
	Load	2.8	±3		2.75	±3		V
	Short-circuit current		50			50		mA
INPUT CHARACTERISTICS								
Input Offset Voltage	Worst case (all configurations)		±5	21		±5	21	mV
Input Offset Voltage Drift			±10			±10		µV/°C
Input Voltage Range	No load		±3			±1.5		V
	R_L = 150 Ω		±3			±1.5		V
Input Capacitance	Any switch configuration		0.6			0.6		pF
Input Resistance	Output enabled	1	10		1	10		MΩ
Input Bias Current	Output enabled		5	12		6	12	µA
SWITCHING CHARACTERISTICS								
Enable On Time			15			15		ns
Switching Time, 2 V Step	50% SELECT to 1% settling		20			20		ns
Switching Transient (Glitch)	IN0 to IN1 switching		70			100		mV p-p

Parameter	Test Conditions/Comments	ADV3219 Min	ADV3219 Typ	ADV3219 Max	ADV3220 Min	ADV3220 Typ	ADV3220 Max	Unit
POWER SUPPLIES								
Supply Current	V+, output enabled, no load		7	8		7.5	9	mA
	V+, output disabled ($\overline{EN}$ high)		1.6	2.0		1.8	2.2	mA
	V−, output enabled, no load		7	8		7.5	9	mA
	V−, output disabled ($\overline{EN}$ high)		1.6	2.0		1.8	2.2	mA
Supply Voltage Range		±4.5		±5.5	±4.5		±5.5	V
PSR	f = 100 kHz		−72			−69		dB
	f = 1 MHz		−62			−60		dB
TEMPERATURE								
Operating Temperature Range	Still air	−40		+85	−40		+85	°C
Operating Junction-to-Ambient Thermal Impedance, θ_{JA}	Still air		85			85		°C/W

Table 2. Logic Levels

V_{IH}	V_{IL}	I_{IH}	I_{IL}
SELECT, $\overline{EN}$	SELECT, $\overline{EN}$	SELECT, $\overline{EN}$	SELECT, $\overline{EN}$
+2.0 V minimum	+0.8 V maximum	±2 µA maximum	±2 µA maximum

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage (V+ – V–)	12 V
Analog Input Voltage	V– to V+
Digital Input Voltage	0 to V+
Output Voltage (Disabled Output)	(V+ – 1 V) to (V– + 1 V)
Output Short-Circuit	
Duration	Momentary
Current	50 mA
Temperature	
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +85°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead LFCSP	85	23	°C/W

POWER DISSIPATION

The ADV3219/ADV3220 are operated with ±5 V supplies and can drive loads down to 150 Ω, resulting in a wide range of possible power dissipations. For this reason, extra care must be taken derating the operating conditions based on ambient temperature.

Packaged in an 8-lead LFCSP, the ADV3219 and ADV3220 junction-to-ambient thermal impedance (θ_{JA}) is 85°C/W. For long-term reliability, the maximum allowed junction temperature of the die, T_J, must not exceed 125°C. Temporarily exceeding this limit can cause a shift in parametric performance due to a change in stresses exerted on the die by the package. Figure 2 shows the range of the allowed internal die power dissipations that meet these conditions over the –40°C to +85°C ambient temperature range. When using Figure 2, do not include the external load power in the maximum power calculation, but do include the load current through the die output transistors.

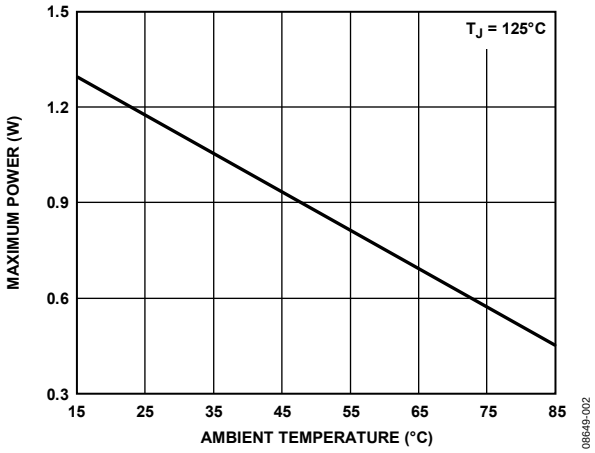

Figure 2. Maximum Die Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

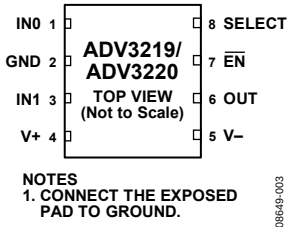

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Descriptions
1	IN0	Analog Input.
2	GND	Ground.
3	IN1	Analog Input.
4	V+	Positive Power Supply.
5	V–	Negative Power Supply.
6	OUT	Analog Output.
7	$\overline{EN}$	Output Enable (Low True).
8	SELECT	Logic Input for Analog Input Selection.
N/A[1]	EP	Exposed Pad. Connect the exposed pad to ground.

[1] N/A means not applicable.

Table 6. Truth Table

SELECT	$\overline{EN}$	OUT
0	0	IN0
1	0	IN1
0	1	High-Z
1	1	High-Z

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±5 V, T_A = 25°C, R_L = 150 Ω, C_L = 4 pF, ADV3219 at G = +1, ADV3220 at G = +2, unless otherwise noted.

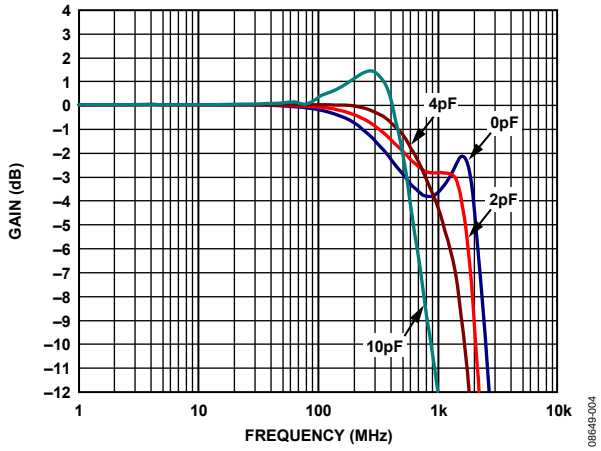

Figure 4. ADV3219 Small Signal Frequency Response with Capacitive Loads, 200 mV p-p Output

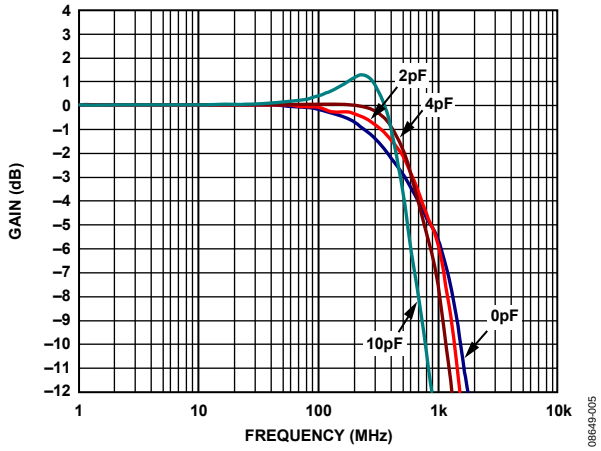

Figure 5. ADV3219 Large Signal Frequency Response with Capacitive Loads, 2 V p-p Output

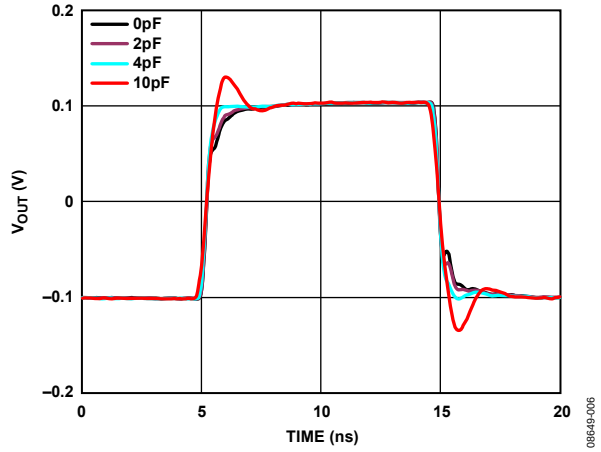

Figure 6. ADV3219 Small Signal Pulse Response vs. Capacitive Load, 200 mV p-p Output

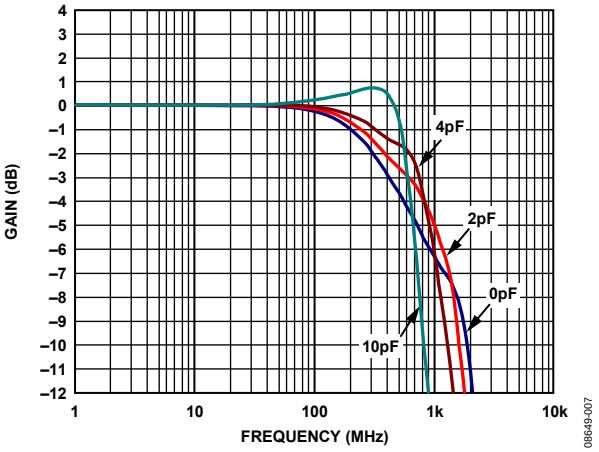

Figure 7. ADV3220 Small Signal Frequency Response with Capacitive Loads, 200 mV p-p Output

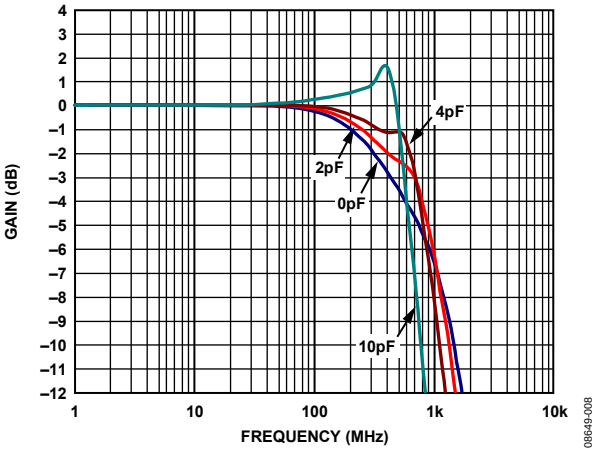

Figure 8. ADV3220 Large Signal Frequency Response with Capacitive Loads, 2 V p-p Output

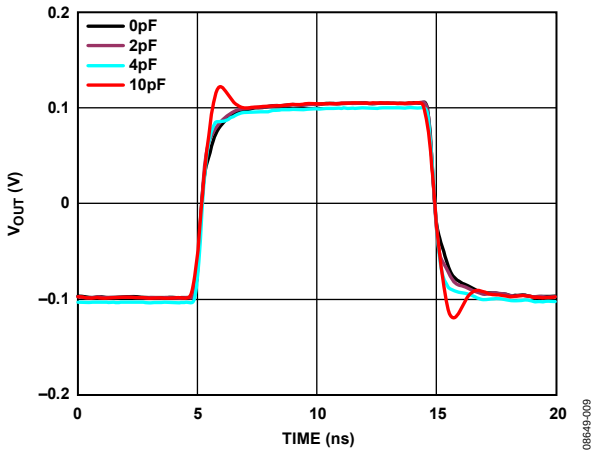

Figure 9. ADV3220 Small Signal Pulse Response vs. Capacitive Load, 200 mV p-p Output

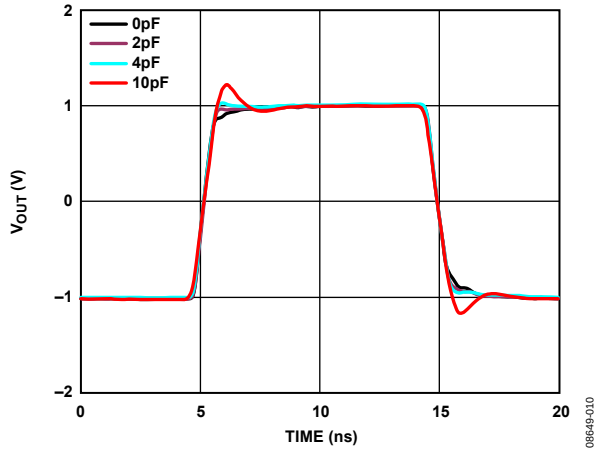

Figure 10. ADV3219 Large Signal Pulse Response vs. Capacitive Load, 2 V p-p Output

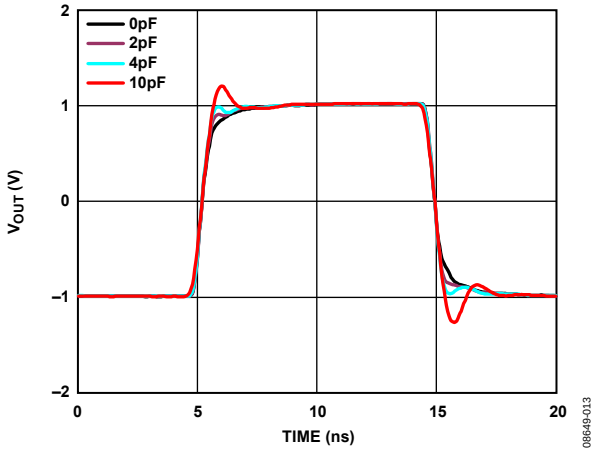

Figure 13. ADV3220 Large Signal Pulse Response vs. Capacitive Load, 2 V p-p Output

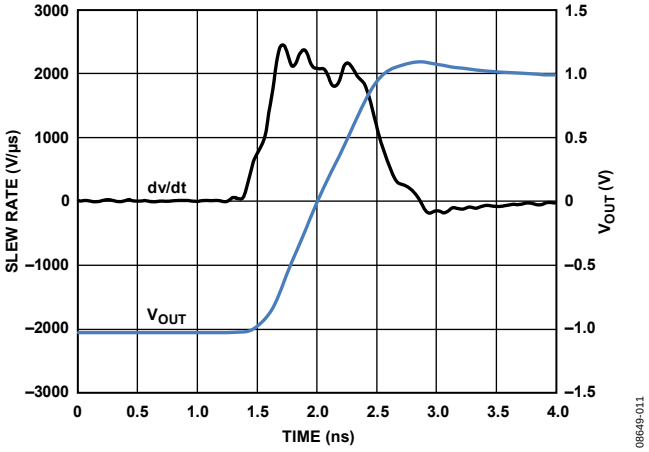

Figure 11. ADV3219 Large Signal Rising Slew Rate with 4 pF Load, 2 V p-p Output

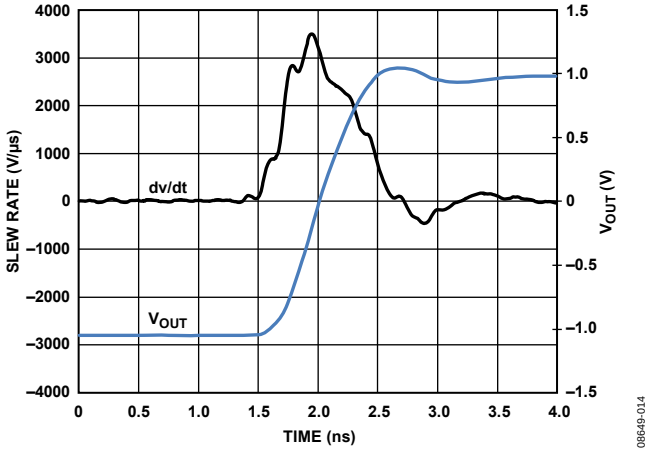

Figure 14. ADV3220 Large Signal Rising Slew Rate with 4 pF Load, 2 V p-p Output

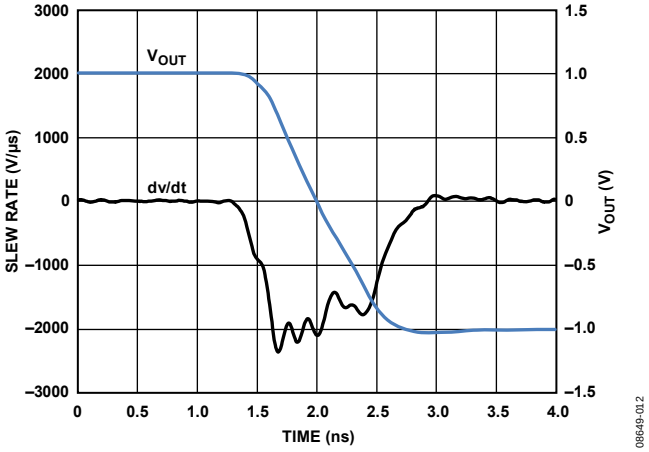

Figure 12. ADV3219 Large Signal Falling Slew Rate with 4 pF Load, 2 V p-p Output

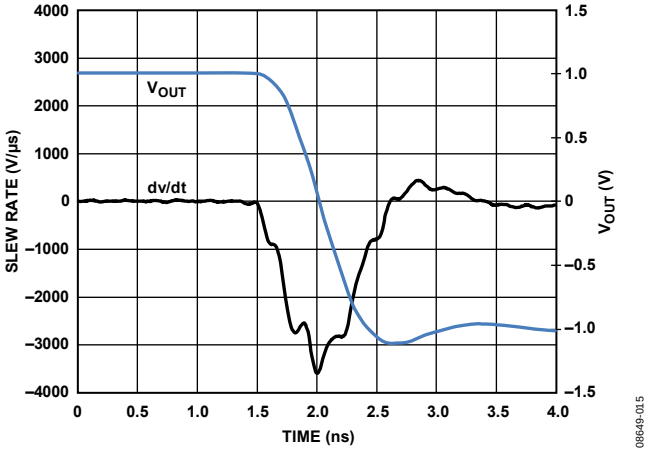

Figure 15. ADV3220 Large Signal Falling Slew Rate with 4 pF Load, 2 V p-p Output

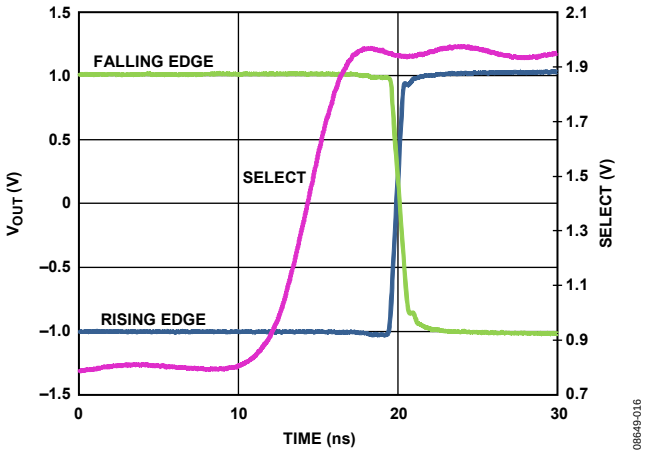

Figure 16. ADV3219 Switching Time

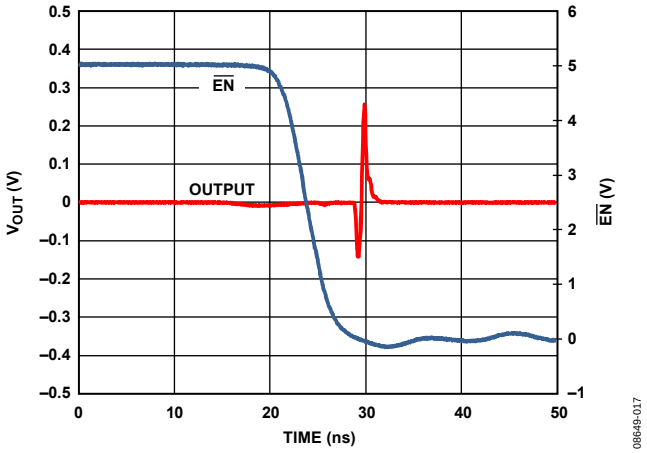

Figure 17. ADV3219 Enable Glitch

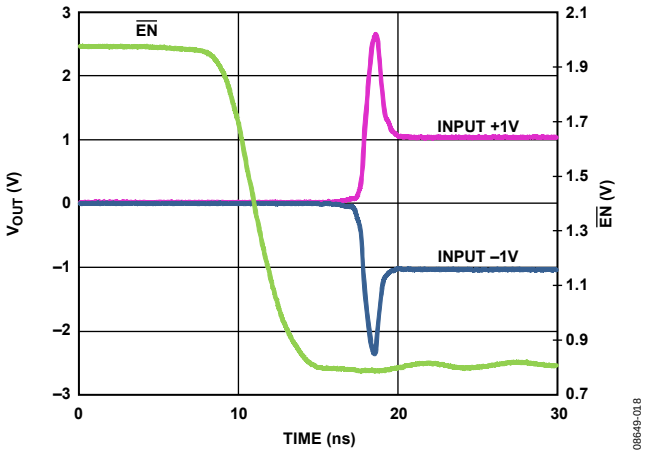

Figure 18. ADV3219 Enable On Timing

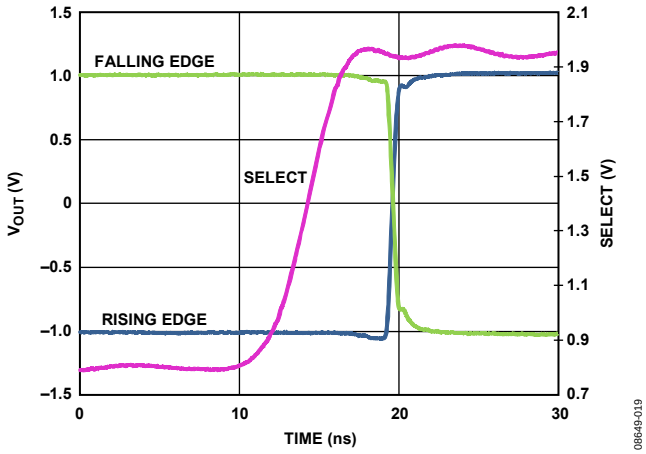

Figure 19. ADV3220 Switching Time

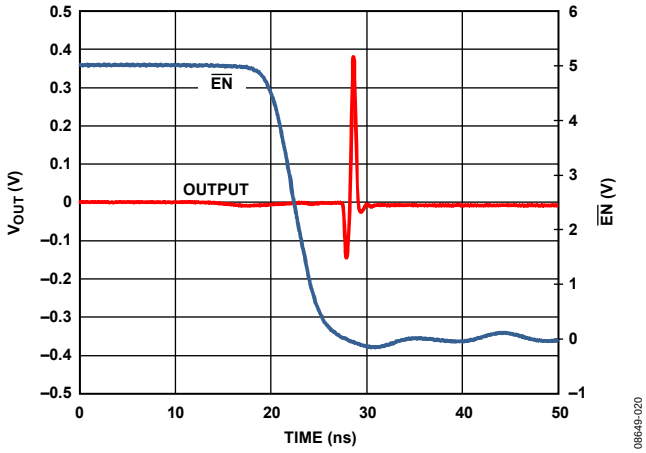

Figure 20. ADV3220 Enable Glitch

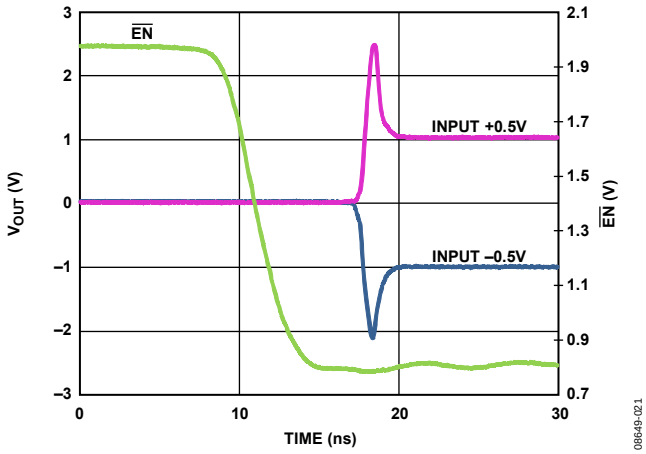

Figure 21. ADV3220 Enable On Timing

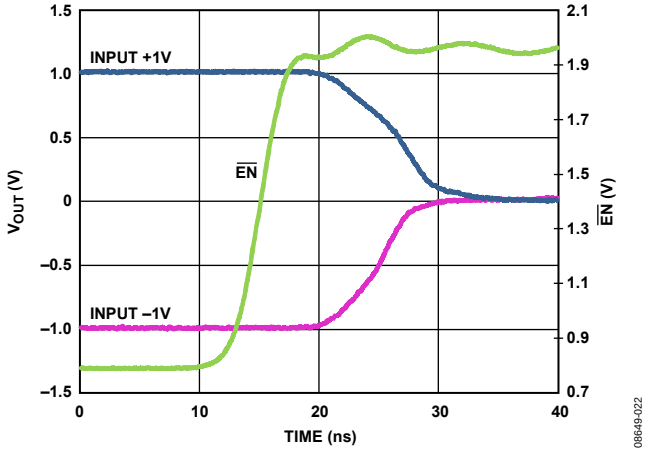

Figure 22. ADV3219 Disable Timing

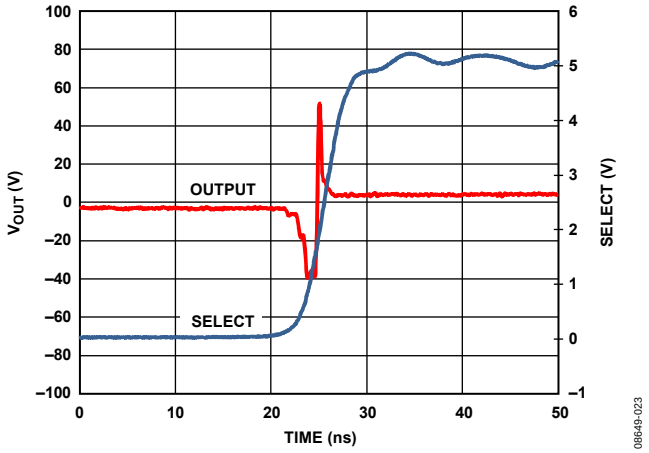

Figure 23. ADV3219 Switching Glitch Rising Edge

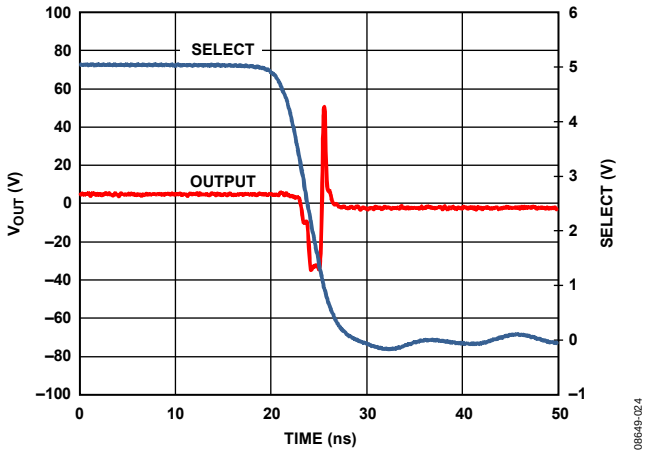

Figure 24. ADV3219 Switching Glitch Falling Edge

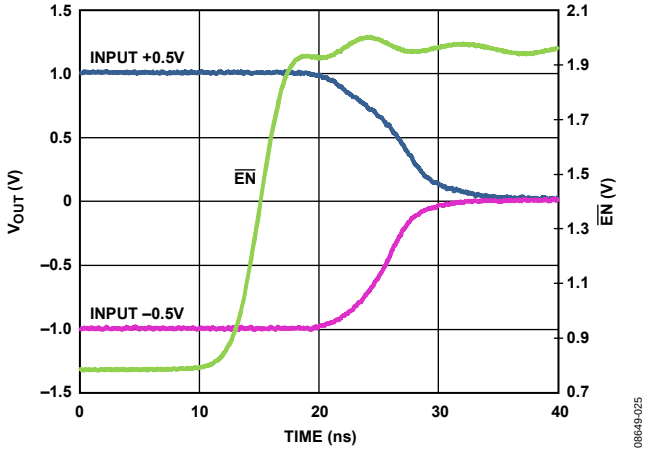

Figure 25. ADV3220 Disable Timing

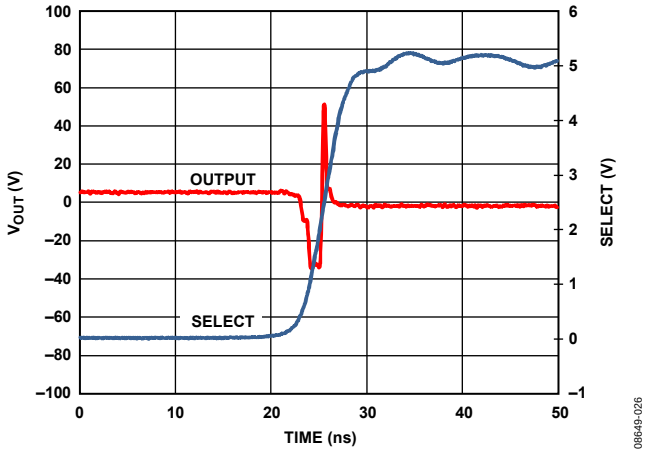

Figure 26. ADV3220 Switching Glitch Rising Edge

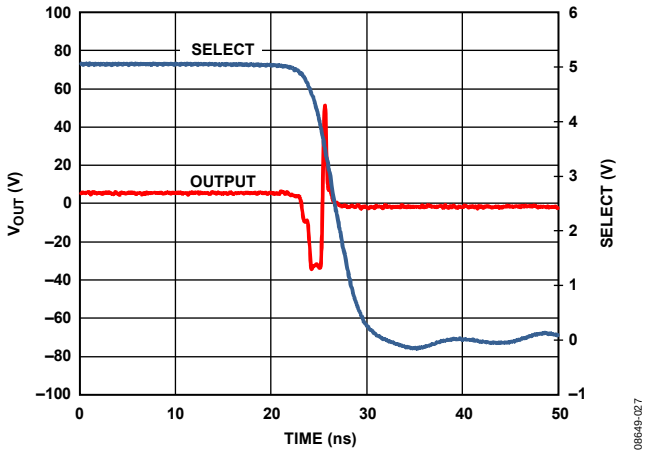

Figure 27. ADV3220 Switching Glitch Falling Edge

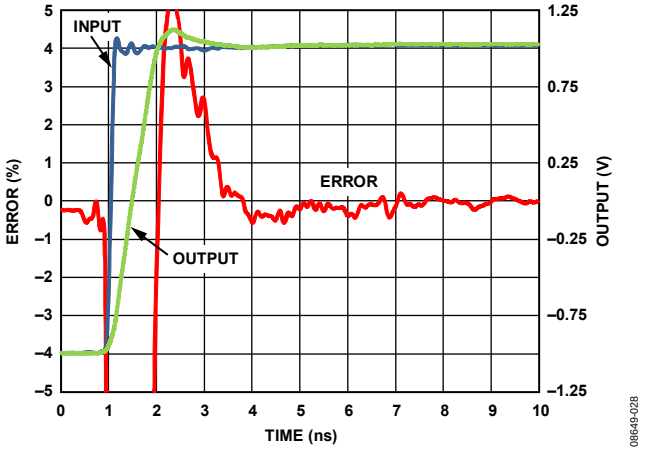

Figure 28. ADV3219 Settling Time 2 V Output Step

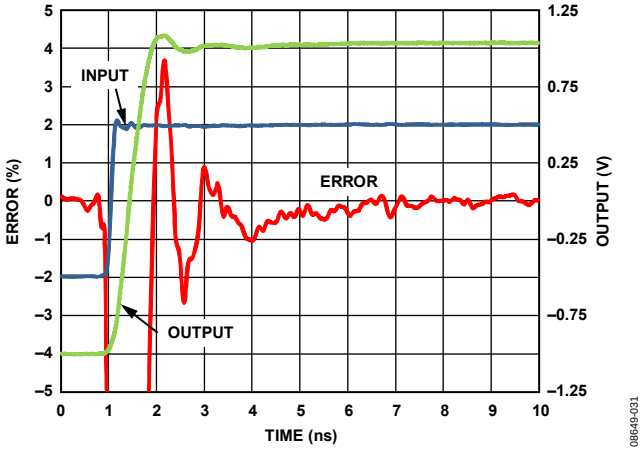

Figure 31. ADV3220 Settling Time 2 V Output Step

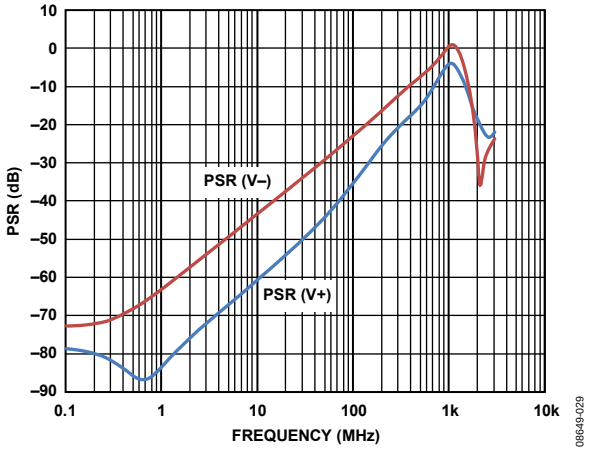

Figure 29. ADV3219 PSR

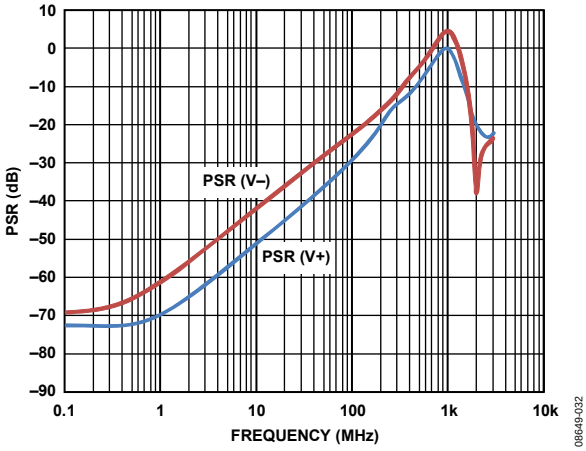

Figure 32. ADV3220 PSR

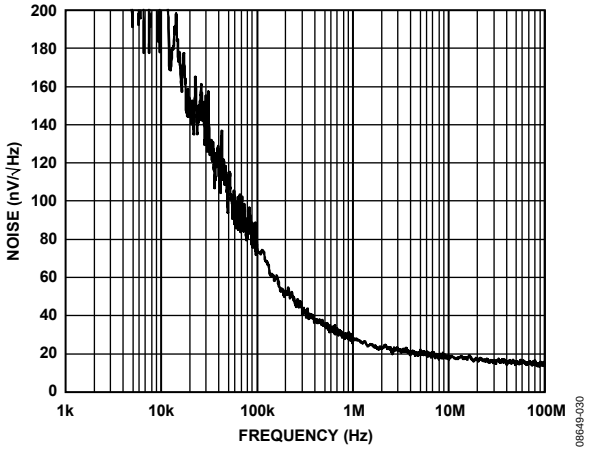

Figure 30. ADV3219 Noise vs. Frequency

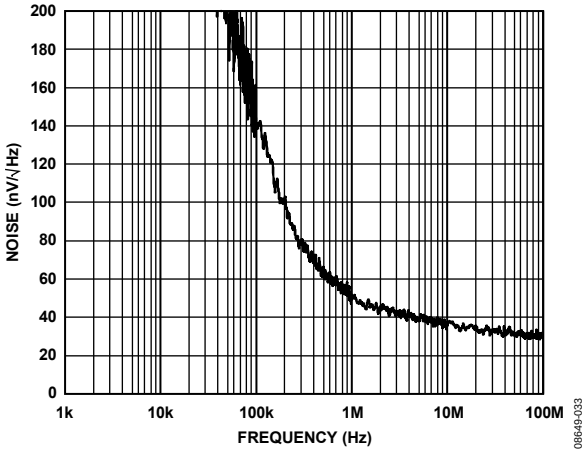

Figure 33. ADV3220 Noise vs. Frequency

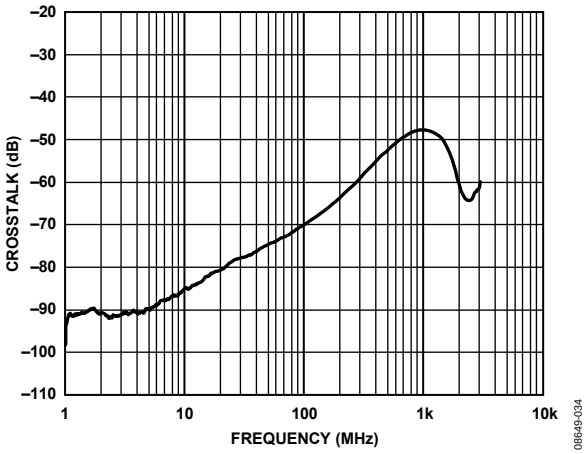

Figure 34. ADV3219 Crosstalk vs. Frequency

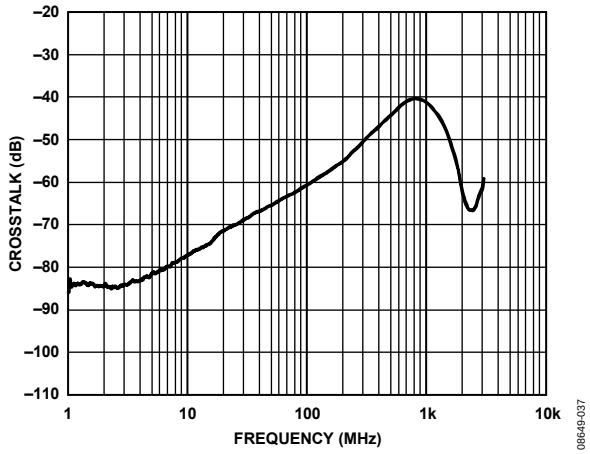

Figure 37. ADV3220 Crosstalk vs. Frequency

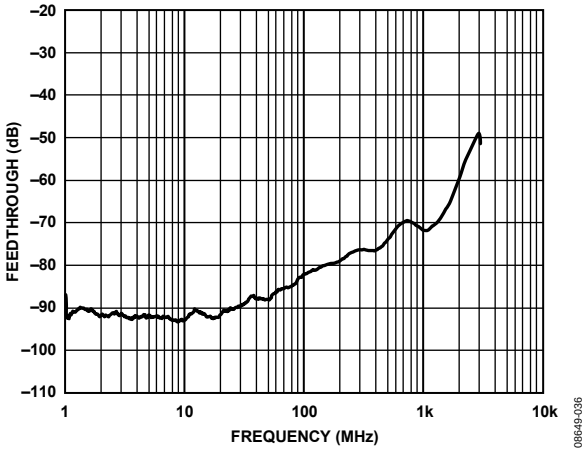

Figure 35. ADV3219 Off Isolation vs. Frequency

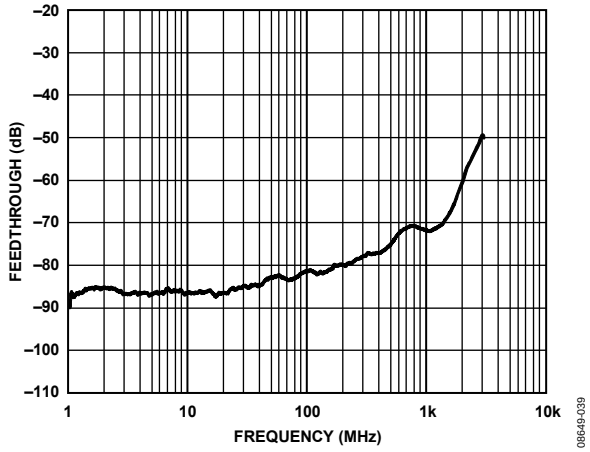

Figure 38. ADV3220 Off Isolation vs. Frequency

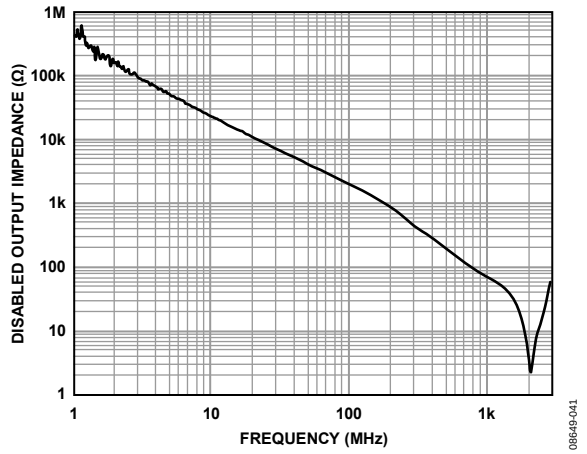

Figure 36. ADV3219 Disabled Output Impedance vs. Frequency

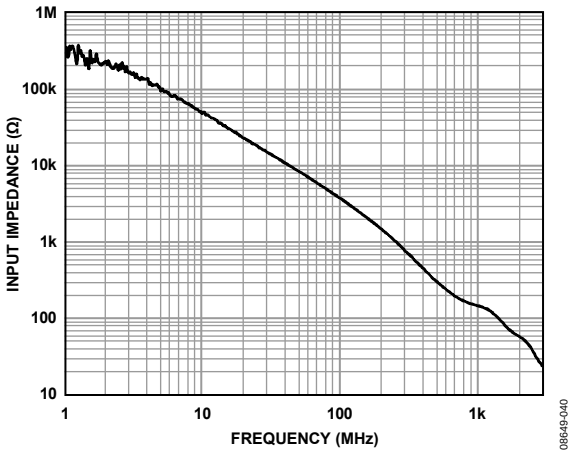

Figure 39. ADV3219/ADV3220 Input Impedance vs. Frequency

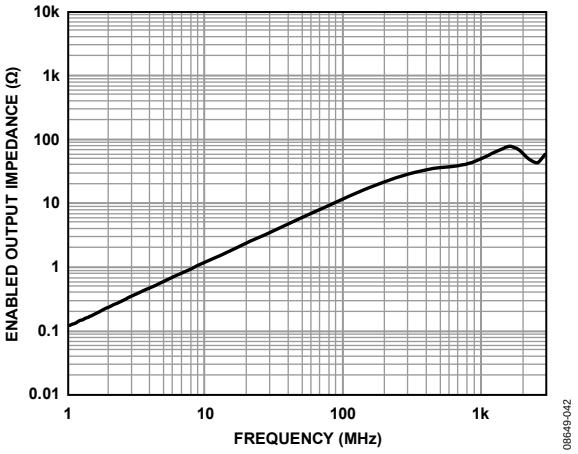

Figure 40. ADV3219 Enabled Output Impedance vs. Frequency

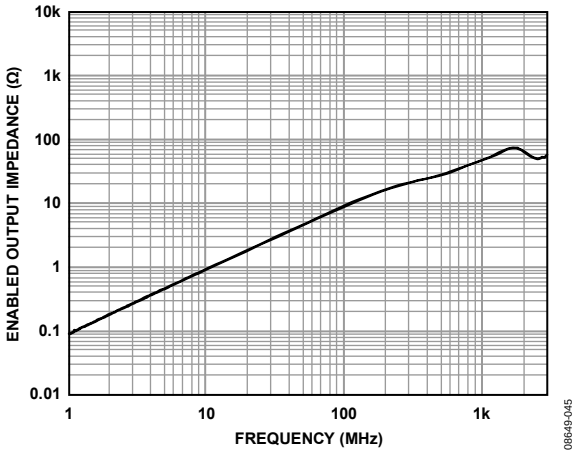

Figure 43. ADV3220 Enabled Output Impedance vs. Frequency

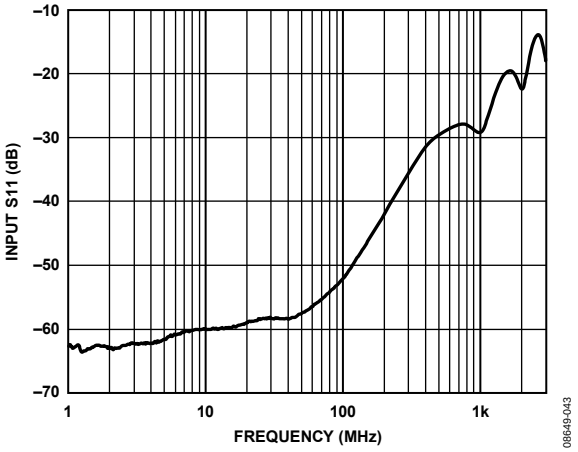

Figure 41. ADV3219/ADV3220, S11 (Measured on Evaluation Board)

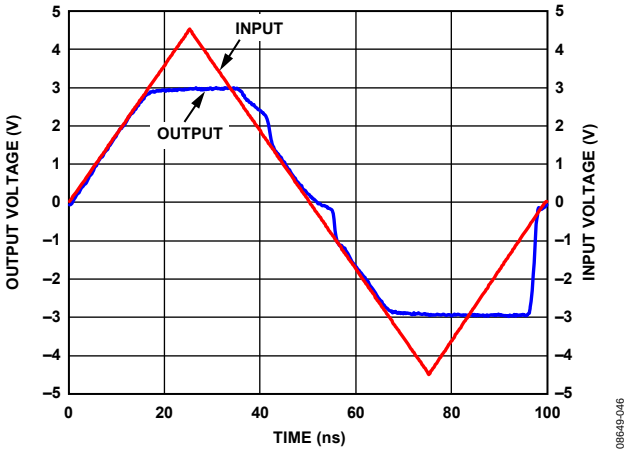

Figure 44. ADV3219 Overdrive Recovery

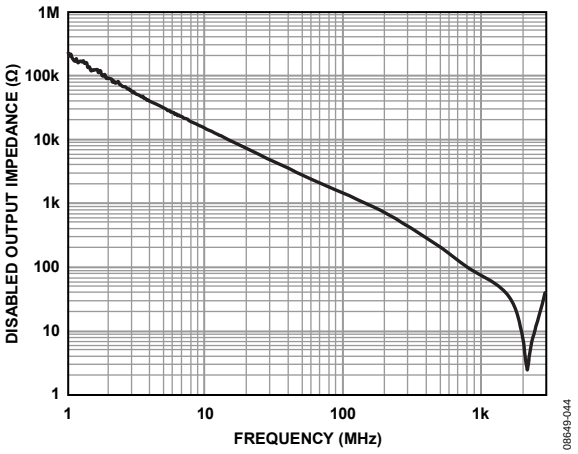

Figure 42. ADV3220 Disabled Output Impedance vs. Frequency

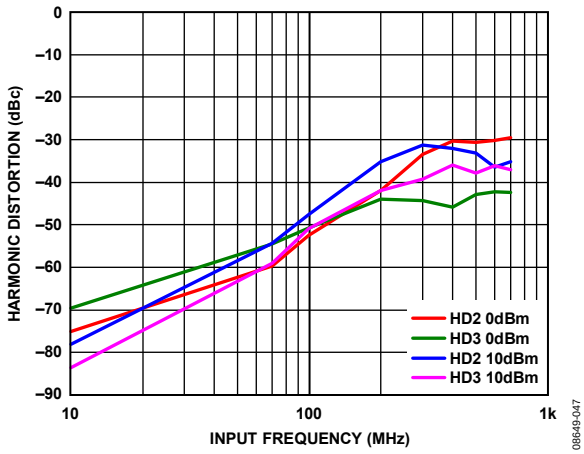

Figure 45. ADV3220 Harmonic Distortion, R_L = 100 Ω, C_L = 4 pF

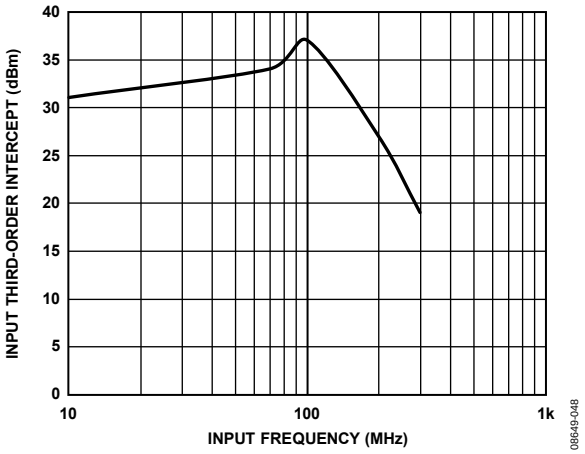

Figure 46. ADV3220 Input Third-Order Intercept, R_L = 100 Ω, C_L = 4 pF, 0 dBm Input

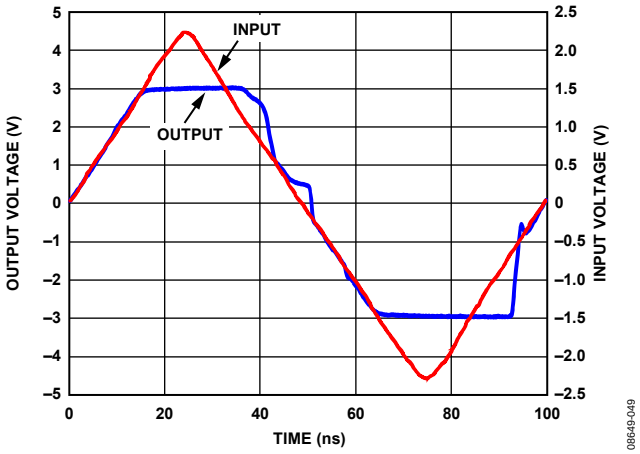

Figure 47. ADV3220 Overdrive Recovery

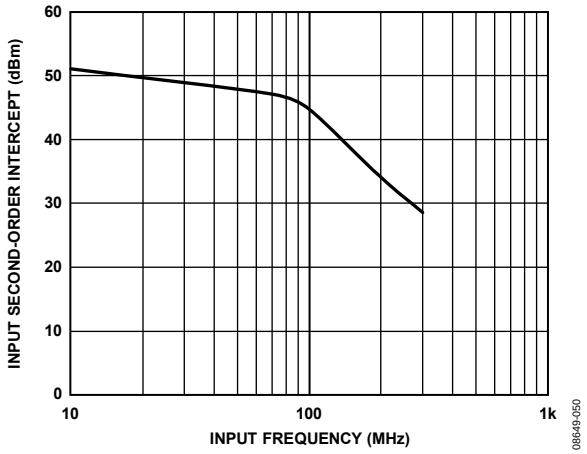

Figure 48. ADV3220 Input Second-Order Intercept, R_L = 100 Ω, C_L = 4 pF, 0 dBm Input

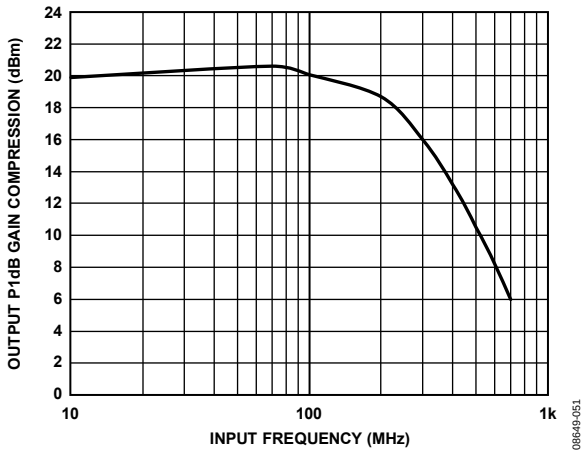

Figure 49. ADV3220 Output P1dB Gain Compression, R_L = 100 Ω, C_L = 4 pF

CIRCUIT DIAGRAMS

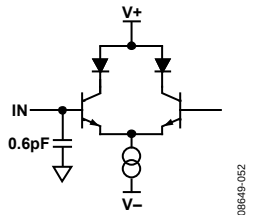

Figure 50. ADV3219/ADV3220 Analog Input

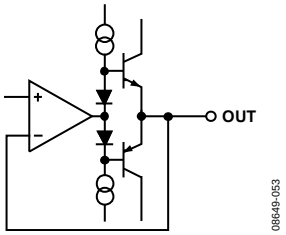

Figure 51. ADV3219 Enabled Analog Output

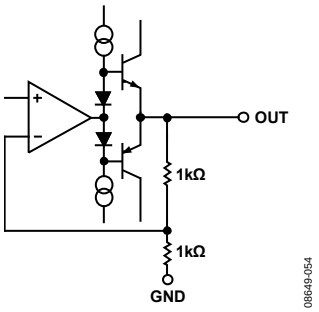

Figure 52. ADV3220 Enabled Analog Output

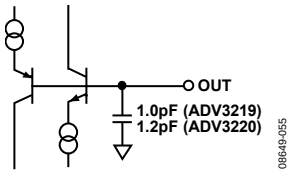

Figure 53. ADV3219/ADV3220 Disabled Output

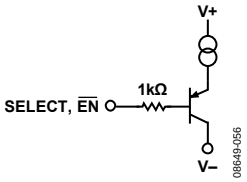

Figure 54. ADV3219/ADV3220 Logic Input

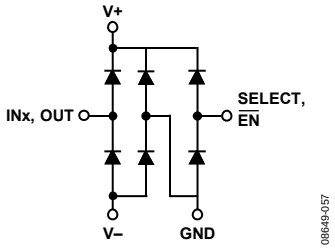

Figure 55. ADV3219/ADV3220 ESD Schematic

THEORY OF OPERATION

The ADV3219/ADV3220 are dual-supply, high performance 2:1 analog multiplexers, optimized for switching between multiple video sources. High peak slew rates enable wide bandwidth operation for large input signals. Internal compensation provides for high phase margin, allowing low overshoot and fast settling for pulsed inputs. Low enabled and disabled power consumption make the ADV3219 and ADV3220 ideal for constructing larger arrays.

The multiplexer is organized as two input transconductance stages tied in parallel with a single output transimpedance stage followed by a unity-gain buffer. Internal voltage feedback sets the gain. The ADV3219 is configured as a gain of 1, whereas the ADV3220 uses a resistive feedback network and ground buffer to realize gain-of-2 operation (see Figure 56). The ground reference for the ADV3220 is taken from the exposed pad of the package. To minimize spurious signals on the output, tie the exposed pad to a low inductance, quiet ground plane.

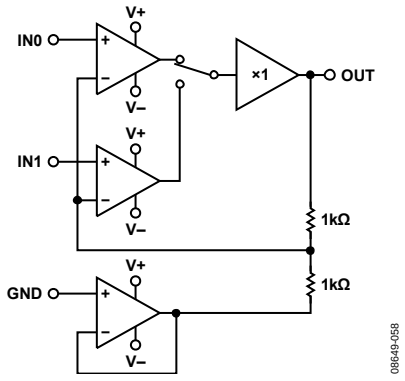

Figure 56. Conceptual Diagram of ADV3220

When not in use, place the OUT pin in a low power, high impedance disabled mode via the $\overline{EN}$ logic input. This mode provides a wideband high impedance on the OUT pin that is useful when paralleling multiple ADV3219/ADV3220 devices in a system to create larger switching arrays.

Switching between the inputs is controlled with the SELECT logic input, with IN0 selected when the SELECT line is a logical low and IN1 selected when the select line is a logical high. When $\overline{EN}$ is a logical low, the output is enabled and connected to one of the two inputs depending on the state of the SELECT pin. When $\overline{EN}$ is a logical high, the output is placed in a high impedance mode.

When not in use, the output can be placed in a low power, high impedance disabled mode via the $\overline{EN}$ logic input.

APPLICATIONS INFORMATION

The ADV3219 and ADV3220 are high speed muxes that can be used to switch video or RF signals. The low output impedance of the ADV3219/ADV3220 allows the output environment to be optimized for use in 75 Ω or 50 Ω systems by choosing the appropriate series termination resistor. For composite video applications, the ADV3220 (gain of +2) is typically used to provide compensation for the loss of the output termination.

CIRCUIT LAYOUT

Use of proper high speed design techniques is important to ensure optimum performance. Use a low inductance ground plane for power supply bypassing and to provide high quality return paths for the input and output signals. For best performance, it is recommended that power supplies be bypassed with 0.1 µF ceramic capacitors placed as close to the body of the device as possible. To provide stored energy for lower frequency, high current output driving, place 10 µF tantalum capacitors farther from the device.

The input and output signal paths should be stripline or microstrip controlled impedance. Video systems typically use a 75 Ω characteristic impedance, whereas RF systems typically use 50 Ω. Various calculators are available to calculate the trace geometry that is required to produce the proper characteristic impedance.

TERMINATION

For a controlled impedance situation, termination resistors are required at the inputs and output of the device. Ensure that the input termination is a shunt resistor to ground with a value matching the characteristic impedance of the input trace. To reduce reflections, place the input termination resistor as close to the device input pin as possible. To minimize the input-to-input crosstalk, it is important to use a low inductance shield between input traces to isolate each input. Consideration of ground current paths must be taken to minimize loop currents in the shields to prevent them from providing a coupling medium for crosstalk.

For proper matching, the output series termination resistor should be the same value as the characteristic impedance of the output trace and placed as close to the output of the device as possible. This placement reduces the high frequency effect of series parasitic inductance, which can affect gain flatness and −3 dB bandwidth.

CAPACITIVE LOAD

A high frequency output generally has difficulty when driving a capacitive load. The usual response is some peaking in the frequency domain or some overshoot in the time domain. If these effects become too large, oscillation can result.

The response of the device under various capacitive loads is shown in Figure 4 to Figure 10 and in Figure 13. If a condition arises wherein excessive load capacitance is encountered and the overshoot is too great or the part oscillates, use a small series resistor of a few tens of ohms to improve the performance.