

FEATURES

- 1.8 V to 5.5 V single supply
- ± 2.5 V dual supply
- 3 Ω on resistance
- 0.75 Ω on resistance flatness
- 100 pA leakage currents
- 14 ns switching times
- Single 8-to-1 multiplexer **ADG708**
- Differential 4-to-1 multiplexer **ADG709**
- 16-lead TSSOP package
- Low power consumption
- TTL-/CMOS-compatible inputs
- Qualified for automotive applications

APPLICATIONS

- Data acquisition systems
- Communication systems
- Relay replacement
- Audio and video switching
- Battery-powered systems

GENERAL DESCRIPTION

The **ADG708/ADG709** are low voltage, CMOS analog multiplexers comprising eight single channels and four differential channels, respectively. The **ADG708** switches one of eight inputs (S1 to S8) to a common output, D, as determined by the 3-bit binary address lines A0, A1, and A2. The **ADG709** switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched off.

Low power consumption and an operating supply range of 1.8 V to 5.5 V make the **ADG708/ADG709** ideal for battery-powered, portable instruments. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels.

These switches are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed, very low on resistance, and leakage currents.

On resistance is in the region of a few ohms and is closely matched between switches and very flat over the full signal range. These parts can operate equally well as either multiplexers or demultiplexers and have an input signal range that extends to the supplies.

The **ADG708/ADG709** are available in a 16-lead TSSOP.

Rev. E

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FUNCTIONAL BLOCK DIAGRAMS

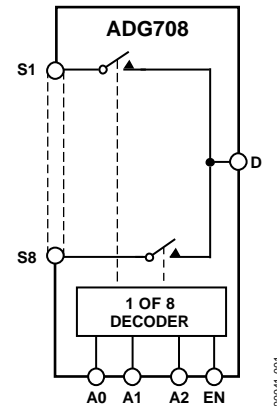


Figure 1.

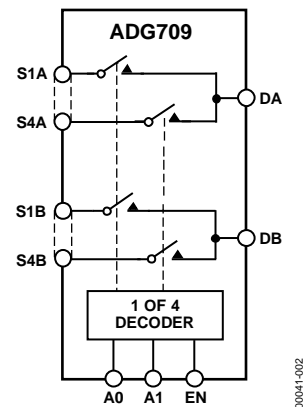


Figure 2.

PRODUCT HIGHLIGHTS

1. Single-/dual-supply operation. The **ADG708/ADG709** are fully specified and guaranteed with 3 V and 5 V single-supply and ± 2.5 V dual-supply rails.
2. Low R_{ON} (3 Ω typical).
3. Low power consumption (<0.01 μ W).
4. Guaranteed break-before-make switching action.
5. Small 16-lead TSSOP package.

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REVISION HISTORY

9/14–Rev. D to Rev. E

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1/13–Rev. C to Rev. D

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10/00—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	B Version			C Version			Unit	Test Conditions/ Comments
	+25°C	-40°C to +85°C	-40°C to +125°C	+25°C	-40°C to +85°C	-40°C to +125°C		
ANALOG SWITCH								
Analog Signal Range		0 V to V_{DD}	0 V to V_{DD}			0 V to V_{DD}	V	
On Resistance (R_{ON})	3			3			Ω typ	$V_S = 0\text{ V to } V_{DD}$, $I_{DS} = 10\text{ mA}$; see Figure 20
On Resistance Match Between Channels (ΔR_{ON})	4.5 0.4	5 7	7	4.5 0.4	5 7	7	Ω max Ω typ	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.75	0.8	1.5	0.75	0.8	1.5	Ω max Ω typ	$V_S = 0\text{ V to } V_{DD}$, $I_{DS} = 10\text{ mA}$ $V_S = 0\text{ V to } V_{DD}$, $I_{DS} = 10\text{ mA}$
		1.2	1.65		1.2	1.65	Ω max	
LEAKAGE CURRENTS								
Source Off Leakage, I_S (Off)	± 0.01			± 0.01			nA typ	$V_{DD} = 5.5\text{ V}$ $V_D = 4.5\text{ V}/1\text{ V}$, $V_S = 1\text{ V}/4.5\text{ V}$; see Figure 21
Drain Off Leakage, I_D (Off)	± 0.01	± 20	± 20	± 0.1 ± 0.01	± 0.3	± 1	nA max nA typ	$V_D = 4.5\text{ V}/1\text{ V}$, $V_S = 1\text{ V}/4.5\text{ V}$; see Figure 22
Channel On Leakage, I_D , I_S (On)	± 0.01	± 20	± 20	± 0.1 ± 0.01	± 0.75	± 6	nA max nA typ	$V_D = V_S = 1\text{ V or } 4.5\text{ V}$; see Figure 23
		± 20	± 20	± 0.1	± 0.75	± 6	nA max	
DIGITAL INPUTS								
Input High Voltage, V_{INH}			2.4			2.4	V min	
Input Low Voltage, V_{INL}			0.8			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		± 0.1	0.005		± 0.1	μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
Digital Input Capacitance, C_{IN}	2			2			pF typ	
DYNAMIC CHARACTERISTICS ¹								
$t_{TRANSITION}$	14			14			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; see Figure 24
Break-Before-Make Time Delay, t_{OPEN}	8	25	25	8	25	25	ns max ns typ	$V_{S1} = 3\text{ V}/0\text{ V}$, $V_{S8} = 0\text{ V}/3\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
$t_{ON(EN)}$	14	1	1	14	1	1	ns min ns typ	$V_S = 3\text{ V}$; see Figure 25 $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
$t_{OFF(EN)}$	7	25	25	7	25	25	ns max ns typ	$V_S = 3\text{ V}$; see Figure 26 $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
Charge Injection	± 3	12	12	± 3	12	12	ns max pC typ	$V_S = 3\text{ V}$; see Figure 26 $V_S = 2.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; See Figure 27
Off Isolation	-60 -80			-60 -80			dB typ dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$ $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28

Parameter	B Version			C Version			Unit	Test Conditions/ Comments
	+25°C	-40°C to +85°C	-40°C to +125°C	+25°C	-40°C to +85°C	-40°C to +125°C		
Channel-to-Channel Crosstalk	-60			-60			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 10 \text{ MHz}$
	-80			-80			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 29
-3 dB Bandwidth	55			55			MHz typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 30
C_S (Off)	13			13			pF typ	$f = 1 \text{ MHz}$
C_D (Off)								
ADG708	85			85			pF typ	$f = 1 \text{ MHz}$
ADG709	42			42			pF typ	$f = 1 \text{ MHz}$
C_D , C_S (On)								
ADG708	96			96			pF typ	$f = 1 \text{ MHz}$
ADG709	48			48			pF typ	$f = 1 \text{ MHz}$
POWER REQUIREMENTS								$V_{DD} = 5.5 \text{ V}$
I_{DD}	0.001			0.001			$\mu\text{A typ}$	Digital inputs = 0 V or 5.5 V
		1.0	1.0		1.0	1.0	$\mu\text{A max}$	

¹ Guaranteed by design, not subject to production test.

$V_{DD} = 3\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	B Version			C Version			Unit	Test Conditions/ Comments
	+25°C	-40°C to +85°C	-40°C to +125°C	+25°C	-40°C to +85°C	-40°C to +125°C		
ANALOG SWITCH								
Analog Signal Range			0 V to V_{DD}			0 V to V_{DD}	V	
On Resistance (R_{ON})	8			8			Ω typ	$V_S = 0\text{ V to } V_{DD}$, $I_{DS} = 10\text{ mA}$; see Figure 20
On Resistance Match Between Channels (ΔR_{ON})	11	12	14	11	12	14	Ω max	$V_S = 0\text{ V to } V_{DD}$, $I_{DS} = 10\text{ mA}$
	0.4			0.4			Ω typ	
		1.2	2		1.2	2	Ω max	
LEAKAGE CURRENTS								
Source Off Leakage, I_S (Off)	± 0.01			± 0.01			nA typ	$V_{DD} = 3.3\text{ V}$ $V_S = 3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3\text{ V}$; see Figure 21
Drain Off Leakage, I_D (Off)	± 0.01	± 20	± 20	± 0.1	± 0.3	± 1	nA max nA typ	$V_S = 3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3\text{ V}$; see Figure 22
		± 20	± 20	± 0.1	± 0.75	± 6	nA max nA typ	
Channel On Leakage, I_D , I_S (On)	± 0.01			± 0.01			nA max nA typ	$V_S = V_D = 1\text{ V or } 3\text{ V}$; see Figure 23
		± 20	± 20	± 0.1	± 0.75	± 6	nA max	
DIGITAL INPUTS								
Input High Voltage, V_{INH}			2.0			2.0	V min	$V_{IN} = V_{INL}$ or V_{INH}
Input Low Voltage, V_{INL}			0.8			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		± 0.1	0.005		± 0.1	μA typ μA max	
Digital Input Capacitance, C_{IN}	2			2			pF typ	
DYNAMIC CHARACTERISTICS¹								
$t_{TRANSITION}$	18			18			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; see Figure 24
Break-Before-Make Time Delay, t_{OPEN}	8	30	30	8	30	30	ns max ns typ	$V_{S1} = 2\text{ V}/0\text{ V}$, $V_{S2} = 0\text{ V}/2\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
		1	1		1	1	ns min ns typ	
t_{ON} (EN)	18	30	30	18	30	30	ns max	$V_S = 2\text{ V}$; see Figure 25 $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
t_{OFF} (EN)	8			8			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$; see Figure 26
		15	15		15	15	ns max	
Charge Injection	± 3			± 3			pC typ	$V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 27
Off Isolation	-60			-60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$
	-80			-80			dB typ	
Channel-to-Channel Crosstalk	-60			-60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$
	-80			-80			dB typ	
-3 dB Bandwidth	55			55			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 30

Parameter	B Version			C Version			Unit	Test Conditions/ Comments
	+25°C	-40°C to +85°C	-40°C to +125°C	+25°C	-40°C to +85°C	-40°C to +125°C		
C _S (Off)	13			13			pF typ	f = 1 MHz
C _D (Off)								
ADG708	85			85			pF typ	f = 1 MHz
ADG709	42			42			pF typ	f = 1 MHz
C _D , C _S (On)								
ADG708	96			96			pF typ	f = 1 MHz
ADG709	48			48			pF typ	f = 1 MHz
POWER REQUIREMENTS								V _{DD} = 3.3 V
I _{DD}	0.001			0.001			μA typ	Digital inputs = 0V or 3.3 V
		1.0	1.0		1.0	1.0	μA max	

¹ Guaranteed by design, not subject to production test.

DUAL SUPPLY

$V_{DD} = 2.5 \text{ V} \pm 10\%$, $V_{SS} = -2.5 \text{ V} \pm 10\%$, $GND = 0 \text{ V}$, unless otherwise noted.

Table 3.

Parameter	B Version			C Version			Unit	Test Conditions/ Comments
	+25°C	-40°C to +85°C	-40°C to +125°C	+25°C	-40°C to +85°C	-40°C to +125°C		
ANALOG SWITCH								
Analog Signal Range			V_{SS} to V_{DD}			V_{SS} to V_{DD}	V	$V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10 \text{ mA}$; see Figure 20
On Resistance (R_{ON})	2.5			2.5			Ω typ	
On Resistance Match Between Channels (ΔR_{ON})	4.5	5	7	4.5	5	7	Ω max Ω typ	$V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10 \text{ mA}$ $V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10 \text{ mA}$
On Resistance Flatness ($R_{FLAT(ON)}$)	0.4	0.8	1.5	0.4	0.8	1.5	Ω max Ω typ	
	0.6	1.0	1.65	0.6	1.0	1.65	Ω max	
LEAKAGE CURRENTS								
Source Off Leakage, I_S (Off)	± 0.01			± 0.01			nA typ	$V_{DD} = +2.75 \text{ V}$, $V_{SS} = -2.75 \text{ V}$ $V_S = +2.25 \text{ V}/-1.25 \text{ V}$, $V_D = -1.25 \text{ V}/+2.25 \text{ V}$; see Figure 21
Drain Off Leakage, I_D (Off)	± 0.01	± 20	± 20	± 0.1 ± 0.01	± 0.3	± 1	nA max nA typ	$V_S = +2.25 \text{ V}/-1.25 \text{ V}$, $V_D = -1.25 \text{ V}/+2.25 \text{ V}$; see Figure 22
Channel On Leakage, I_D, I_S (On)	± 0.01	± 20	± 20	± 0.1 ± 0.01	± 0.75	± 6	nA max nA typ	$V_S = V_D = +2.25 \text{ V}/-1.25 \text{ V}$; see Figure 23
		± 20	± 20	± 0.1	± 0.75	± 6	nA max	
DIGITAL INPUTS								
Input High Voltage, V_{INH}			1.7			1.7	V min	$V_{IN} = V_{INL}$ or V_{INH}
Input Low Voltage, V_{INL}			0.7			0.7	V max	
Input Current I_{INL} or I_{INH}	0.005		± 0.1	0.005		± 0.1	μA typ μA max	
Digital Input Capacitance, C_{IN}	2			2			pF typ	
DYNAMIC CHARACTERISTICS¹								
$t_{TRANSITION}$	14			14			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$; see Figure 24
Break-Before-Make Time Delay, t_{OPEN}	8	25	25	8	25	25	ns max ns typ	$V_S = 1.5 \text{ V}/0 \text{ V}$; see Figure 24 $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
$t_{ON(EN)}$	14	1	1	14	1	1	ns min ns typ	$V_S = 1.5 \text{ V}$; see Figure 25 $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
$t_{OFF(EN)}$	8	25	25	8	25	25	ns max ns typ	$V_S = 1.5 \text{ V}$; see Figure 26 $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
Charge Injection	± 3	15	15	± 3	15	15	ns max pC typ	$V_S = 1.5 \text{ V}$; see Figure 26 $V_S = 0 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$; see Figure 27
Off Isolation	-60			-60			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 10 \text{ MHz}$
	-80			-80			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 28

Parameter	B Version			C Version			Unit	Test Conditions/ Comments
	+25°C	-40°C to +85°C	-40°C to +125°C	+25°C	-40°C to +85°C	-40°C to +125°C		
Channel-to-Channel Crosstalk	-60			-60			dB typ	$R_L = 50 \Omega$, $C_L = 5$ pF, $f = 10$ MHz
	-80			-80			dB typ	$R_L = 50 \Omega$, $C_L = 5$ pF, $f = 1$ MHz; see Figure 29
-3 dB Bandwidth	55			55			MHz typ	$R_L = 50 \Omega$, $C_L = 5$ pF; see Figure 30
C_S (Off)	13			13			pF typ	$f = 1$ MHz
C_D (Off)								
ADG708	85			85			pF typ	$f = 1$ MHz
ADG709	42			42			pF typ	$f = 1$ MHz
C_D , C_S (On)								
ADG708	96			96			pF typ	$f = 1$ MHz
ADG709	48			48			pF typ	$f = 1$ MHz
POWER REQUIREMENTS								
I_{DD}	0.001			0.001			μ A typ	$V_{DD} = 2.75$ V
		1.0	1.0		1.0	1.0	μ A max	Digital inputs = 0 V or 2.75 V
I_{SS}	0.001			0.001			μ A typ	$V_{SS} = -2.75$ V
		1.0	1.0		1.0	1.0	μ A max	Digital inputs = 0 V or 2.75 V

¹ Guaranteed by design not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to V_{SS}	7 V
V_{DD} to GND	-0.3 V to +7 V
V_{SS} to GND	+0.3 V to -3.5 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ¹	-0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum)	100 mA
Continuous Current, S or D	30 mA
Operating Temperature	
Industrial Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
TSSOP Package, Power Dissipation	432 mW
θ_{JA} Thermal Impedance	150.4°C/W
θ_{JC} Thermal Impedance	27.6°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

¹ Overvoltages at A, EN, S, or D are clamped by internal codes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

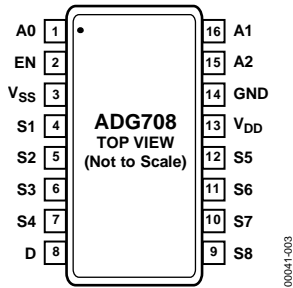


Figure 3. ADG708 Pin Configuration

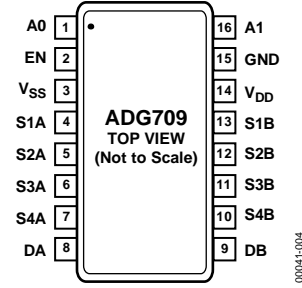


Figure 4. ADG709 Pin Configuration

Table 5. ADG708 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Digital Input. Controls the configuration of the switch, as shown in the truth table (see Table 7).
2	EN	Digital Input. Controls the configuration of the switch, as shown in the truth table (see Table 7).
3	V _{SS}	Most Negative Power Supply Pin in Dual-Supply Applications. For single-supply applications, it should be tied to GND.
4	S1	Source Terminal. Can be an input or output.
5	S2	Source Terminal. Can be an input or output.
6	S3	Source Terminal. Can be an input or output.
7	S4	Source Terminal. Can be an input or output.
8	D	Drain Terminal. Can be an input or output.
9	S8	Source Terminal. Can be an input or output.
10	S7	Source Terminal. Can be an input or output.
11	S6	Source Terminal. Can be an input or output.
12	S5	Source Terminal. Can be an input or output.
13	V _{DD}	Most Positive Power Supply Pin.
14	GND	Ground (0 V) Reference.
15	A2	Digital Input. Controls the configuration of the switch, as shown in the truth table (see Table 7).
16	A1	Digital Input. Controls the configuration of the switch, as shown in the truth table (see Table 7).

Table 6. ADG709 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Digital Input. Controls the configuration of the switch, as shown in the truth table (see Table 8).
2	EN	Digital Input. Controls the configuration of the switch, as shown in the truth table (see Table 8).
3	V _{SS}	Most Negative Power Supply Pin in Dual-Supply Applications. For single-supply applications, it should be tied to GND.
4	S1A	Source Terminal. Can be an input or output.
5	S2A	Source Terminal. Can be an input or output.
6	S3A	Source Terminal. Can be an input or output.
7	S4A	Source Terminal. Can be an input or output.
8	DA	Drain Terminal. Can be an input or output.
9	DB	Drain Terminal. Can be an input or output.
10	S4B	Source Terminal. Can be an input or output.
11	S3B	Source Terminal. Can be an input or output.
12	S2B	Source Terminal. Can be an input or output.
13	S1B	Source Terminal. Can be an input or output.
14	V _{DD}	Most Positive Power Supply Pin.
15	GND	Ground (0 V) Reference.
16	A1	Digital Input. Controls the configuration of the switch, as shown in the truth table (see Table 8).

TRUTH TABLES

Table 7. ADG708 Truth Table

A2	A1	A0	EN	Switch Condition
X ¹	X ¹	X ¹	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

¹X = Don't care.

Table 8. ADG709 Truth Table

A1	A0	EN	On Switch Pair
X ¹	X ¹	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

¹X = Don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

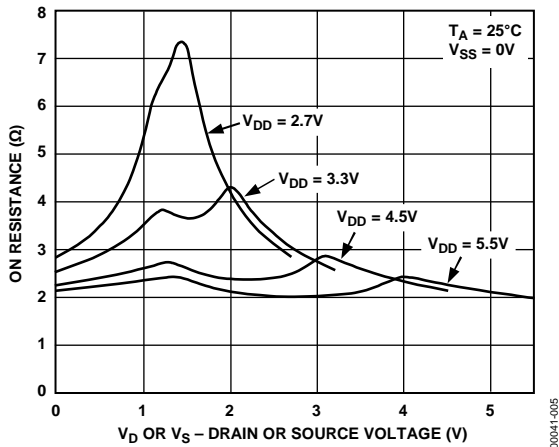


Figure 5. On Resistance as a Function of V_D (V_S) for Single Supply

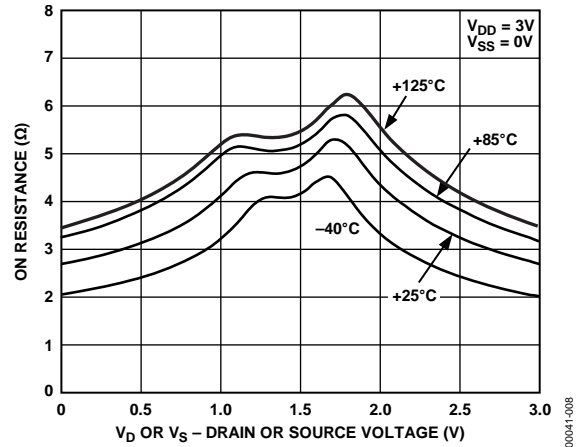


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

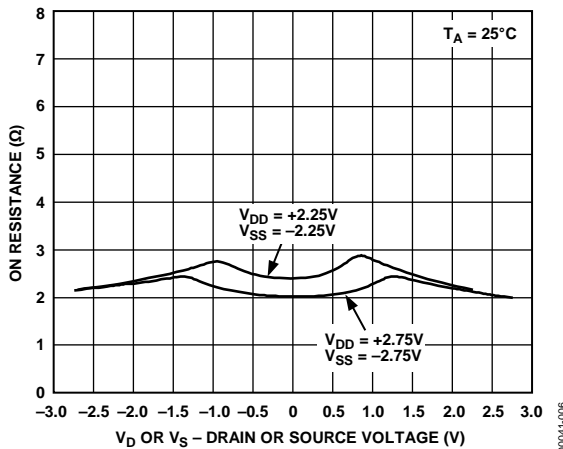


Figure 6. On Resistance as a Function of V_D (V_S) for Dual Supply

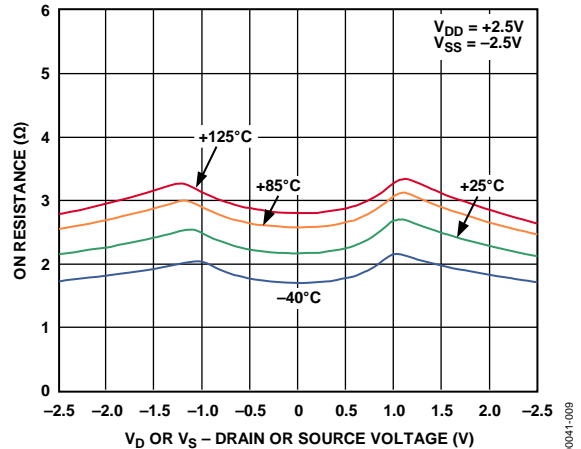


Figure 9. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

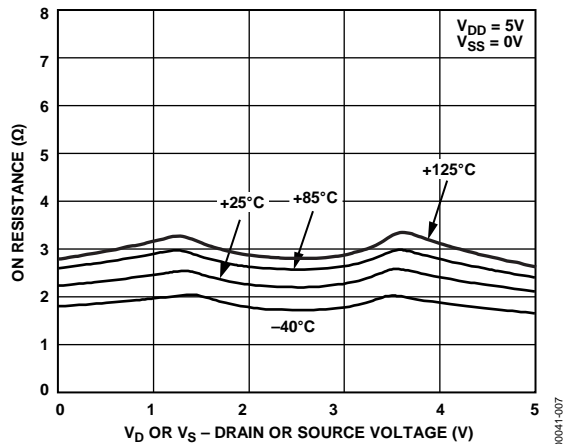


Figure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

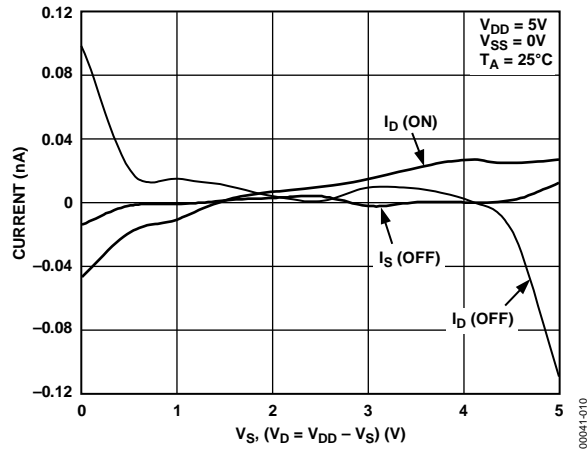


Figure 10. Leakage Currents as a Function of V_D (V_S)

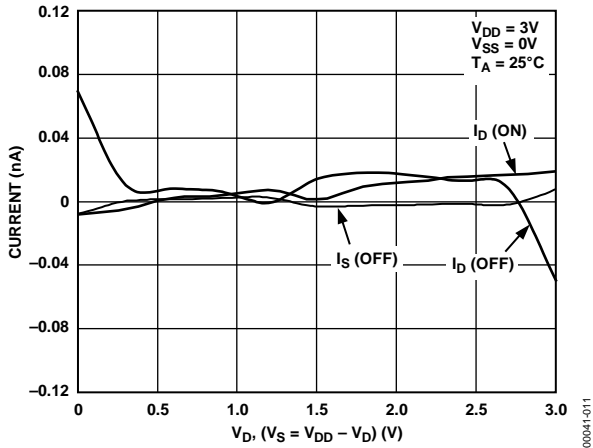


Figure 11. Leakage Currents as a Function of V_D (V_S)

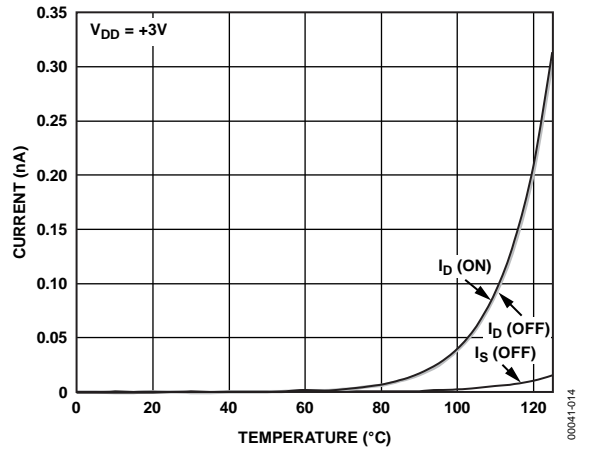


Figure 14. Leakage Currents as a Function of Temperature

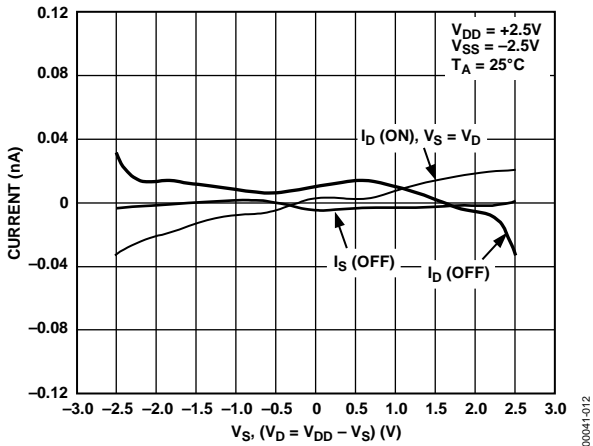


Figure 12. Leakage Currents as a Function of V_D (V_S)

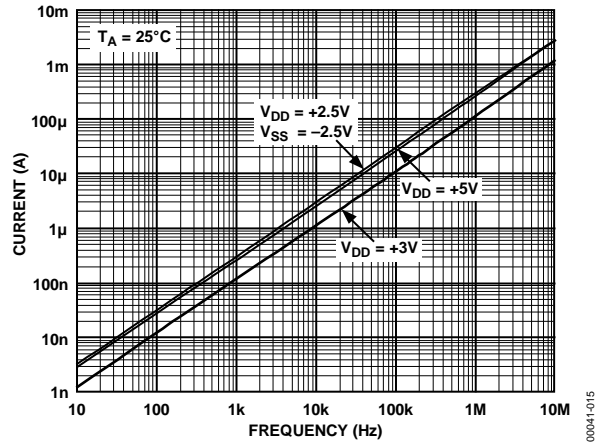


Figure 15. Supply Current vs. Input Switching Frequency

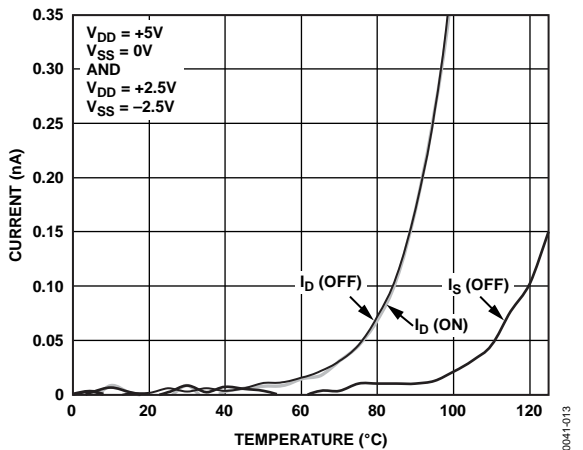


Figure 13. Leakage Currents as a Function of Temperature

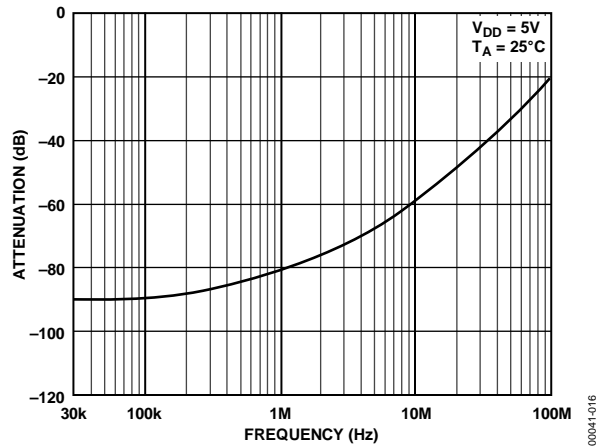


Figure 16. Off Isolation vs. Frequency

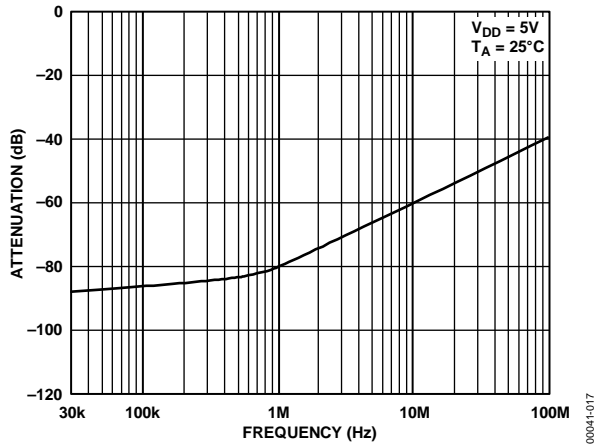


Figure 17. Crosstalk vs. Frequency

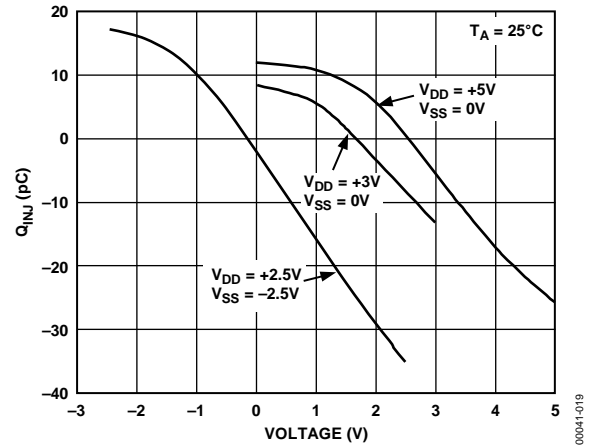


Figure 19. Charge Injection vs. Source Voltage

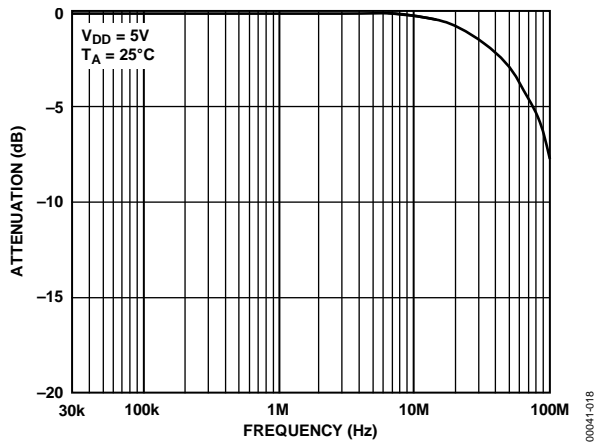


Figure 18. On Response vs. Frequency

TEST CIRCUITS

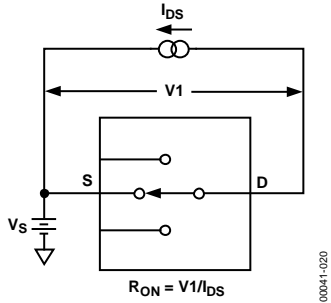


Figure 20. On Resistance

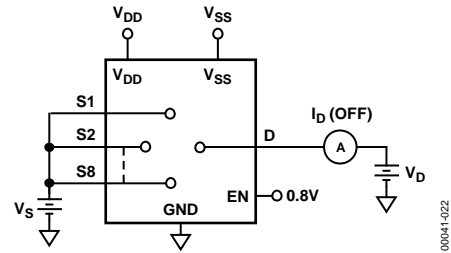


Figure 22. I_D (OFF)

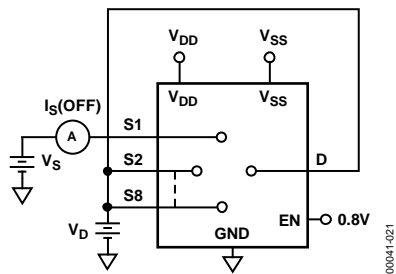


Figure 21. I_S (OFF)

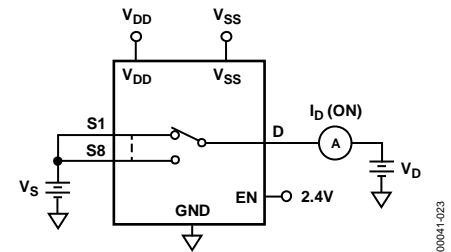
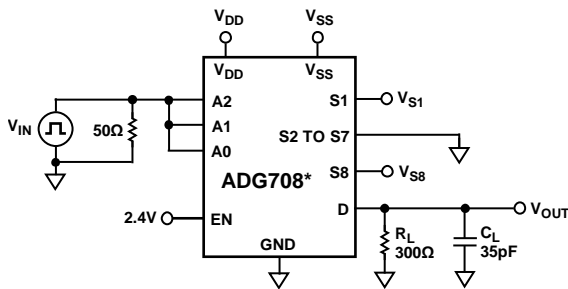
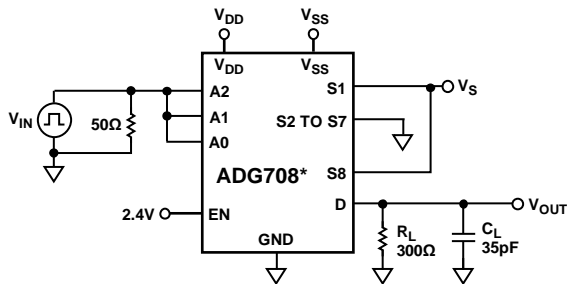
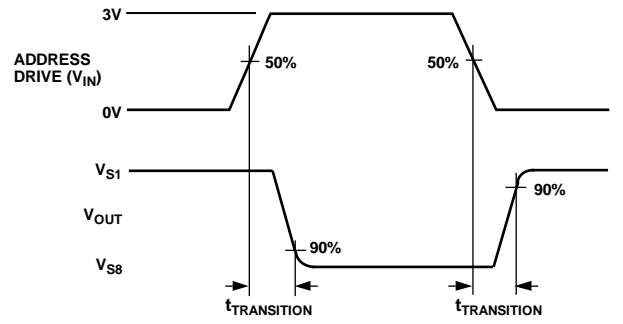


Figure 23. I_D (ON)



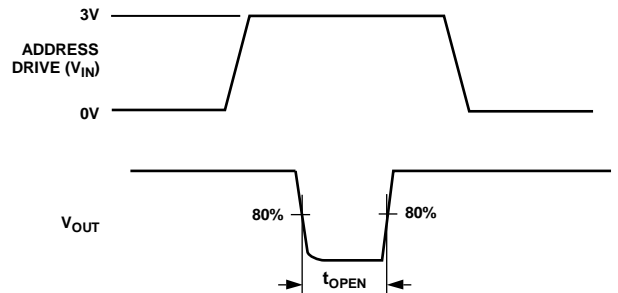
*SIMILAR CONNECTION FOR ADG709.

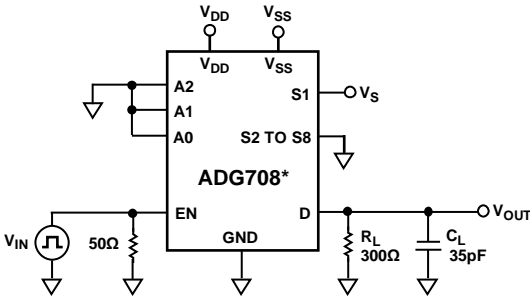
Figure 24. Switching Time of Multiplexer, $t_{\text{TRANSITION}}$



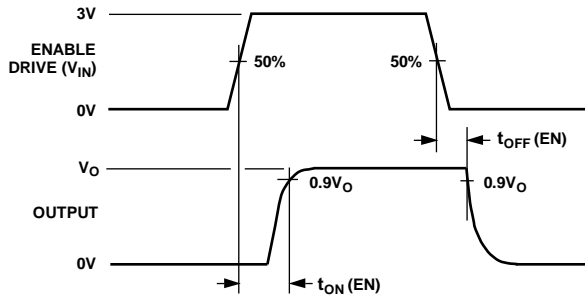
*SIMILAR CONNECTION FOR ADG709.

Figure 25. Break-Before-Make Delay, t_{OPEN}



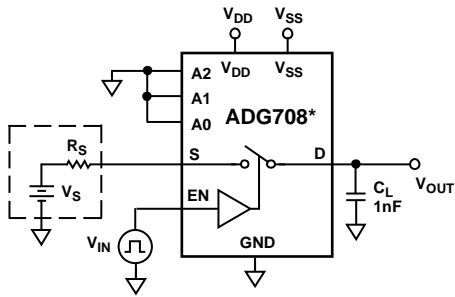


*SIMILAR CONNECTION FOR ADG709.

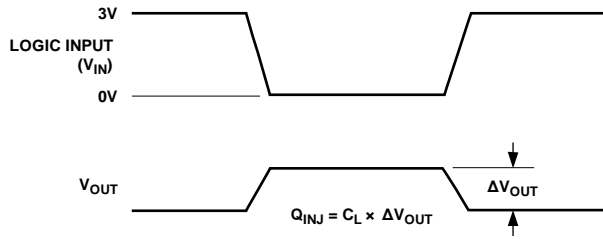


00041-026

Figure 26. Enable Delay, t_{ON}(EN), t_{OFF}(EN)

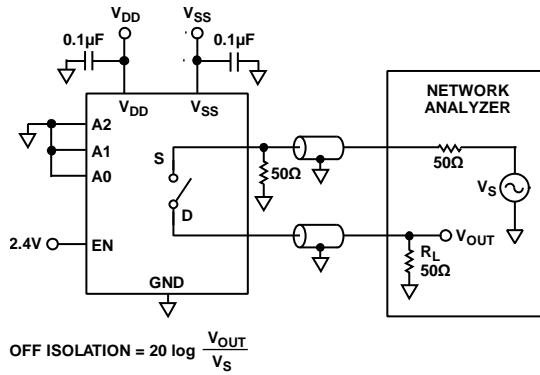


*SIMILAR CONNECTION FOR ADG709.



00041-027

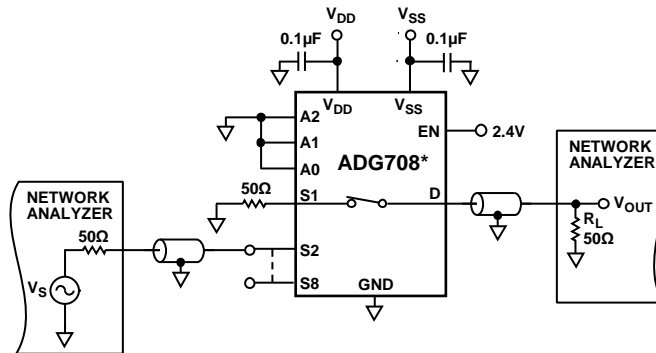
Figure 27. Charge Injection



$$\text{OFF ISOLATION} = 20 \log \frac{V_{\text{OUT}}}{V_S}$$

00041-028

Figure 28. Off Isolation

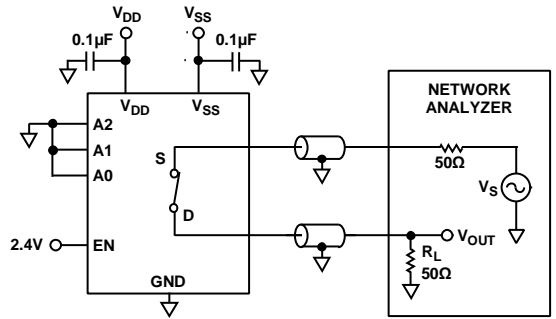


*SIMILAR CONNECTION FOR ADG709.

$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{\text{OUT}}}{V_S}$$

00041-029

Figure 29. Channel-to-Channel Crosstalk



$$\text{INSERTION LOSS} = 20 \log \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

Figure 30. Bandwidth

00041-030

TERMINOLOGY

V_{DD}

Most positive power supply potential.

V_{SS}

Most negative power supply in a dual-supply application. In single-supply applications, tie V_{SS} to ground at the device.

GND

Ground (0 V) reference.

S

Source terminal. Can be an input or output.

D

Drain terminal. Can be an input or output.

A_x

Logic control input.

EN

Active high enable.

R_{ON}

Ohmic resistance between D and S.

$R_{FLAT (ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

$I_S (Off)$

Source leakage current with the switch off.

$I_D (Off)$

Drain leakage current with the switch off.

$I_D, I_S (On)$

Channel leakage current with the switch on.

$V_D (V_S)$

Analog voltage on Terminal D and Terminal S.

$C_S (Off)$

Off switch source capacitance. Measured with reference to ground.

$C_D (Off)$

Off switch drain capacitance. Measured with reference to ground.

$C_D, C_S (On)$

On switch capacitance. Measured with reference to ground.

C_{IN}

Digital input capacitance.

$t_{TRANSITION}$

Delay time measured between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

$t_{ON (EN)}$

Delay time between the 50% and 90% points of the EN digital input and the switch on condition.

$t_{OFF (EN)}$

Delay time between the 50% and 90% points of the EN digital input and the switch off condition.

t_{OPEN}

Off time measured between the 80% points of both switches when switching from one address state to another.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Charge

A measure of the glitch impulse transferred from injection of the digital input to the analog output during switching.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

On Loss

The loss due to the on resistance of the switch.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

$I_{INL} (I_{INH})$

Input current of the digital input.

I_{DD}

Positive supply current.

I_{SS}

Negative supply current.

APPLICATIONS INFORMATION

POWER SUPPLY SEQUENCING

When using CMOS devices, take care to ensure correct power supply sequencing. Incorrect power supply sequencing can result in the device being subjected to stresses beyond the maximum ratings listed in Figure 4.

Always apply digital and analog inputs after power supplies and ground. For single-supply operation, tie V_{SS} to GND as close to the device as possible.