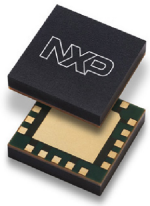
NXP Semiconductors
Technical Data

Document Number: AFRX5G272
Rev. 0, 07/2020

RF Front-End Receiver Module

AFRX5G272

**2300–2690 MHz, 33 dB, 1.2 dB NF
AIRFAST RX MODULE**



6.2 mm × 6.2 mm Module

The AFRX5G272 is an integrated multi-chip module designed for TD-LTE and 5G mMIMO applications. It consists of a T/R switch, a two-stage low noise amplifier and support circuitry to work from a 5 V supply and a 1.8 V logic-level T/R control.

The device has Tx and Rx modes, which are controlled via T/R logic signaling. In Tx mode, internal RF switches direct the signal from the antenna port to an external termination resistor. In Rx mode, internal RF switches direct the signal from the antenna port to internal LNAs. While in Tx mode, the LNA is in idle mode with minimized current consumption.

Features

- Frequency: 2300–2690 MHz
- Rx mode (2500 MHz)
  - Gain: 33.0 dB
  - IIP3: 0 dBm
  - NF: 1.2 dB
- Tx mode (2500 MHz)
  - Robustness short-term incidents: 39.0 dBm (Avg.), 47.0 dBm (Peak)
  - Robustness indefinitely incidents: 37.0 dBm (Avg.), 45.0 dBm (Peak)
- ANT port return loss:
  - Rx mode: –20 dB
  - Tx mode: –20 dB
- Reverse isolation: 55 dB
- Insertion loss ANT to Tx/TERM port: –0.75 dB
- 1.8 V logic JEDEC-compliant control interface
- 5 V supply
- Power consumption:
  - Rx mode: 500 mW
  - Tx mode: 70 mW
- 50 ohm operation with no external matching
- Compact 6.2 mm × 6.2 mm LGA package, which is compatible with QFN 6 × 6 footprint

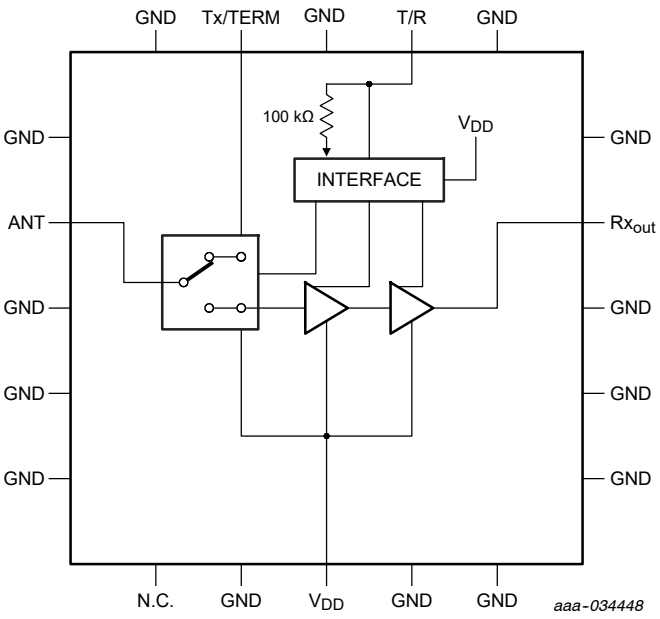


Figure 1. Functional Block Diagram

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Operating Voltage	V_{DD}	5.25	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +105	°C
Operating Junction Temperature (1)	T_J	150	°C
Input Power (Rx mode, P_{avg}, CW)	P_{in}	20	dBm
Input Power (Tx mode, 10 sec. Duration, 10 MHz LTE, 8 db PAR)	P_{in}	39.0	dBm

Table 2. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	2
Charge Device Model (per JS-002-2014)	C3

Table 3. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

1. Continuous use at maximum temperature will affect MTTF.

Table 4. Electrical Characteristics (V_{DD} = 5 Vdc, 2500 MHz, T_A = 25°C, 50 ohm system, in NXP Application Circuit)

Characteristic	Symbol	Min	Typ	Max	Unit
Rx Mode					
Gain (ANT to Rx_{out})	G_p	—	33.0	—	dB
Third Order Input Intercept Point	IIP3	—	0	—	dBm
P_{in} @ 1 dB Compression Point	P1dBi	—	–15	—	dBm
Noise Figure ANT to Rx_{out} 100°C 25°C	NF	—	 1.6 1.2	—	dB
Return Loss ANT Port Rx_{out} Port	RL	—	 –20 –20	—	dB
Reverse Isolation	$\|S_{12}\|^2$	—	55	—	dB
Tx Mode					
Return Loss ANT Port Tx Port	RL	—	 –20 –20	—	dB
Insertion Loss ANT to Tx/TERM	IL	—	–0.75	—	dB
P_{out} @ 0.1 dB Compression Point (ANT to Tx)	P0.1dB	—	45	—	dBm
Power Handling — Derating and Incidence					
Tx Port, Normal Operation: 2500 MHz, –40°C to +100°C, P_{avg}, 20 MHz LTE, 8 dB PAR Incident on ANT P_{in}	—	—	37.0	—	dBm
Tx Port, Short-Term Incident (10S): 2500 MHz, –40°C to +100°C, P_{avg}, 20 MHz LTE, 8 dB PAR Incident on ANT P_{in}	—	—	39.0	—	dBm
Rx Port, Normal Operation: 2500 MHz, –40°C to +100°C, P_{avg}, CW, Incident on ANT P_{in}	—	—	20.0	—	dBm
Timing					
ANT to Rx_{out} Gain Setting Time to within 0.3 dB of Final after T/R Command, –10°C to +105°C	—	—	< 1.0	—	μsec
ANT to Termination Path Insertion Loss Setting Time to within 0.3 dB of Final after T/R Command, –10°C to +105°C	—	—	0.5	—	μsec
T/R Interface					
JEDEC T/R Interface Voltage	V_{IL}	—	—	0.6825	V
	V_{IH}	1.0725	—	—	V

Table 5. Ordering Information

Device	Tape and Reel Information	Package
AFRX5G272T4	T4 Suffix = 2,500 Units, 16 mm Tape Width, 13-inch Reel	6.2 mm × 6.2 mm Module

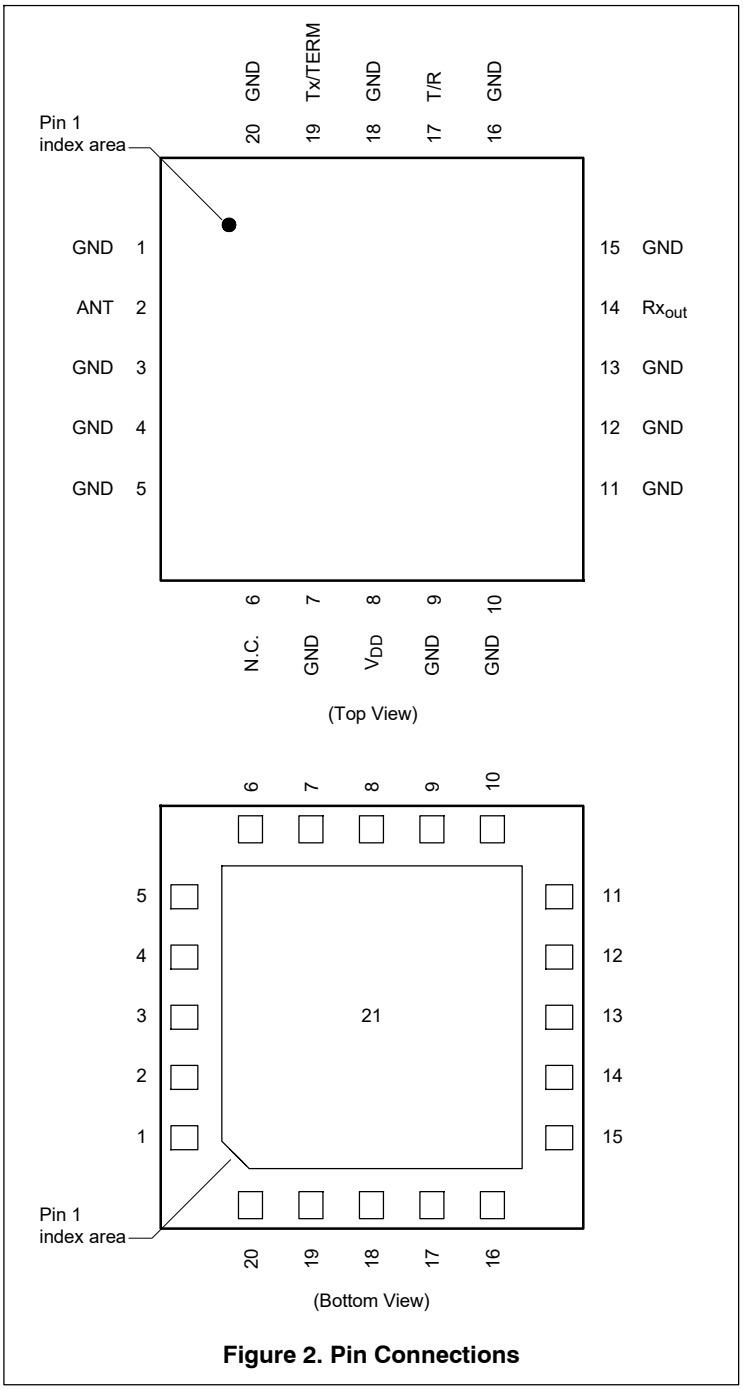


Figure 2. Pin Connections

Table 6. Functional Pin Description

Pin Number	Pin Function	Pin Description
1, 3, 4, 5, 7, 9, 10, 11, 12, 13, 15, 16, 18, 20, 21	GND	Ground
2	ANT	Antenna Port/RF Input Port
6	N.C.	No Connection
8	V_{DD}	DC Bias Voltage
14	Rx_{out}	RF Output for LNA
17[1]	T/R	Digital Control for Transmit/Receive Switch (100 kΩ pulldown is integrated internally)
19	Tx/TERM	50 Ω Termination Port (user will need to provide 50 Ω termination externally)

1. T/R = Low, ANT to Tx. T/R = High, ANT to Rx_{out}.

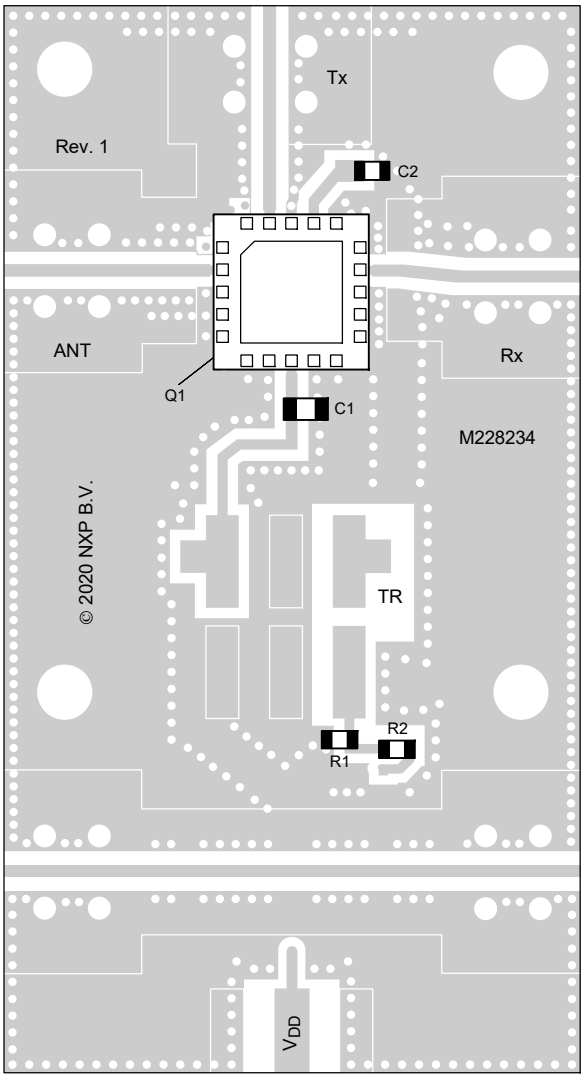


Figure 3. AFRX5G272 Application Circuit Component Layout

Table 7. AFRX5G272 Application Circuit Designations and Values

Part	Description	Part Number	Manufacturer
C1	10 μF Chip Capacitor	GRM188R61A106ME69	Murata
C2	10 pF Chip Capacitor	GRM1555C1E100JA01	Murata
Q1	Receiver Module	AFRX5G272	NXP
R1	10 kΩ, 1/16 W Chip Resistor	RC0402JR-0710KL	Yageo
R2	20 kΩ, 1/16 W Chip Resistor	RC0402JR-0720KL	Yageo
PCB	Rogers R04350B, 0.010", ε_r = 3.66	M228234	MTL

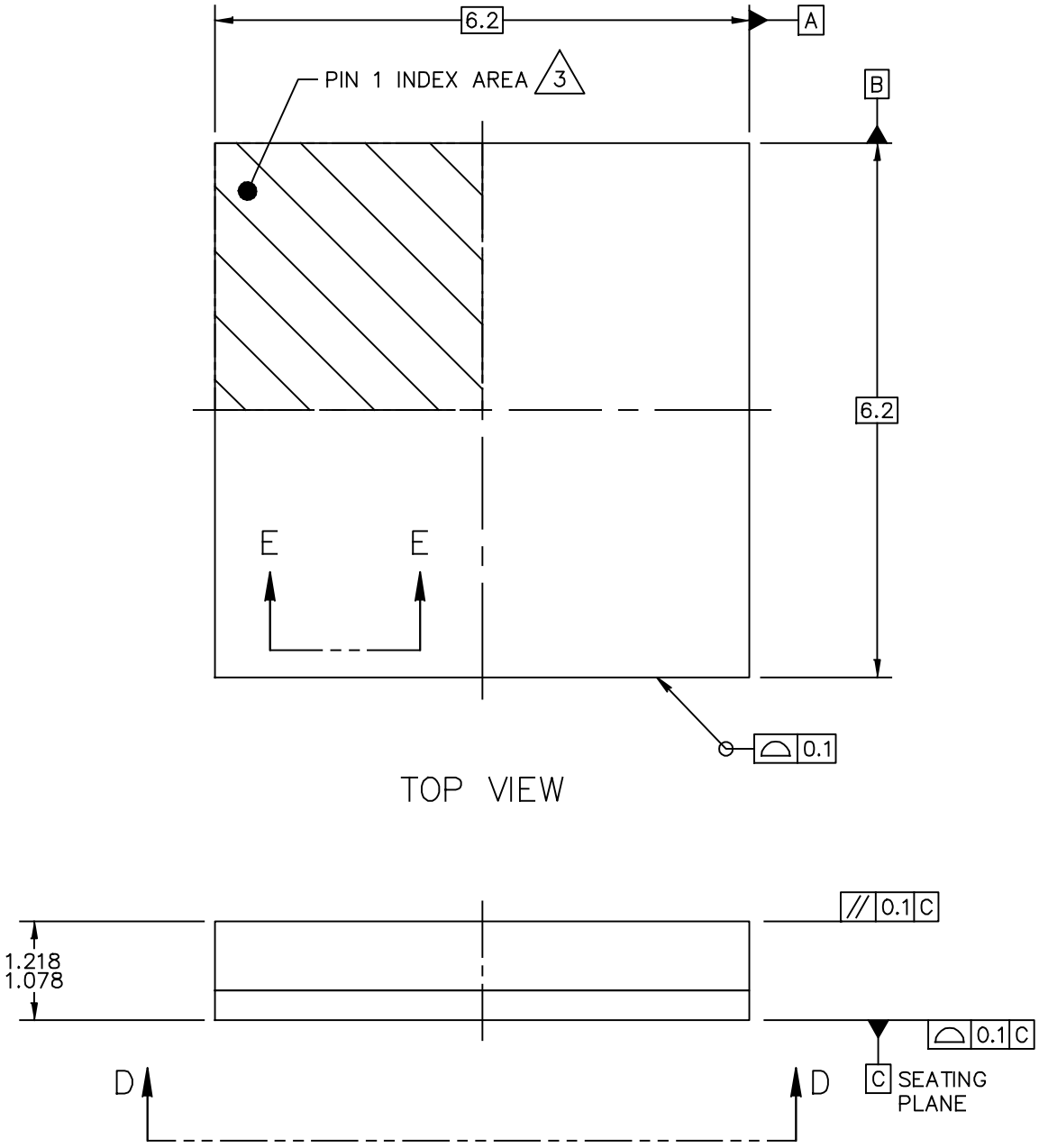
NOTE: R1 and R2 components are needed only when the NXP application circuit (Figure 3) is used in conjunction with a jumper for the convenient application of a T/R control voltage. R1 and R2 are not required in customer end application board designs.

Figure 4. Product Marking

PACKAGE INFORMATION

PLGA–21 I/O
6.2 X 6.2 X 1.148 PKG, 0.9 PITCH

SOT1996–1



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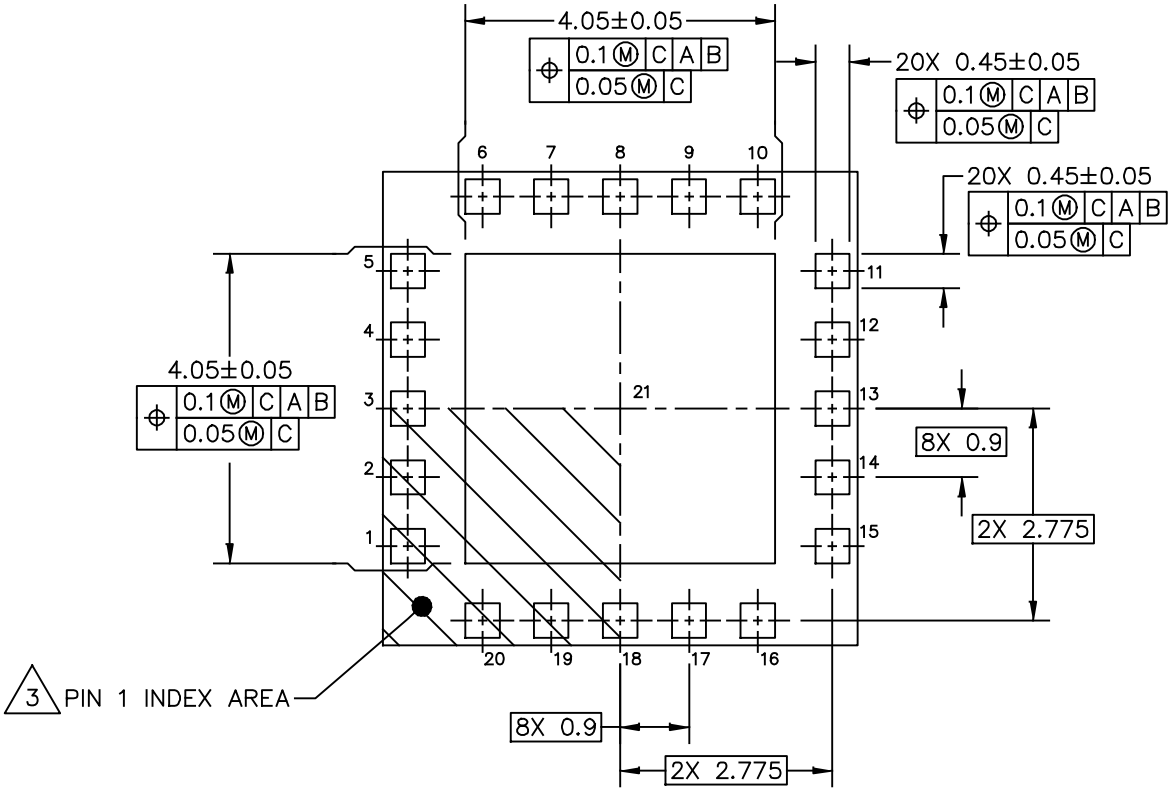
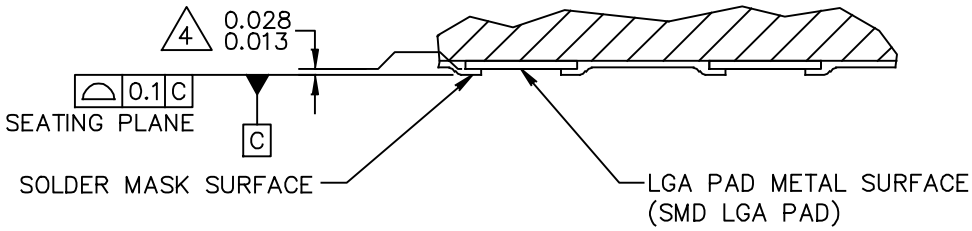


VIEW D–D
(BOTTOM VIEW)



SECTION E–E 5

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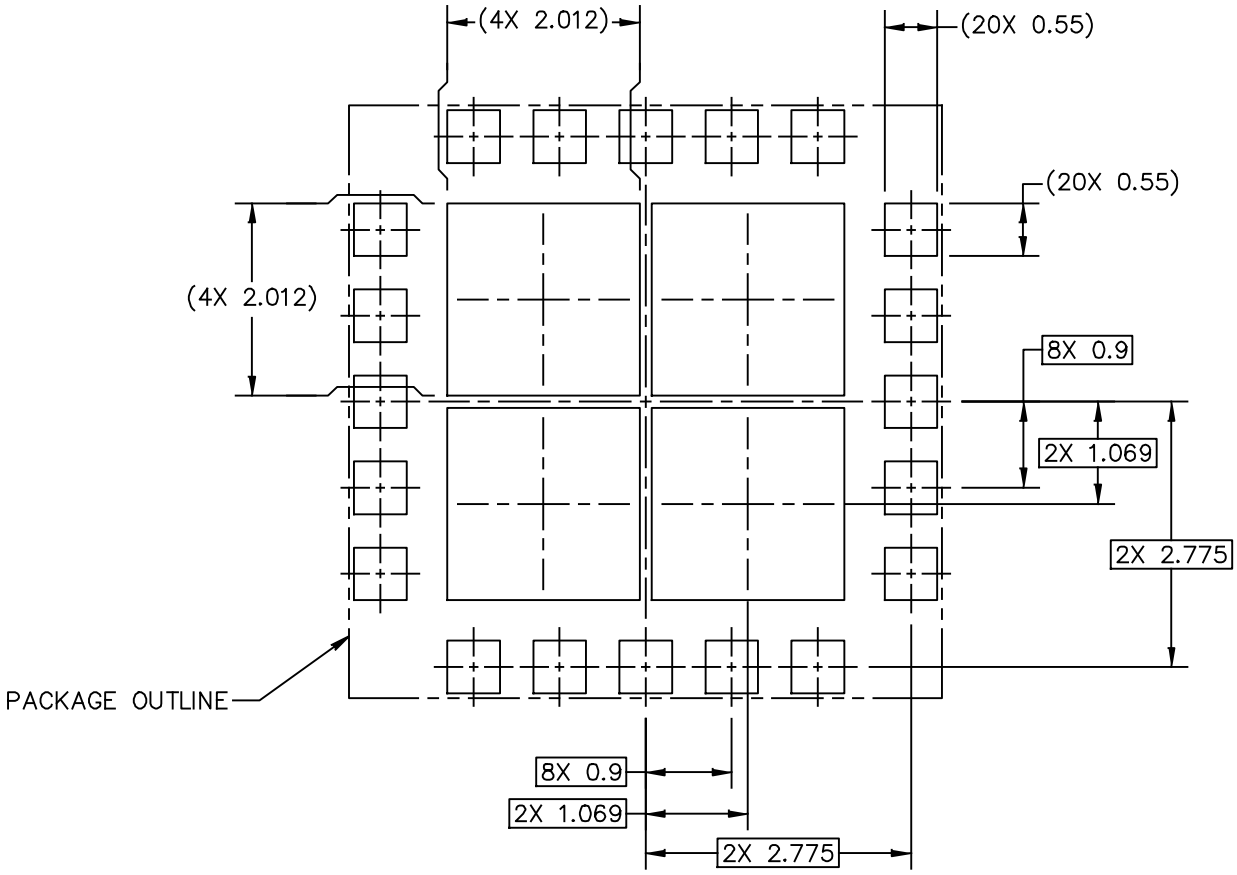

PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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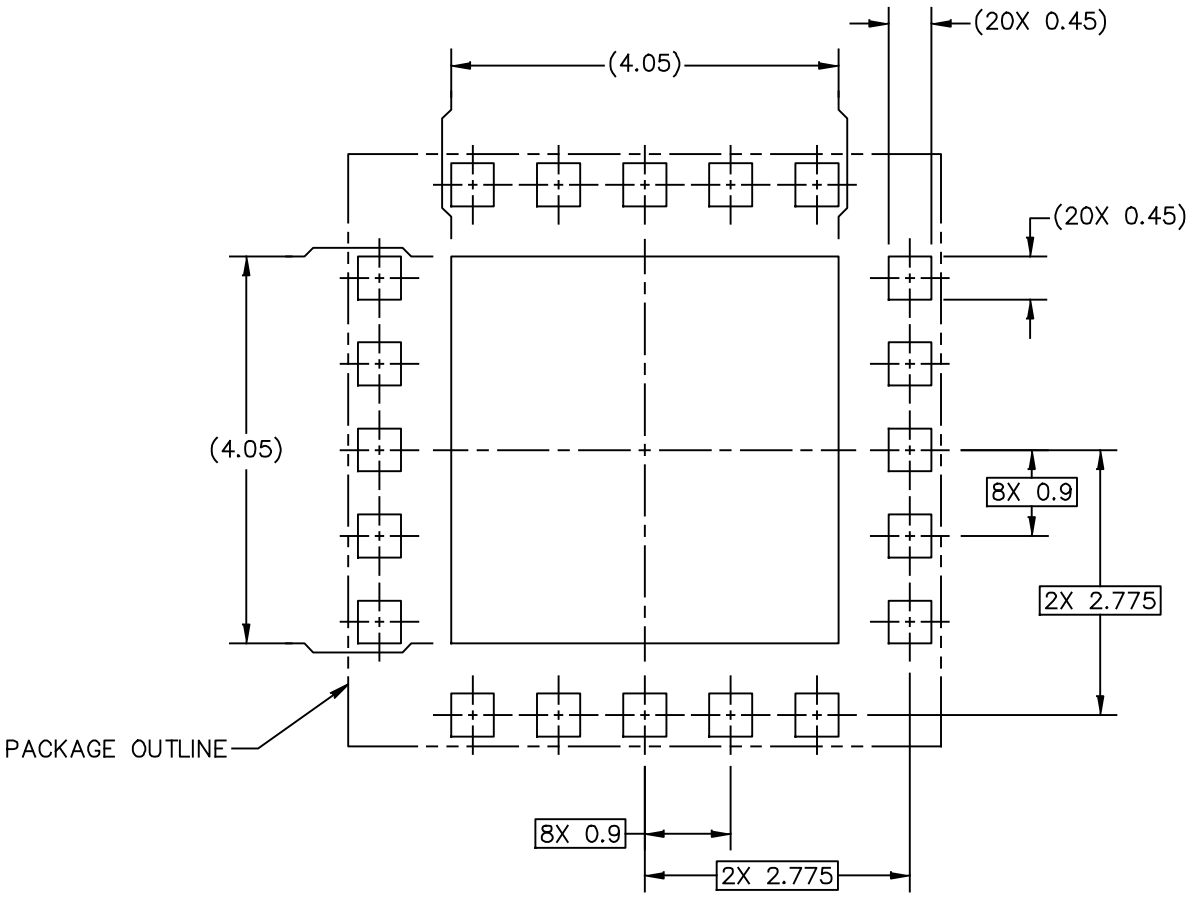

PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREAS

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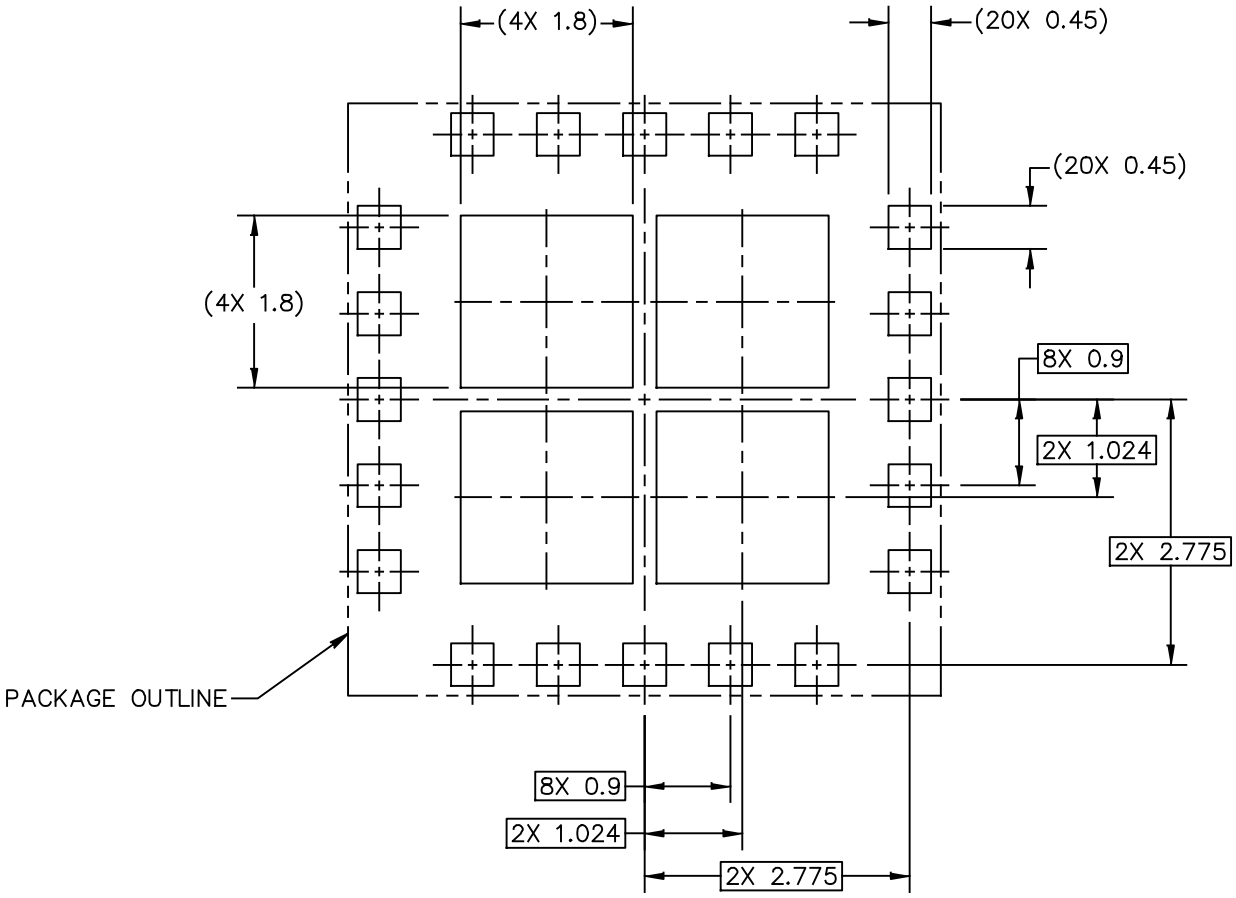

RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. DIMENSION APPLIES TO ALL LEADS AND FLAG.
5. THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PIN 21) AND THE PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD).

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PRODUCT TOOLS

Refer to the following resource to aid your design process.

Development Tools

- Printed Circuit Boards

FAILURE ANALYSIS

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2020	• Initial release of data sheet